Semiconductor Memory: Opportunities and Challenges

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(Acknowledging Fabio Pellizzer and Hongmei Wang for content)

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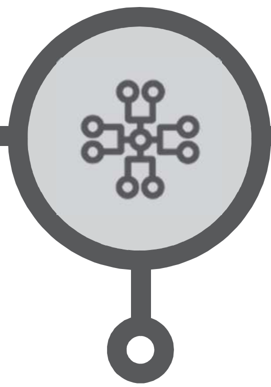
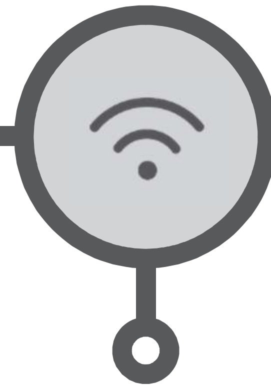
Outline of Talk

- ❑ Memory Trends
- ❑ Storage Class Memory
- ❑ Path for Emerging Memories
- ❑ Conclusions

Trends Driving Increased Data Traffic





Enterprise	Automotive	Cloud/ Big Data	Networking	Mobile/ Client	IoT
Online Transaction Processing systems with low-latency in-memory compute	Global sales of autonomous vehicles to reach ~600,000 units by 2025	Data center storage installed capacity to grow ~5X to 1.8 ZB between 2015 and 2020	Global IP traffic grows at a CAGR of 24% from 2016 to 2020	Global mobile data traffic to rise ~7X between 2016 and 2021	27.1 billion networked devices by 2021

Source, September 2017: Cisco, Gartner, IDC, Automobile manufacturers
IoT – Internet of Things

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Markets Positioned for Opportunity

CY18 **$156B** → CY21 **$165B**

Data Economy

$200B

Mobile Era

Flash

PC / Internet Era

DRAM

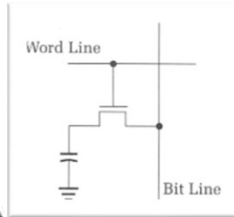
$0

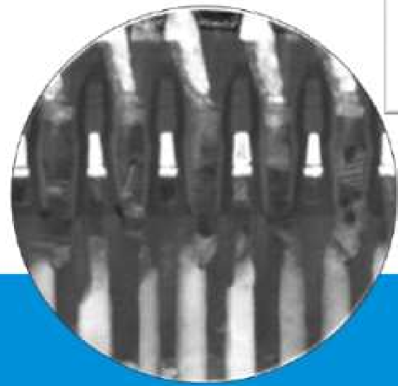
CY90 CY91 CY92 CY93 CY94 CY95 CY96 CY97 CY98 CY99 CY00 CY01 CY02 CY03 CY04 CY05 CY06 CY07 CY08 CY09 CY10 CY11 CY12 CY13 CY14 CY15 CY16 CY17 CY18 CY19 CY20 CY21

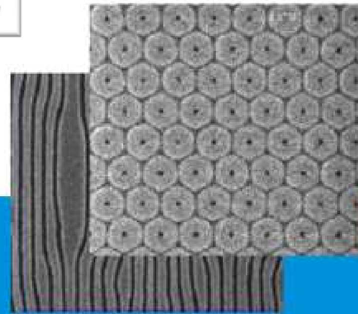
- Trends such as AI, ADAS and IoT driving demand for tailored DRAM solutions
- Ongoing adoption of SSDs in enterprise, cloud and client driving NAND demand

Source: Micron
AI – Artificial Intelligence
ADAS – Advanced Driver Assistance Systems

DRAM Memory

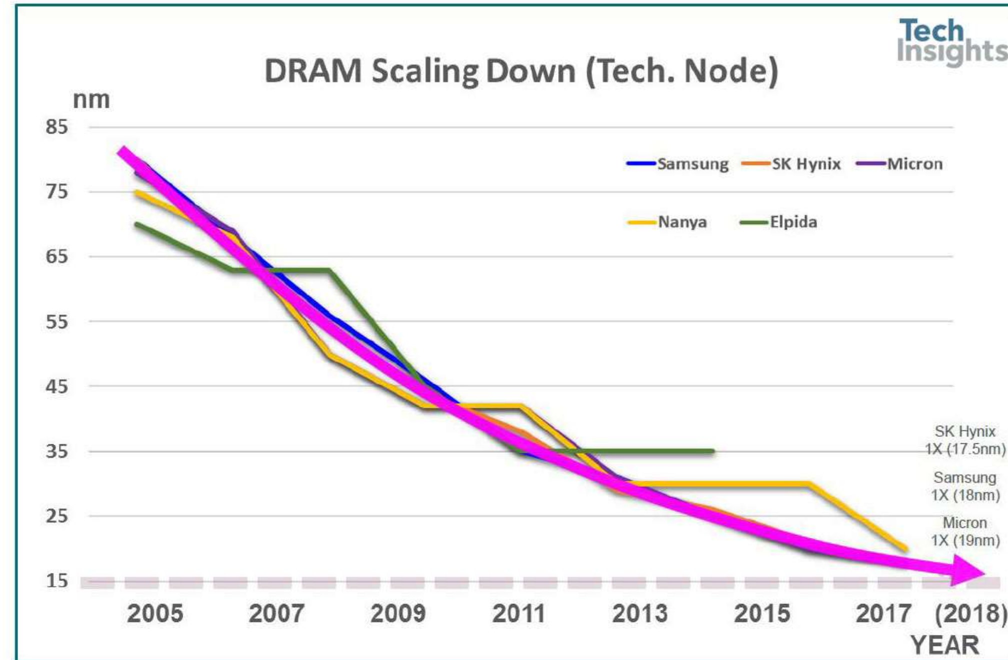






1β Early Process Integration

1γ Architectural Pathfinding



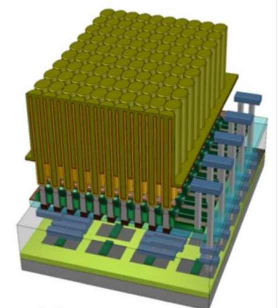
- DRAM has evolved from a planar to a vertical approach
  - Planar capacitor cell; 1978: Stacked capacitor cell structure; 1982: Trench capacitor cell structure; 2003: 3D access transistor; 2008: buried WL
- Current DRAM in production are 15/17nm node (6F2) with cylindrical STC with buried WL access transistor
- A few more generations are possible. What's next?

3D DRAM?

Reuse: Storage Capacitor

Replace: Cell Transistor

Reuse: Memory Logic



Picture source: BeSang

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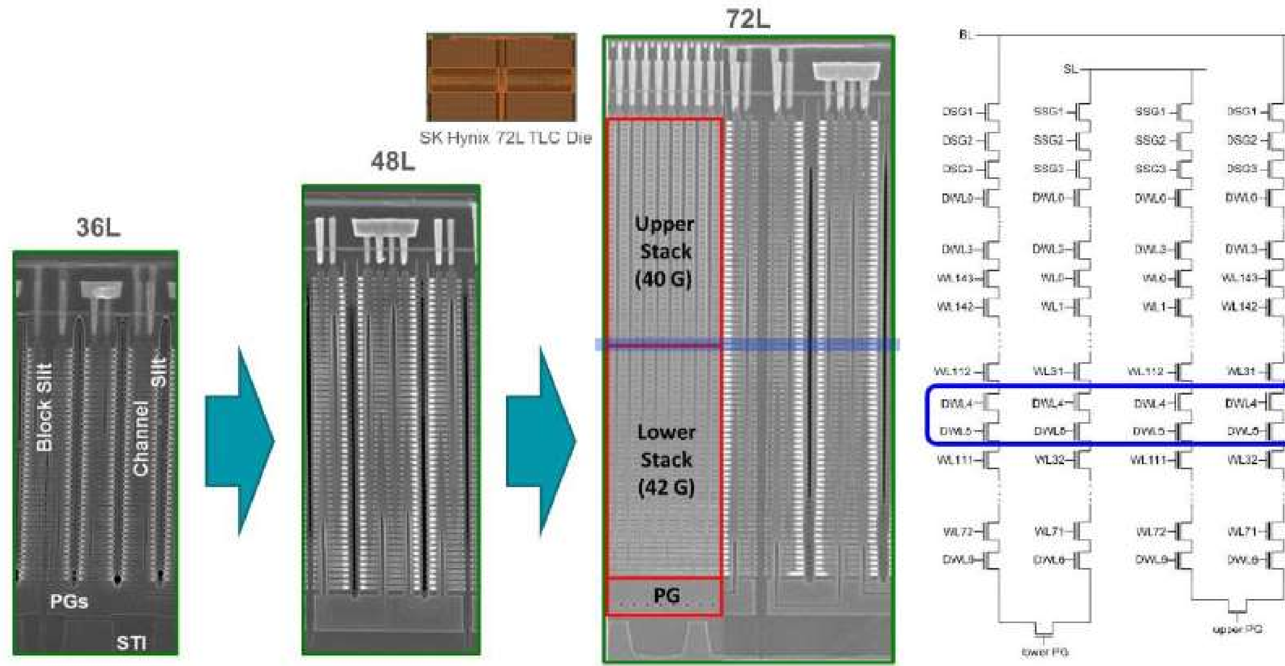
NAND Memory



- ✓ **Low NAND cell current issue**
  - Junction Engineering, S/A Design
  - Mobility (GB, trimmed Si Channel) Engineering
- ✓ **Multi-stack NAND Strings**
  - Currently 2 stacked (64L, 128L)
  - 4 stacked (128L, 256L) or more (512L)
- ✓ **HAR Plasma Etching and Filling**
  - Channel tube etch, CSL etch (> 90:1, 96/128L)
  - Uniform Filling (Si or metal)
- ✓ **WL Cell Contacts Formation**
  - Throughput and cost issue
- ✓ **Decoder TR Reliability**
  - HV + MV
- ✓ **Select Transistor VT Controllability**
  - Fringing Field, Doping, Programmed SG
- ✓ **PGM/ERS Speed @ same retention**
  - Dtox (narrow SiON profile)
- ✓ **e-migration in CTL**
  - Deep trap, Laminated CTL
- ✓ **Cell coupling, Cell VT distribution issue**
  - ONOA uniformity,
- ✓ **PGM/ERS Controllability**
  - Negative WL PGM VT
  - PGM bias condition
- ✓ **COP Opt., Triple Oxide (LLV, LV, HV), Chip size, Defect free, Yield, Low Power**

Manufacturers | 2014 | 2015 | 2016 | 2017 | 2018 | 2019 | 2020 | 2021 | 2022

SAMSUNG: 2D 1X 19 nm, 1Y 16 nm, 1Z 14 nm; Z-NAND (Z-SSD for NVDIMM, 3D V-NAND Cell); 3D V-NAND 32L 20 nm, 48L 20 nm, 64L 20 nm, 64GB/128GB, 9XL 20 nm, 9XLx1, 128L 20 nm, 64Lx2, 128x1, 1XXL 9XLx2, 2XXL

TOSHIBA / WD Western Digital: 2D 19Y, 15nm_1st, 15nm_2nd; XL-FLASH (Enterprise, Datacenter); 3D NAND 48L (BiCS2) 19 nm, 32GB TLC, 64L (BiCS3) 19 nm, 32GB/64GB, 96L (BiCS4) 19 nm, TLC/QLC, 128L (BiCS5) 19 nm, 64Lx2, 192L (BiCS6) 96Lx2, 2XXL

Micron / intel / IM Flash Technologies: 2D 16nm, 1Z; XPoint™ Optane SSD, Intel XPoint™ NVDIMM, Micron QuantX; 3D NAND 32T 40nm, FG, 64T 20 nm, FG, 32Lx2, 32/64GB, 96T 20nm, FG, 48Lx2, 128T Intel, Micron (CTF?), 192T Intel, Micron (CTF?)

SK hynix: 2D 16nm, 1Y/1Y'/1Z 15/14 nm, E3NAND, 1Z'; 3D NAND 36L (V2_3D) 31 nm, 16 GB MLC, 48L (V3_3D) 31 nm, 32GB TLC, 72L (V4_3D) 31 nm, 2-step D/E, 96L (V5_4D) 4D NAND, 48Lx2, Sol., 128L (V6_4D) 4D NAND, Solution, 192L (V7_4D) 4D NAND

YMTC: 3D NAND 32L (Gen.1) Conventional, 8GB, 64L (Gen.2) Xtacking™, 128L (Gen.3) Xtacking™, 64Lx2, 192L

Integration Innovation: Gate Materials (CoSi/NiSi → W); DPT → QPT, Airgap (20/19nm → 15/14nm); 3D GAA/CTF/FG, 32L/36L/48L/64L/72L (BiCS, TCAT, P-BiCS, CuA, Double-stacked); 9XL/128L/192L/256L (Stack, 4D NAND, Xtacking, Triple Ox.)

TechInsights

- ❑ Transitioned from planar to 3D ~ 2015.
- ❑ Today in production: 94 tiers, 256 Gbits, 59 mm^2
- ❑ The roadmap is to increase tiers. How far can it go?

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Storage Class Memory and the Future Path

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Position of emerging memory

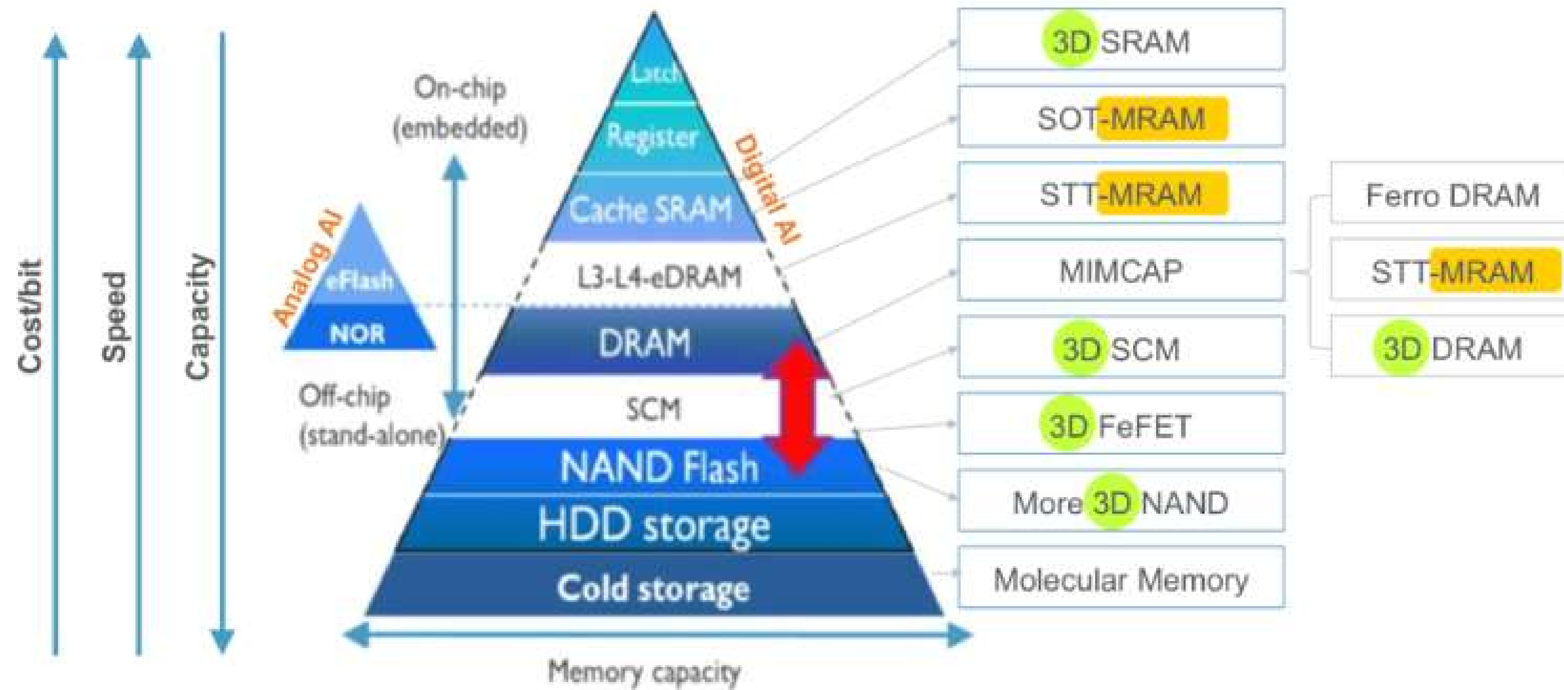
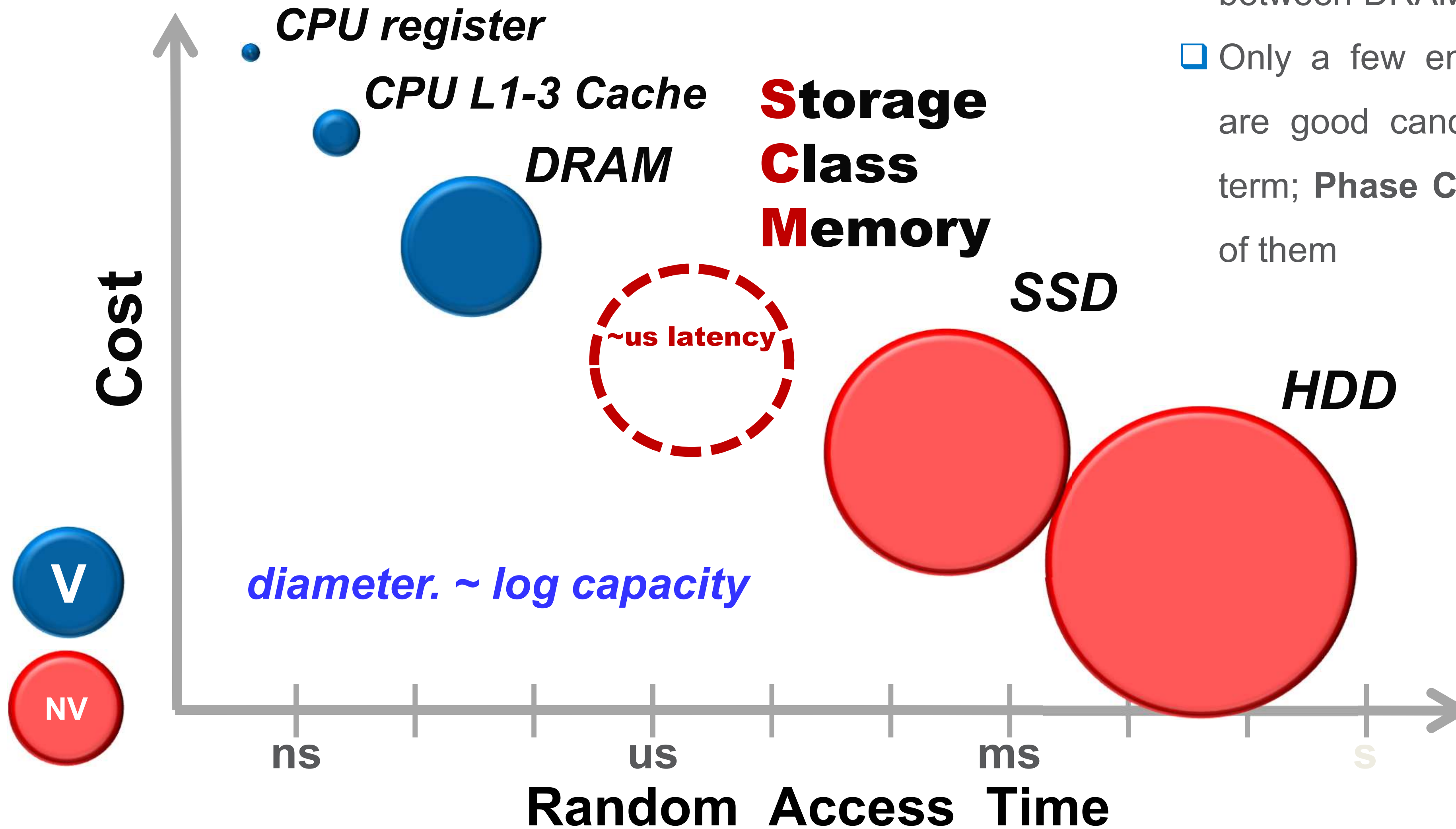


Fig 1: Emerging Memories for Pervasive Data and Compute Source: Applied Materials

- It's hard to directly replace DRAM and NAND with emerging memory as they continue to scale
- Emerging memory deployment has been confined to niche markets with low density devices
- Storage class memory offers the opportunity for new memories to access a much larger market

Why Storage Class Memory?

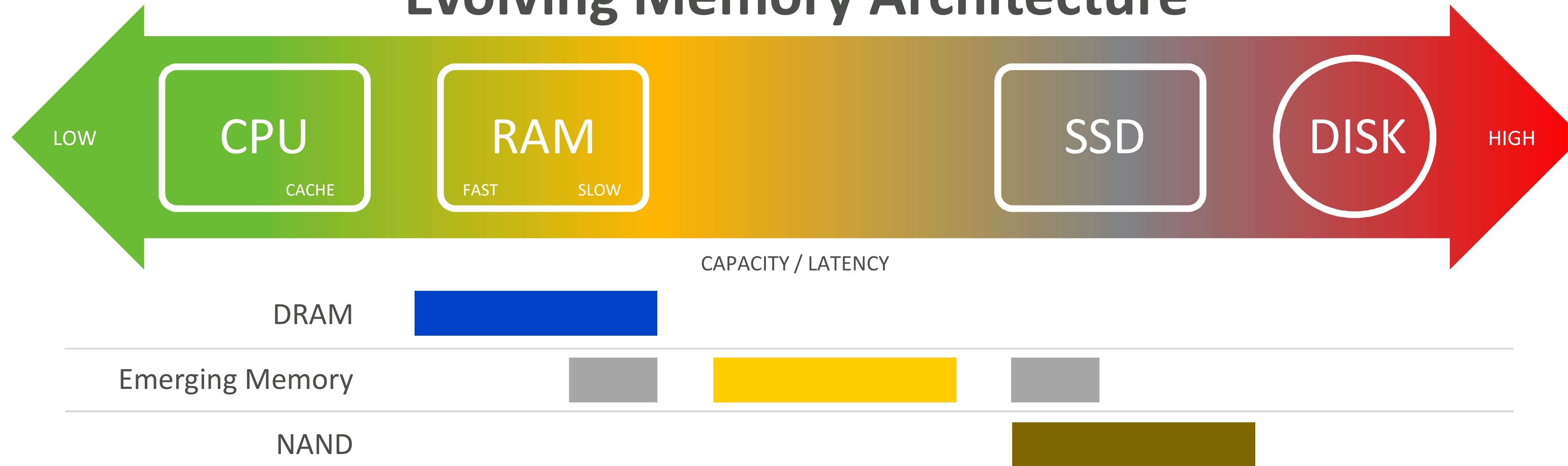


- Fills the gap in the memory hierarchy between DRAM and NAND.
- Only a few emerging memory technologies are good candidates for SCM in the short term; **Phase Change Memory (PCM)** is one of them

From Rich Fackenthal, ISSCC 2014 Micron

Addressing the Performance Gap

Evolving Memory Architecture



Balancing Values: Latency, Endurance, Volatility, Cost

	DRAM			NAND
Latency	**1x**			**1000x**
Endurance	**$\sim10^{15}$**			**$\sim10^{3}$**
Non-Volatility	**NO**			**YES**
Areal Density	**DRAM**			**NAND**

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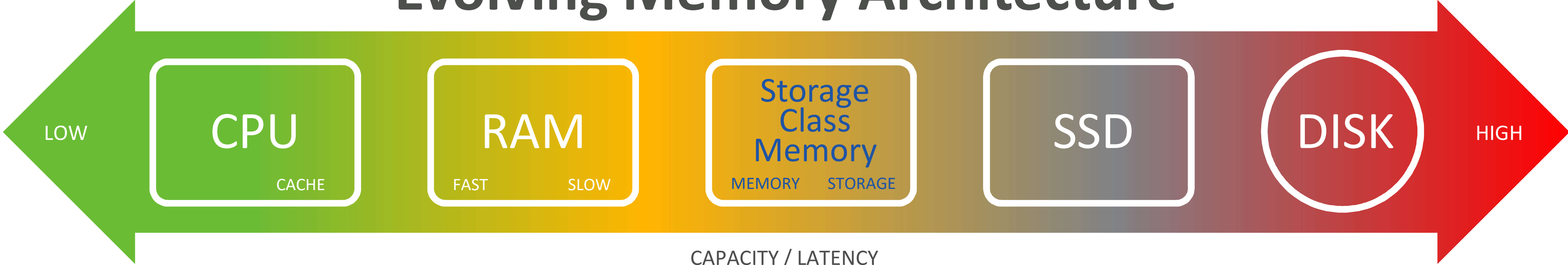
Addressing the Performance Gap

Evolving Memory Architecture



DRAM

Emerging Memory

NAND

Balancing Values: Latency, Endurance, Volatility, Cost

	DRAM	Memory Mapped	Storage Mapped	NAND
Latency	1x	2x	2x-10x	1000x
Endurance	$\sim 10^{15}$	$\sim 10^{13}$	$\sim 10^{7}$	$\sim 10^{3}$
Non-Volatility	NO	NO ($>10x\ t_{refresh}$)	YES	YES
Areal Density	DRAM	~DRAM	~10x DRAM	NAND

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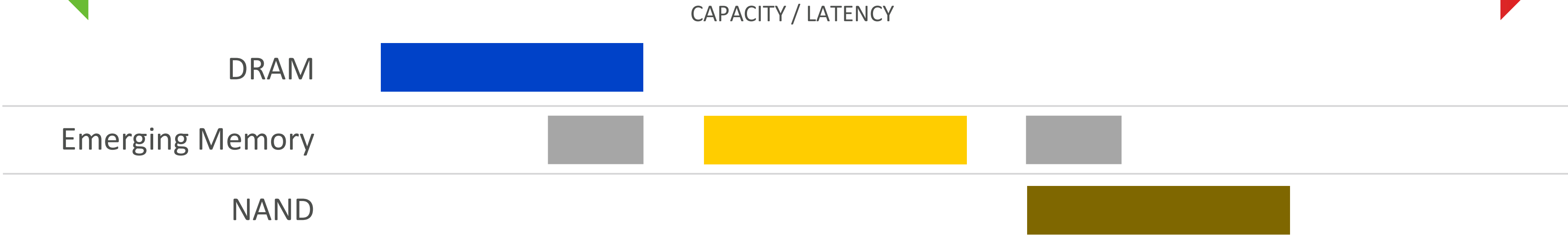
Addressing the Performance Gap

Evolving Memory Architecture



Balancing Values: Latency, Endurance, Volatility, Cost

	DRAM	Storage Mapped	PCM*	RRAM*
Latency	1x	2x-10x		
Endurance	~10^{15}	~10^{7}		
Non-Volatility	NO	YES		
Areal Density	DRAM	~10x DRAM		

*** Color codes referred to "Storage Mapped" specifications**

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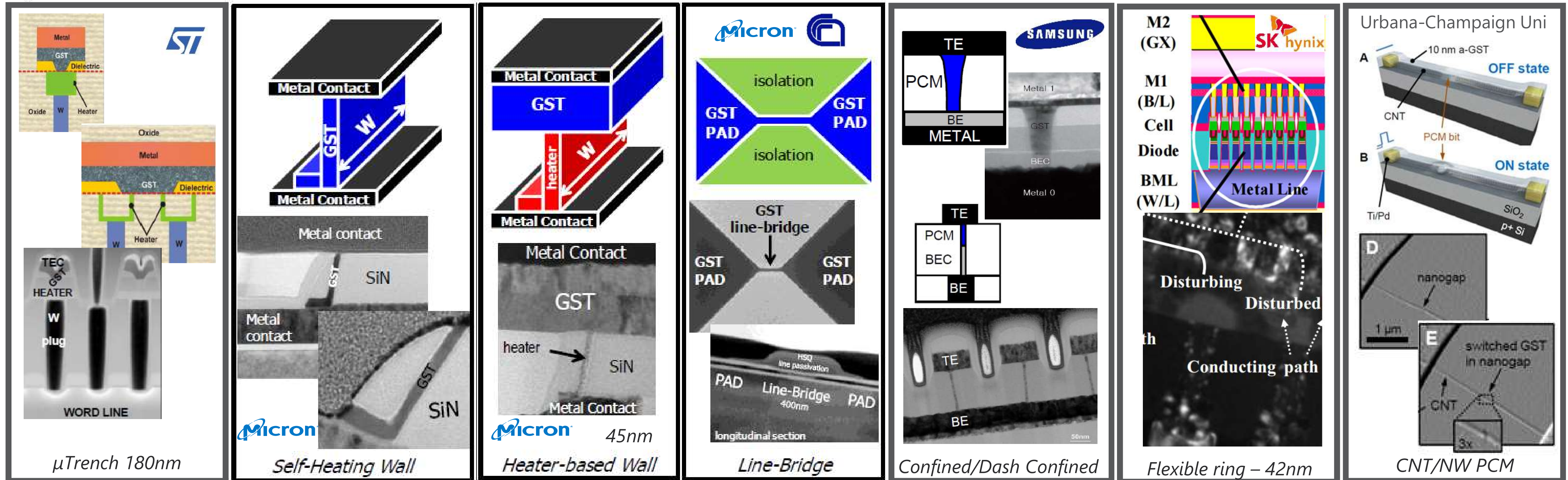
PCM Cell Architectures design



- Two families: self-heating PCM and heater-based PCM
- The different architectures aim at minimize both power consumption and latency
- All of them use a silicon based selector, which limits density and cost

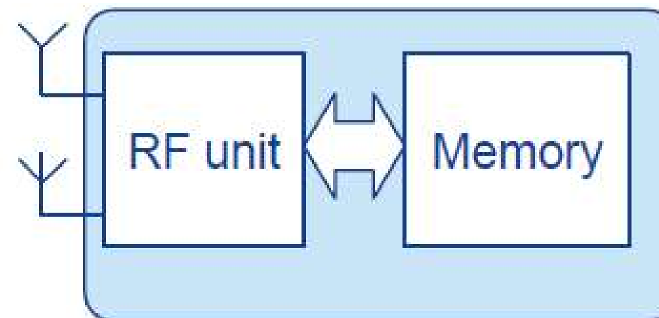
PCM Applications

- **Low to mid–end mobile phones**
  - NOR replacement with better performance:
    - Higher throughput
    - Single bit overwrite
  - Execution in place (XIP)
- **PCM SSD prototype**
  - Improved performances vs. NAND SSD
  - Much higher cost
- **Wireless Memory**
  - TAG (RF Memory TAG System)

Asha phones

IMW 2012 Nokia/Micron

Wireless memory



RF memory tag

Without battery

PCM SSD prototype

		PCM Prototype SSD	NAND NAND SSD
System Interface		PCIe 3.0x8	PCIe 2.0x8
Sector Access Granularity		4096 byte	4096 byte
Random Reads	Bandwidth	5.5 GB/s $>$ 1M IOPS	3.0 GB/s 725,000 IOPS
	HW Latency	5μs	~50μs
	SW Latency	TBD	
Random Writes	Bandwidth	~625 MB/s	400 MB/s
	HW Latency	$\leq$ ~204 μs	300 μs
	SW Latency	TBD	
Density		64 GByte	350GB, 700GB
Total Pbytes (Life)		$\geq$ 120 PB	25 PB (350GB)

G. Atwood, **"Phase change memory: device physics, reliability and applications"**, Springer 2018

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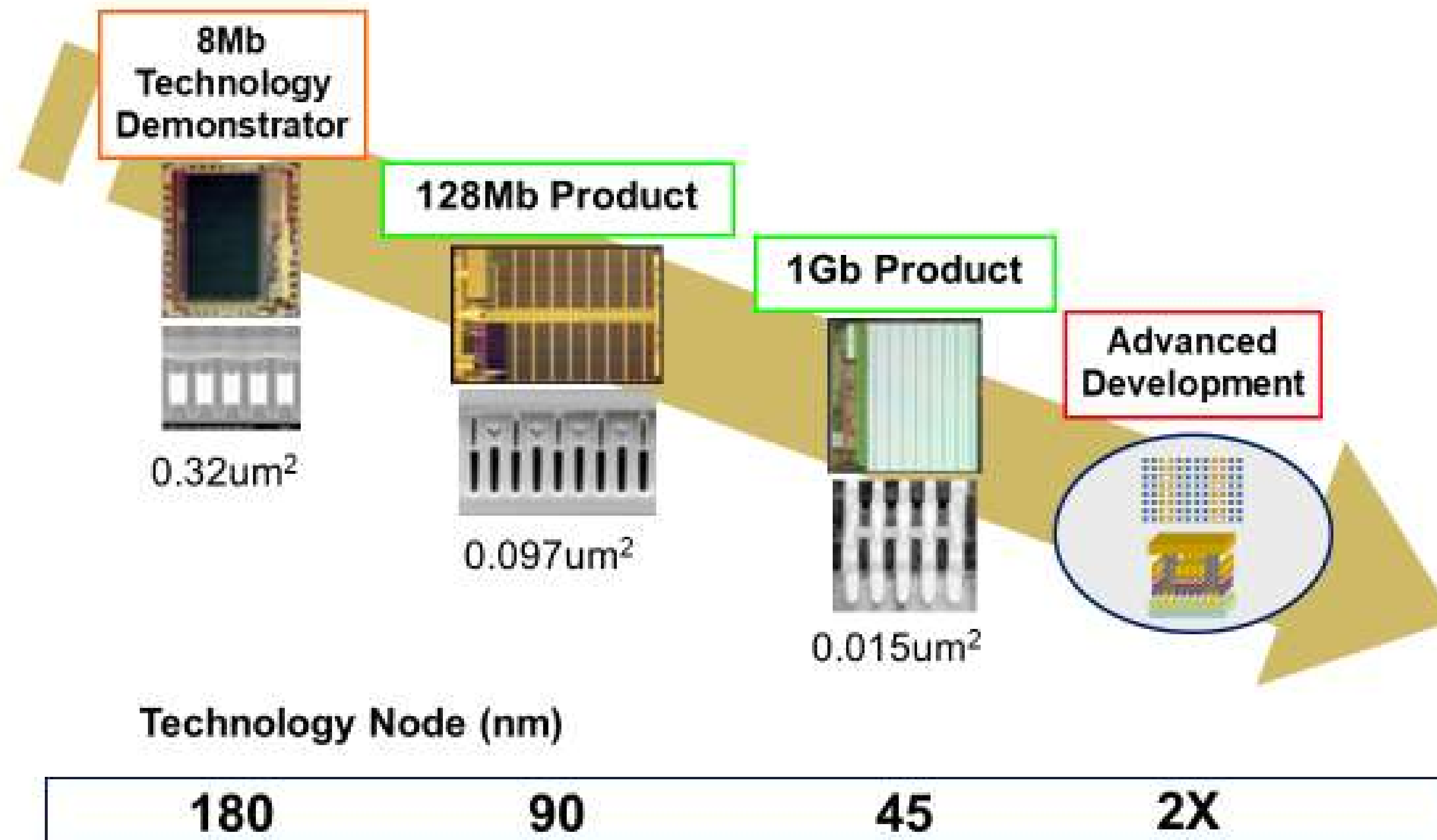
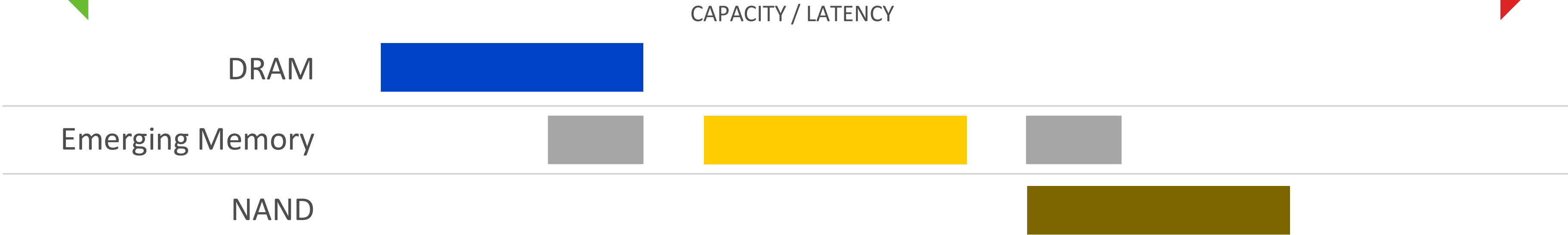
From my 2012 Presentation



- PCM technology was capable
- Scaling path showed insufficient market opportunity

Addressing the Performance Gap

Evolving Memory Architecture



Balancing Values: Latency, Endurance, Volatility, Cost

	DRAM	Storage Mapped	PCM*	RRAM*
Latency	1x	2x-10x		
Endurance	~10^{15}	~10^{7}		
Non-Volatility	NO	YES		
Areal Density	DRAM	~10x DRAM		

*** Color codes referred to "Storage Mapped" specifications**

Addressing the Performance Gap

Evolving Memory Architecture

Balancing Values: Latency, Endurance, Volatility, Cost

	DRAM	Storage Mapped	PCM*	RRAM*
Latency	1x	2x-10x		
Endurance	~10^{15}	~10^{7}		
Non-Volatility	NO	YES		
Areal Density	DRAM	~10x DRAM		

→ **Cross Point stackable cell**

*** Color codes referred to "Storage Mapped" specifications**

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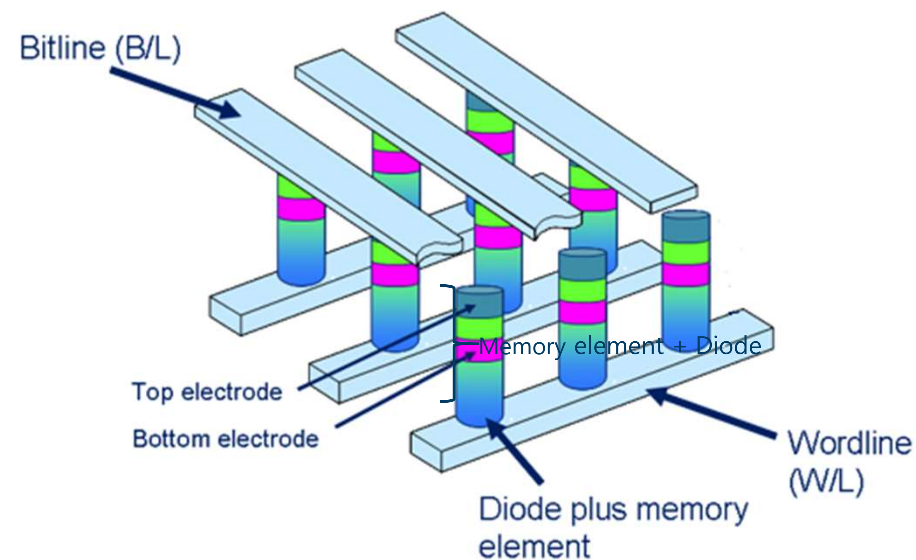
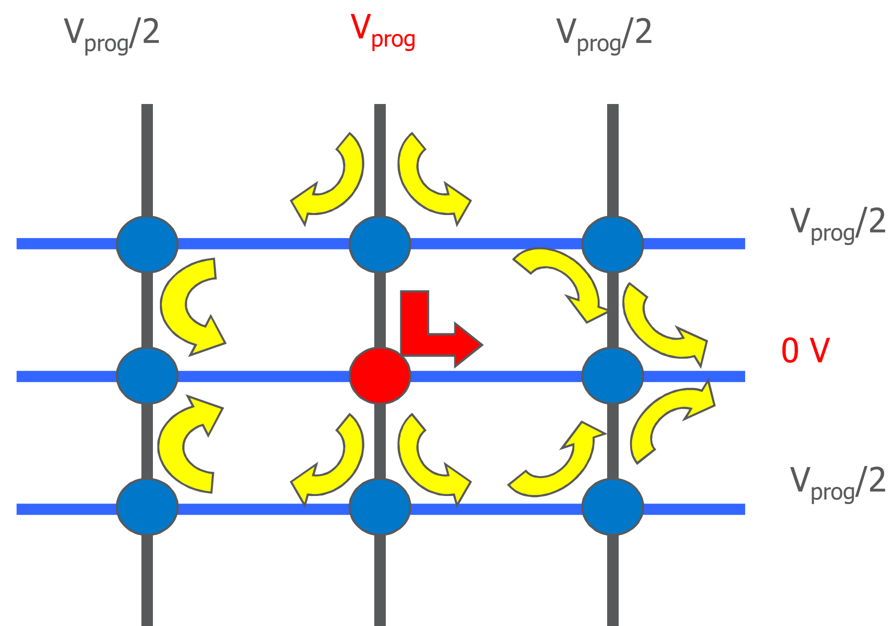
Cross Point Memory Architecture

- To compete in the mainstream memory market, cost must be competitive. 3D stacking is required for any emerging memory.
- The cross point memory attracts great interest
  - "Simple" structure and minimum cell size ($4F^2$) → low cost
  - Suitable for 3D stacking → cell size $(4/n)F^2$
  - Array over circuitry → better array efficiency
- The cross point's 2-terminal architecture requires a selector device to be integrated in the BEOL
  - Parasitic paths exist through neighboring cells
  - Programming and reading can disturb the array





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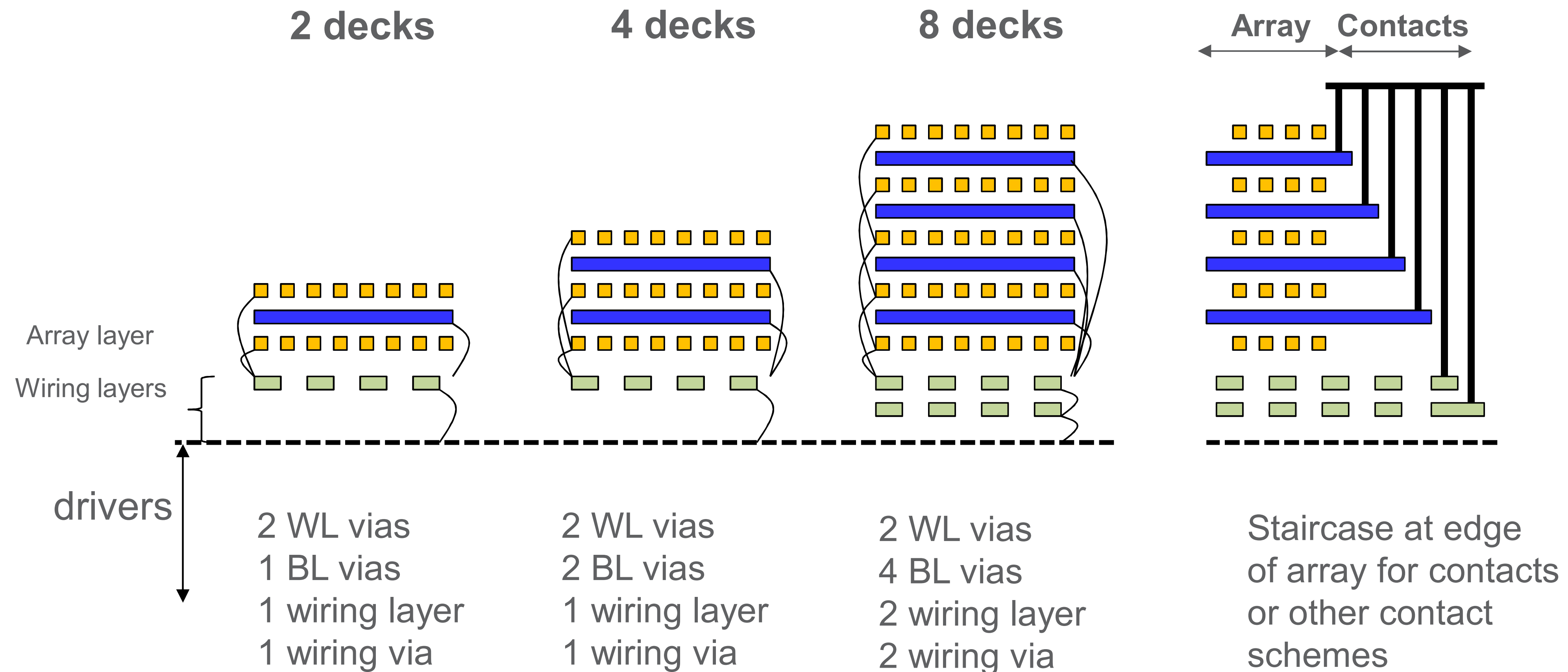
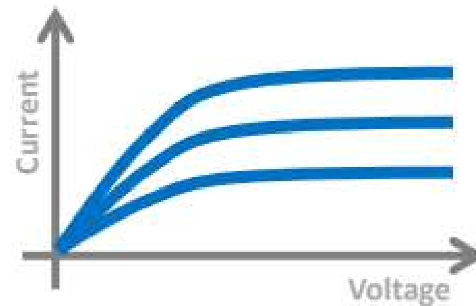
Planar 3D Stacking



- As the number of decks increases, interconnect and via levels increase
- Cost Increases, complexity increases

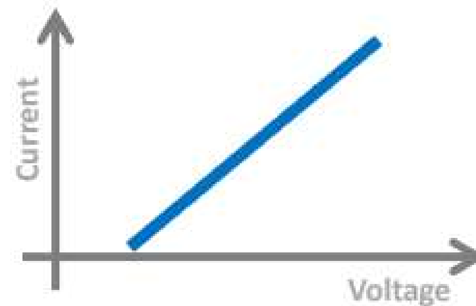
Selector Types

Transistor
3-Terminal



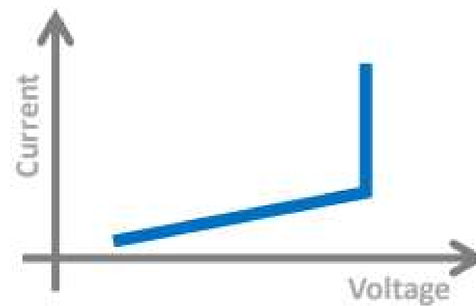
- High ON current to program
- Low OFF current to suppress sneaks paths
- Need a third terminal! Usually is $6F^2$.
- High performance can be achieved

Non-Thresholding
2-Terminal



- Achieving High ON current and simultaneously achieving low off current is difficult with these selectors
- Moderate performance is expected

Thresholding
2-Terminal



- Minimum foot-print ($4F^2$)
- Both high ON current and low OFF current can be achieved with relatively low non-linearity
- High performance can be achieved

Nirmal Ramaswamy, 2017 IEDM Short Course

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Cross Point Selector Requirements

- Selector device requirements:
  - Very high forward bias current when selected
    - Greater than the switching current
  - Low deselect current
    - Prevent loss of signal
    - Leakage may set the block size
  - Composition compatible with memory material
  - Low temperature process
  - Bipolar operation is preferred

- Selector device options:
  - Homojunctions → poly Si p/n junctions
  - Heterojunctions → p-CuO/n-InZnO
  - Schottky diode → Ag/n-ZnO
  - Mixed Ionic Electronic Conduction (MIEC) materials
  - Thin-film chalcogenide selector

- In addition, selector reliability must be capable of meeting the cell reliability requirements.

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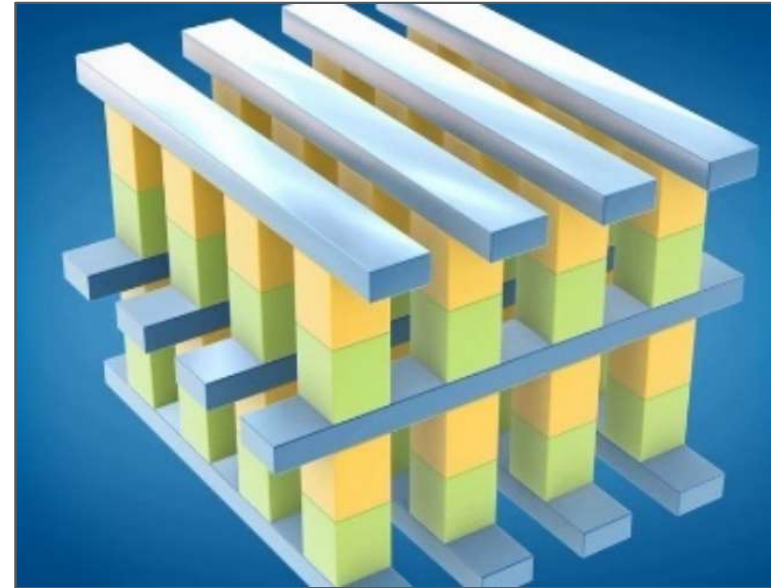
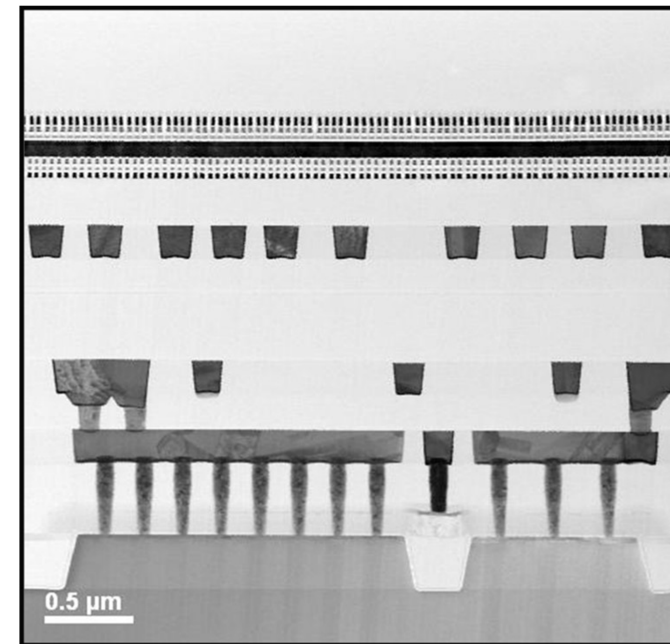
3D XPoint™ Technology

- Cross Point architecture
  - Storage element
  - Fast and reliable switching device based on thin-film material
  - Circuitry under the array
  - 2 decks of 64Gb each
- 3D XPoint key advantages
  - Better performance than NAND and lower cost than DRAM
  - Low-latency and fast writes
- Intel and Micron announced 3D XPoint technology in 2015. Objective Analysis (2019 Flash Memory Summit) predicts that 3D XPoint media revenue will grow to more than $3 billion in 2023.



Storage element
+
Switching element



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Conclusions

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Conclusions

- The semiconductor memory market is rapidly expanding, fueled by new market trends.
- Conventional NAND and DRAM currently dominate the market and should continue to do so in the near future.
- Most memory technologies have developed or are investigating 3D architectures due to limitations with 2D scaling.
  - 3D capability is a requirement for any emerging memory seeking to replace the incumbents.
- There is an opportunity for a storage class memory to improve system level performance. SCM could create a significant market opportunity for a new memory.
- Success of emerging memory as an SCM depends both on the technology's capability as well as enabling the ecosystem.
- With Intel/Micron's vertical integration capability, 3DXpoint™ is the ideal candidate as an SCM both in the storage and memory replacement.

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