STT-MRAM Technology and Productization

NCCAVS
Thin Film Users Group (TFUG)
ADVANCED MEMORY
Thursday April 21, 2016

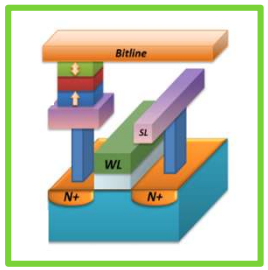
4/21/2016

Outline

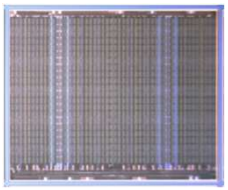
- *Introduction*
- *Key process technologies*
  - *Core MTJ process*
  - *BEOL process integration*
- *Performance with Avalanche stand-alone chips*
- *Embedded solutions*
- *Summary*

Avalanche Technology — at a Glance

Breakthrough pMTJ STT MRAM Technology



Stand-alone ***SPMEM***™



Avalanche 64 Mb chip

Embedded ***AvRAM***™

Large Markets

Enterprise Storage, Mobile, Telecom & Computing

Founded in 2006

Led by an Experienced Team

Industry Veterans Delivering Innovative Storage Solutions

Supported by extensive patent portfolio

250+ patents filed
with 190+ granted/allowed

Backed by Top Tier VCs

THOMVEST VENTURES

VTB Capital INVESTMENT MANAGEMENT

RVP

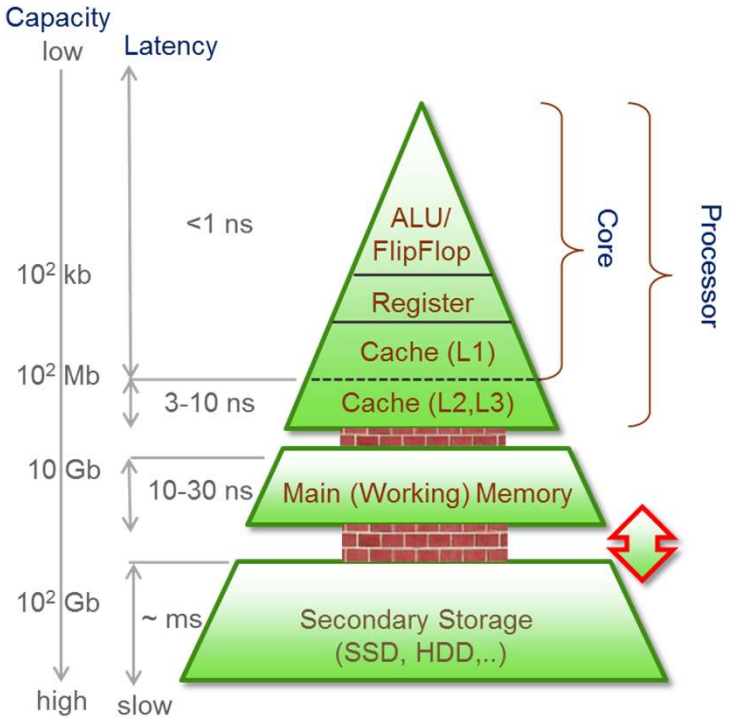
VULCAN Capital

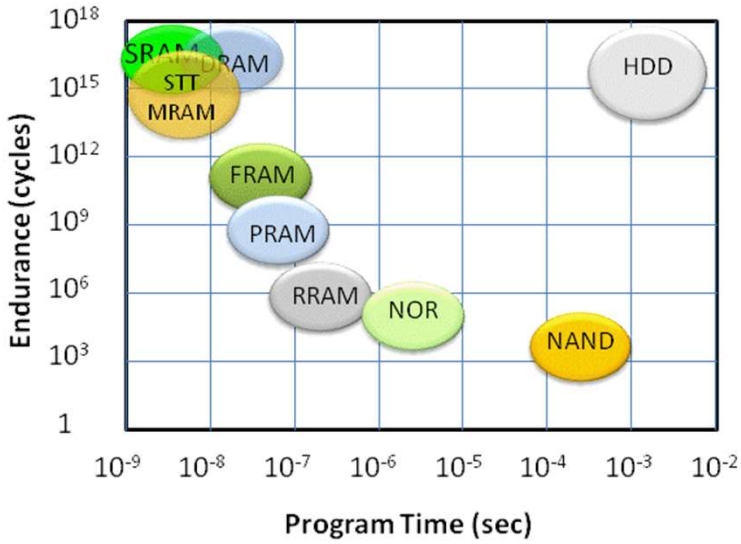
3

avalanchetechnology

Increasing Needs for Emerging NVM

- Existing memory technologies facing increasing challenges beyond 20 nm
- Need low power consumption for mobile/wearable applications and data centers
- Memory performance is increasingly limiting system performance





Endurance and program time comparison of memory technologies

STT-MRAM boasts unique combination of high speed and low power with unlimited endurance

avalanchetechnology

STT-MRAM: A Wide Range of Applications

Stand Alone Applications

- Memory buffers
  - Persistent DRAM
- Battery backup SRAM
- DRAM
- New Market Applications
  - Storage class memory (L4)

STT- MRAM

Embedded Applications

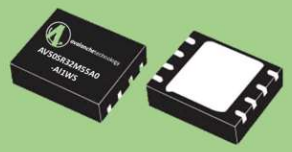
- eNVM
  - eFlash, eOTP, eFuse
- Cache Memory
  - L3,L2..
- eDRAM
- New Market Applications
  - Low standby-power connectivity systems (IoT, wearable electronics)

- **High speed**
- **Low power consumption**
- **Low manufacturing cost**

avalanchetechnology

Industry's Leading pMTJ 55nm STT-MRAM Chip on 300mm Wafers (Avalanche Jul/2015 PR)

Avalanche Quad SPI SPNOR™



10X Faster Program compared to SPI NOR FLASH and Byte Alterable

Avalanche Quad SPI SPMEM based on proprietary pMTJ delivers faster program time (<32us per page), very high endurance (> 100 million) and 20 Years retention @85°C

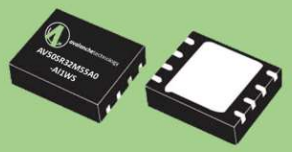
Key Features

32Mb 55nm STT-MRAM Technology
Dual/Quad SPI Interface (108MHz)
Byte Alterable (No Erase)
Fast Write > 3MB/s
Endurance > 100 Million Writes
Retention 20 Years at 85C
Industrial Temp -45C to 85C

Applications

Raid Storage
Power fail storage
Setup box and LCD display
Digital consumer applications

Avalanche Quad SPI SPSRAM™



Fastest and Largest Density NvSRAM achieving 50MB/s Write and Read throughput

Avalanche Quad SPI SPMEM based on proprietary pMTJ delivers SRAM speed (50MB/s), very high endurance (>1 Billion) and 20 Years retention @85°C

Key Features

32Mb 55nm STT-MRAM Technology
Dual/Quad SPI Interface (100MHz)
No wait write
Fast Read & Write > 50MB/s
Endurance > 1 Trillion Writes
Retention > 20 Years at 85C
Industrial Temp -45C to 85C

Applications

Internet of Things (IOT)
Automotive Crash Recorder
Digital consumer application
Smart Meters

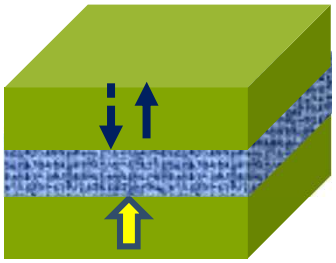
- Fully functional chip with Industry standard SPI and SRAM mode
- Manufactured with 55 nm LP CMOS at world class foundry
- In customer sampling

avalanchetechnology

MRAM Building Block: Magnetic Tunnel Junction (MTJ)

MTJ basic structure:

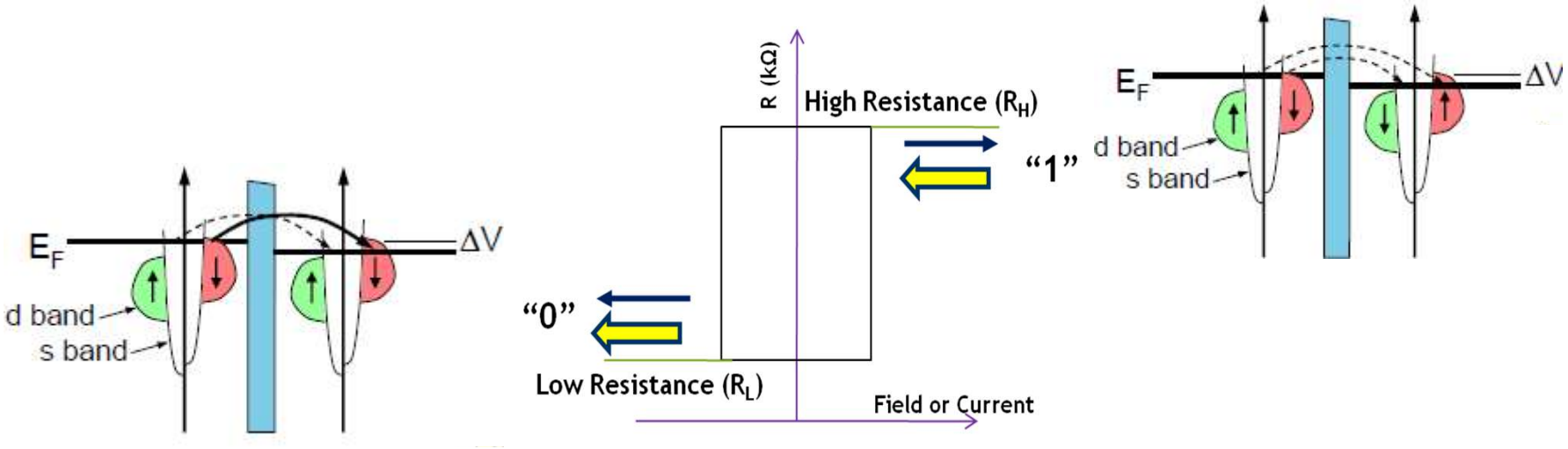
Perpendicular MTJ



TMR>200%

Tunnel barrier -MgO

- Information stored by magnetic polarization (nonvolatile), not by charge
- Well understood physics and materials

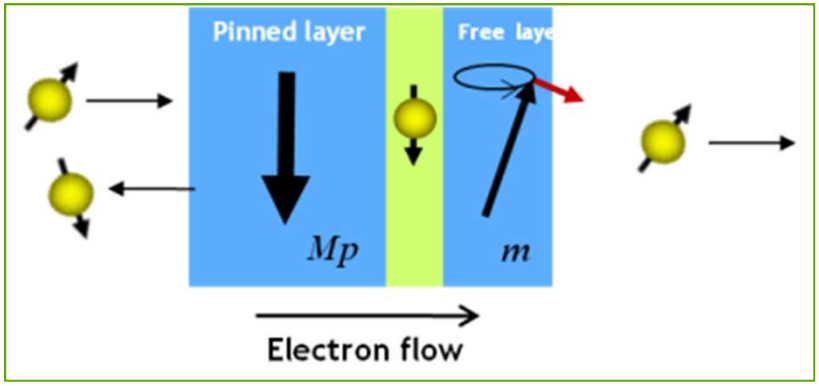


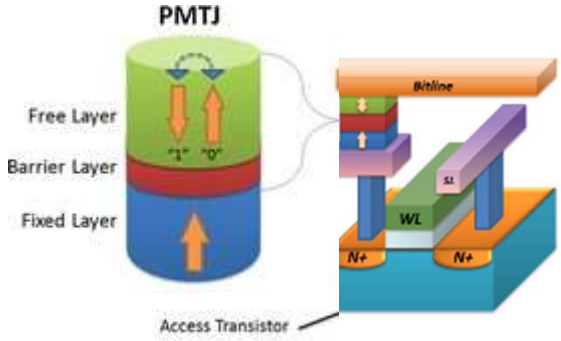
- In-plane MTJ widely used in HDD read heads and field MRAM applications
- pMTJ desirable for STT-MRAM due to improved data retention and scalability

Spin-Transfer Torque (STT) MRAM – Write Mechanism

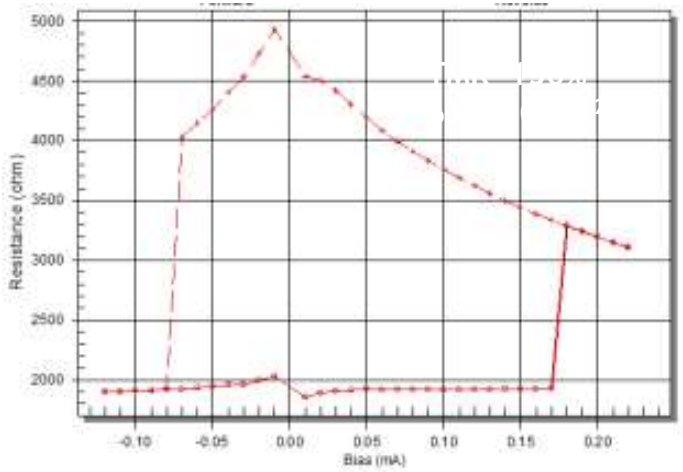
Switching magnetization direction by using spin current, instead of Oersted field

Spin Transfer Torque Writing in MTJ





STT-MRAM Schematic using

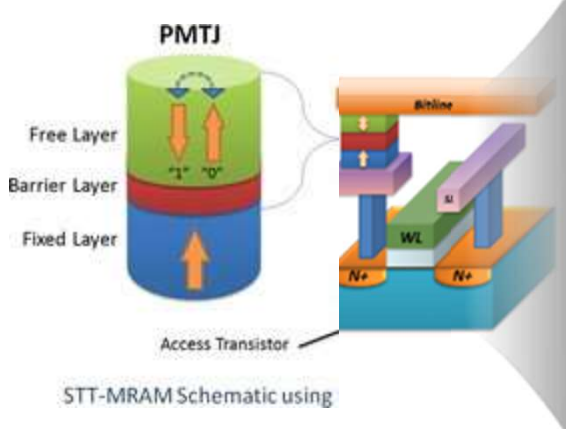


A revolutionary writing technology for MRAM

- Much more energy efficient: lower current & power consumption
- Highly scalable down to 1x nm
- Local, rather than long-range Oersted field: no neighboring bit disturb

avalanchetechnology

pMTJ: Enabling Disruptive STT MRAM



STT-MRAM Schematic using

1. **High TMR ~200% (targeting 300% in near future)**
   → fast read speed and high read margin

2. **Thermally stable TMR at up to 400 ^{o}C >one hour**
   → fully compatible with standard CMOS process (embedded memory applications)

3. **Low write current (~*F* uA) with high speed (sub ns)**
   → - low power and high performance embedded memory applications;
   - High density (Gb) memory

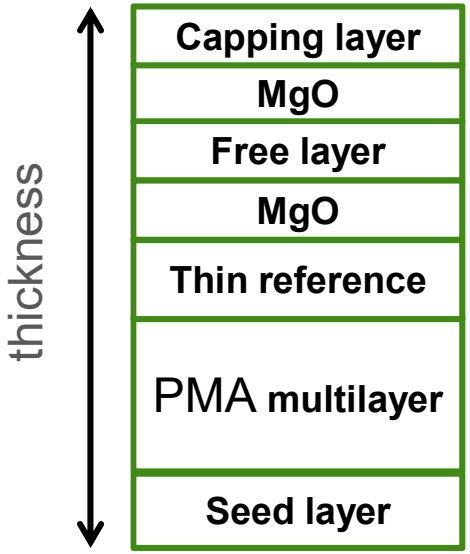
4. **High thermal stability Δ: >10 years data retention** (at up to 150^{o}C)

5. **High Endurance> 10^{16} cycles**

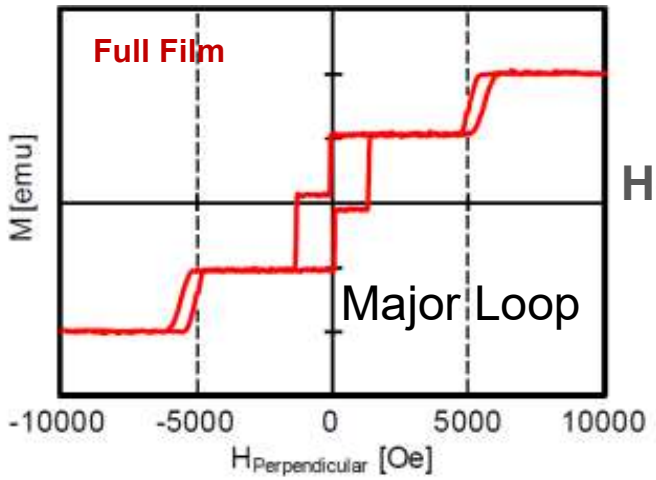
6. **Excellent Manufacturability**
   1. Circular pMTJ bit
   2. Very thin MTJ stack <150 Å (scalability to 1x node)
   3. High thermal budget

pMTJ delivered all attributes required for a disruptive NVM

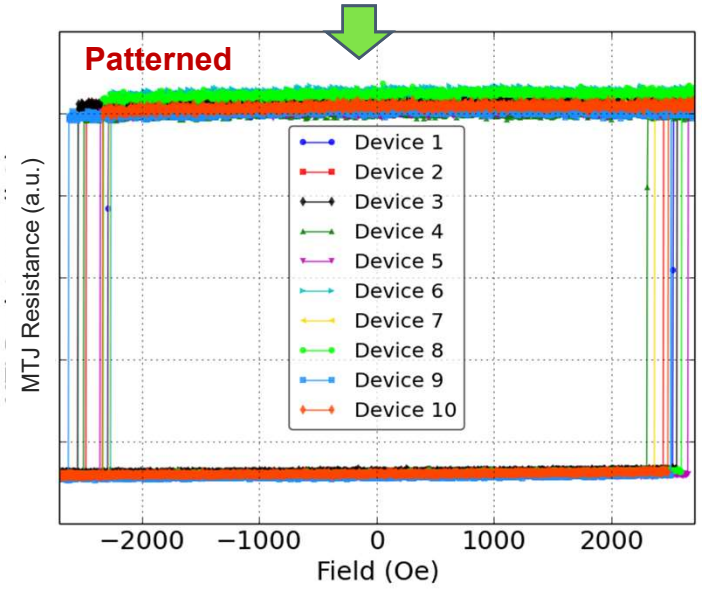
Robust pMTJ Design and PVD Process



RA ~10 Ohm μm^2
TMR > 200%
Total Thickness <150Å
After 400°C 60 min. anneal.



Hex>5kOe

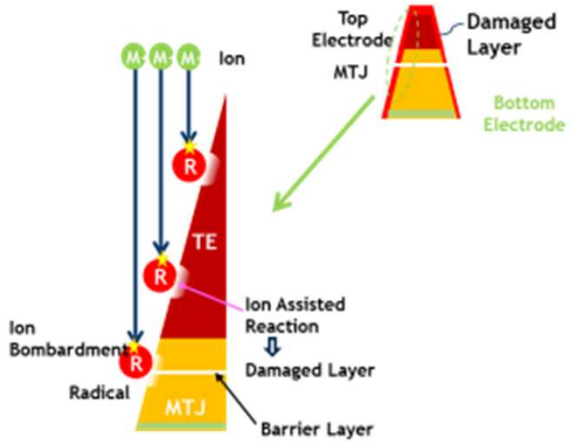


>3kOe Hc feasible with further design/process optimization - critical for HT retention

avalanchetechnology

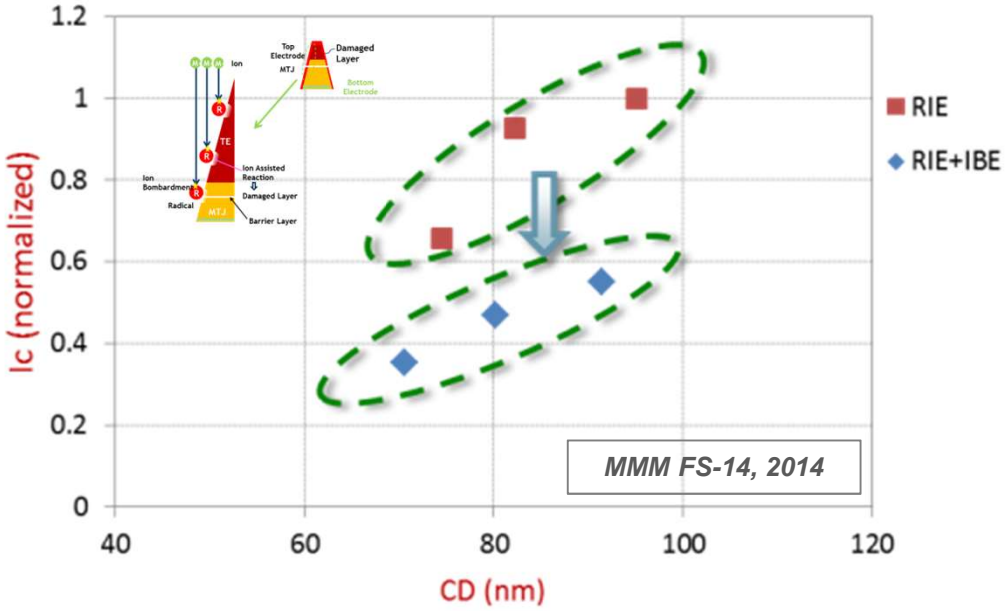
Advanced MTJ Etch Process

- Chemical-damage-free etch
  - Improve device-level TMR and STT efficiency (next slide)



- MTJ etch profile - BEOL metallization margin improvement (proven)

Chemical-damage-free Etch - Electrical Validation

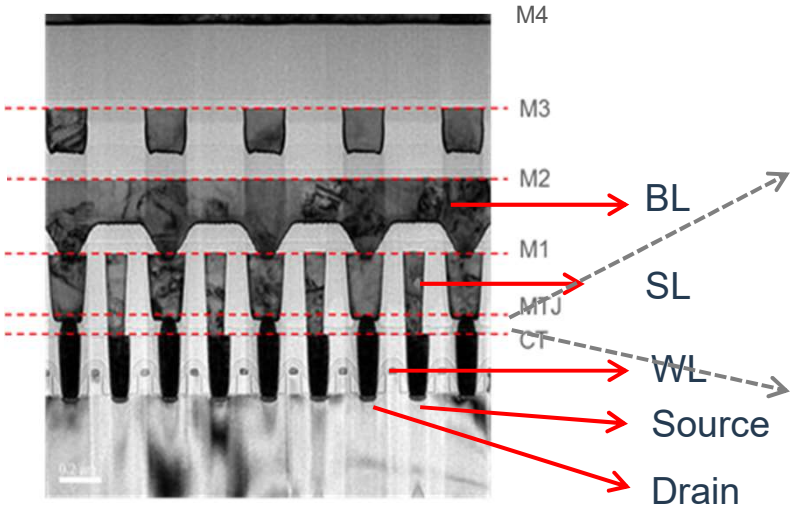


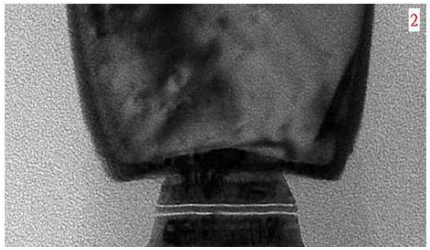
- Ic at fixed electrical CD (switching current density) improved by up to 40%
  - Attributed to physical removal of chemically damaged layers
- Device-level TMR also improves by up to 20%

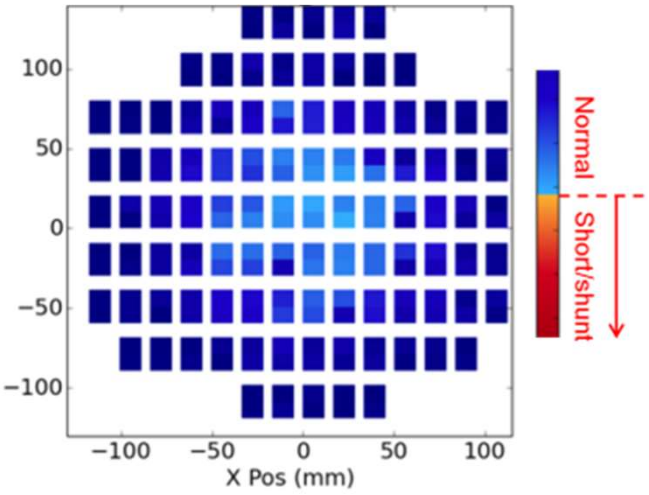
Advanced 300 mm BEOL Integration

Paper AB-07, INTERMAG, 2015

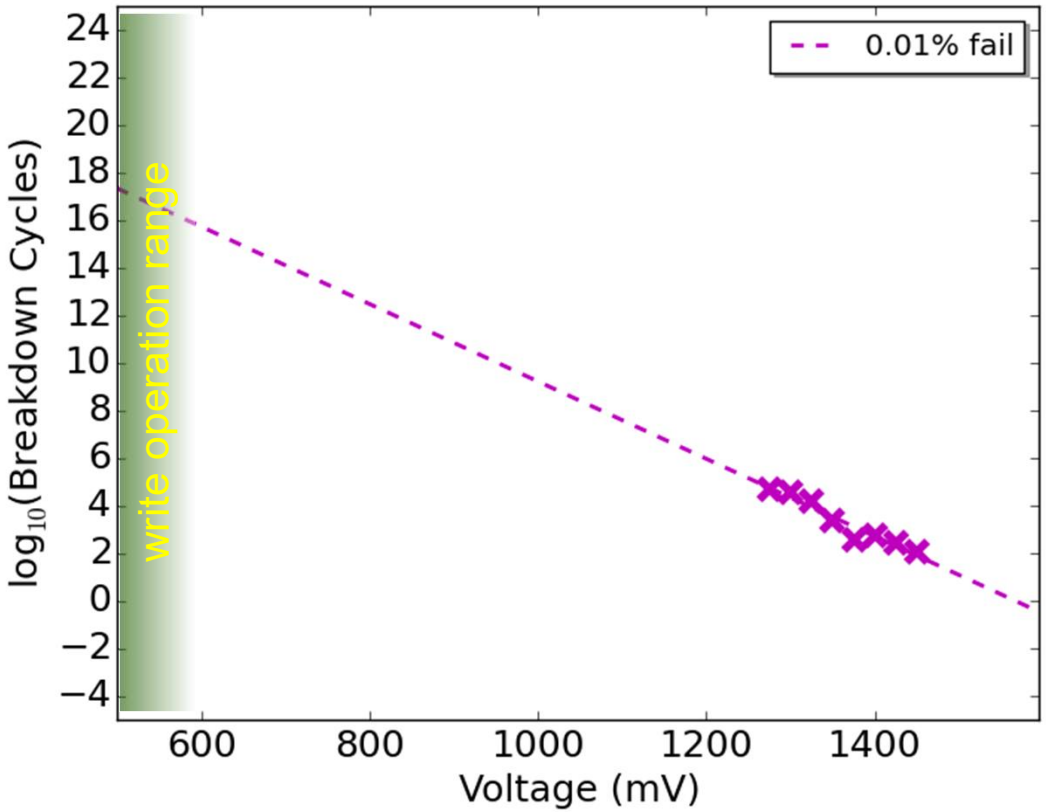
- Early adoption of 300mm process
  - Demonstrated ppm/sub-ppm level integration bit yield loss
- Low cost adder – MTJ etch with single mask
  - Scalable (<1xnm) MTJ BEOL integration process flow (portable to any foundry)
- TMR thermally stable up to 400 °C, compatible with embedded applications
  - Allow MTJ placement in lower metal layers (for smaller cell size)





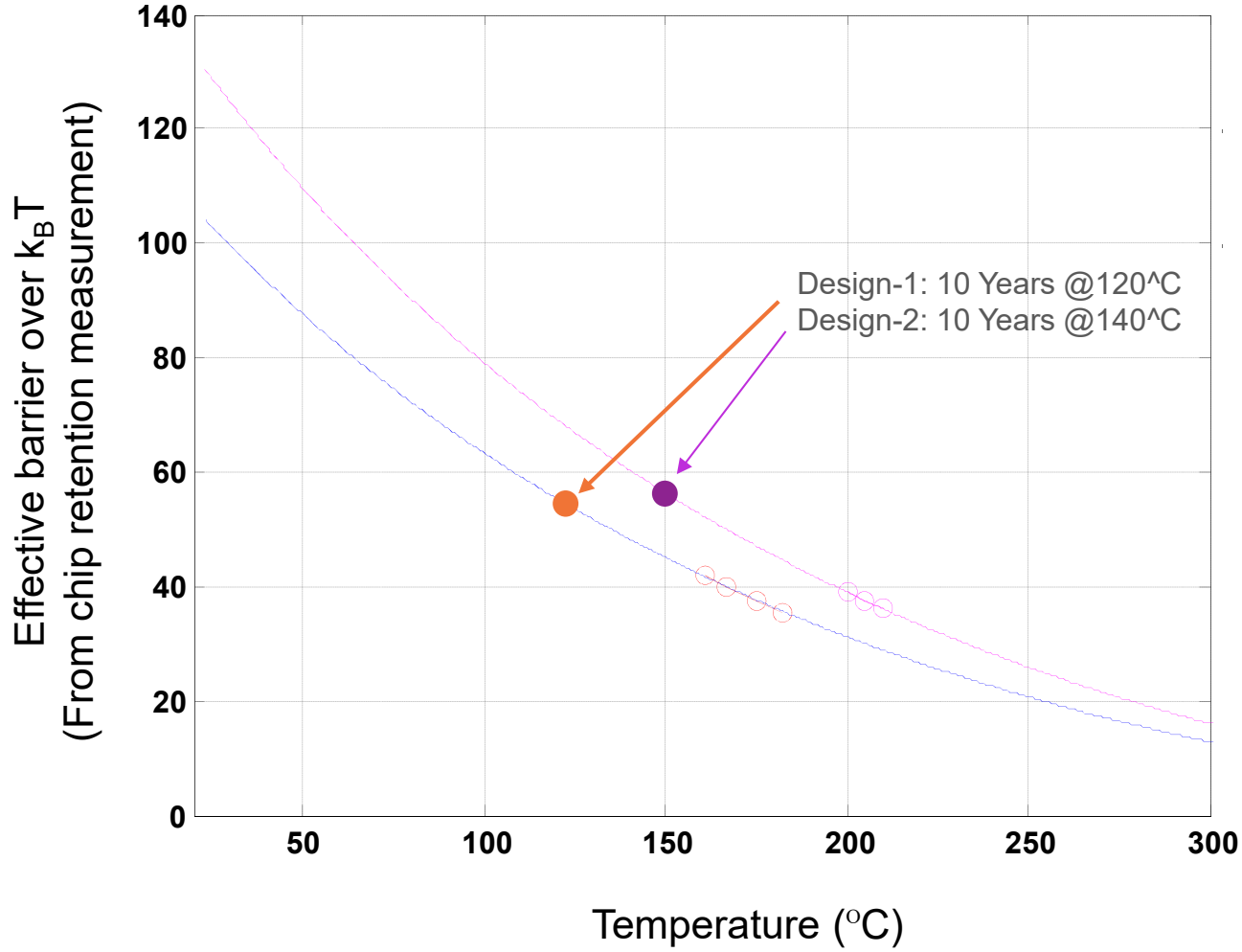


pMTJ STT-MRAM Shows Excellent Endurance



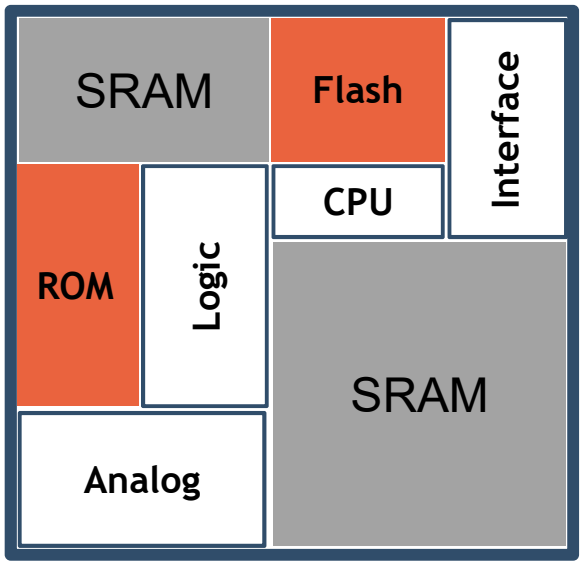
- >10^16 endurance based on TDDB results
- Excellent endurance further validated by full-chip cycling (test time limited)

Data Retention



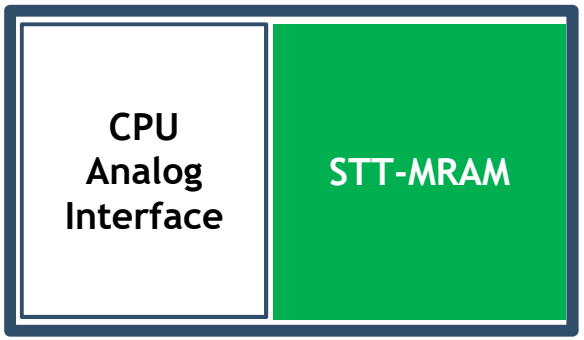
STT-MRAM - Disruptive Embedded Memory Solution

SoC with multiple memories



1.0X

45% die size saving



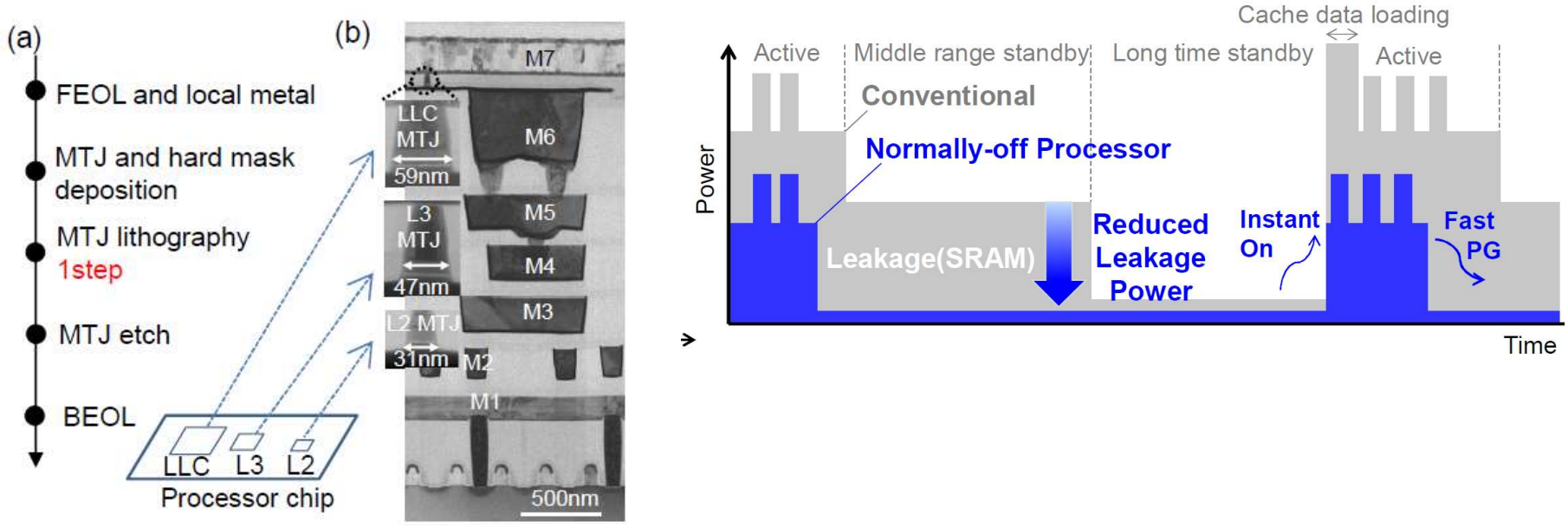
0.55X

eSTT-MRAM delivers cost and performance advantages

- *Smaller die size due to converged memory*
- *Simplified system architecture enhances performance*
- *Highly reliable nonvolatile memory*
- *Modular integration with CMOS – Ava advanced integration scheme allows MTJ placement between any 2 metal layers*

avalanchetechnology

MTJ-Based "Normally-Off Processors" (2015 IEDM, Toshiba)

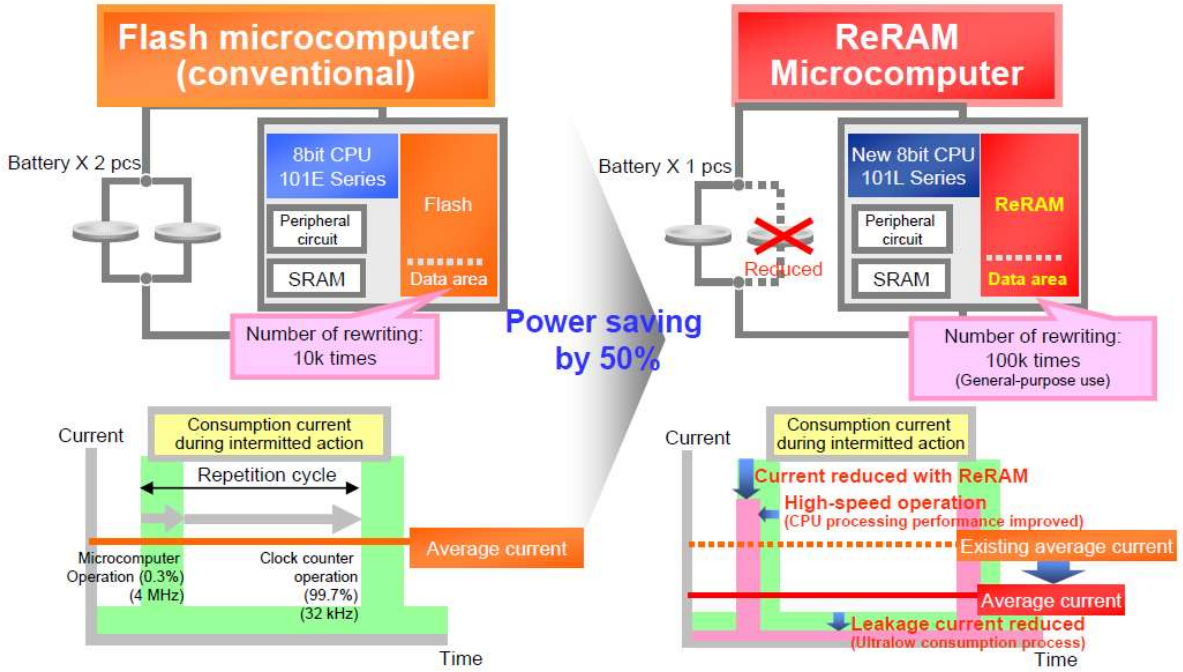


- *Compared to conventional processors, with low power pMTJ-based memory hierarchy*
  - *CPU power reduced by 65%*
  - *Chip area reduced 37%*

Commercially Available Embedded ReRAM (Panasonic)

50% lower power consumption with ReRAM and high-performance CPU

Thanks to low-power consumption ReRAM, shorter processing time and voltage control by high-performance CPU, and leakage current reduction of new fabrication process, power consumption has been reduced by 50%, compared to the existing Flash microcomputer.



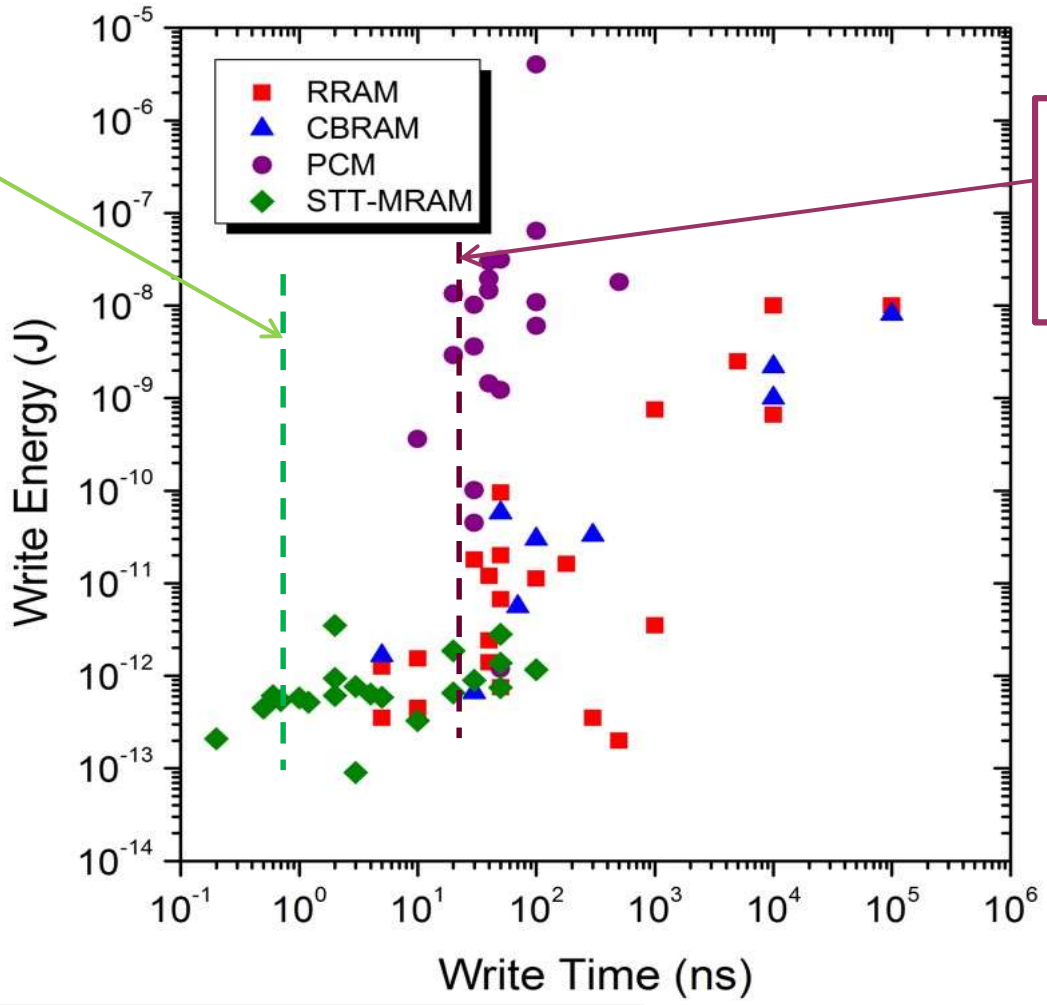
		①低電力タイプ	②汎用タイプ
CPU		8ビット 101Lシリーズ	
内蔵メモリ容量	ReRAM	128KB（プログラム領域）＋8KB（データ領域）	
	RAM	2KB	8KB
タイマ	8bit / 16bit / RTC	6本 / 3本 / 1本	
シリアルIF	UART（同期式兼用）/ IIC	3本 / 1本	
A/D コンバータ		–	12bit：16ch
DMA		1ch	
LCDドライバ端子		SEG:51、COM:4	
ピン数/パッケージ		100ピン/LQFP（14mm角）	
動作範囲（最高動作周波数）		1.1～3.6V（500kHz） 0.9～3.6V（64kHz）	1.8～3.6V（10MHz） 1.1～3.6V（64kHz）

- Panasonic 8-bit MCU with embedded ReRAM (announced 2013)
  - 50% power consumption reduction vs. flash
  - Endurance (per datasheet) - 100K data area

Energy vs. Speed: Emerging NVMs

STT-MRAM is the fastest NVM; only NVM w/ unlimited endurance

Fastest NVM Solution



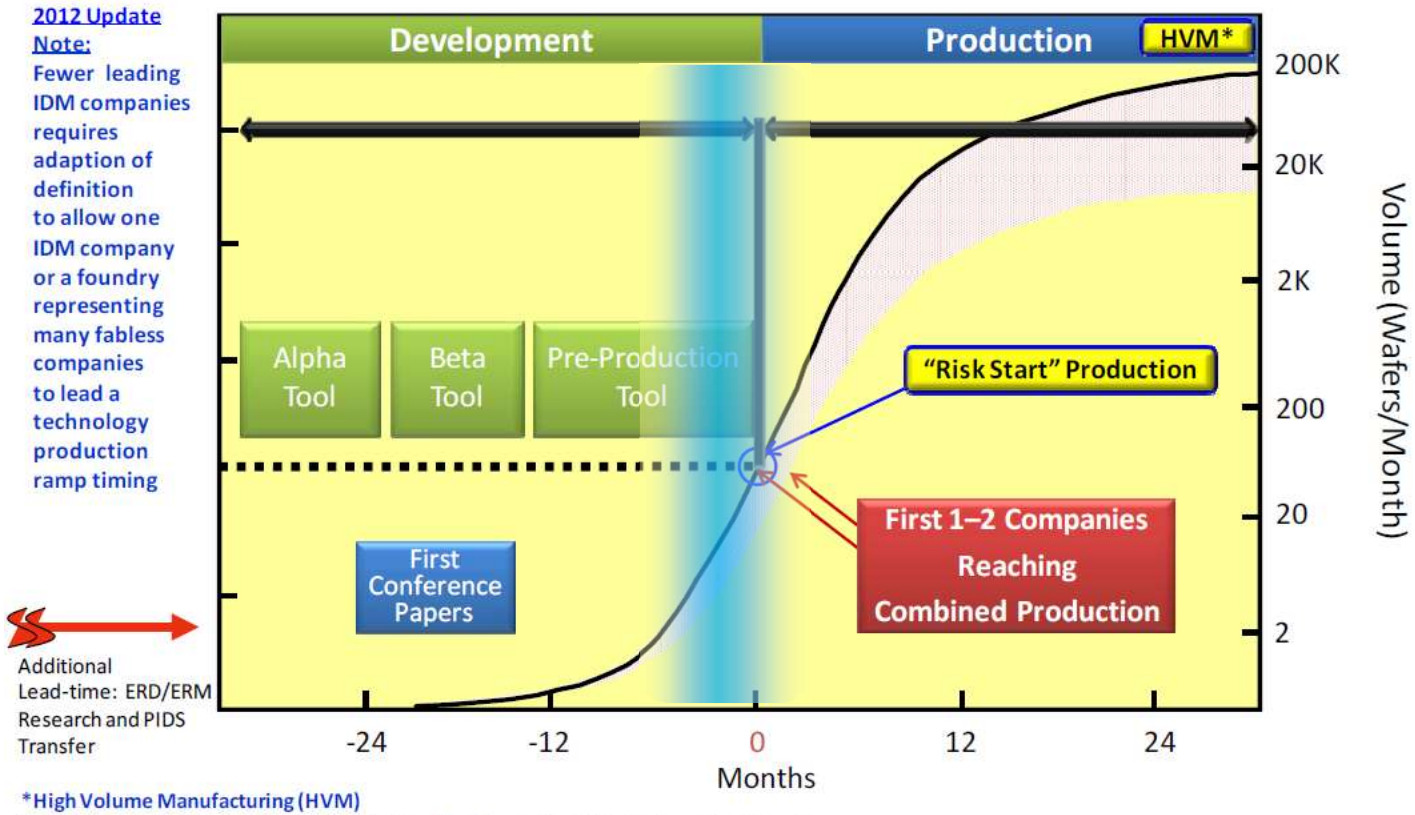
Speed limited by Basic Switching **Physics**

Source - https://nano.stanford.edu/stanford-memory-trends

Where are We with STT-MRAM?

ITRS generic view of new technology launch and Production Ramp-up

2013 ITRS Figure X [unchanged from 2012 ITRS version: Production Ramp-up Model and Technology/Cycle Timing



*High Volume Manufacturing (HVM)

Source: Semiconductor Industry Association. The International Technology Roadmap for Semiconductors, 2011 edition. SEMATECH: Albany, NY, 2011. Based on Figure 2a, Executive Summary

Summary

- *STT-MRAM mechanism is well established and understood*
- *Production-worthy MTJ technology is ready for market entry*
  - *Full-chip functionality and reliability have been validated by customers*
  - *However, there is always room to improve ……*
- *Yield/cost is at tipping point to cross development finish line for productization*
  - *Process/performance margin and tail bit containment is critical*
- *Coherent efforts by all stakeholders in ecosystem needed to gain critical momentum*
  - *Upstream – tool vendors (process, test, EDA, etc.)*
  - *Downstream – system designers and application developers*

THANK YOU

46600 Landing Parkway – Fremont CA 94538 – T: 510| 897-3300 – F: 510| 438-0143 – www.Avalanche-Technology.com