NAND Flash: Where we are, where are we going?

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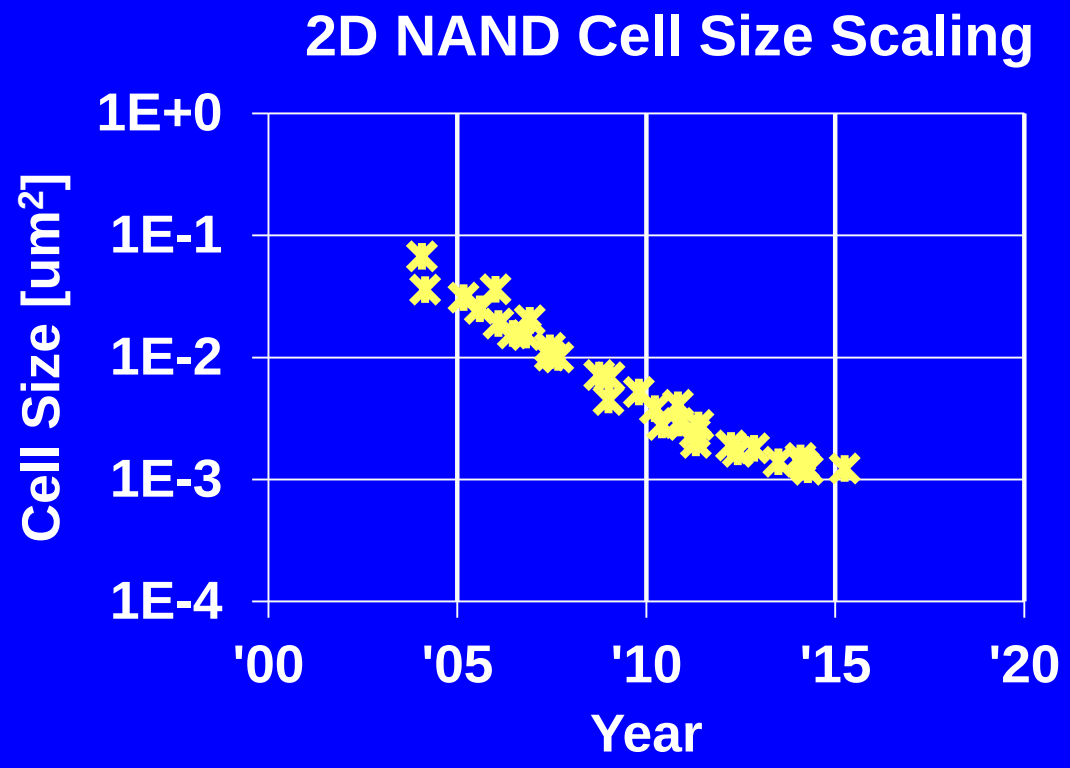
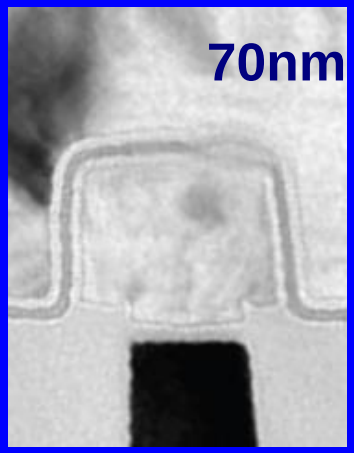
Intel Corporation

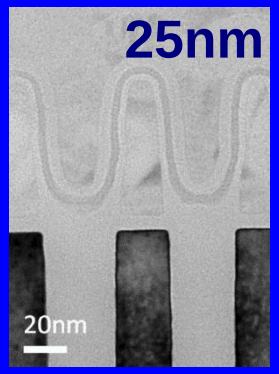
Outline

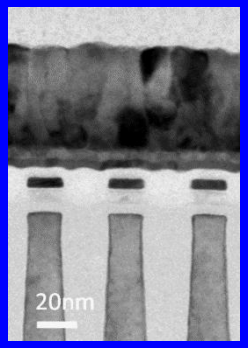
- Introduction
- 3D NAND
- Floating Gate 3D NAND Technology
- CMOS Under Array
- Cell Characteristics
- Summary

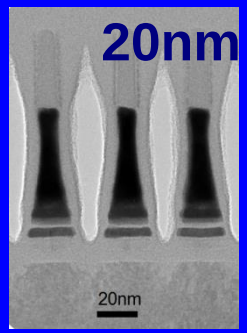
NAND Scaling Trend







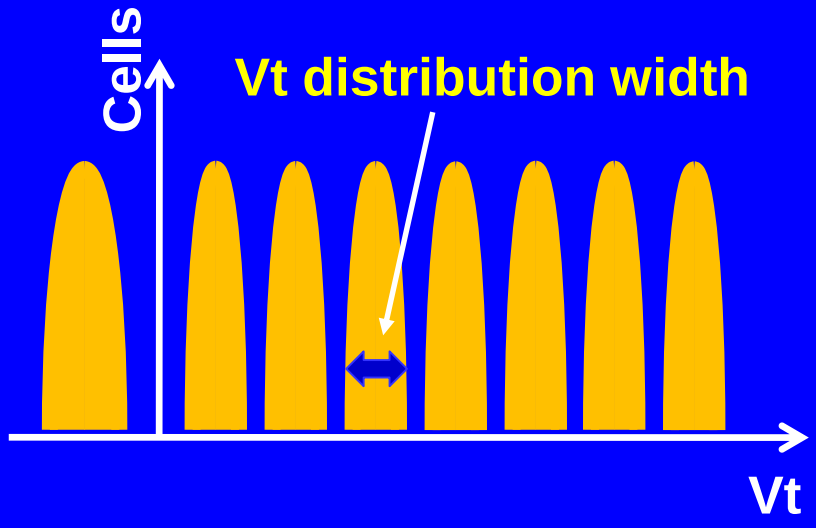


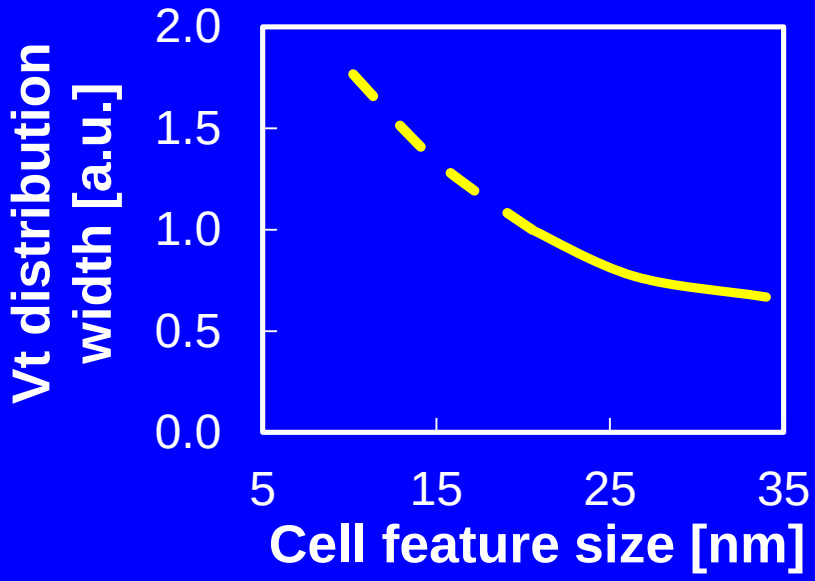


2D NAND scaling has slowed down

2D NAND Scaling Limiters

- Lithography Limitations
- Small Cell Area Effects: Number Fluctuation
- Proximity Effects: Cell to Cell interference
- High Electric Field Effects





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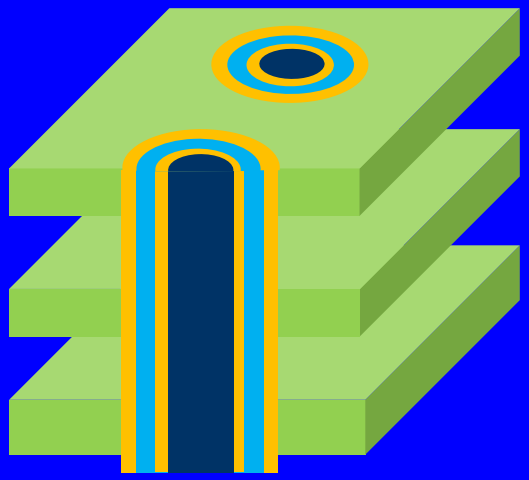
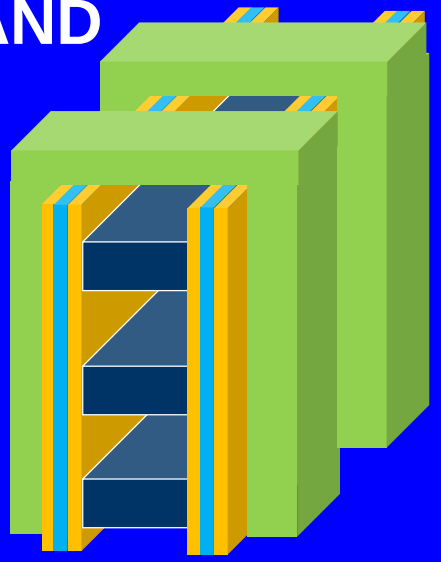
3D NAND - Scaling Through Stacking

Vertical channel 3D NAND



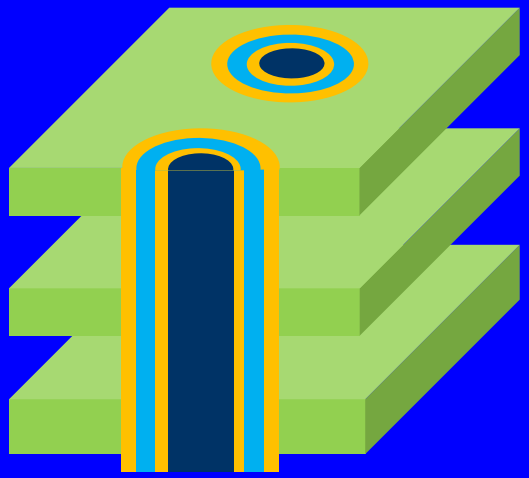
Horizontal channel 3D NAND

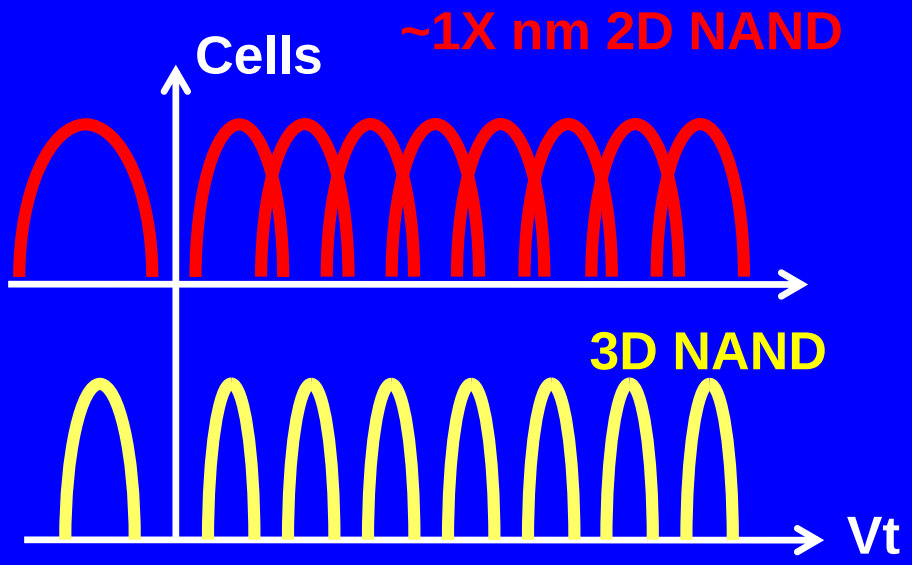


Vertical String vs. Horizontal String

- Vertical string more attractive electrically
- Horizontal string more attractive for cell size

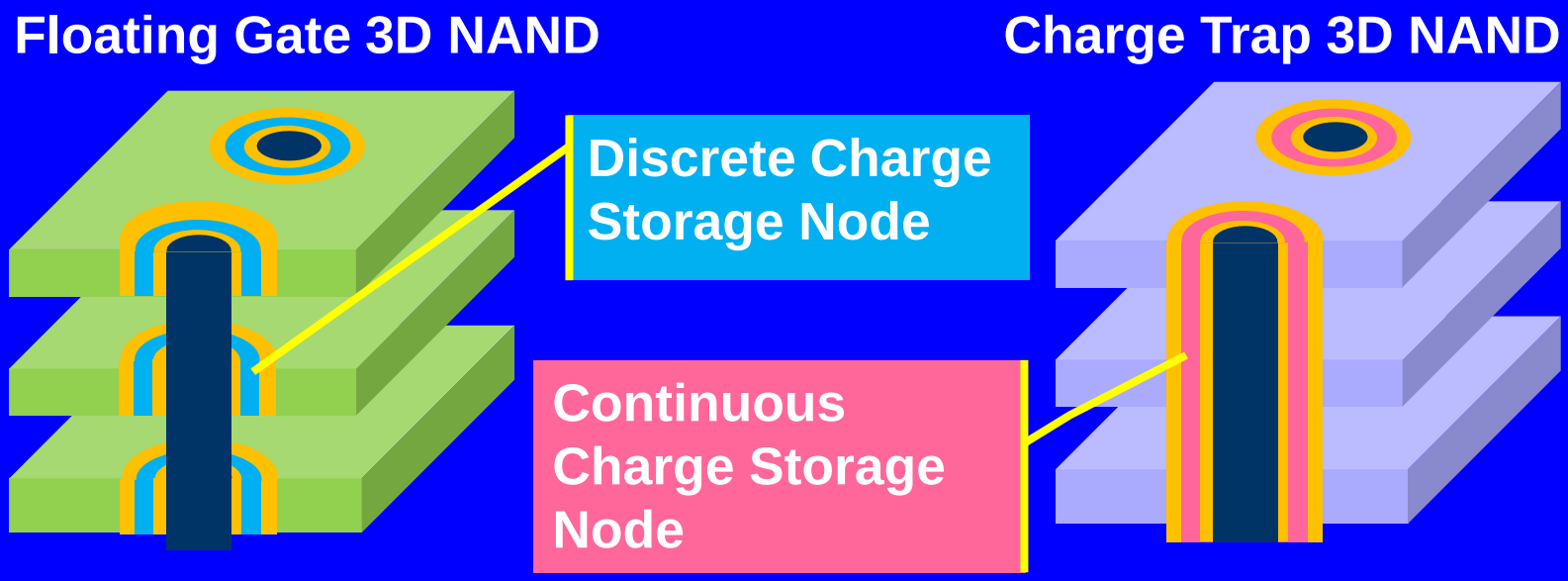
3D NAND Advantage





- Eliminates lithography constraint
- Larger cell size and cell to cell spacing ➔ Less parasitic effects and tighter threshold voltage distributions

3D NAND – Floating Gate vs Charge Trap



- Floating Gate – Good Program/Erase Vt window and Charge isolation between cells
- Charge Trap – Charge dispersion between cells & Need for Metal Gate process

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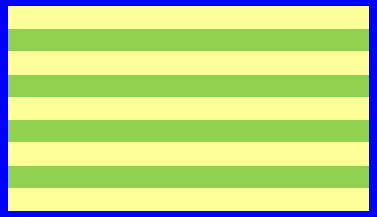
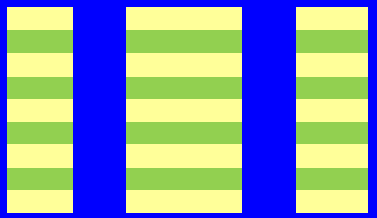
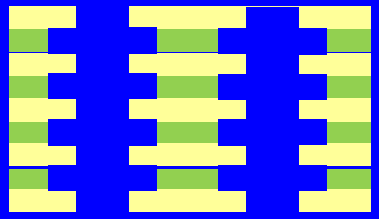
3D FG NAND Cell Formation



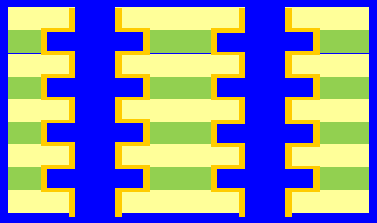
(a) Tier deposition



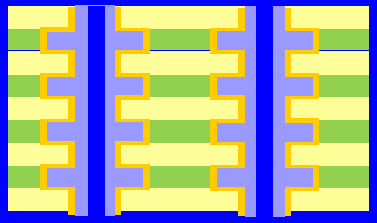
(b) Cell hole etch



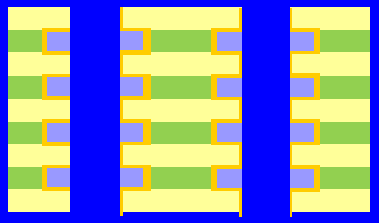
(c) Recess Formation



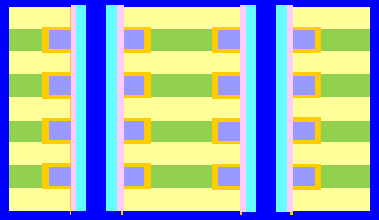
(d) IPD formation



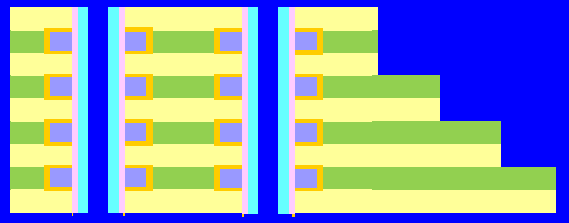
(e) FG deposition



(f) FG isolation

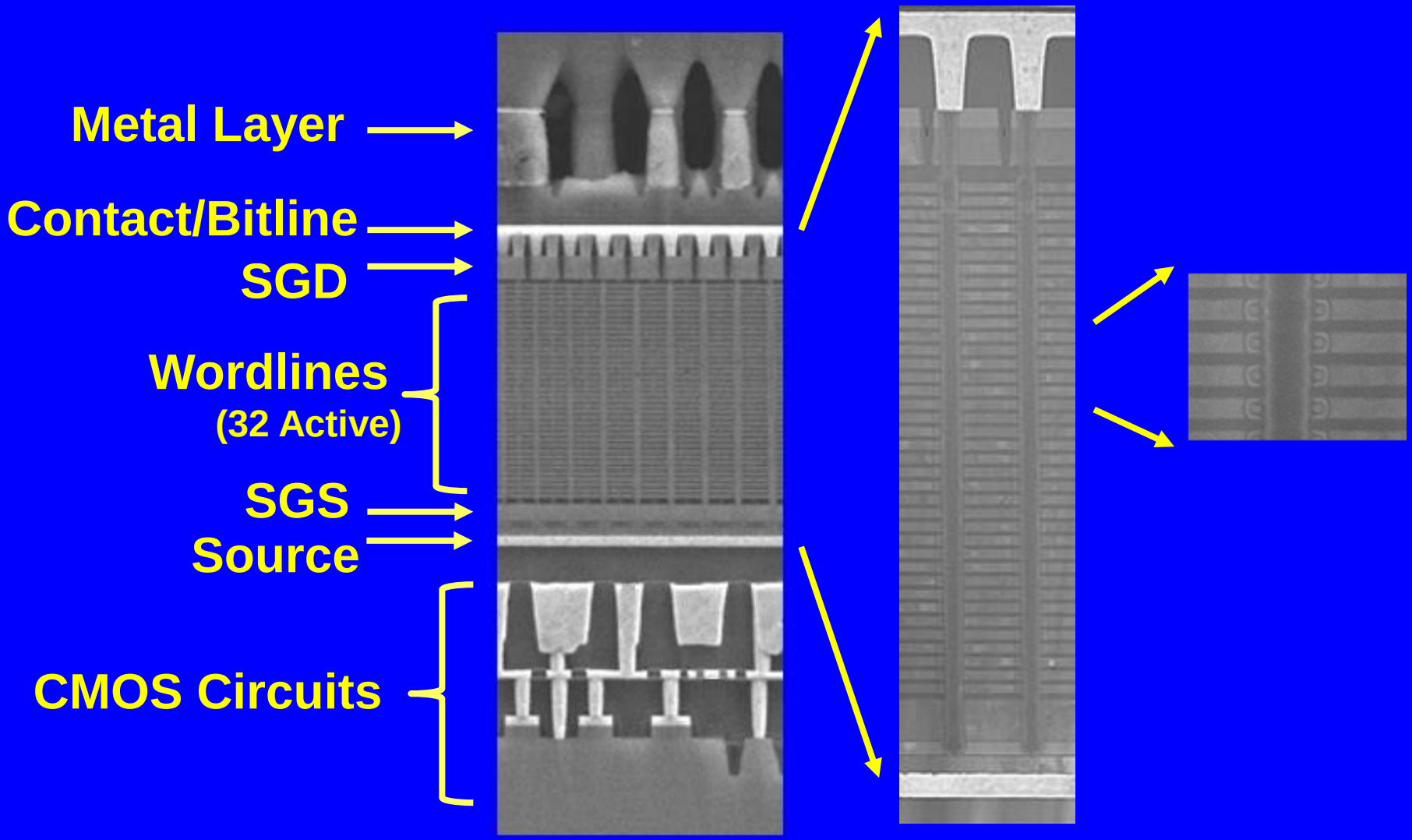


(g) Tunnel-oxide and channel formation



(h) WL Step formation for contacting

3D FG NAND Technology



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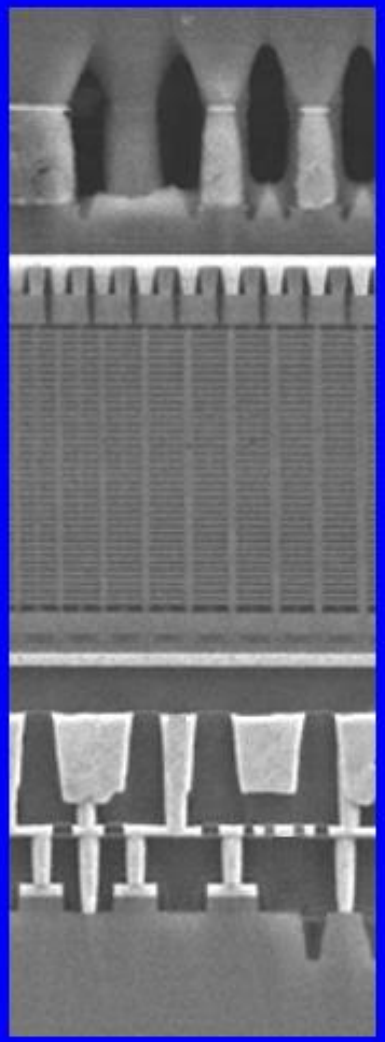
CMOS Under Array

- 3D NAND String is formed fully above the silicon.
- Enables silicon area under for CMOS circuitry
  - 2 Metal Layers below array for CMOS connections
  - 2 Metal layers above the array for Bitline and Bussing



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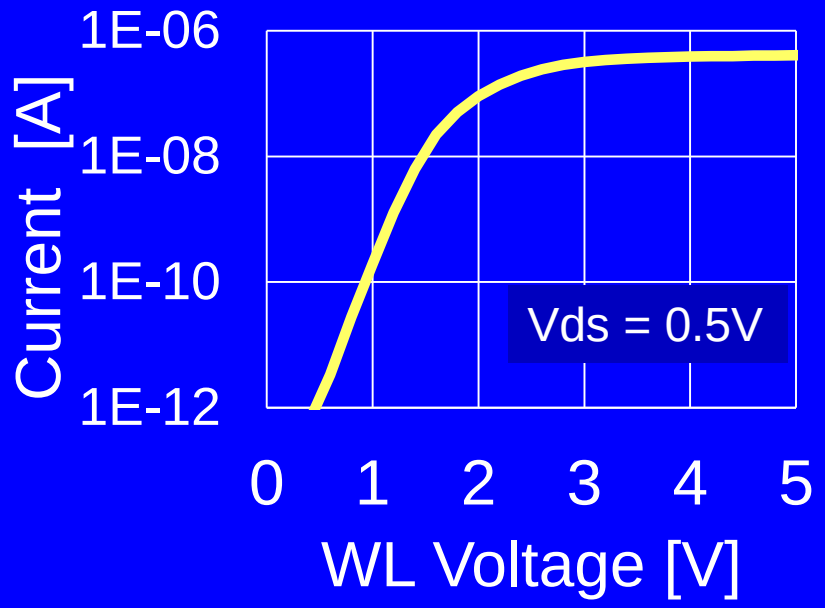
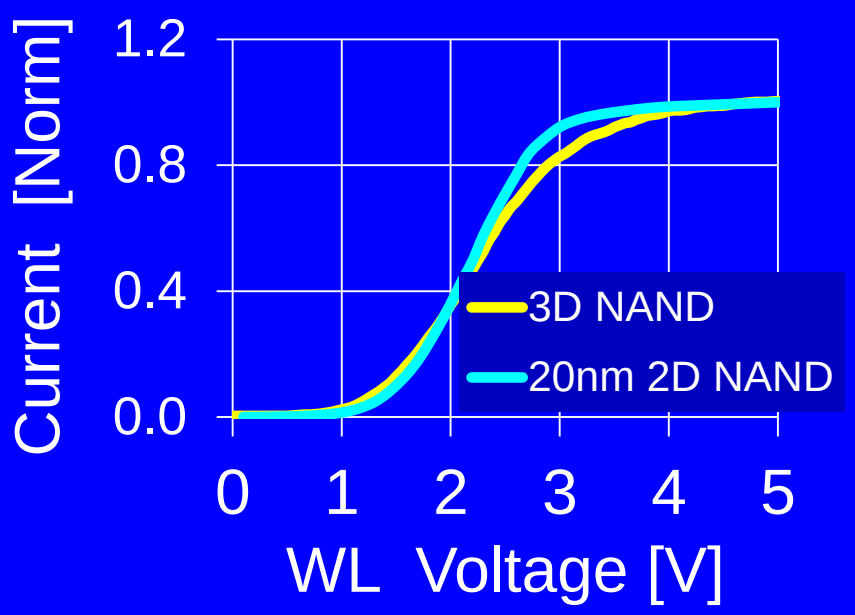
Key Cell Characteristics

- Cell Id-Vg Characteristics
- Erase Operation
- Program/Erase Vt
- Program Disturb
- Cell Vt distributions
- Cell to Cell Interference

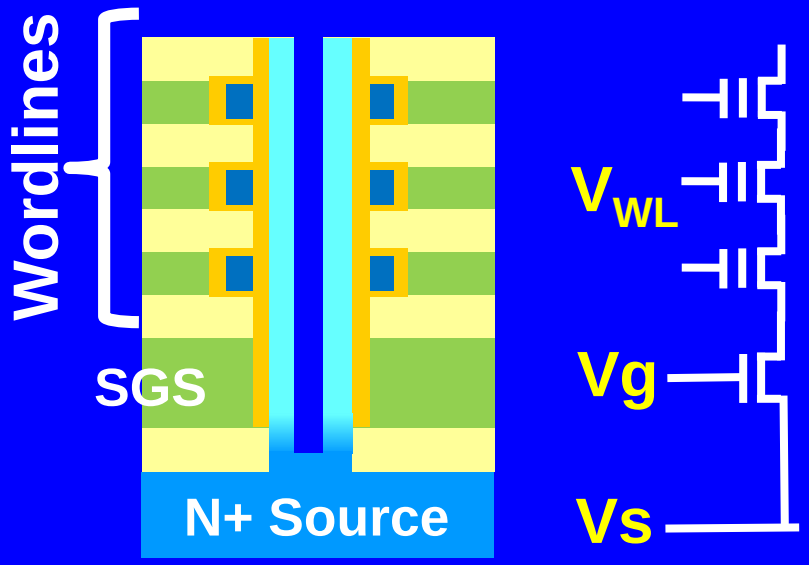
Cell Id-Vg Characteristics

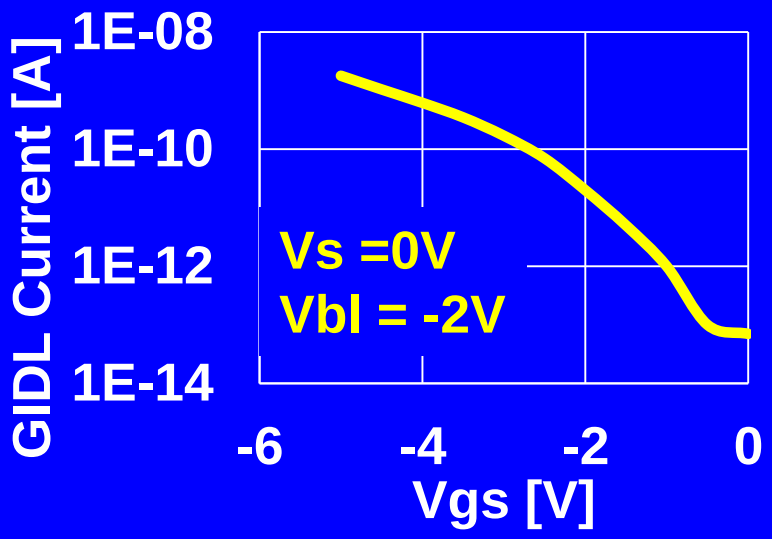




- **Surround gate structure of 3D NAND provides for good gate control**
- **3D NAND String on-current matches that of 2D NAND**

Erase Operation

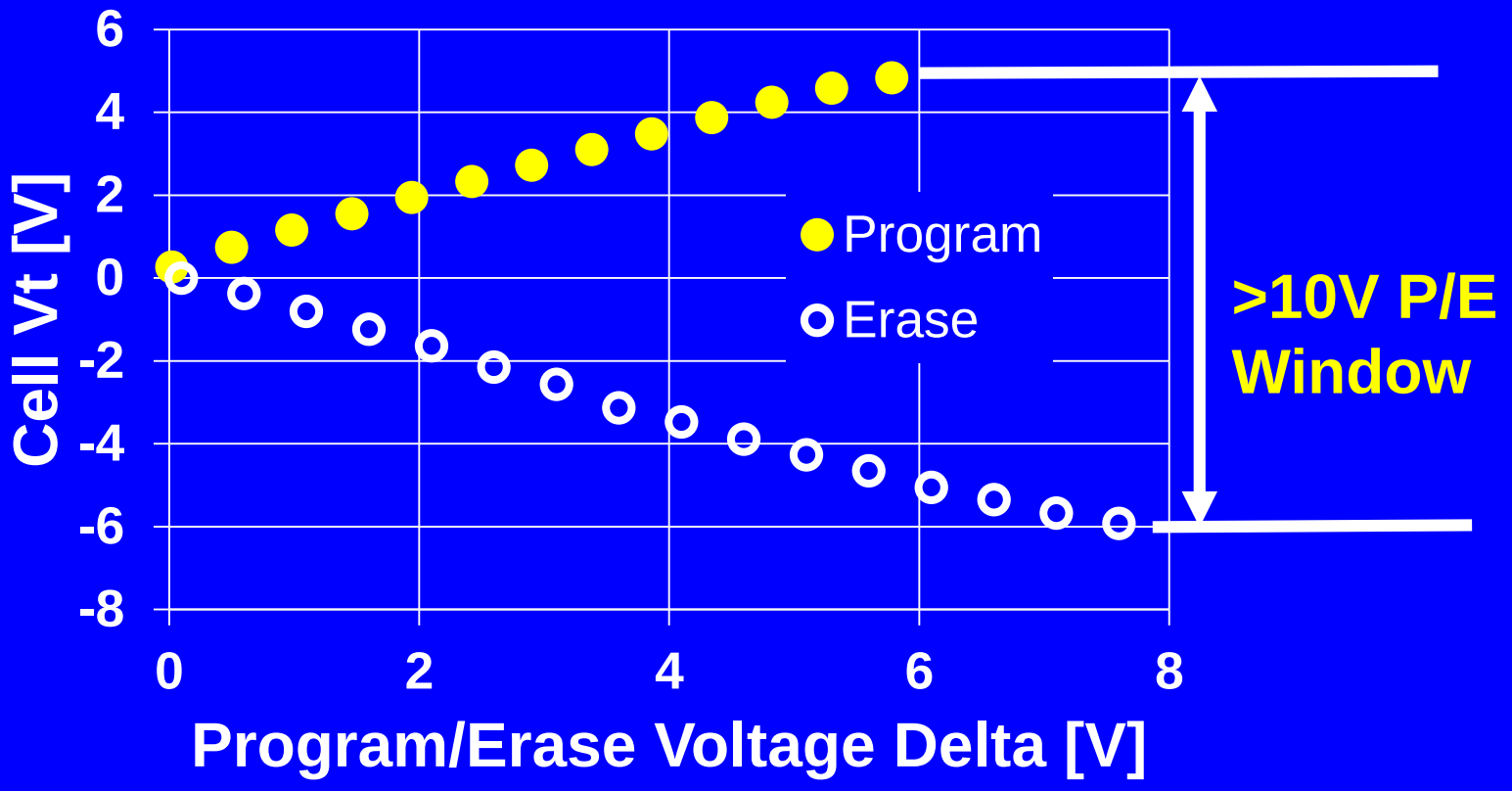




Erase bias applied to the Source

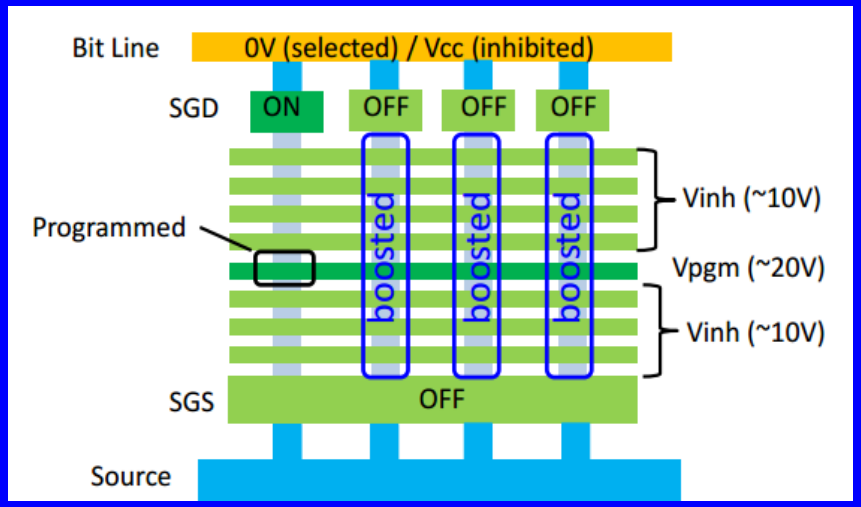
➔ Body biased up by the SGS GIDL

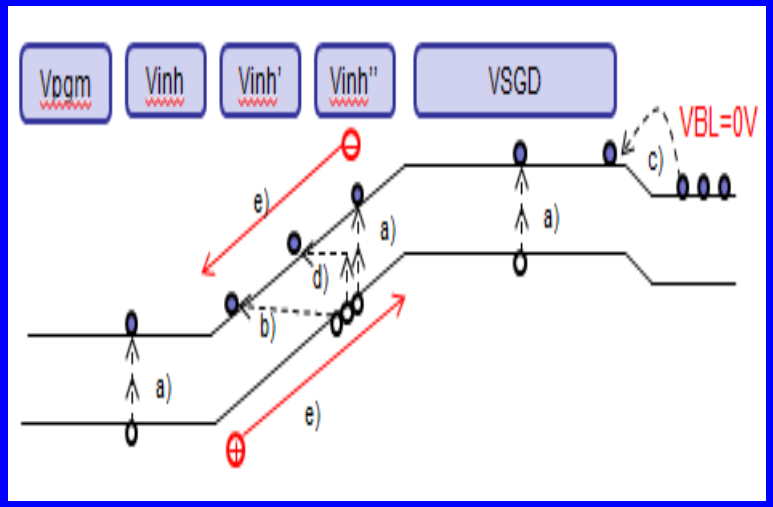
Program/Erase Characteristics



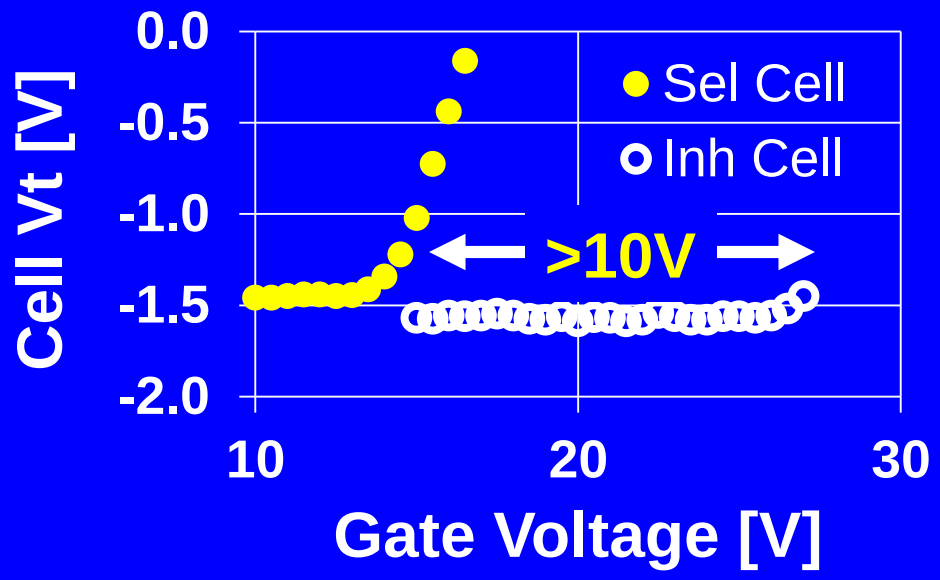
>10V Cell Program/Erase Vt Window is achieved

Program Disturb

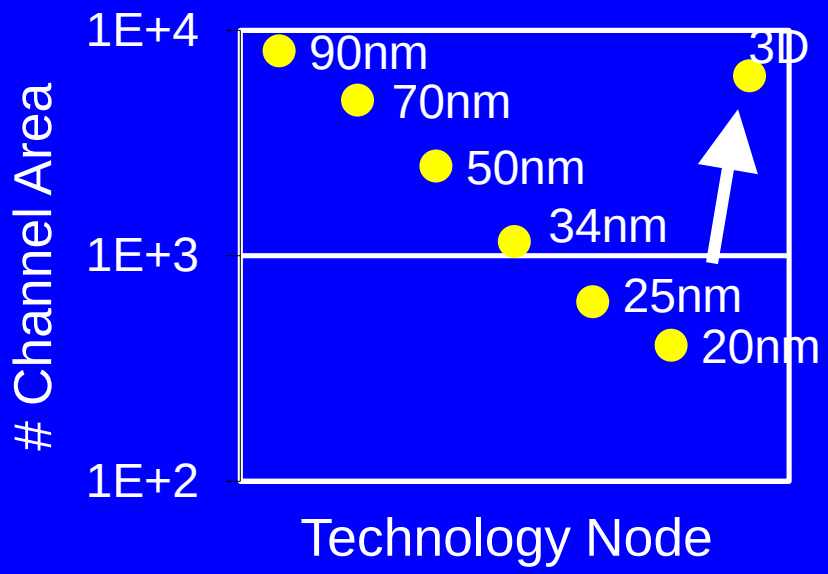


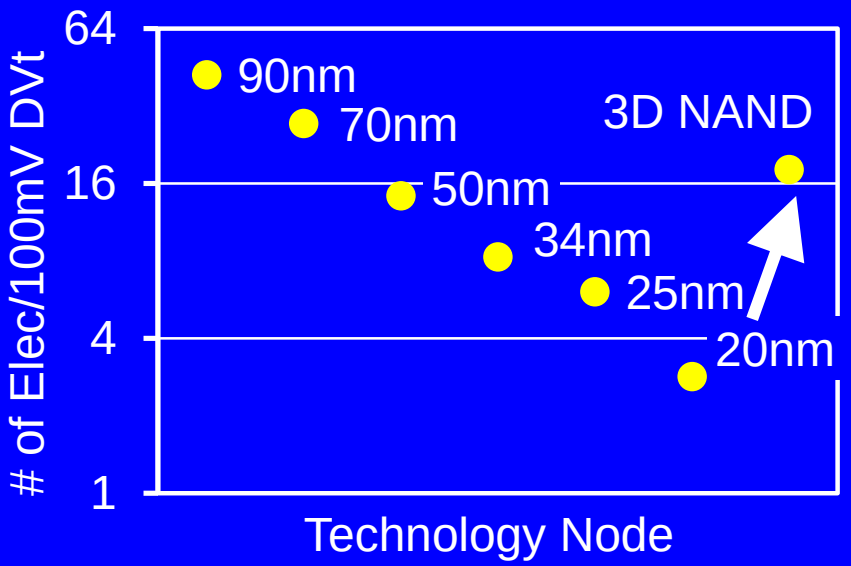


>10V Disturb Window Achieved

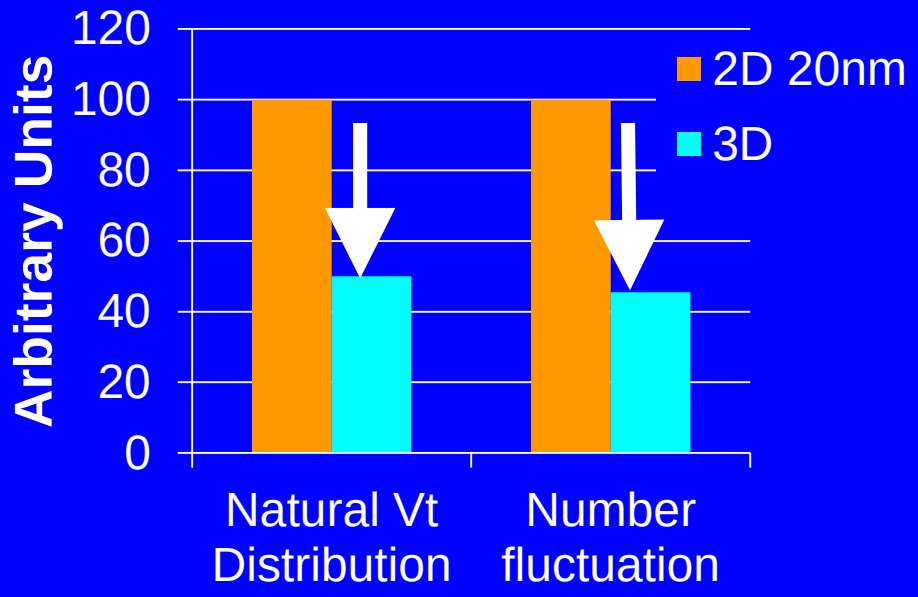


Vt Distributions

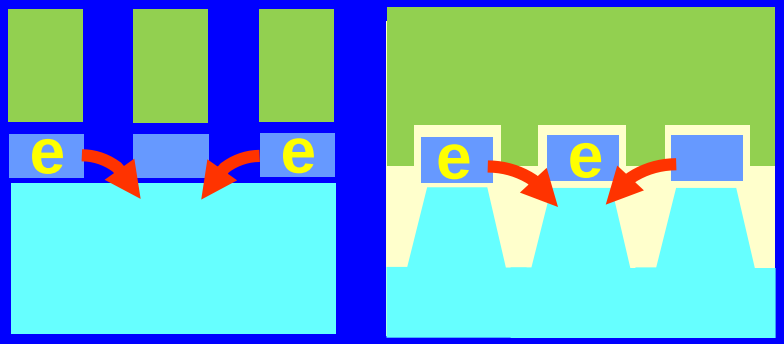




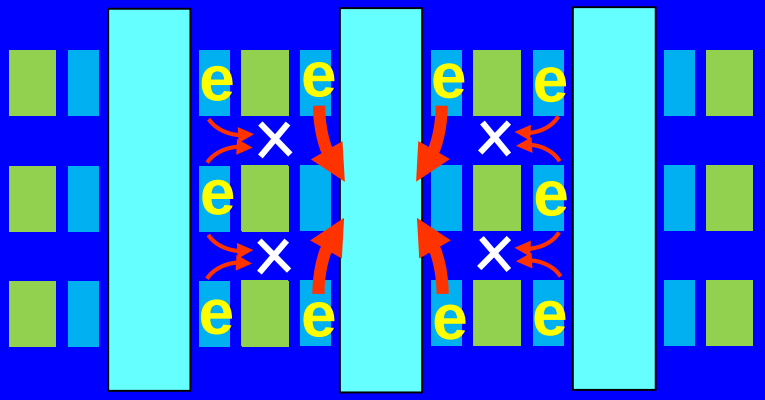
Larger physical cell size of 3D NAND improves Vt distributions



Cell to Cell Interference

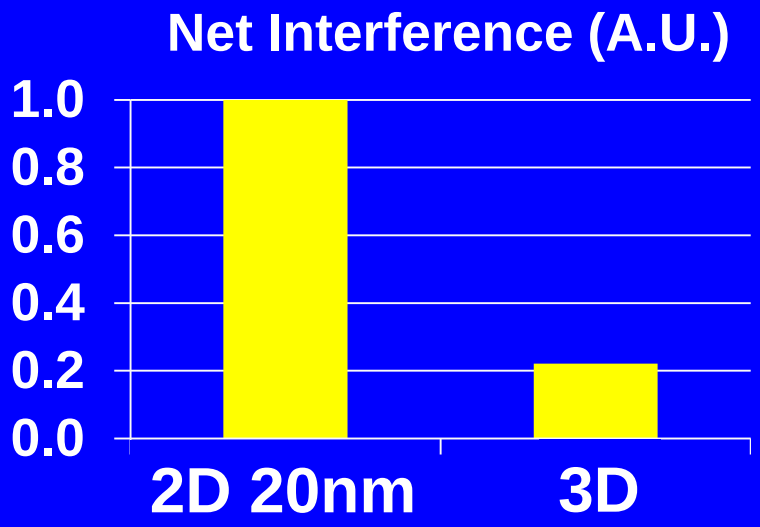


2D NAND

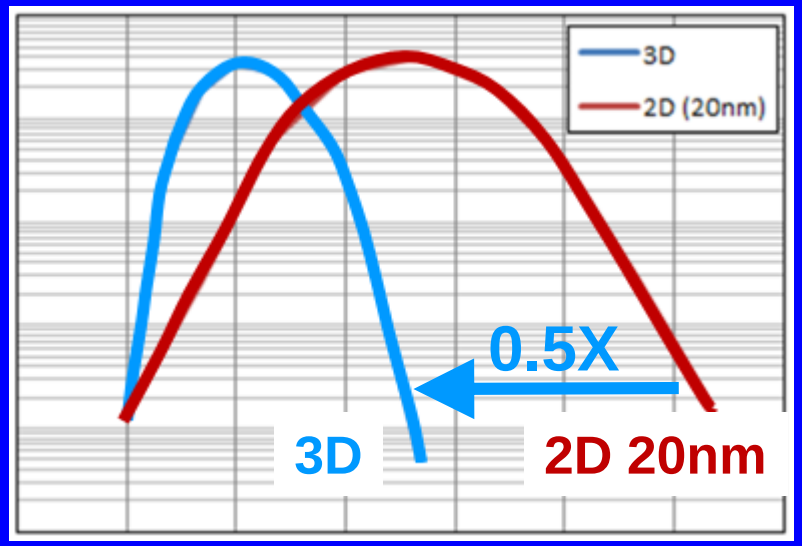


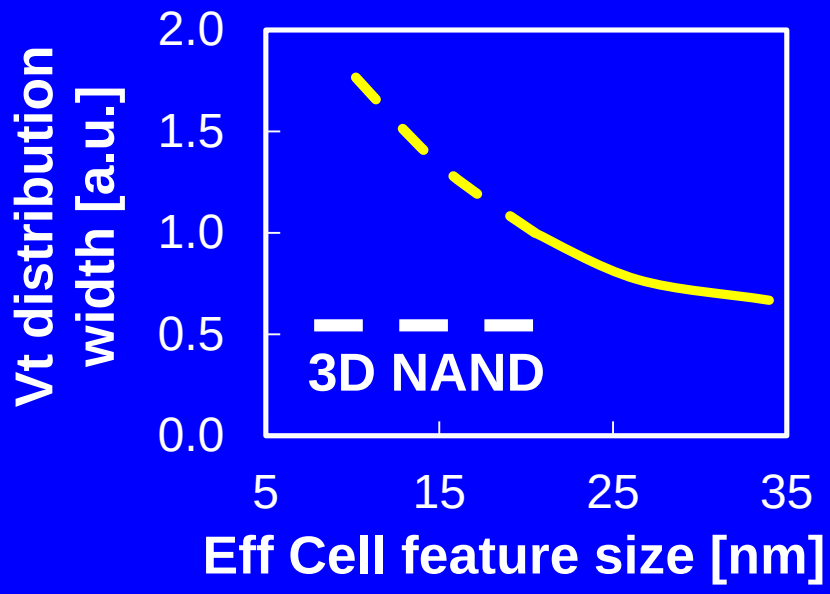
3D NAND

Better shielding from the control gate in the 3D NAND reduces interference by ~80%



MLC Vt Distribution Width





- Better intrinsic distribution and lower interference leads to an overall tighter Vt distribution for 3D NAND

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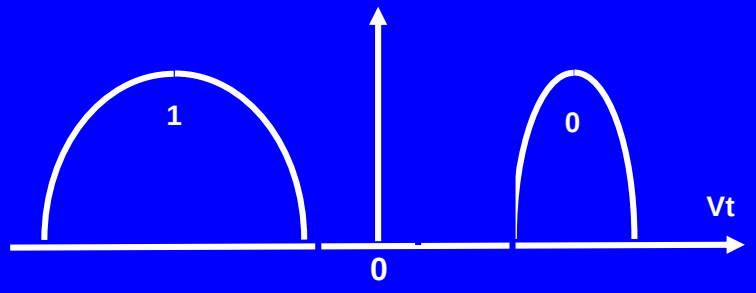
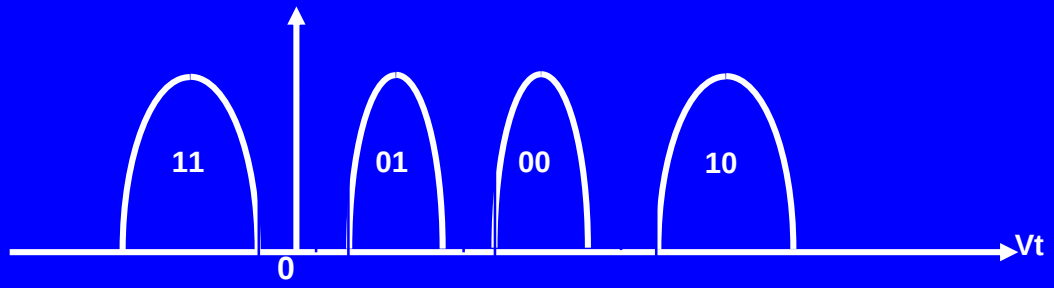
SLC → MLC → TLC → QLC?

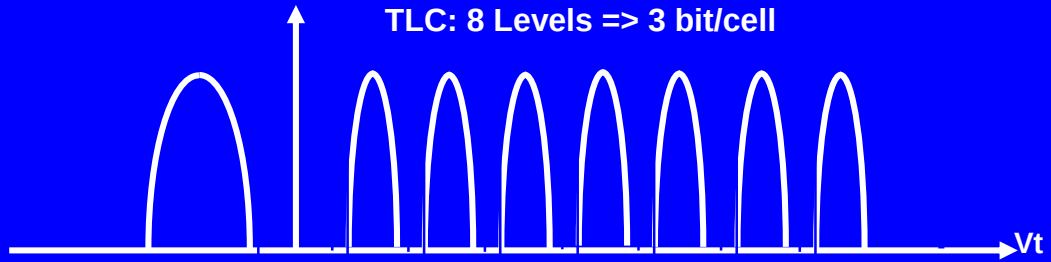
SLC: 2 Levels => 1 bit/cell



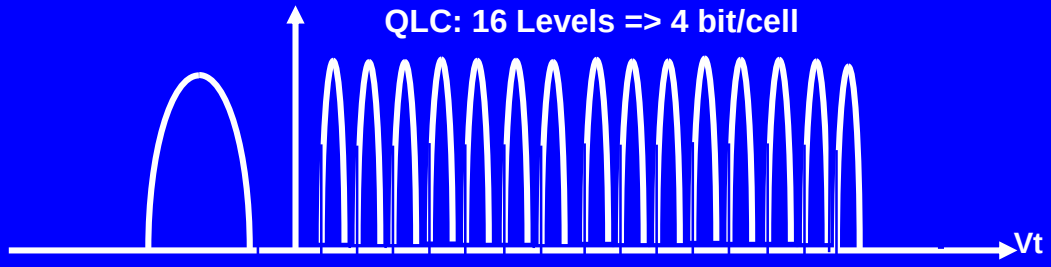
MLC: 4 Levels => 2 bit/cell



TLC: 8 Levels => 3 bit/cell



QLC: 16 Levels => 4 bit/cell



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- 3D NAND extends NAND scaling with cell characteristics superior to that of scaled 2D NAND
- More bits / cell accelerates the scaling: facilitated by superior characteristics of 3D NAND