eMRAM: From Technology to Applications
David Eggleston
VP Embedded Memory
10,000 foot view
What are we trying to achieve?
Memory is...

Know

Remembering.

Think

Events
Memory is...

Code

Data

State

Persistence.
Distance to Compute

State

Data

Code

Store

Load
Distance to Compute

State | Data | Code

Load \( f(\text{Distance}) \)

Time, Energy

Store
Distance to Compute

Time, Energy = \( f(Distance) \)

Embedded Memory reduces the Distance; saves Time and Energy
Embedded Memory…

Persist:
1. Code
2. Data
3. State

Saves:
4. Time
5. Energy
Embedded Memory NV Options
Embedded Memory: Non-Volatile Options

- eMRAM
- eFlash
- eRRAM
- PCM
- CNT

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Embedded Memory: Non-Volatile Options

- **eMRAM**
  - **Pro:** speed, endurance, versatility, masks
  - **Con:** complex stack, data retention

- **eFlash**
  - **Pro:** data retention
  - **Con:** speed, masks

- **eRRAM**
  - **Pro:** simple stack, masks
  - **Con:** speed, endurance, data retention

- **PCM**
  - Specialized

- **CNT**
  - Immature
Embedded Memory: Customer Usage

- **Automotive**
  - ADAS
  - Engine Control
  - Infotainment
  - Battery monitoring
  - Vision systems
  - Navigation

- **MCU**
  - Smartcards
  - Set-top boxes
  - White goods
  - Industrial Controls
  - Touch sensors

- **IoT**
  - Wearables
  - Intelligent sensors
  - Gateways
  - Smart TVs
  - Smart Cities

- **Storage**
  - HDD and SSD storage controllers
  - Storage arrays
  - NV buffers/tiers
  - NV caches

- **Compute**
  - Fast caches
  - Persistent memory
  - Server processors
  - Network processors

**Retention** | **Efficiency** | **Speed**
Embedded Memory: Technology

- Automotive
- MCU
- IoT
- Storage
- Compute

- eFlash
- eMRAM

- Retention
- Efficiency
- Speed

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Embedded Memory: Time Horizon

- Automotive
- MCU
- IoT
- Storage
- Compute

**eFlash**

- Sooner
- eMRAM
- Later

Retention  Efficiency  Speed

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eMRAM: Two bitcells

By varying the materials in the MRAM bitcell, the memory can be tuned for data retention (-F), or speed and endurance (-S)
Embedded Memory: Technology

- **eFlash**: Harsh Environment Reliability
- **eMRAM-F**: Power & Area Efficient
- **eMRAM-S**: Performance & Endurance

Retention | Efficiency | Speed
## Embedded Memory: Technology Comparison

<table>
<thead>
<tr>
<th></th>
<th>eFlash</th>
<th>eMRAM-F</th>
<th>eMRAM-S</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Speed (Rd/Wr)</strong></td>
<td>20ns / 20us</td>
<td>20ns / &lt;50ns</td>
<td>≈ 5ns / 10ns</td>
</tr>
<tr>
<td><strong>Cell size</strong></td>
<td>40F²</td>
<td>45F²</td>
<td>70F²</td>
</tr>
<tr>
<td><strong>Endurance</strong></td>
<td>10⁵</td>
<td>≈10⁸</td>
<td>≈10¹⁴</td>
</tr>
<tr>
<td><strong>Data Retention</strong></td>
<td>&gt;20 years</td>
<td>10 years</td>
<td>1 month</td>
</tr>
<tr>
<td><strong>Op Temp (Ambient)</strong></td>
<td>125C Auto grade 1</td>
<td>105C Industrial</td>
<td>TBD</td>
</tr>
</tbody>
</table>

**DRAFT SPECIFICATIONS ONLY**
Applications
Target Application: IoT

Power and Area Efficiency
IoT: Architectural Elements

Connectivity
RF

State
NV-Logic

Code
eMRAM-F

Data
eMRAM-S

SOC

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IoT: Architectural Elements

Three fundamental magnetic-based architectural elements for IoT SOCs

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The “Killer Combo” for IoT

- Secure, connected, zero power things
- Realized in FDSOI process for maximum power efficiency
IoT Benefits from eMRAM based SoC

1. Area efficiency
2. Speed
3. Endurance
4. Power efficiency
5. Very fast wake up
6. Normally off compute

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NV Logic
Moore’s Law – Economics AND Power


Power Efficiency Supplants Delay  Power Efficiency Supplants Delay

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Spintronic options show the most promise for lowest energy, with smallest gate delay.

How can we get to the future sooner?
NV-Logic

- What is it?
  - Completely new NV library
  - NV-FF, NVE, NVSRAM, NV-LIM
  - Use MTJ as a nv-memory circuit element

- How to use it?
  - NV-FPGAs
  - NV-ASICs
  - Normally off computing
  - Extreme low power consumption/very fast wake-up and resume

- What will it take?
  - Stable eMRAM technology built on advanced logic process
  - NV compute architecture
  - NV-FPGAs
**New operation concept of MTJ/CMOS Latch**

Input data → CMOS → Output data

Passive filter function using $t_A$ of MTJ

- $t_A \geq 1/2t$
- $t_A + t_B < t_{PG}$

No write
No need for controller

- MTJ
- CMOS
- MTJ

- Write
- Load

Working mode
Power gating mode

- $f > 1/(2t_A)$: Only CMOS works
- $f < 1/[2(t_A+t_B)]$: MTJ also switches

**NV-Logic Power Savings**

- Combination MTJ-CMOS latch allows realization of NV-logic now (can use eMRAM-F)
- Research has shown dramatic energy reduction in 32b MPU’s
- 4.6B units and $7.4B annual shipments of 32b microcontrollers

**Experimental Result for the Energy Reduction of MPU with NV-F/F**

Microphotograph of fabricated 32bit MPU

![Microphotograph of fabricated 32bit MPU](image)

Effect of energy reduction

- Operation Duty: 10%, 20%, 40%
- Energy Reduction Rate: 1/28, 1/14, 1/5

- 300k Tr., 7k MTJ, 100MHz

- Applying MTJ-based embedded nonvolatile memory (NV-F/F) to general-purpose MPU, significant energy reduction has been achieved.

H. Koike et al., SSDM, Paper A-7-1, Sep. 2014, pp. 448-449. @Endoh Gr. of Tohoku Univ.
NV-Logic Ecosystem

SOC designers need:
- IP vendors designing NV-Logic elements
- NV-Logic elements integrated into popular design libraries
- NV-Logic compatible simulation tools
- NV-FPGA’s for prototyping and small scale production
- Foundry support for NV-Logic compatible processes

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eMRAM and eFlash Bitcells
eMRAM bitcell operation: Store magnetic polarity

- Direction of voltage bias applied across the MTJ stack causes Free Layer to switch direction of magnetic polarity (P → AP, or AP → P)
- Polarity of the Free Layer can be read as low (P) or high (AP) resistance
- Free Layer polarity is retained after power is removed

Key Parameters

**Free Layer**
- $E_b$ (Energy Barrier) → Retention Time | Switching Threshold
- $M_s$ (Saturation Magnetization) → Switching Speed
- $\Omega$ (Volume) → Switching Speed
- $H_k$ (Intrinsic Switching Field) → Stability | Density
- $\alpha$ (Damping) → Switching Speed | Switching Threshold

**Reference Layer**
- $E_b$ (Energy Barrier) → Reference Layer Stability
- $\eta$ (Injection Efficiency) → TMR | Switching Efficiency & Threshold

**MTJ Stack**
- $I_{c0}, V_{c0}$: Threshold Switching Current or Voltage
- $TMR$: Tunneling Magneto Resistance
- $R_p$: Minimum Resistance (Parallel State)
- $E_b/I_{c0}$: Efficiency

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eFlash bitcell operation: Store charge

- Application of high voltage bias on the coupling gate or erase gate moves charge to/from the Floating Gate (no charge → charge, or charge → no charge)
- Charge on the Floating Gate can be read as low (no charge) or high (charge) resistance
- Floating gate charge is retained after power is removed

<table>
<thead>
<tr>
<th></th>
<th>WL</th>
<th></th>
<th>BL</th>
<th></th>
<th>SL</th>
<th></th>
<th>CG</th>
<th></th>
<th>EG</th>
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<tbody>
<tr>
<td>Sel.</td>
<td>Vrd</td>
<td>0</td>
<td>Vbl</td>
<td>Rd</td>
<td>0</td>
<td>0</td>
<td>Vrd</td>
<td>Vrd</td>
<td>0</td>
</tr>
<tr>
<td>Unsel.</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>Vhe</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Vpwl</td>
<td>0</td>
<td>Vbl</td>
<td>p</td>
<td>Vinh</td>
<td>MVp</td>
<td>0</td>
<td>H vp</td>
<td>Vrd</td>
</tr>
</tbody>
</table>
Comparison of eMRAM and eFlash

<table>
<thead>
<tr>
<th></th>
<th>eMRAM</th>
<th>eFlash</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Storage mechanism</strong></td>
<td>Polarity</td>
<td>Charge</td>
</tr>
<tr>
<td><strong>Storage element</strong></td>
<td>Free Layer</td>
<td>Floating Gate</td>
</tr>
<tr>
<td><strong>Switching bias</strong></td>
<td>Logic voltage</td>
<td>High voltage</td>
</tr>
<tr>
<td><strong>Best attribute</strong></td>
<td>Write speed, endurance</td>
<td>Data retention</td>
</tr>
<tr>
<td><strong>Worst attribute</strong></td>
<td>Complex stack</td>
<td>Doesn’t scale</td>
</tr>
<tr>
<td><strong>Integration</strong></td>
<td>BEOL; btw metal layers</td>
<td>FEOL; in substrate</td>
</tr>
<tr>
<td><strong>Mask adders</strong></td>
<td>+3</td>
<td>+12</td>
</tr>
<tr>
<td><strong>Select device</strong></td>
<td>Logic transistor</td>
<td>Built-in sel transistor</td>
</tr>
<tr>
<td><strong>Bitcell configuration</strong></td>
<td>1T + 1 MTJ</td>
<td>0.5T + 1FG</td>
</tr>
<tr>
<td><strong>System usage</strong></td>
<td>Code, Data</td>
<td>Code</td>
</tr>
<tr>
<td><strong>Macro types</strong></td>
<td>eFlash, SRAM</td>
<td>eFlash</td>
</tr>
</tbody>
</table>
Barriers
Technical Barriers

1. Solder reflow retention
   - 260°C, 5 mins
2. Magnetic immunity
   - 500-800 Oe (Gauss)
3. Bit density vs. eFlash
   - 15% smaller macro

1. Bit density vs. HD SRAM
   - 4x more dense
2. Speed vs. F$^2$
   - Write/Read < 5ns
3. Leading edge processes
   - 14nm, 7nm FinFET

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Processing Barriers

1. Deposition
   ➢ Complex stack of thin materials; many different atoms
2. Etch
   ➢ pMTJ definition; etching dissimilar materials, small CD
3. Magnetic Anneal
   ➢ Set magnetic polarity; no existing production tool
Commercial Barriers

1. Cost, cost, cost
   - Customers will NOT pay for speed/endurance/power
2. CapEx/Tool throughput
   - Cost of dedicated tooling and throughput too high
3. Customer adoption
   - Schedule and reliability risk must be offset by cost
GLOBALFOUNDRIES Position
# GLOBALFOUNDRIES Company Highlights

## REVENUE

| $6B* |

## MORE THAN

| 25,000 Patents & Applications |
| 250 Customers |
| 18,000 Employees |

## FAB LOCATIONS

- Burlington
- East Fishkill
- Dresden
- Malta
- Singapore

## FAB CAPACITY

- Trusted Foundry
  - 300mm
  - 133K Wafers/Mo
- 200mm
  - 200K Wafers/Mo

*Based upon analysts' estimates
### eMRAM and MRAM

<table>
<thead>
<tr>
<th>Standalone MRAM</th>
<th>eMRAM</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology</td>
<td>STT</td>
</tr>
<tr>
<td>Bitcell</td>
<td>in-plane → perpendicular</td>
</tr>
<tr>
<td>Usage</td>
<td>data</td>
</tr>
<tr>
<td>Capacity</td>
<td>256Mb → 1Gb</td>
</tr>
<tr>
<td>Interface</td>
<td>DDR</td>
</tr>
<tr>
<td>Feature</td>
<td>Speed, endurance</td>
</tr>
</tbody>
</table>

GLOBALFOUNDRIES is fabricating both types
Lead customer success with GLOBALFOUNDRIES built MRAM

Everspin Releases Highest Density MRAM Products to Create Fastest And Most Reliable Non-Volatile Storage Class Memory

Everspin plans production of 256Mb & 1Gb products, bringing the most advanced memory solutions to the multi-billion dollar market for persistent memory in storage devices and servers.

Chandler, AZ, April 13, 2016

Everspin Technologies announced today that it is shipping 256Mb ST-MRAM samples to global customers, enabling new product solutions using a true MRAM-based Storage Class Memory (SCM). This 256Mb ST-MRAM product breaks the record for the highest density commercial MRAM currently available in the market. Everspin, having held the previous record, has

Con Tutto: Prototyping Platform

- **Prepare for Future Memories**: Enable MRAM, PCM, RRAM on the P8 memory bus
- **Evaluate NVDIMMs**: Enable NVDIMM-N/F in Power systems, functionally evaluate
- **Innovate**: Enable industry and OpenPOWER partners to innovate on the P8 Differential Memory Interface link

Activity
- NVmem Software Stack Changes
- Technology Enablement
  - NVDIMM-N – Ongoing ~2Q16
  - MRAM – Operational now - Everspin
  - Investigating other technologies
- Near-Memory Acceleration – Zurich Research Lab
GLOBALFOUNDRIES eMRAM
Final word...
Embedded Memory…

**Persist**:s

1. Code  eMRAM-F
2. Data  eMRAM-S
3. State  NV-Logic

**Saves**:

4. Time
5. Energy

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Embedded Memory
Solving your product challenges for the hyperconnected world
Thank you
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