eMRAM: From Technology to Applications

David Eggleston

VP Embedded Memory

GLOBALFOUNDRIES®

10,000 foot view

What are we trying to achieve?

Memory is…

Remembering.

Know

Think

Events

Memory is…

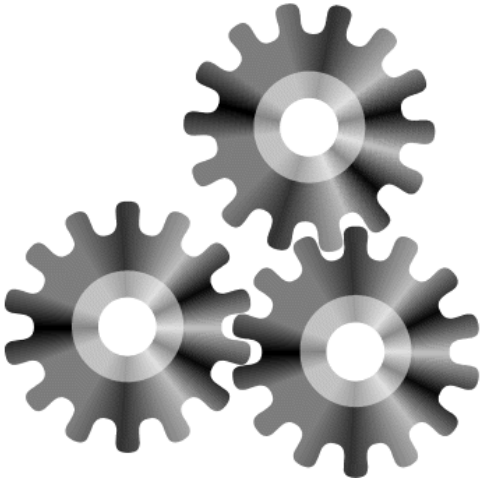
Persistence.

Code

Data

State

Distance to Compute



State

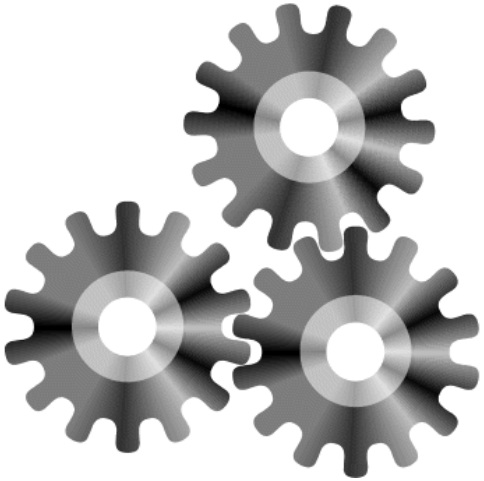
Data

Code

Store

Load

Distance to Compute



State

Data

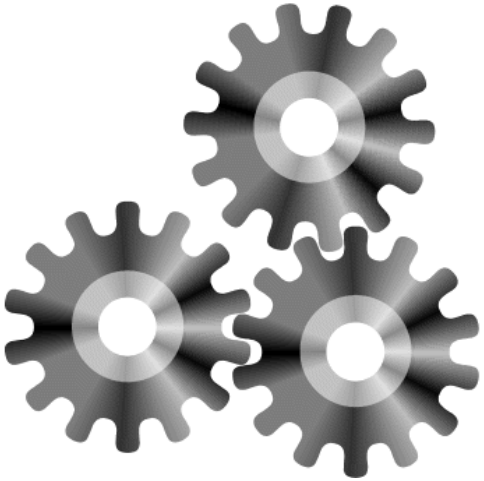
Code

Store

Load

Time, Energy = f(Distance)

Distance to Compute



State

Data

Code

Time, Energy = *f* (Distance)

Embedded Memory reduces the Distance; saves <u>Time</u> and <u>Energy</u>

Embedded Memory…

Persists:

1. Code
2. Data
3. State

Saves:

4. Time
5. Energy

Embedded Memory NV Options

Embedded Memory: Non-Volatile Options

eMRAM

eFlash

PCM

eRRAM

CNT

Embedded Memory: Non-Volatile Options

eMRAM

Pro: speed, endurance, versatility, masks
Con: complex stack, data retention

eFlash

Pro: data retention
Con: speed, masks

eRRAM

Pro: simple stack, masks
Con: speed, endurance, data retention

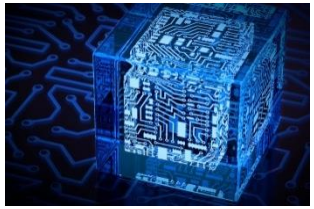
PCM

Specialized

CNT

Immature

Embedded Memory: Customer Usage

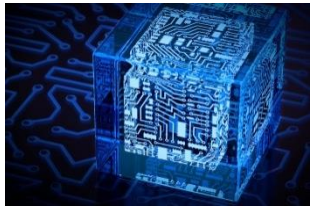
Automotive	MCU	IoT	Storage	Compute
				
ADAS Engine Control Infotainment Battery monitoring Vision systems Navigation	Smartcards Set-top boxes White goods Industrial Controls Touch sensors	Wearables Intelligent sensors Gateways Smart TVs Smart Cities	HDD and SSD storage controllers Storage arrays NV buffers/tiers NV caches	Fast caches Persistent memory Server processors Network processors

Retention ← Efficiency → Speed

Embedded Memory: Technology

Automotive	MCU	IoT	Storage	Compute

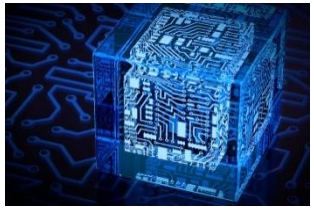


Embedded Memory: Time Horizon

Automotive	MCU	IoT	Storage	Compute

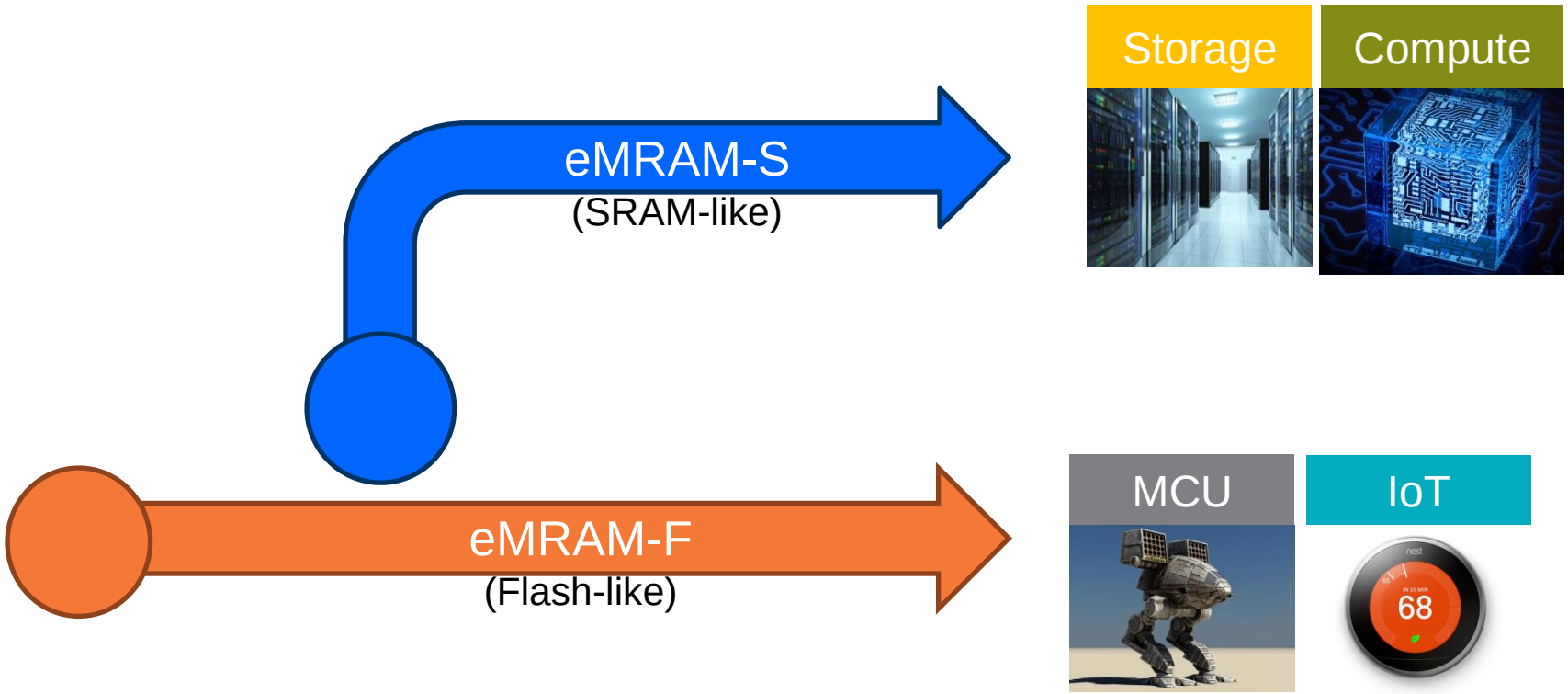


eFlash | Sooner | eMRAM | Later

Retention ⟷ Efficiency ⟷ Speed

eMRAM: Two bitcells



- By varying the materials in the MRAM bitcell, the memory can be tuned for data retention (-F), or speed and endurance (-S)

Embedded Memory: Technology

eFlash	eMRAM-F	eMRAM-S
		
Harsh Environment Reliability	Power & Area Efficient	Performance & Endurance

Retention ⟷ Efficiency ⟷ Speed

Embedded Memory: Technology Comparison

	eFlash	eMRAM-F	eMRAM-S
Speed (Rd/Wr)	20ns / 20us	20ns / <50ns	≈ 5ns / 10ns
Cell size	$40F^2$	$45F^2$	$70F^2$
Endurance	10^5	$\approx 10^8$	$\approx 10^{14}$
Data Retention	>20 years	10 years	1 month
Op Temp (Ambient)	125C Auto grade 1	105C Industrial	TBD

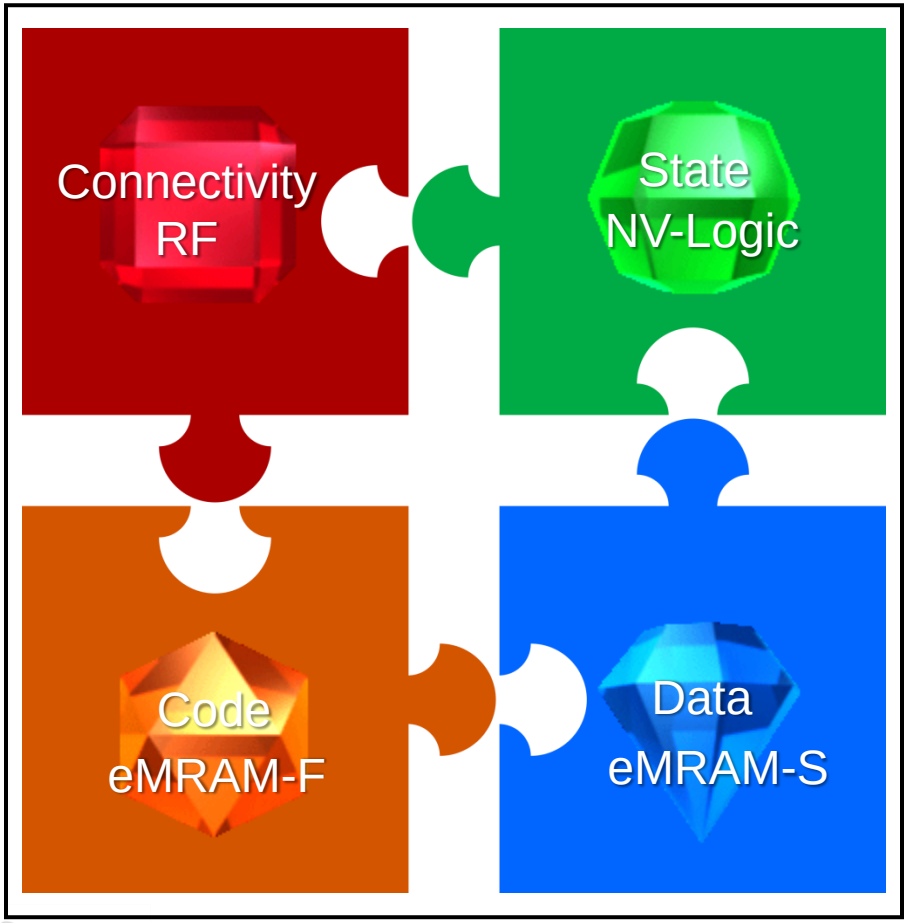
DRAFT SPECIFICATIONS ONLY

Applications

Target Application: IoT

Power and Area Efficiency

IoT: Architectural Elements

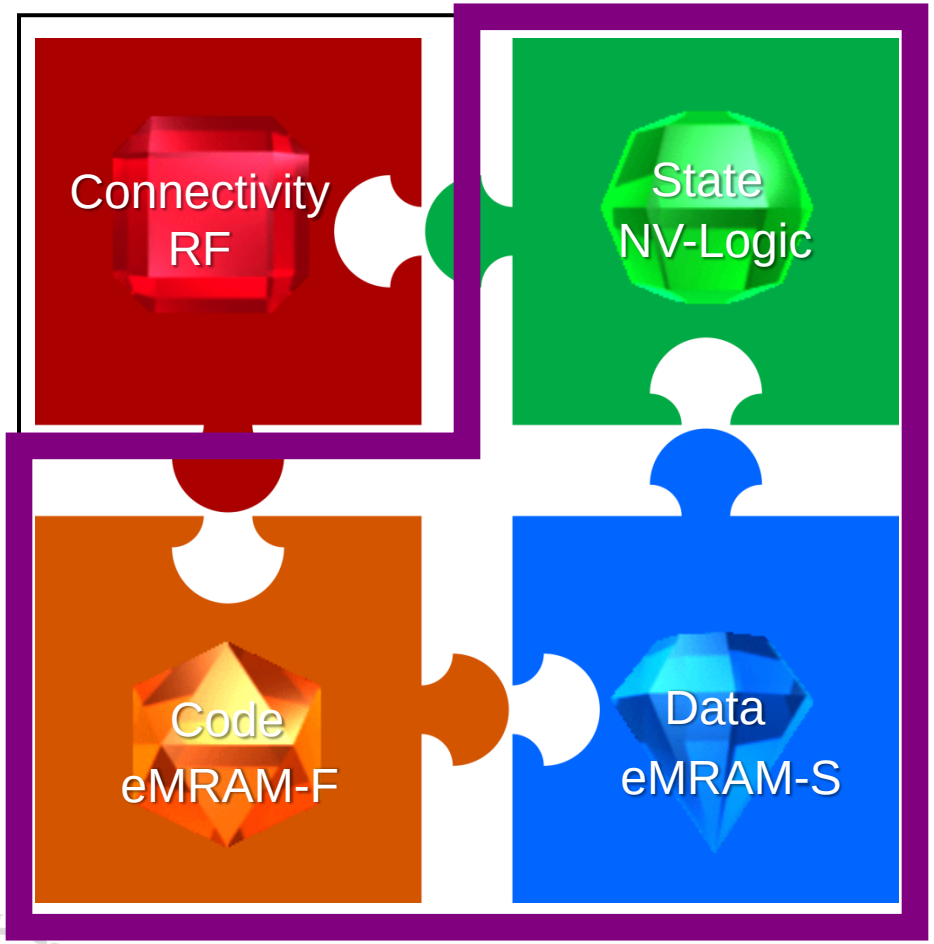


SOC

IoT

eMRAM

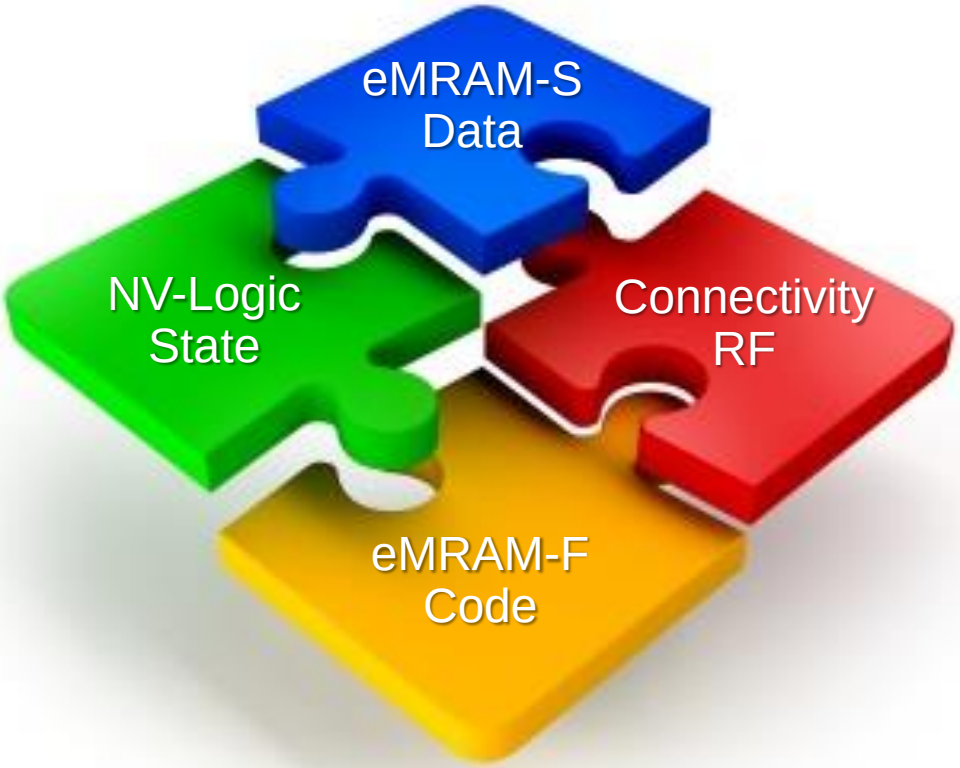
IoT: Architectural Elements



SOC

Three fundamental magnetic-based architectural elements for IoT SOCs

The “Killer Combo” for IoT



- Secure, connected, zero power things
- Realized in FDSOI process for maximum power efficiency

IoT Benefits from eMRAM based SoC

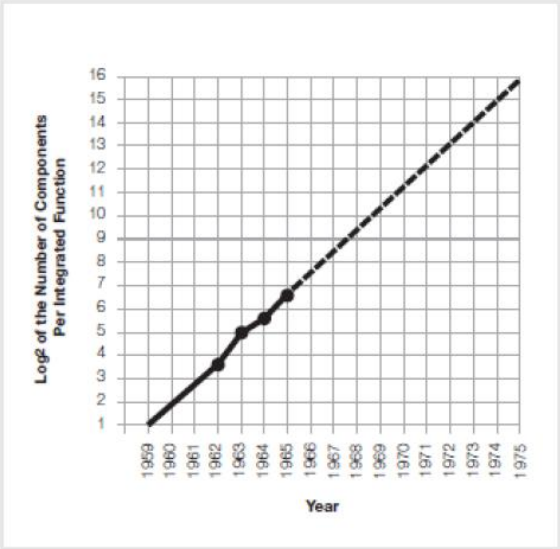
1. Area efficiency
2. Speed
3. Endurance
4. Power efficiency
5. Very fast wake up
6. Normally off compute

IoT

eMRAM

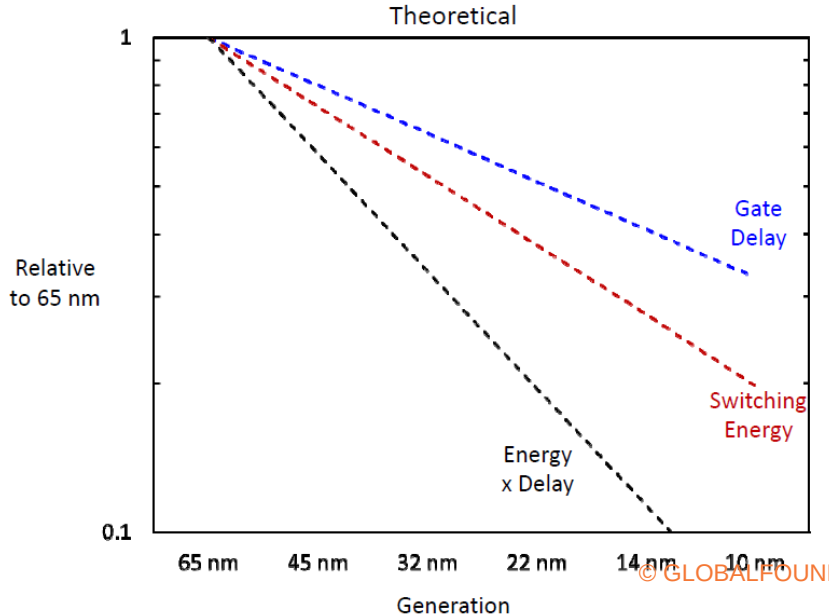
NV Logic

Moore's Law – Economics AND Power

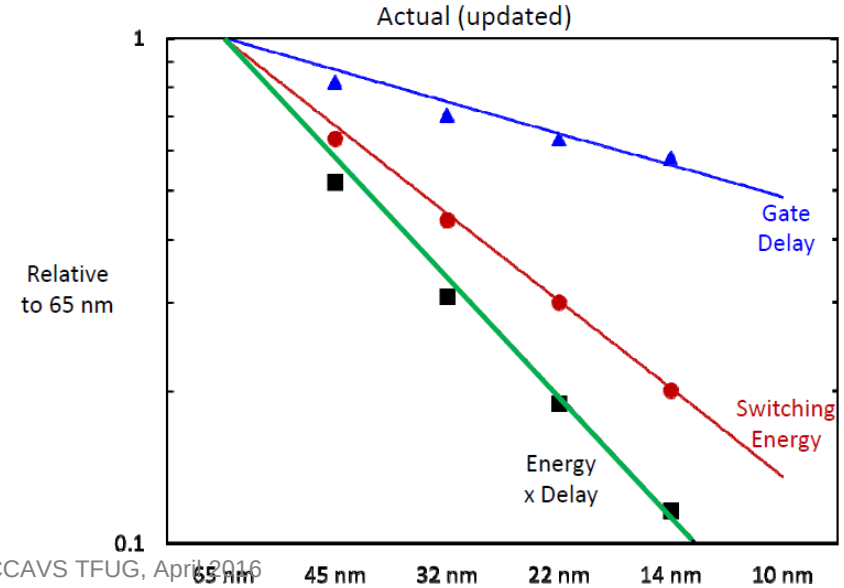


Source: Moore's Law: A Path Forward, B. Holt, Intel, ISSCC 2016

Power Efficiency Supplants Delay

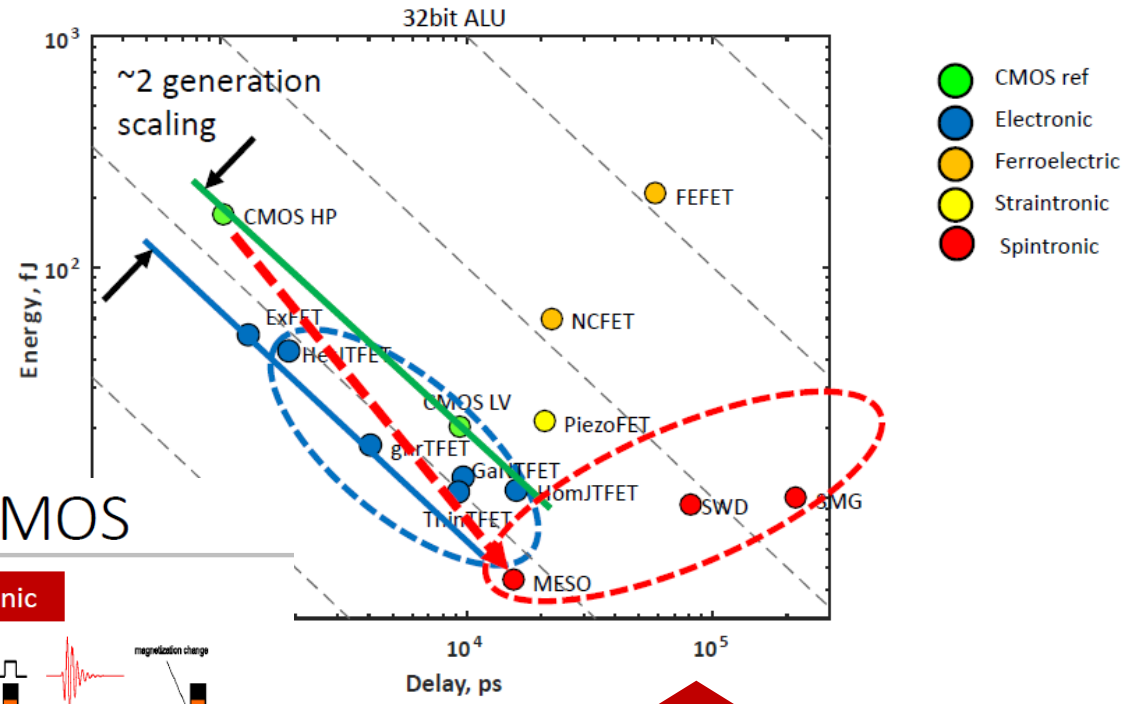


Power Efficiency Supplants Delay



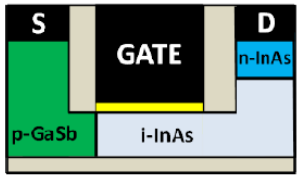
The Changing Measure of Improvement

Source: Moore's Law: A Path Forward, B. Holt, Intel, ISSCC 2016



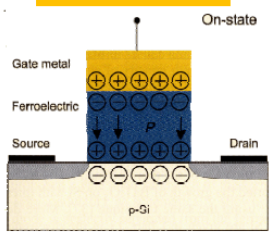
Options for Beyond CMOS

Electronic



Tunneling FET

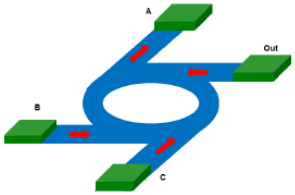
Ferroelectric



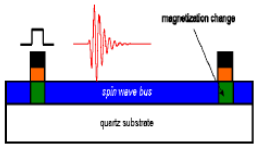
FEFET

Source: Intel

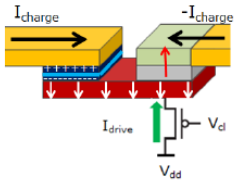
Spintronic



Spin Majority Gate (SMG)



Spin Wave Device (SWD)



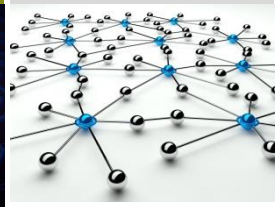
Magneto-Electric Spin-Orbital (MESO)

Device	Physics
MOSFET	Conduction over gate controlled barrier
Tunneling FET	Quantum tunneling band to band conduction through a gate controlled barrier
MESO	Magneto-electric effect Spin Orbit Torque effect

Spintronic options show the most promise for lowest energy, with smallest gate delay.

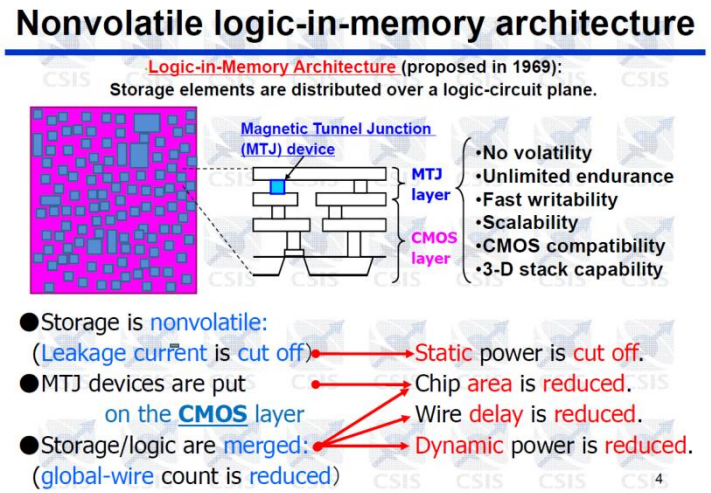
How can we get to the future sooner?

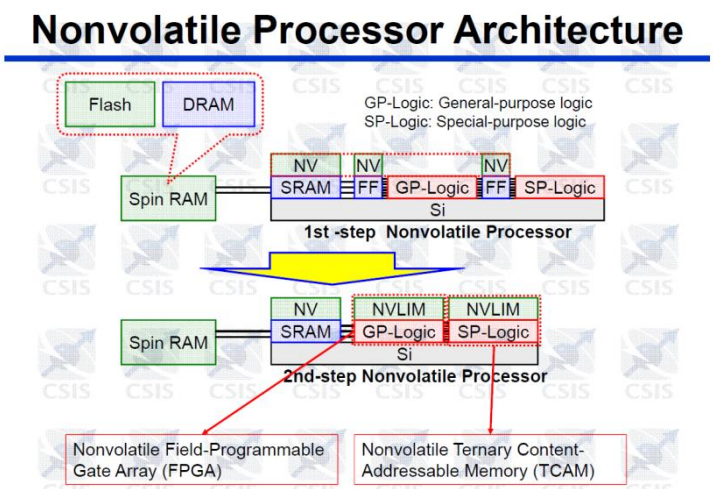
Compute | Network



NV-Logic

- What is it?
  - Completely new NV library
  - NV-FF, NVE, NVSRAM, NV-LIM
  - Use MTJ as a nv-memory circuit element
- How to use it?
  - NV-FPGAs
  - NV-ASICs
  - Normally off computing
  - Extreme low power consumption/very fast wake-up and resume
- What will it take?
  - Stable eMRAM technology built on advanced logic process
  - NV compute architecture
  - NV-FPGAs

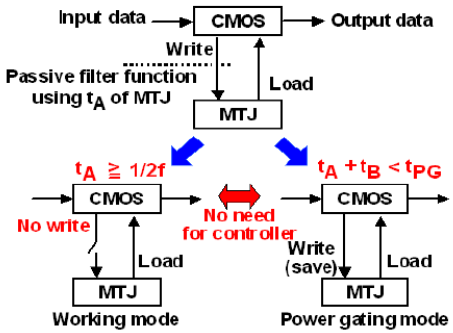




Source: Hanyu, et al; Tohoku University; 2011 NVMTS

8

New operation concept of MTJ/CMOS Latch



$f > 1/(2t_A)$ ⇒ Only CMOS works

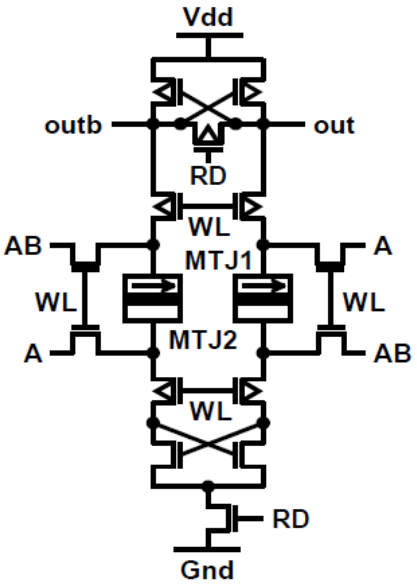
$f < 1/[2(t_A+t_B)]$ ⇒ MTJ also switches

⇒
- High-performance
- Low-power
- Small transistors

T. Endoh et al., IEDM, pp. 75-78, Dec. 2011. @ Endoh Gr. of Tohoku Univ.

NV-Logic Power Savings

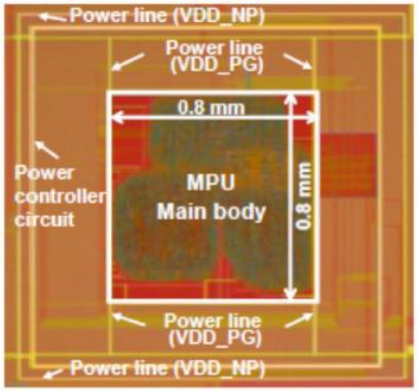
- Combination MTJ-CMOS latch allows realization of NV-logic now (can use eMRAM-F)
- Research has shown dramatic energy reduction in 32b MPU's
- 4.6B units and $7.4B annual shipments of 32b microcontrollers



Circuit schematic of proposed MTJ based NV-latch

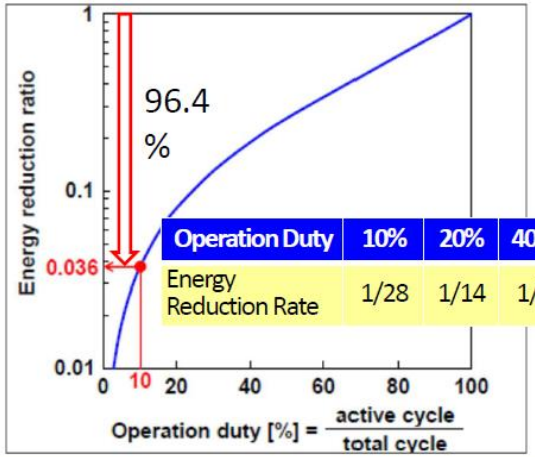
Experimental Result for the Energy Reduction of MPU with NV-F/F

Microphotograph of fabricated 32bit MPU



300k Tr., 7k MTJ, 100MHz

Effect of energy reduction



Operation Duty	10%	20%	40%
Energy Reduction Rate	1/28	1/14	1/5

Applying MTJ-based embedded nonvolatile memory (NV-F/F) to general-purpose MPU, significant energy reduction has been achieved.

H. Koike et al., SSDM, Paper A-7-1, Sep. 2014, pp. 448-449. *@Endoh Gr. of Tohoku Univ.*

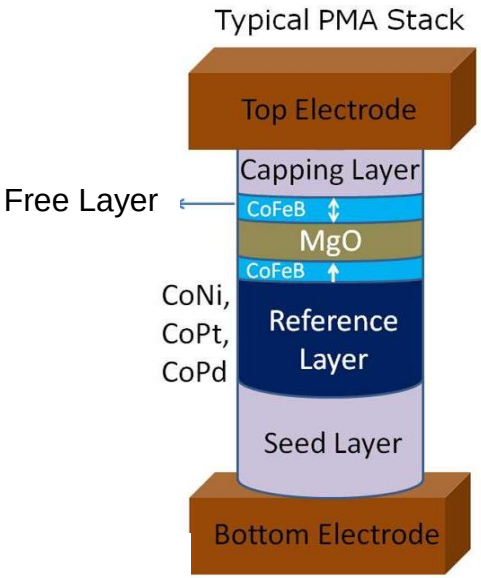
NV-Logic Ecosystem

<u>SOC designers need:</u>

- IP vendors designing NV-Logic elements
- NV-Logic elements integrated into popular design libraries
- NV-Logic compatible simulation tools
- NV-FPGA's for protoyping and small scale production
- Foundry support for NV-Logic compatible processes

eMRAM and eFlash Bitcells

eMRAM bitcell operation: Store magnetic polarity



Key Parameters

Free Layer

E_b(Energy Barrier)→ Retention Time | Switching Threshold
M_s(Saturation Magnetization) → Switching Speed
Ω (Volume) → Switching Speed
H_k (Intrinsic Switching Field) → Stability | Density
α (Damping) → Switching Speed | Switching Threshold

Reference Layer

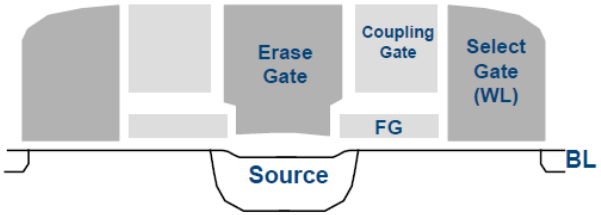
E_b(Energy Barrier) → Reference Layer Stability
η (Injection Efficiency) →TMR |Switching Efficiency & Threshold

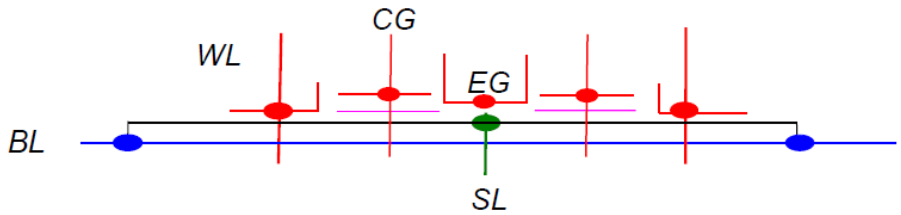
MTJ Stack

I_{c0},V_{c0}: Threshold Switching Current or Voltage
TMR: Tunneling Magneto Resistance
R_p: Minimum Resistance (Parallel State)
E_b/I_{c0}: Efficiency

- Direction of voltage bias applied across the MTJ stack causes Free Layer to switch direction of magnetic polarity (P → AP, or AP → P)
- Polarity of the Free Layer can be read as low (P) or high (AP) resistance
- Free Layer polarity is retained after power is removed

eFlash bitcell operation: Store charge





Example of cell operating conditions:

	WL		BL		SL		CG		EG
	Sel.	Unsel.	Sel.	Unsel.	Sel.	Unsel.	Sel.	Unsel.	Sel.
Read	Vrd	0	Vblrd	0	0	0	Vrd	Vrd	0
Erase	0	0	0	0	0	0	0	0	Hve
Program	Vpwl	0	Vblp	Vinh	MVp	0	HVp	Vrd	MVp

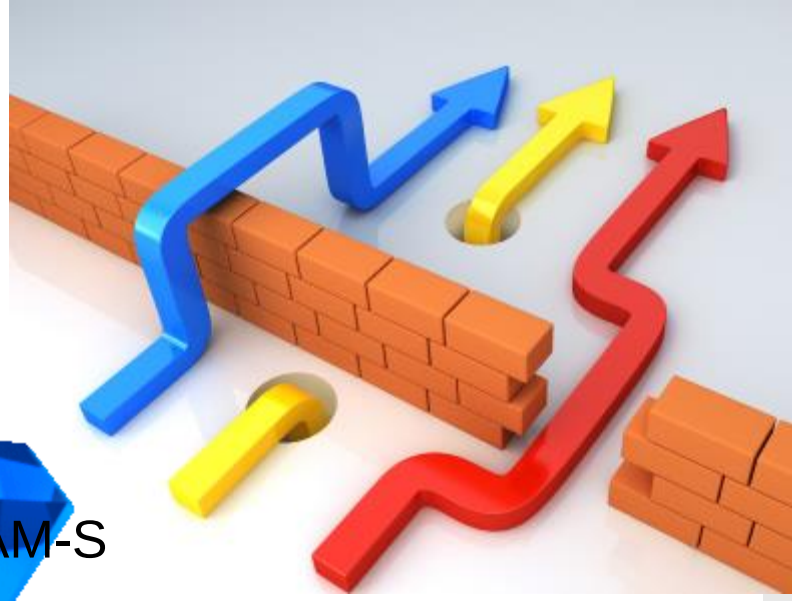
- Application of high voltage bias on the coupling gate or erase gate moves charge to/from the Floating Gate (no charge → charge, or charge → no charge)
- Charge on the Floating Gate can be read as low (no charge) or high (charge) resistance
- Floating gate charge is retained after power is removed

Comparison of eMRAM and eFlash

	eMRAM	eFlash
Storage mechanism	Polarity	Charge
Storage element	Free Layer	Floating Gate
Switching bias	Logic voltage	High voltage
Best attribute	Write speed, endurance	Data retention
Worst attribute	Complex stack	Doesn't scale
Integration	BEOL; btw metal layers	FEOL; in substrate
Mask adders	+3	+12
Select device	Logic transistor	Built-in sel transistor
Bitcell configuration	1T + 1 MTJ	0.5T + 1FG
System usage	Code, Data	Code
Macro types	eFlash, SRAM	eFlash

Barriers

Technical Barriers



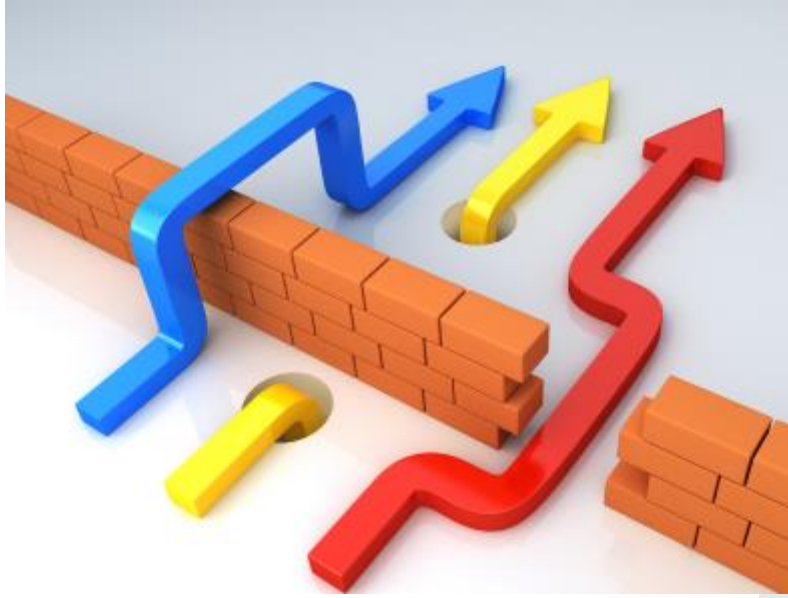
eMRAM-F

1. Solder reflow retention
   - 260°C, 5 mins
2. Magnetic immunity
   - 500-800 Oe (Gauss)
3. Bit density vs. eFlash
   - 15% smaller macro

eMRAM-S

1. Bit density vs. HD SRAM
   - 4x more dense
2. Speed vs. F^2
   - Write/Read < 5ns
3. Leading edge processes
   - 14nm, 7nm FinFET

Processing Barriers

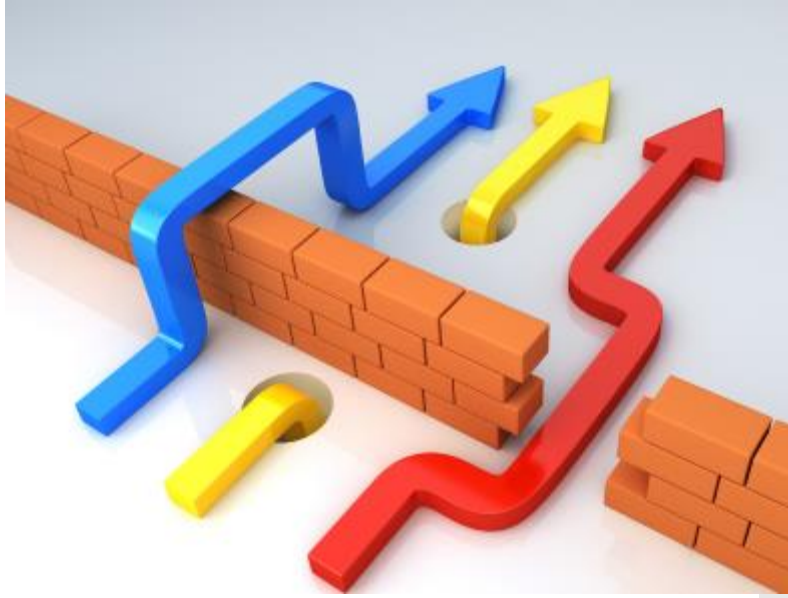


eMRAM-F

eMRAM-S

1. Deposition
   - Complex stack of thin materials; many different atoms
2. Etch
   - pMTJ definition; etching dissimilar materials, small CD
3. Magnetic Anneal
   - Set magnetic polarity; no existing production tool

Commercial Barriers



eMRAM-F

eMRAM-S

1. Cost, cost, cost
   - Customers will NOT pay for speed/endurance/power
2. CapEx/Tool throughput
   - Cost of dedicated tooling and throughput too high
3. Customer adoption
   - Schedule and reliability risk must be offset by cost

GLOBALFOUNDRIES Position

GLOBALFOUNDRIES Company Highlights

REVENUE

~6B*

2nd Largest Foundry

MORE THAN

25,000
Patents & Applications

250
Customers

18,000
Employees

FAB LOCATIONS

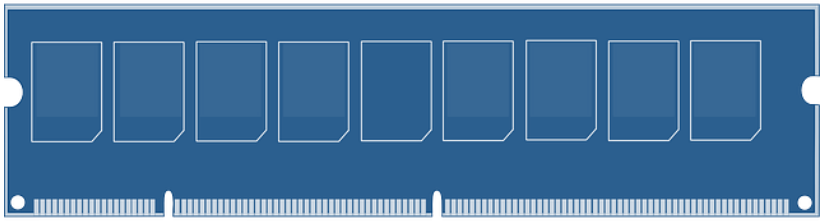
Trusted Foundry

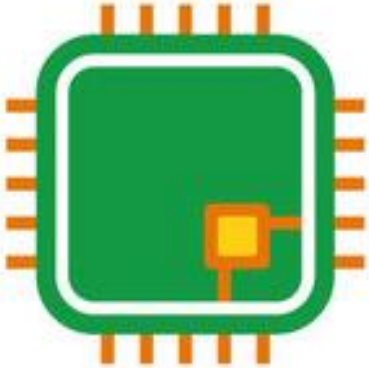
FAB CAPACITY

300mm
200K Wafers/Mo

200mm
133K Wafers/Mo

eMRAM and MRAM

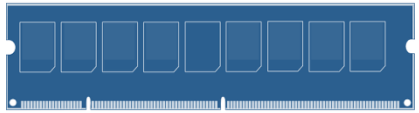




	Standalone MRAM	eMRAM
Technology	STT	STT
Bitcell	in-plane → perpendicular	perpendicular
Usage	data	code, data
Capacity	256Mb → 1Gb	32Mb, 64Mb, 128Mb
Interface	DDR	eFlash or SRAM
Feature	Speed, endurance	Data retention

GLOBALFOUNDRIES is fabricating both types

Lead customer success with GLOBALFOUNDRIES built MRAM



Everspin Releases Highest Density MRAM Products to Create Fastest And Most Reliable Non-Volatile Storage Class Memory

Everspin plans production of 256Mb & 1Gb products, bringing the most advanced memory solutions to the multi-billion dollar market for persistent memory in storage devices and servers.

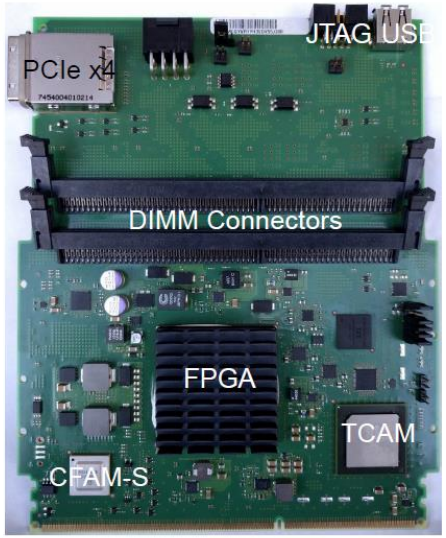
Chandler, AZ, April 13, 2016

Everspin Technologies announced today that it is shipping 256Mb ST-MRAM samples to global customers, enabling new product solutions using a true MRAM-based Storage Class Memory (SCM). This 256Mb ST-MRAM product breaks the record for the highest density commercial MRAM currently available in the market. Everspin, having held the previous record, has

POWER System with MRAM Memory

Revolutionizing the Datacenter

Con Tutto: Prototyping Platform

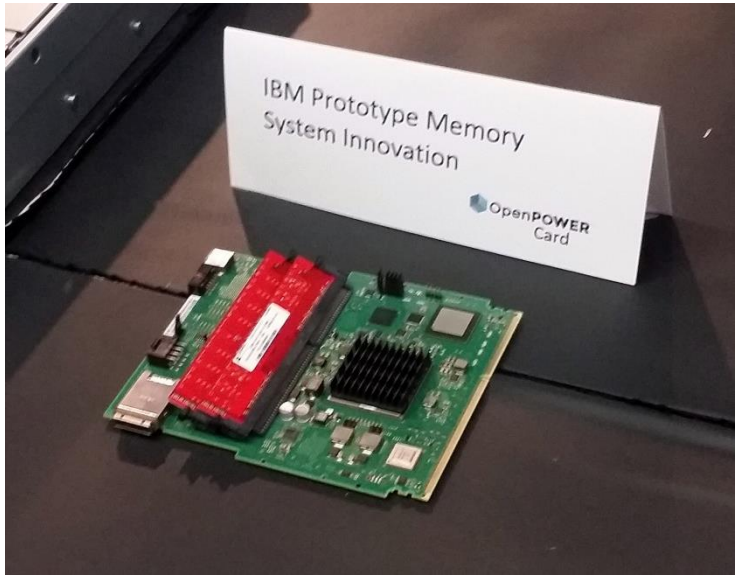


Differential Memory Interface Connector

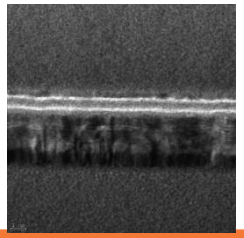
- Prepare for Future Memories: Enable MRAM, PCM, RRAM on the P8 memory bus
- Evaluate NVDIMMs: Enable NVDIMM-N/F in Power systems, functionally evaluate
- Innovate: Enable industry and OpenPOWER partners to innovate on the P8 Differential Memory Interface link

Activity

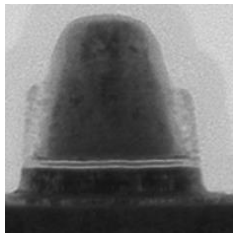
- NVmem Software Stack Changes
- Technology Enablement
  - NVDIMM-N – Ongoing ~2Q16
  - **MRAM – Operational now - Everspin**
  - Investigating other technologies
- **Near-Memory Acceleration** – Zurich Research Lab



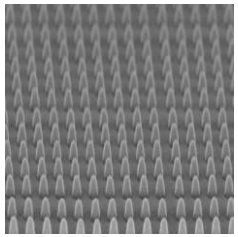
GLOBALFOUNDRIES eMRAM



Films

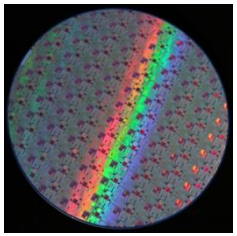


Integration



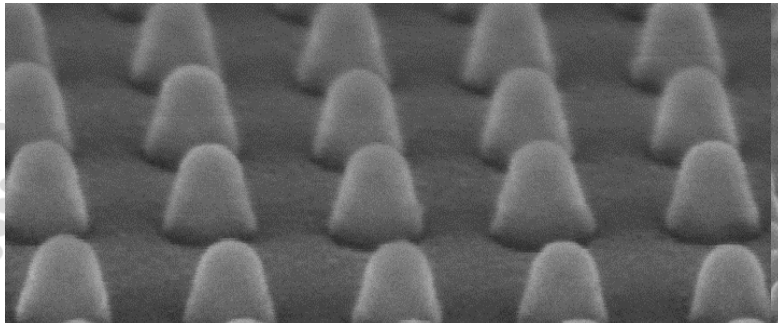
pMTJArrays

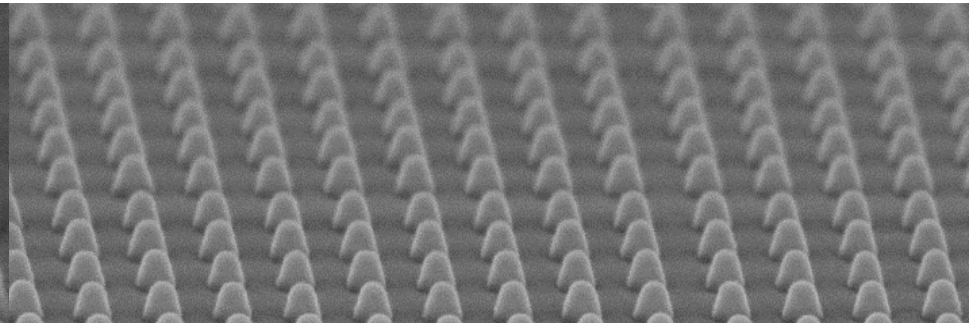
Now



Yield/Rel

Production





Final word…

Embedded Memory…

Persists:

1. Code

2. Data

3. State

Saves:

4. Time
5. Energy

GLOBALFOUNDRIES®

Embedded Memory

Solving your product challenges for the hyperconnected world

Thank you

dave.eggleston@globalfoundries.com

GLOBALFOUNDRIES®