

# NEMS memory for low power application

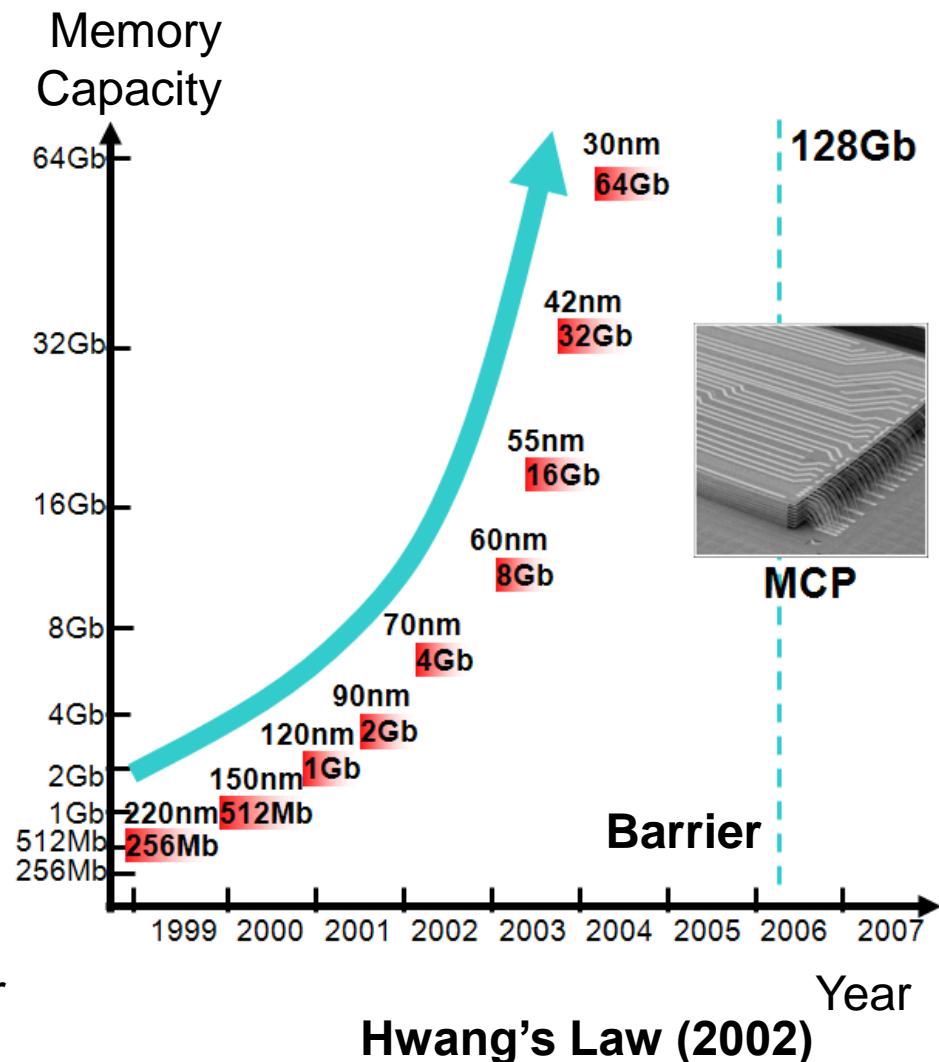
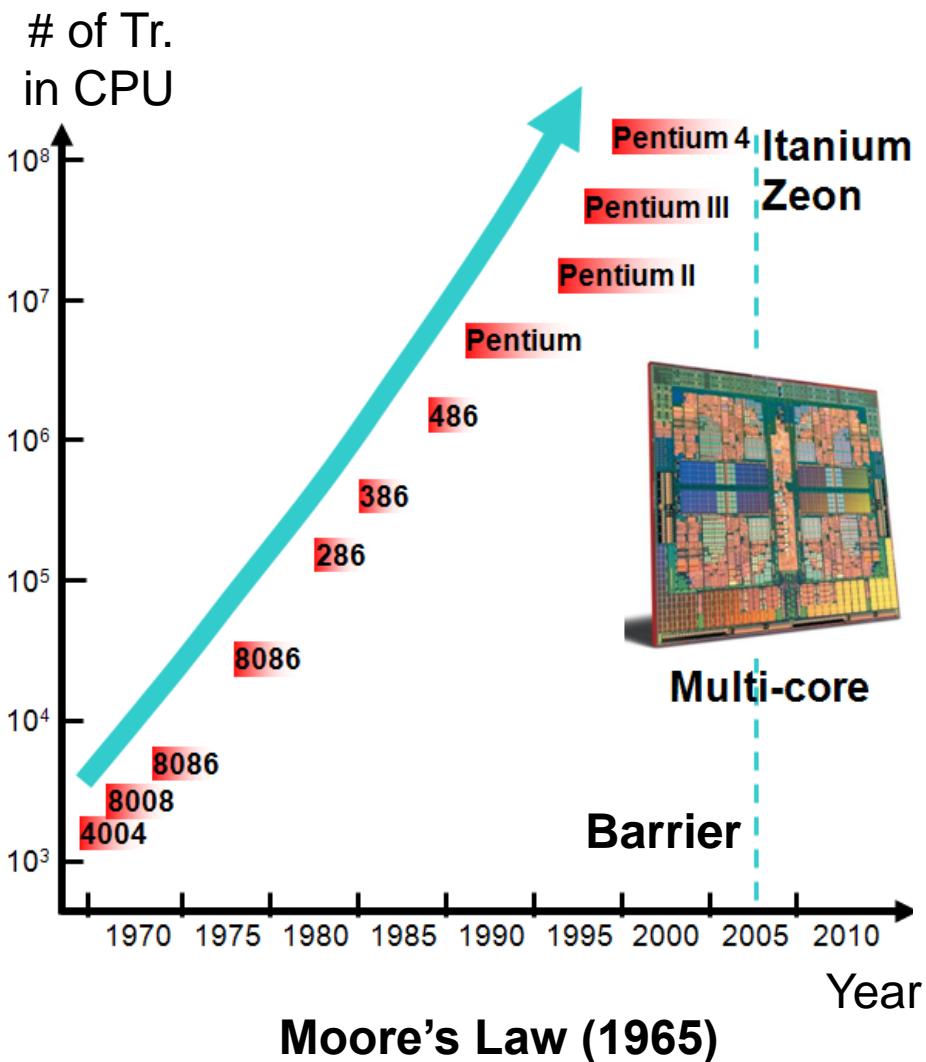
**Jin-Woo Han, Ph. D.**

*jin-woo.han@nasa.gov*

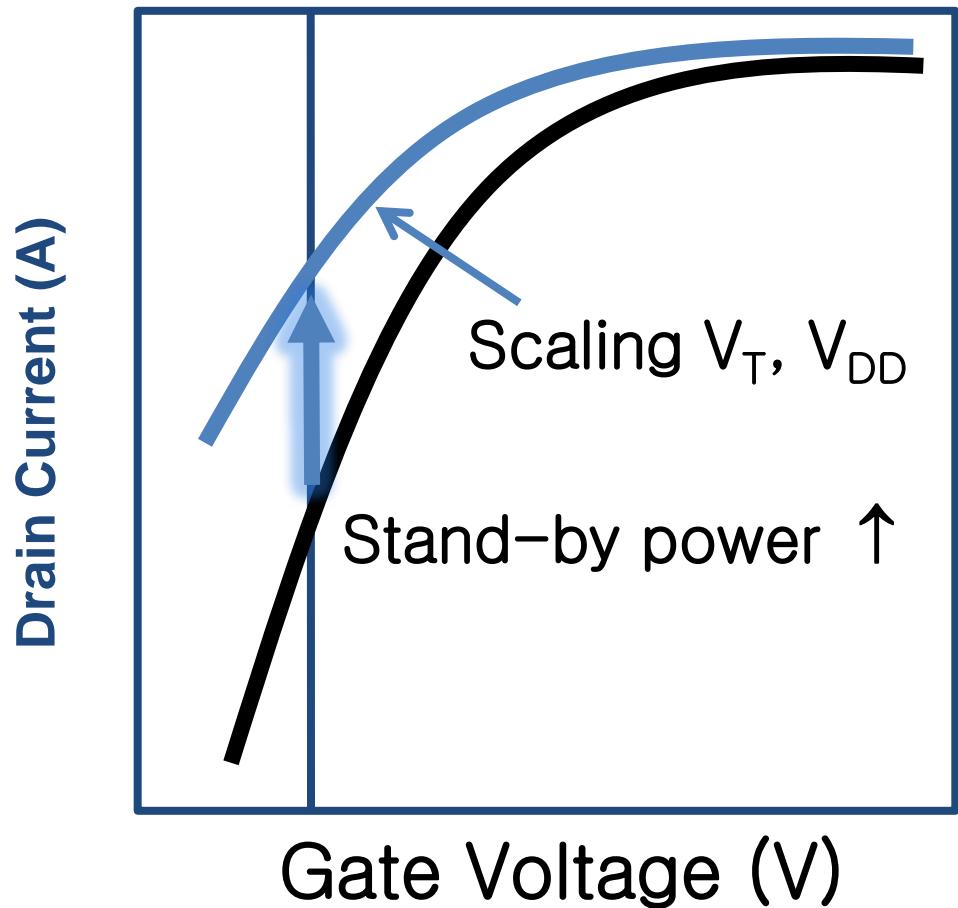
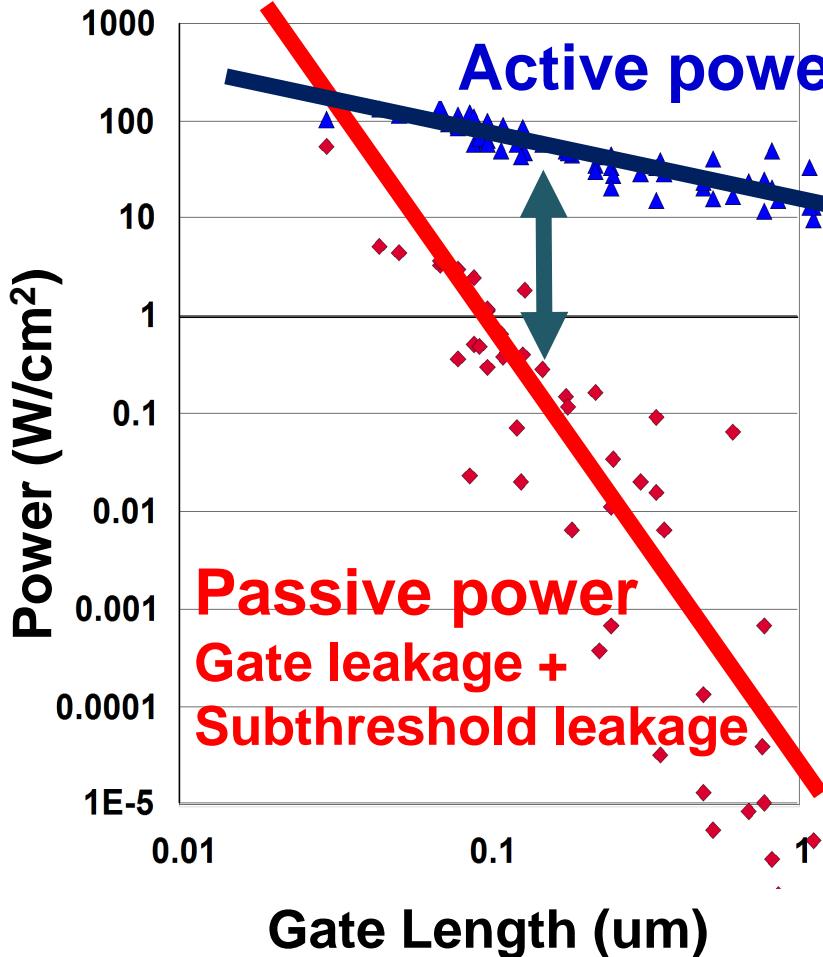
*Center for Nanotechnology, NASA Ames Research Center*

12/16/2014

# Moore's (Hwang's) Law

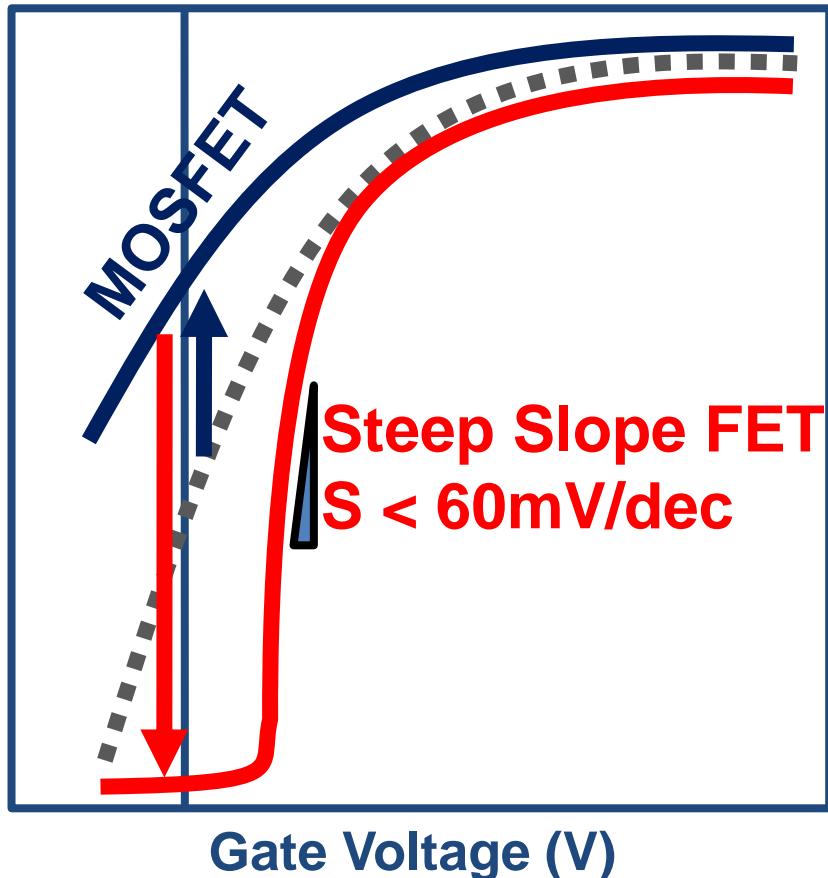


# Power Crisis in Scaling



$KT/q$  doesn't scale, lowering  $V_T$  increases leakage.

# Power Crisis & Steep Slope Transistor



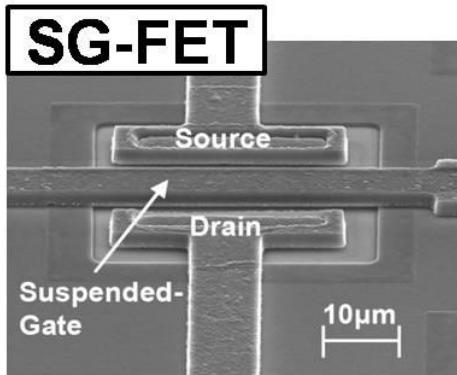
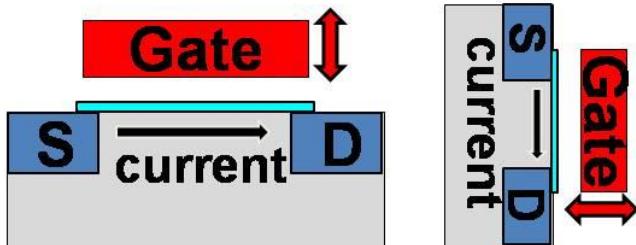
## Steep Slope FETs

- I-MOS
  - T-FET
  - Ferroelectric FET
  - NEM FET
- (Nano-Electro-Mechanical)

Steep slope device suppresses the stand-by leakage

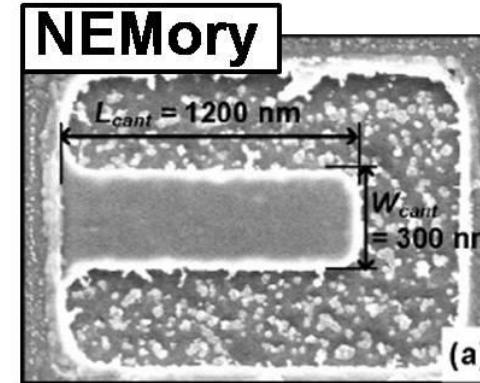
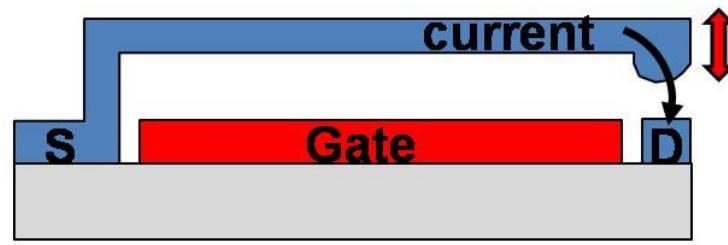
# Nano-Electro-Mechanical Switches

## Suspended-Gate Type

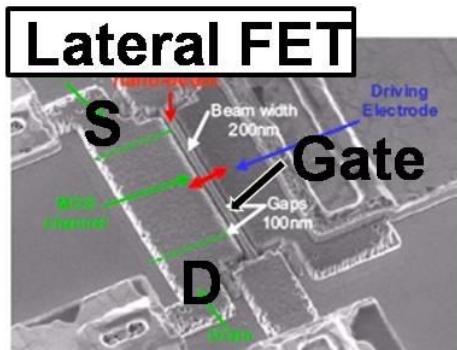


EPFL  
IEDM 2006  
UC Berkeley  
IEDM 2005

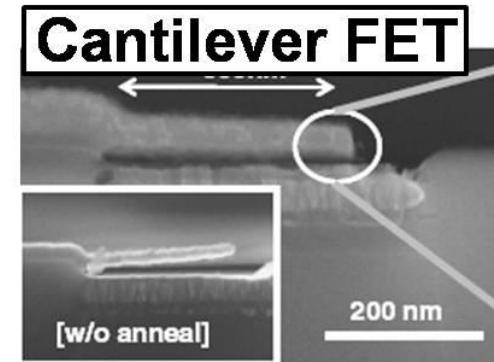
## Cantilever Type



UC Berkeley  
IEDM 2007



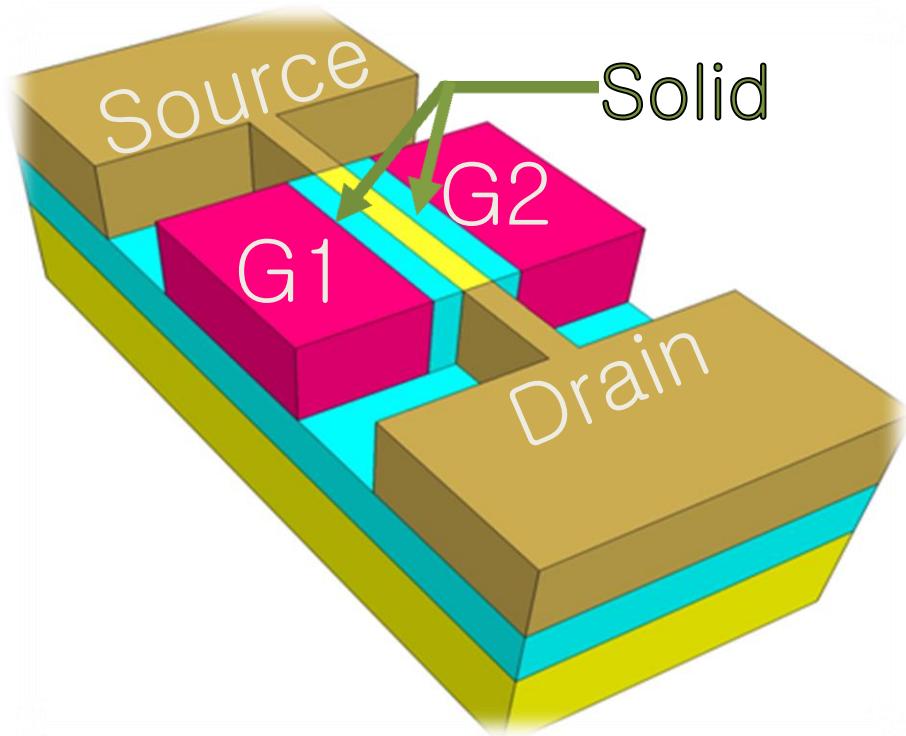
CEA-LETI  
MEMS 2008



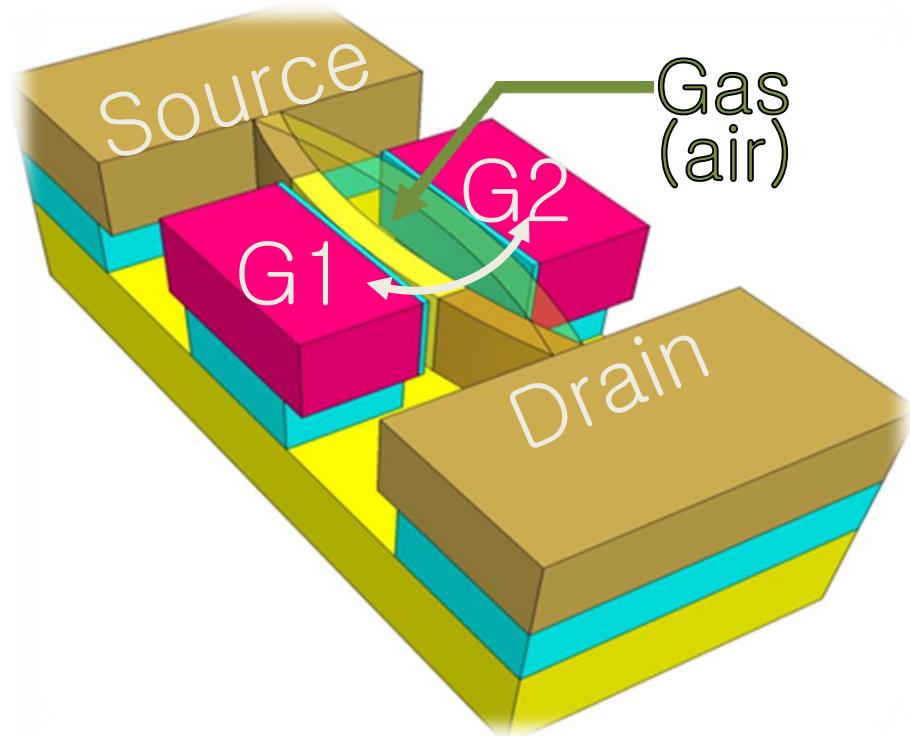
KAIST  
APL 2008  
Stanford  
IEDM 2007

# Our NEM Switch

## Gate oxide removal and re-oxidation



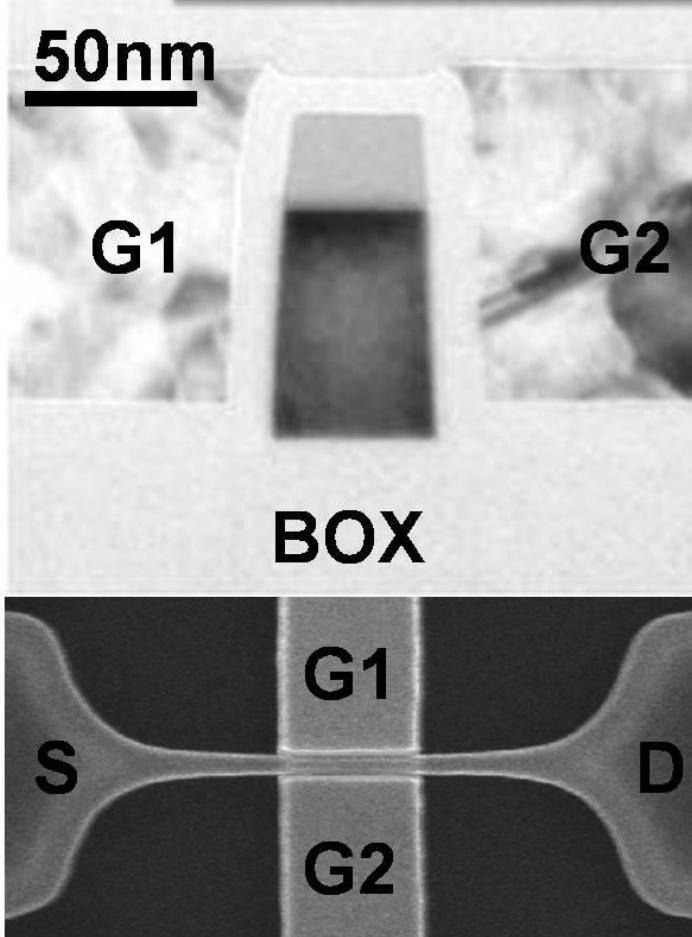
**Independent gate  
FinFET**



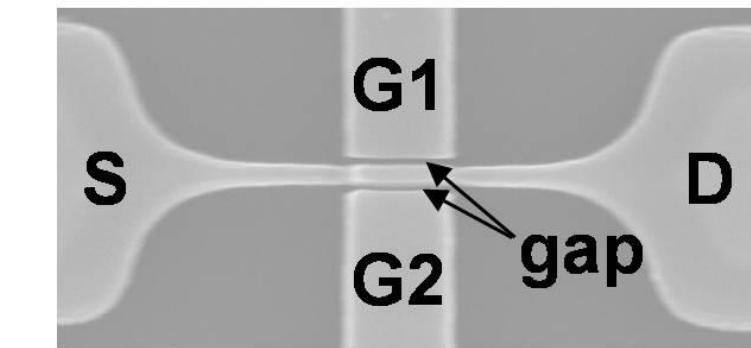
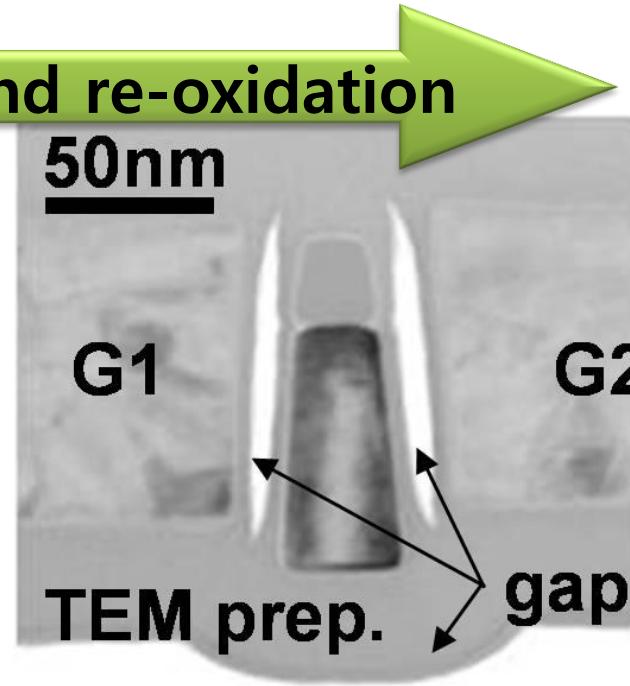
**Fin Flip-Flop  
FinFET**

# TEM/SEM Images

Gate-oxide removal and re-oxidation

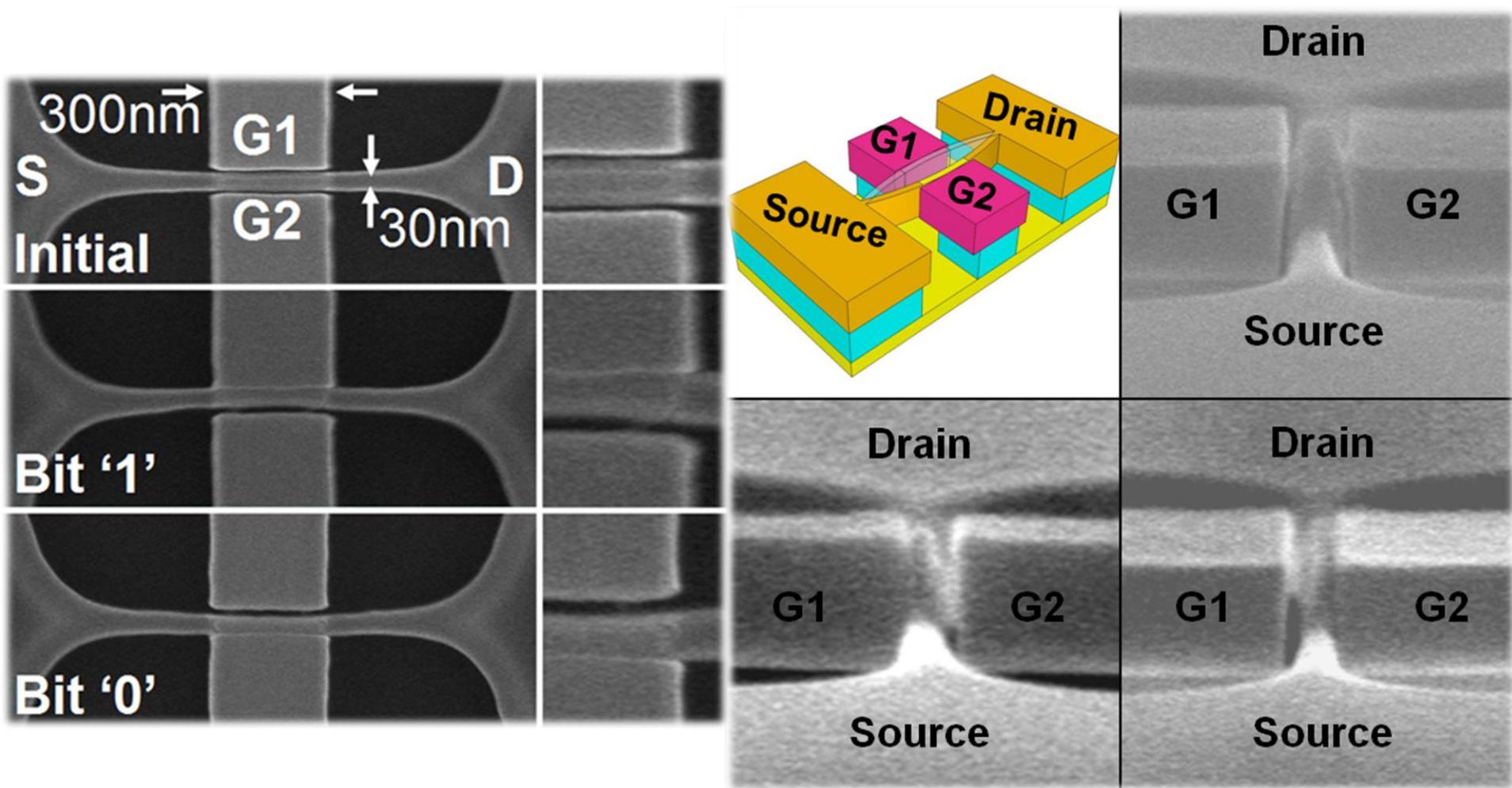


IDG FinFET

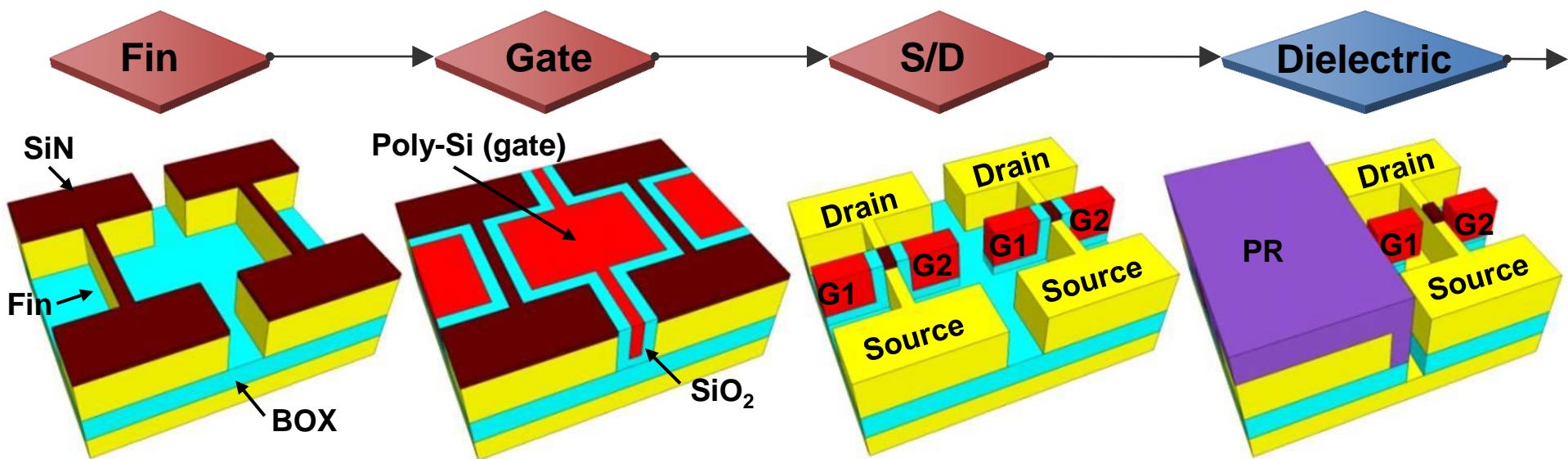


Nanogap DG FinFET

# TEM/SEM Images



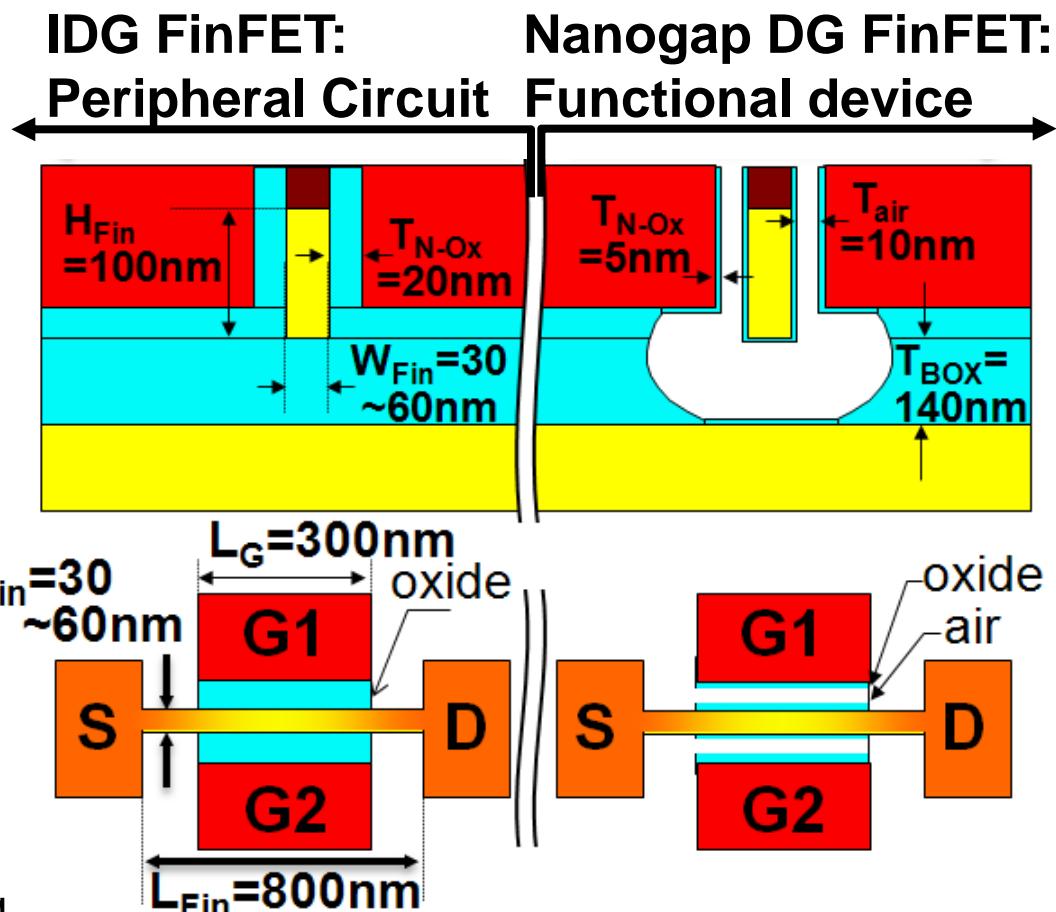
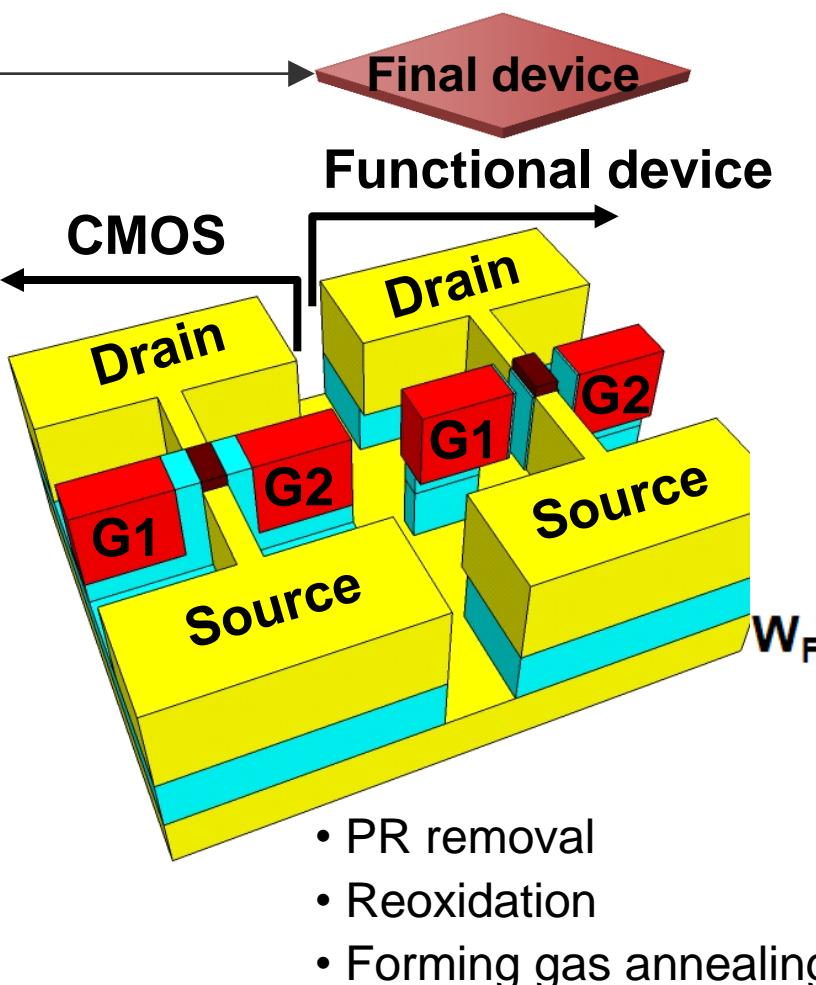
# Monolithic Integration with IDG FinFET



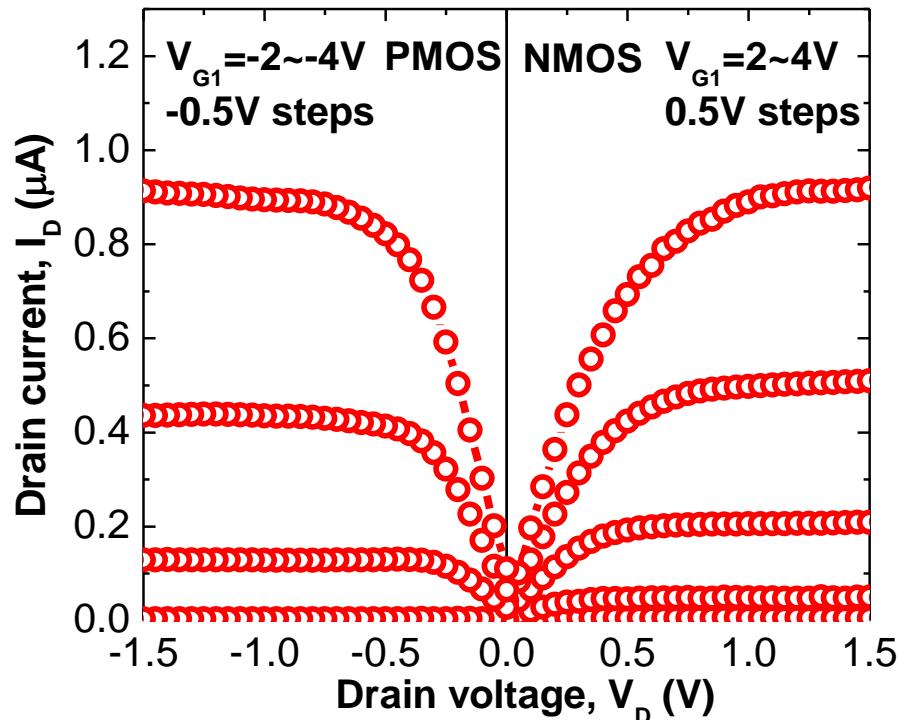
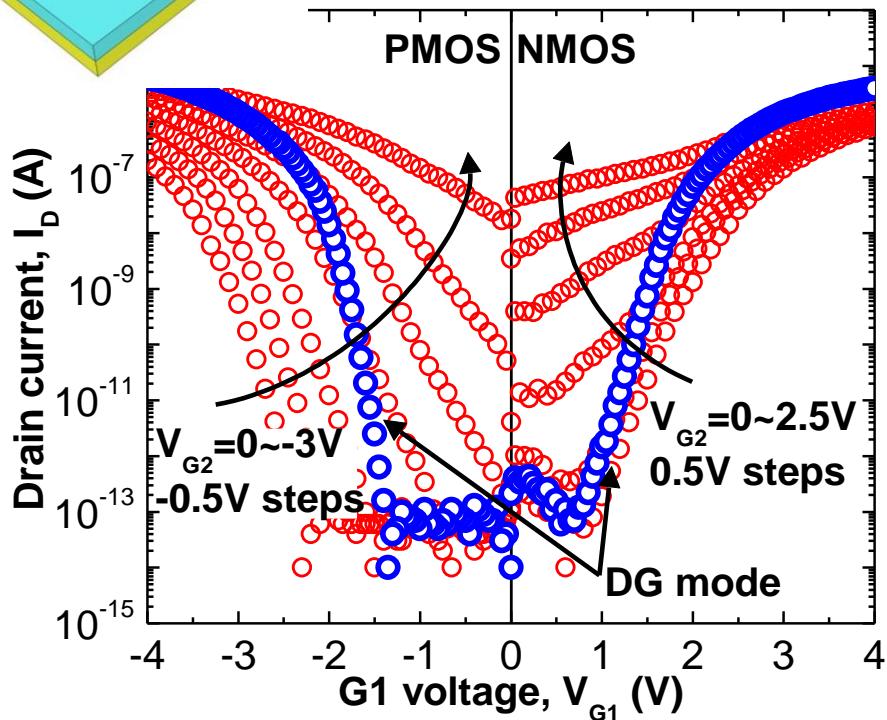
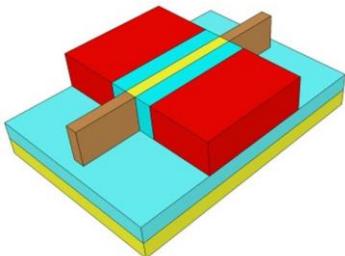
- (100) 8" SOI Wafer
- Channel IIP
- SiN dep. (50nm)
- Fin formation (30nm)
- SiO<sub>2</sub> depo. (20nm)
- Poly-Si depo. (100nm)
- Poly-Si CMP
- Poly-Si patterning
- S/D IIP
- Activation
- PR shielding
- SiO<sub>2</sub> removal

\* 0.18μm CMOS foundry technology

# Monolithic Integration with IDG FinFET



# IV Characteristics of IDG FinFET

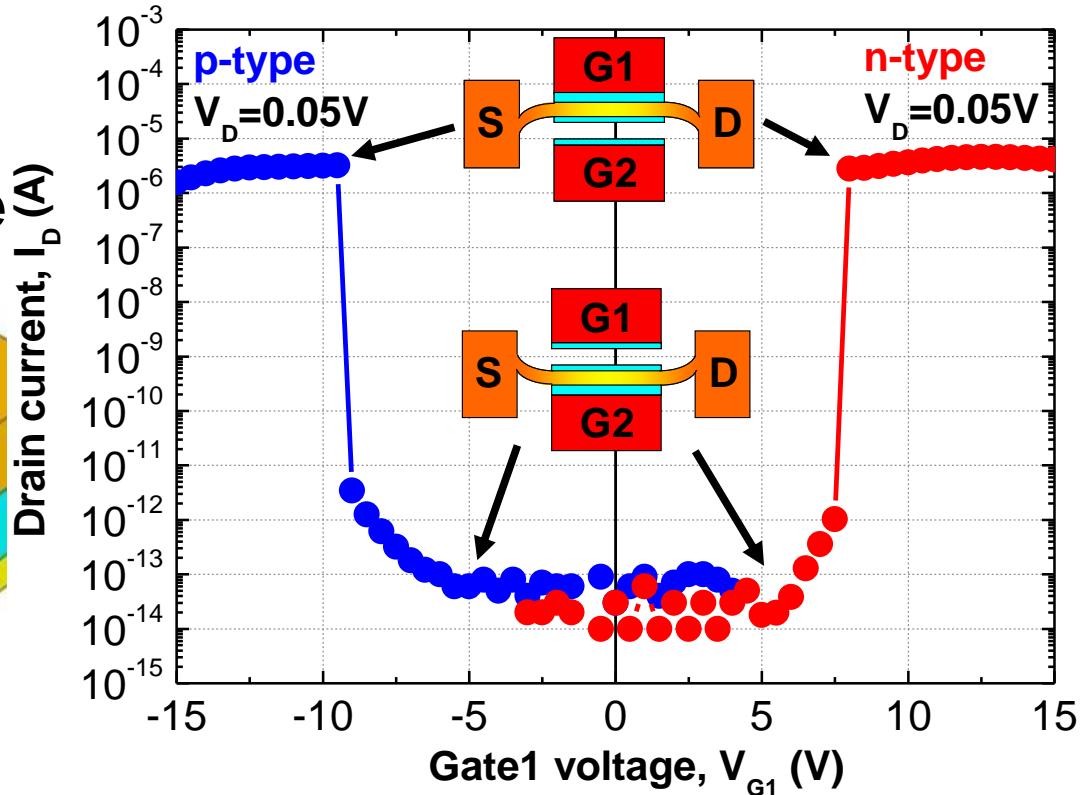
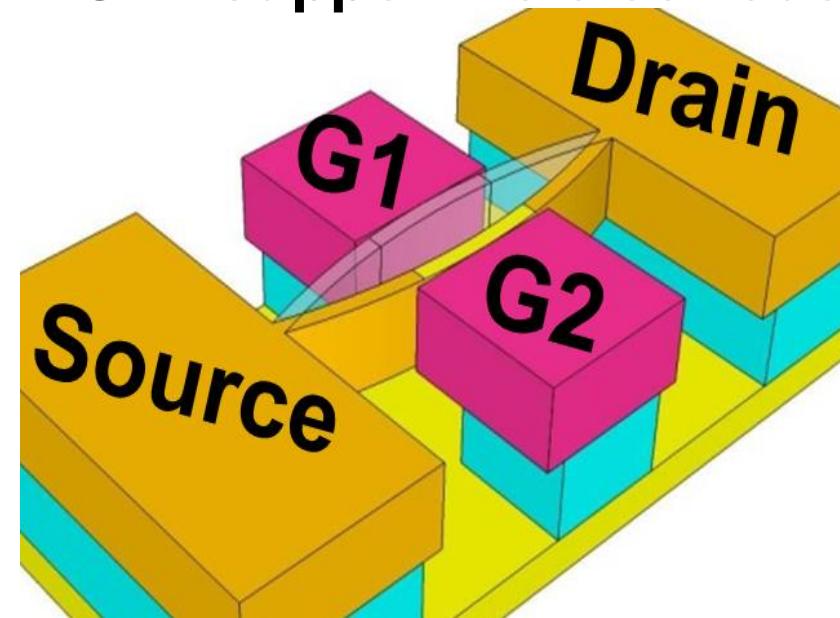


Back-gate factors of  $dV_T/dV_{G_2} \sim 0.66$  at  $W_{Fin} = 30\text{nm}$

# New NEM Switch – FinFACT\*

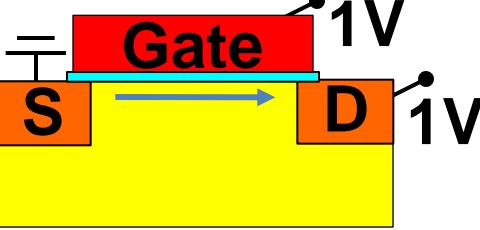
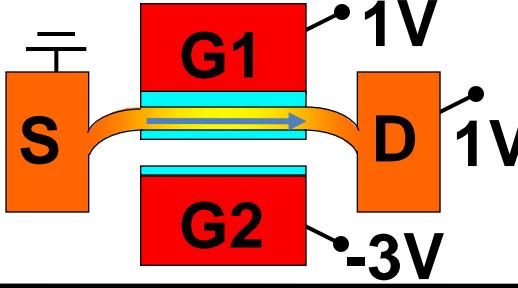
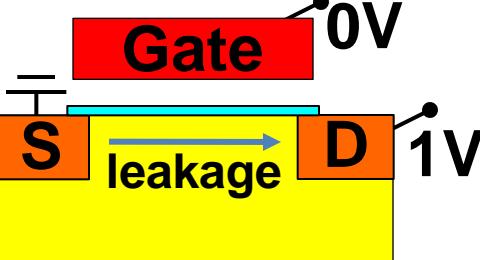
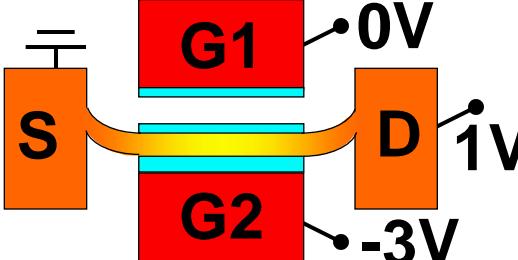
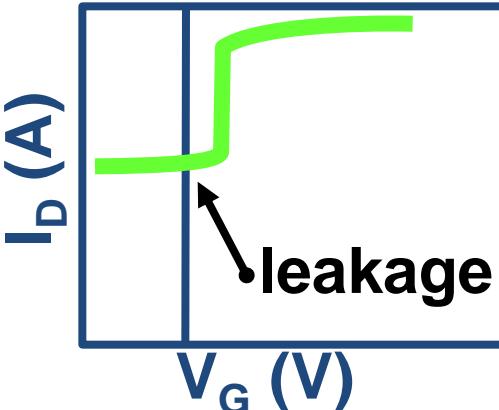
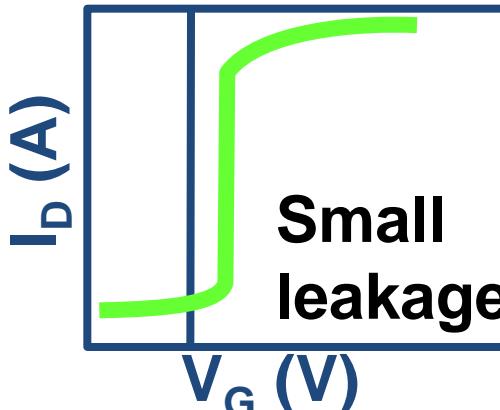
## (Fin Flip-flop Actuation Channel Transistor)

- Fin : lateral flip-flop
- G1 : driving electrode
- G2 : supportive electrode

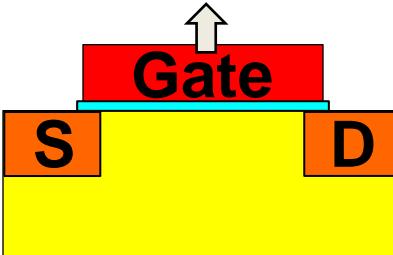
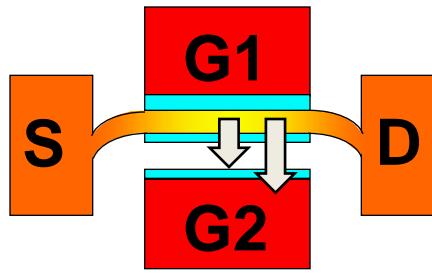


\* J.-W. Han *et al.*, IEEE Electron Device Letters, Jul. 2010

# Comparison with SG MOS: Off-current

	SG-MOSFET	FinFACT
On-state		
Off-state		
Transfer Curve		

# Comparison with SG MOS: Pull-off

	SG-MOSFET	FinFACT
On-state		
Restore (pull-off) source	Elastic force of gate	1) Elastic force of fin 2) Electrostatic force → Stiction immunity
Actuation	Out-of-plane (vertical)	In-plane (lateral)
Spring factor	Gate thickness (single $k^*$ )	Fin width (multiple $k^*$ )

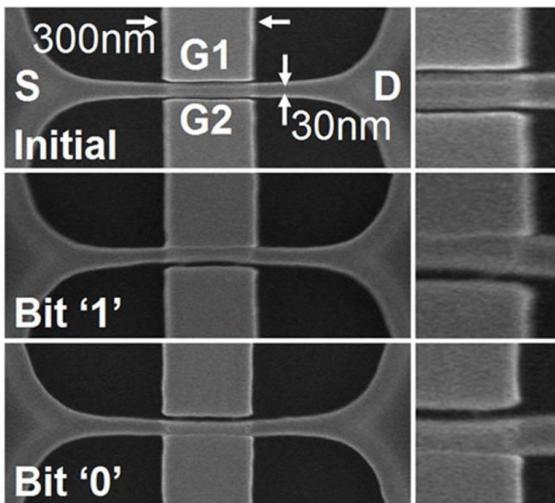
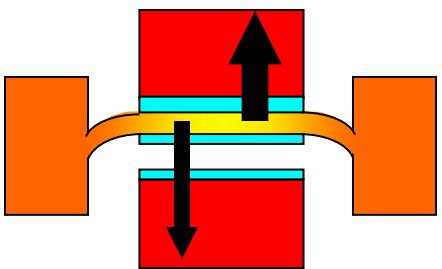
# Comparison with Cantilever: Reliability

	Cantilever FET	FinFACT
On-state		
Actuation		
Current flow		
Direction of actuation & current flow	Coupled	Decoupled
In-use stiction	Arc welding & Joule heating	Free of arc & Joule heating

# Ultra Low Power Nonvolatile Memory

## Retention of Mechanical State

Surface Adhesion  
: Van Der Walls

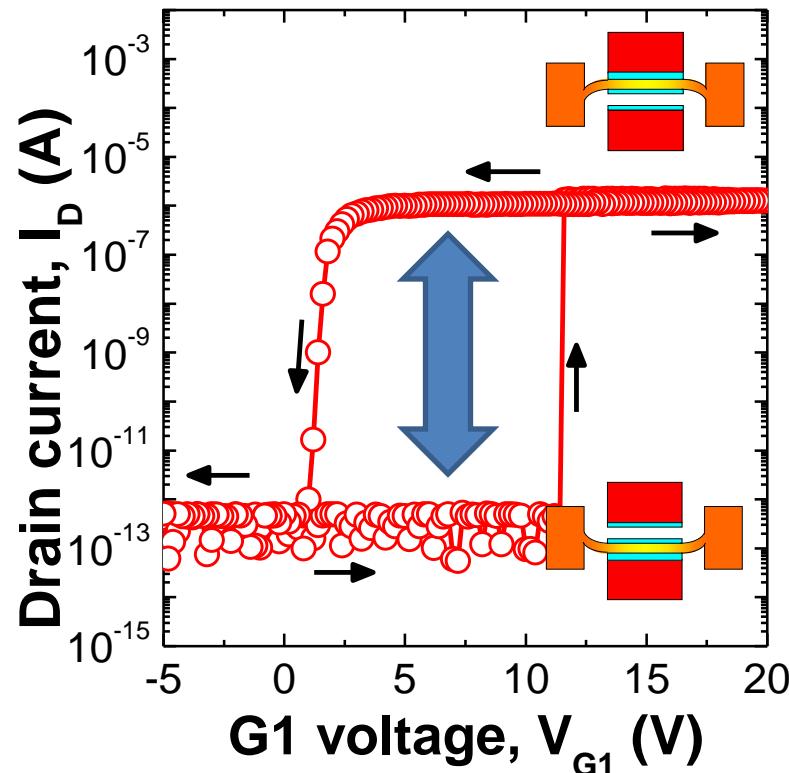


Restoration  
: Elastic

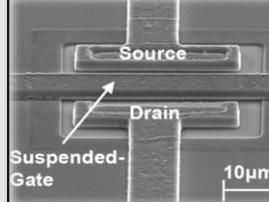
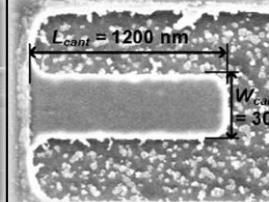
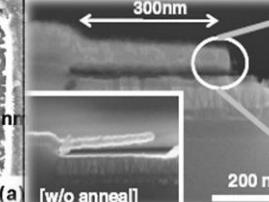
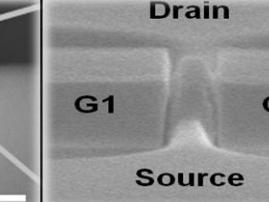
If, fin is narrow enough,  
adhesion force > Elastic force

$$F_{Spring} = kx, \quad k = 16E_Y H_{Fin} (W_{Fin} / L_{Fin})^3$$

## Hysteric I-V Curves



# Comparison of NEMS Memory

	SG MOSFET (IEDM 2006) EPFL	NEMORY (IEDM 2007) Berkeley	Cantilever (APL 2008) KAIST	FinFACT (IEDM 2009)
Image				
Material	AISI (1%)	Al	TiN	Si
Beam thickness (nm)	18000	100	35	30, 40, 50, 60
Dimension (nm X nm)	34000 X 6000	1200 X 300	200 X 300	100 X 300
Gap width (nm)	40	30	15	10
Sensing window(A/A)	< 10 <sup>4</sup> (High off-leakage)	<10 <sup>5</sup> (low on-current)	<10 <sup>5</sup> (low on-current)	>10 <sup>7</sup>
Retention in air (sec)	~ 10 <sup>4</sup>	N. A.	10 <sup>3</sup>	~ 10 <sup>4</sup>
Endurance (#)	>10 <sup>5</sup>	< 10	10 <sup>5</sup>	10 <sup>4</sup>
Operation Voltage (V)	10	5	25	12
Issue	Pull-off	Welding	Welding	Mechanical Stability