Memory Selector Devices

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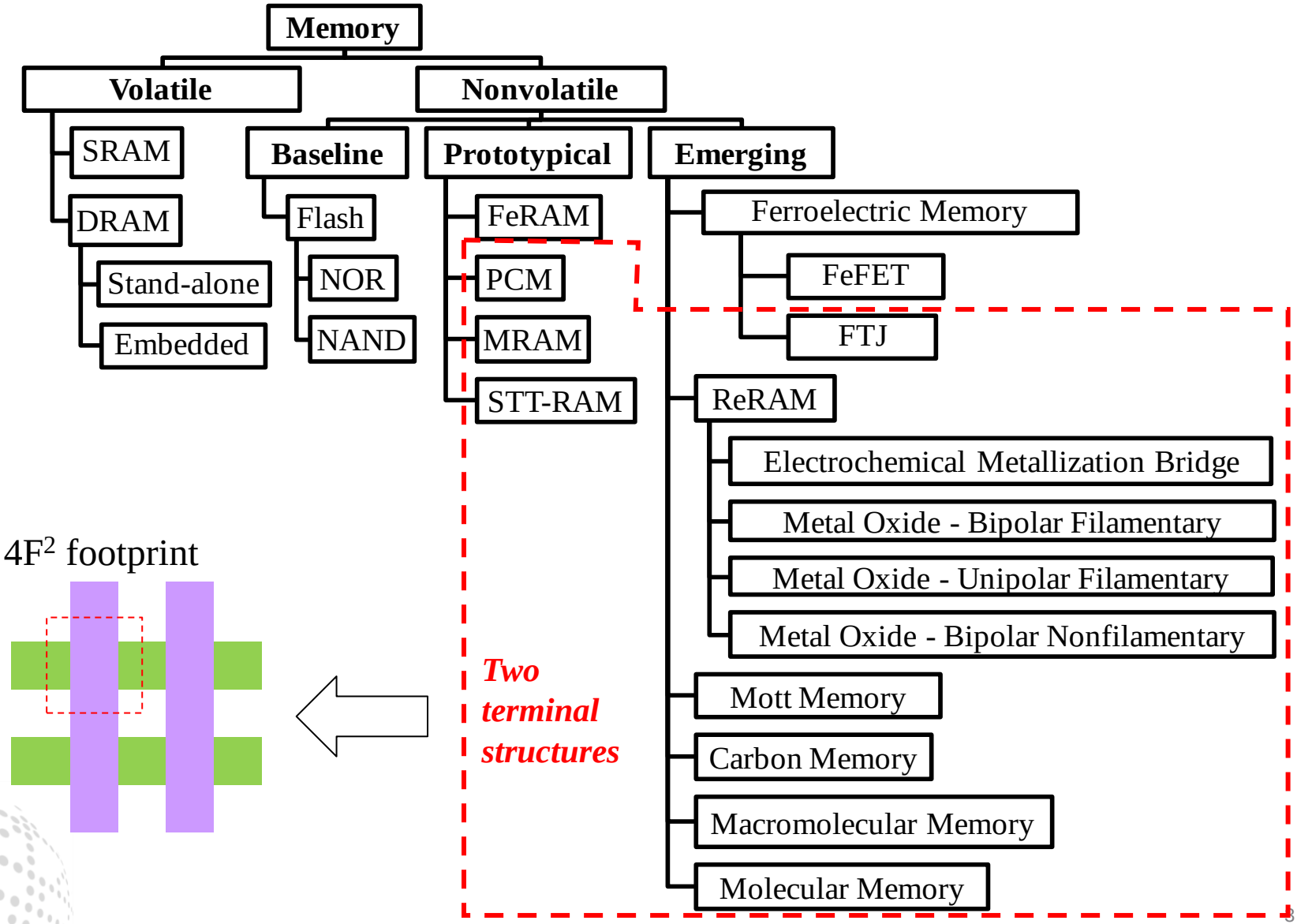
2014 AVS TFUG Seminar

GLOBALFOUNDRIES®

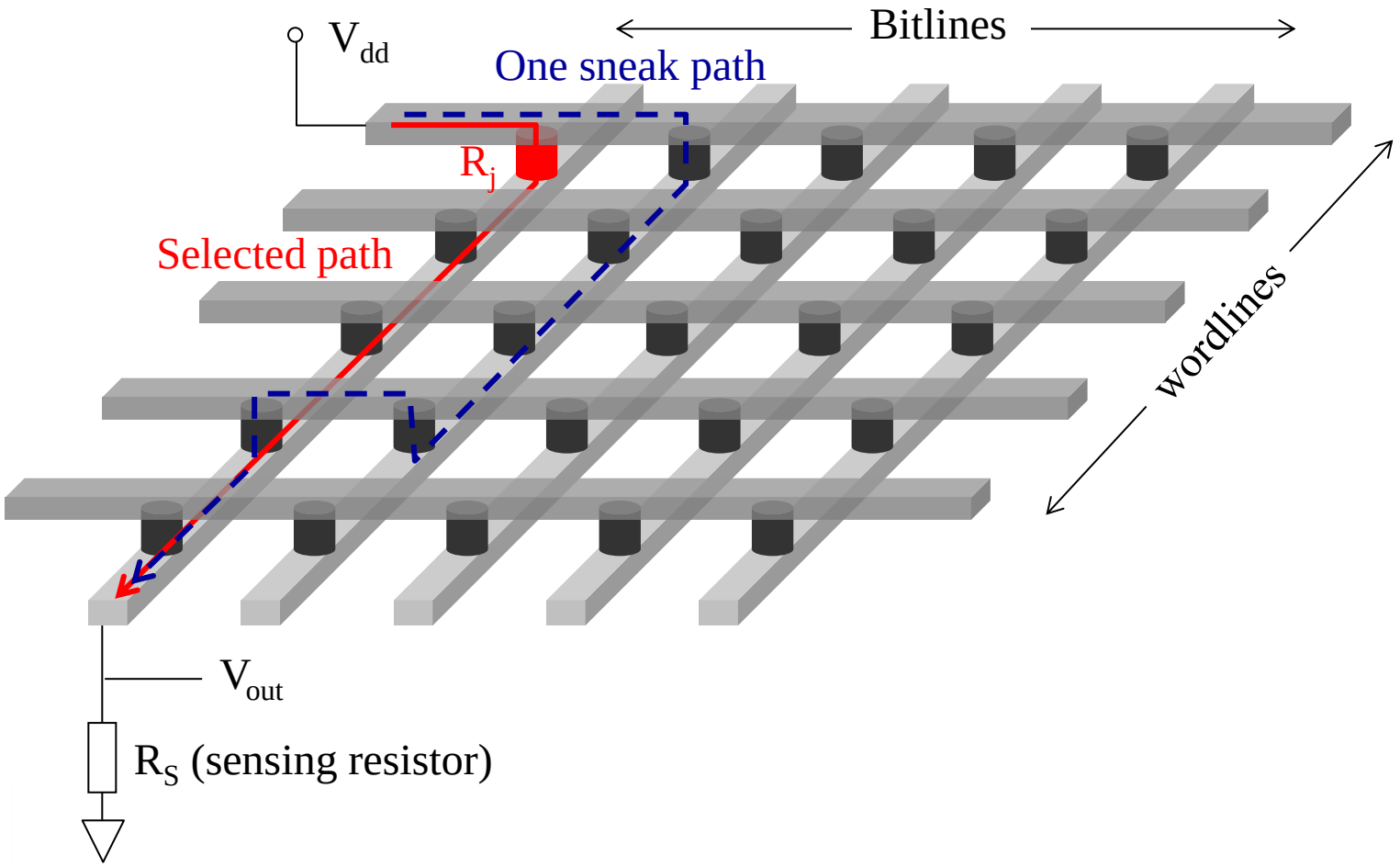
Outline

- Emerging memories and crossbar array architecture
- Memory selector device options and requirements
  - Asymmetry and nonlinearity for device selection
  - Selector device requirements
- Crossbar array modeling with selector device
  - Crossbar array model and parameters
  - Impact of selectors on crossbar array operations
  - A case study: 4kb crossbar array with nonlinear selectors
- Summary

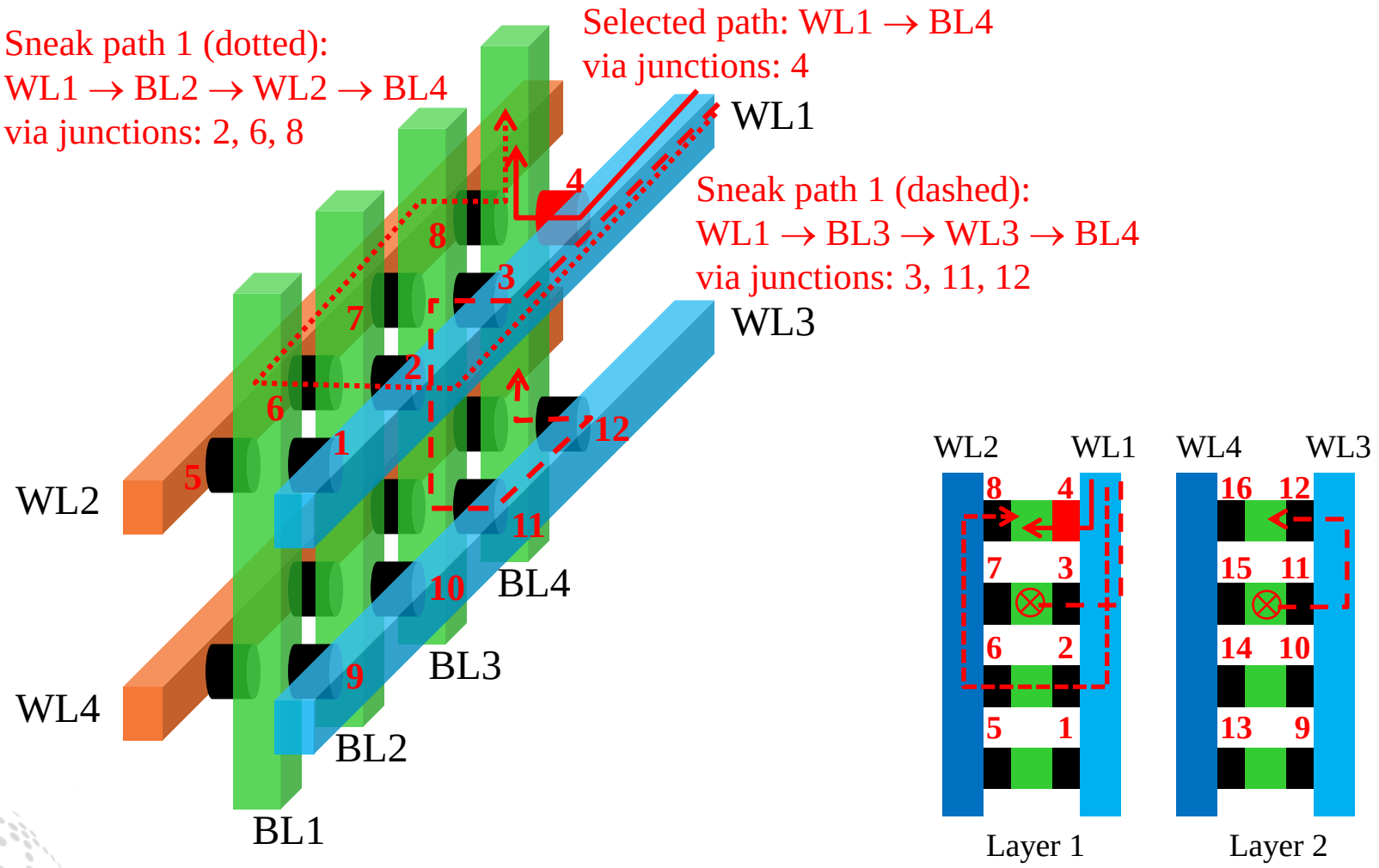
Emerging Memory Taxonomy



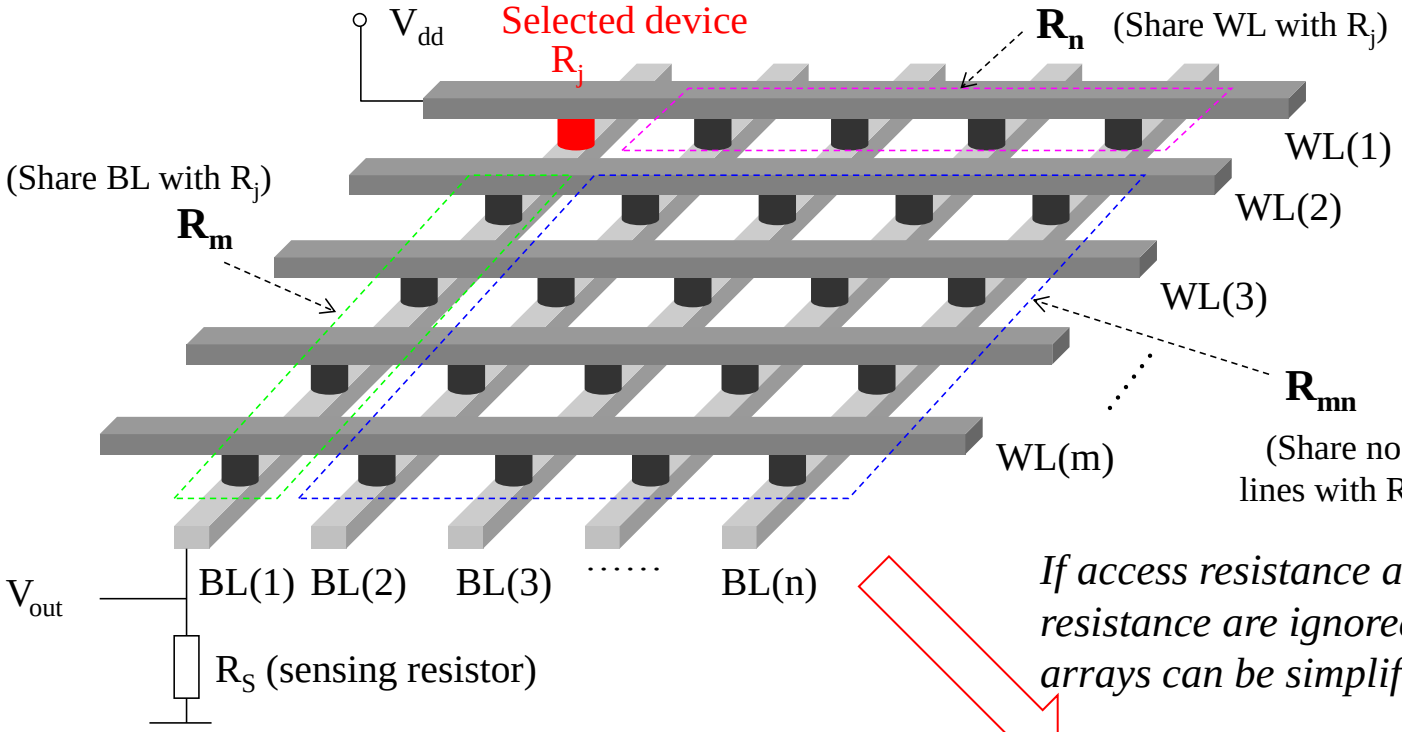
Crossbar Array and Sneak Paths



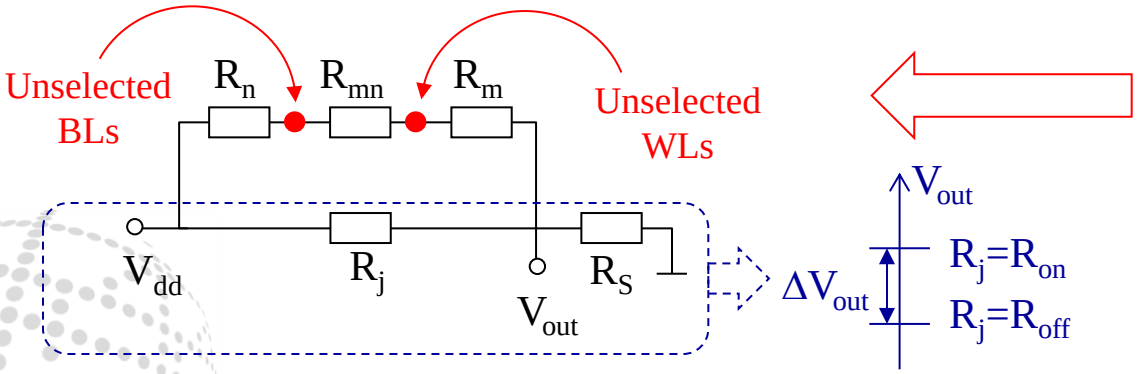
Vertical Crossbar Array and Sneak Paths

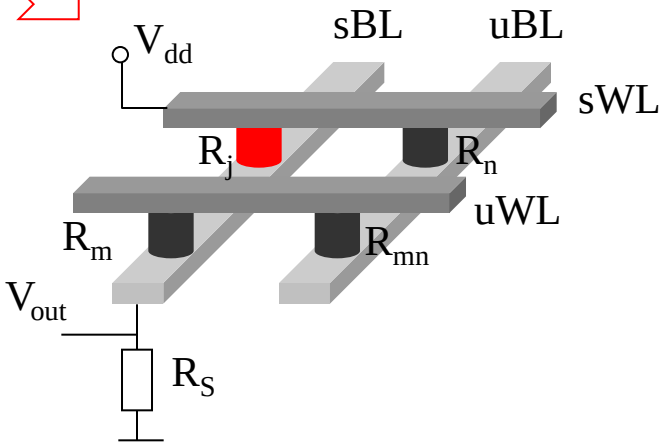


Sensing Margin (SM)

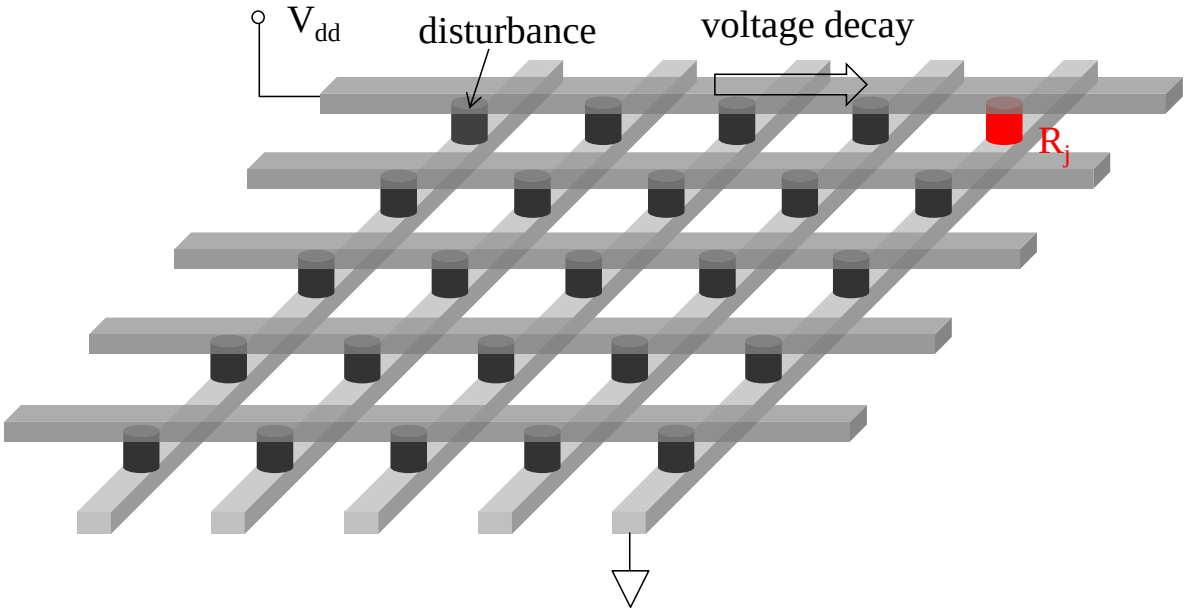


If access resistance and line resistance are ignored, crossbar arrays can be simplified

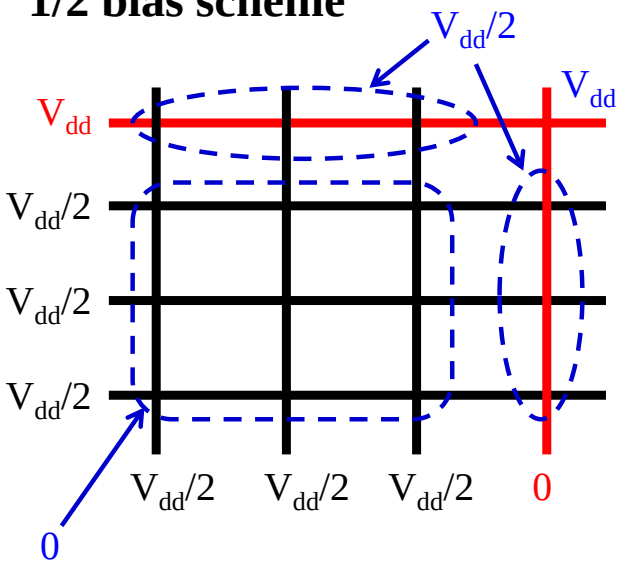




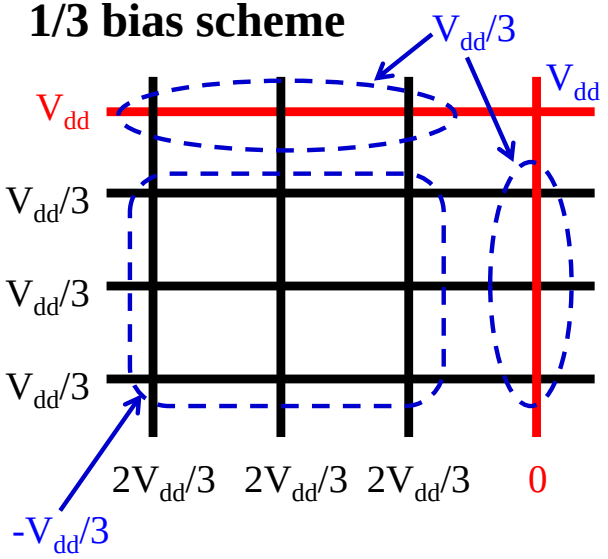
Writing Voltage Margin (WVM)



1/2 bias scheme



1/3 bias scheme



- Location affect voltage
- Line resistance cause voltage decay

$$WVM = V_{(\text{selected device})} - \max. V_{(\text{unselected devices})}$$

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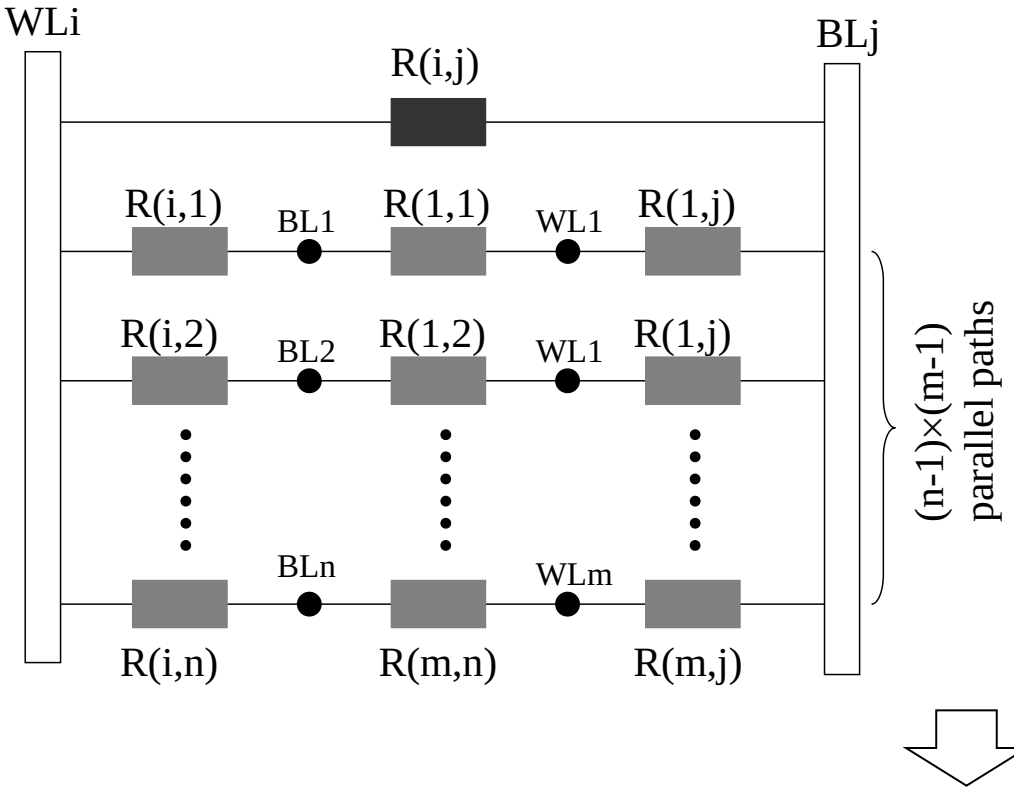
Asymmetry/Nonlinearity for Device Selection

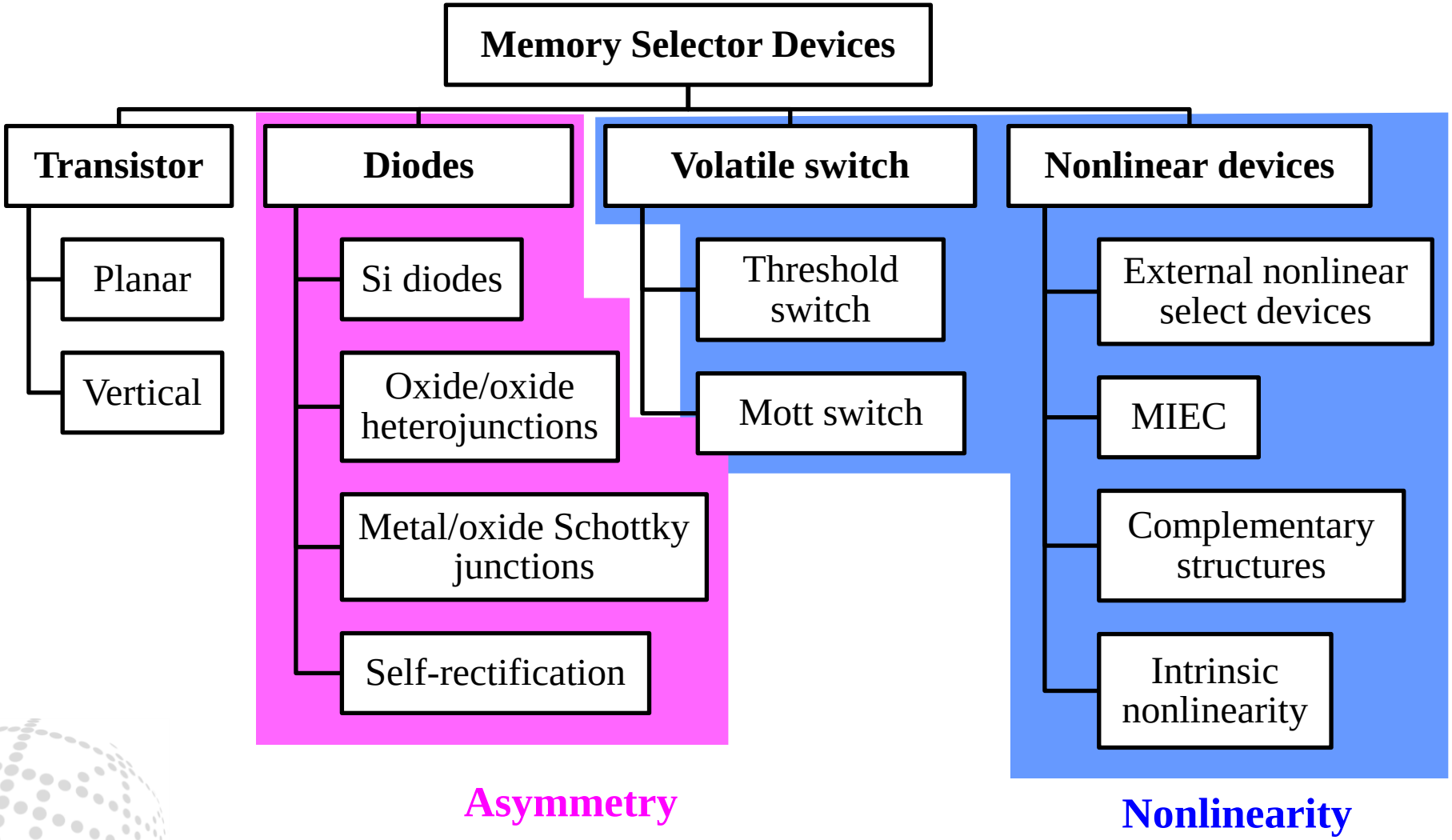


Features of sneak paths:

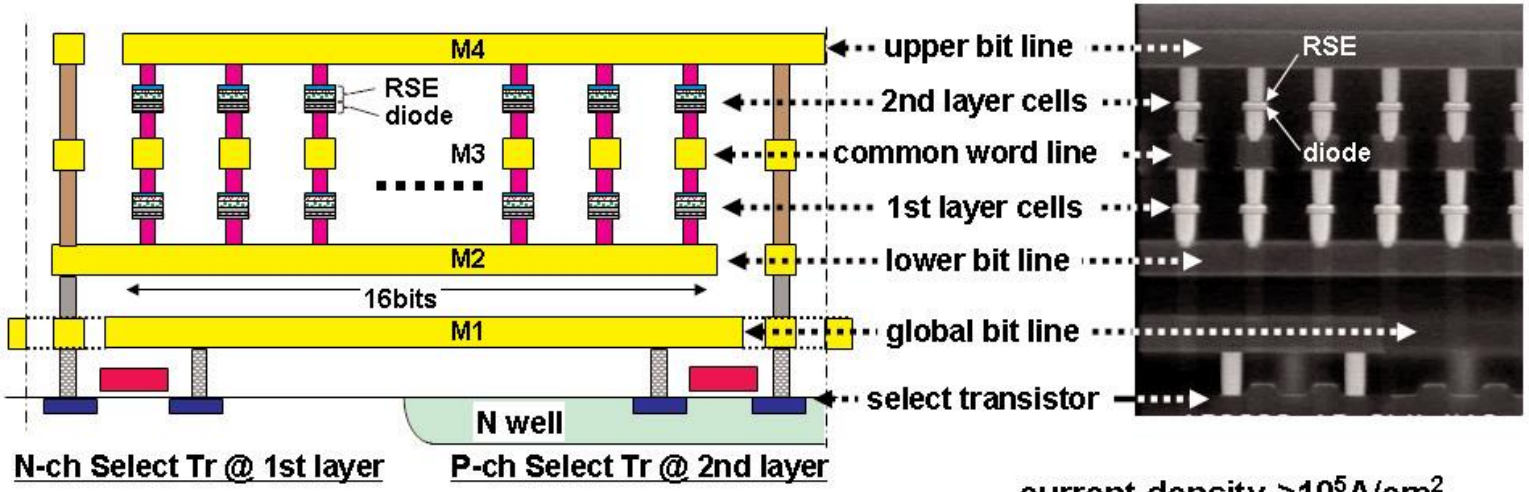
- There is always a reverse conduction segment
- Unselected devices typically have lower voltage than the selected device

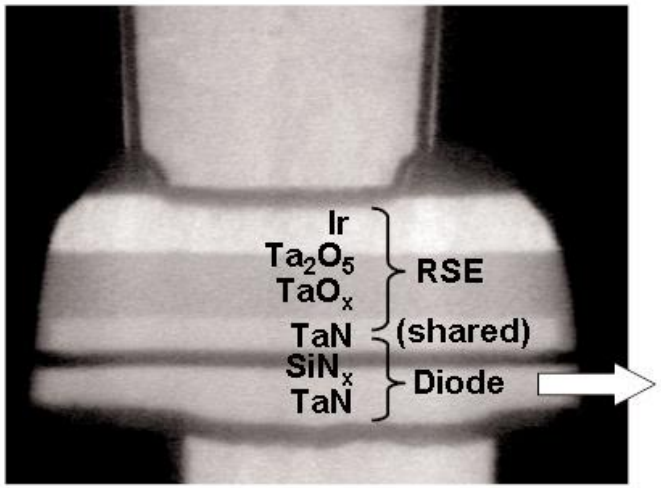
- **Asymmetry** (reverse resistance >> forward resistance) → sneak path resistance is increased by reverse resistance
- **Nonlinearity** (voltage-dependent resistance) → unselected devices with lower voltage are more resistive and reduce leakage through leakage paths

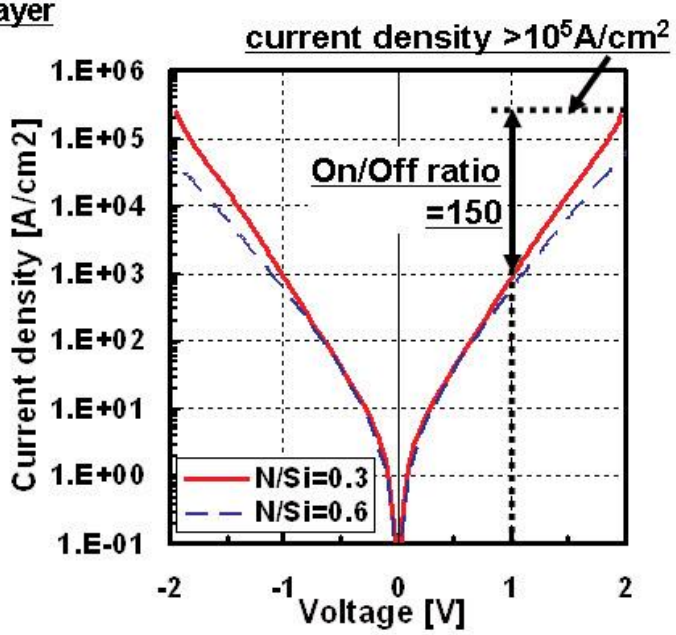
Selector Device Options



Nonlinear Bidirectional Diode Selector

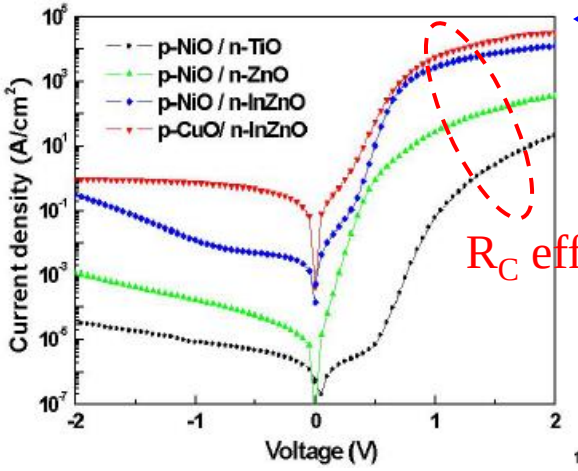






Panasonic: ISSCC 25.6 (2012)

Oxide Heterojunction Selector



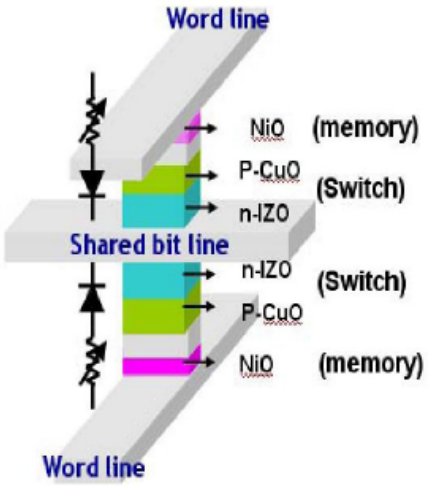
(a)

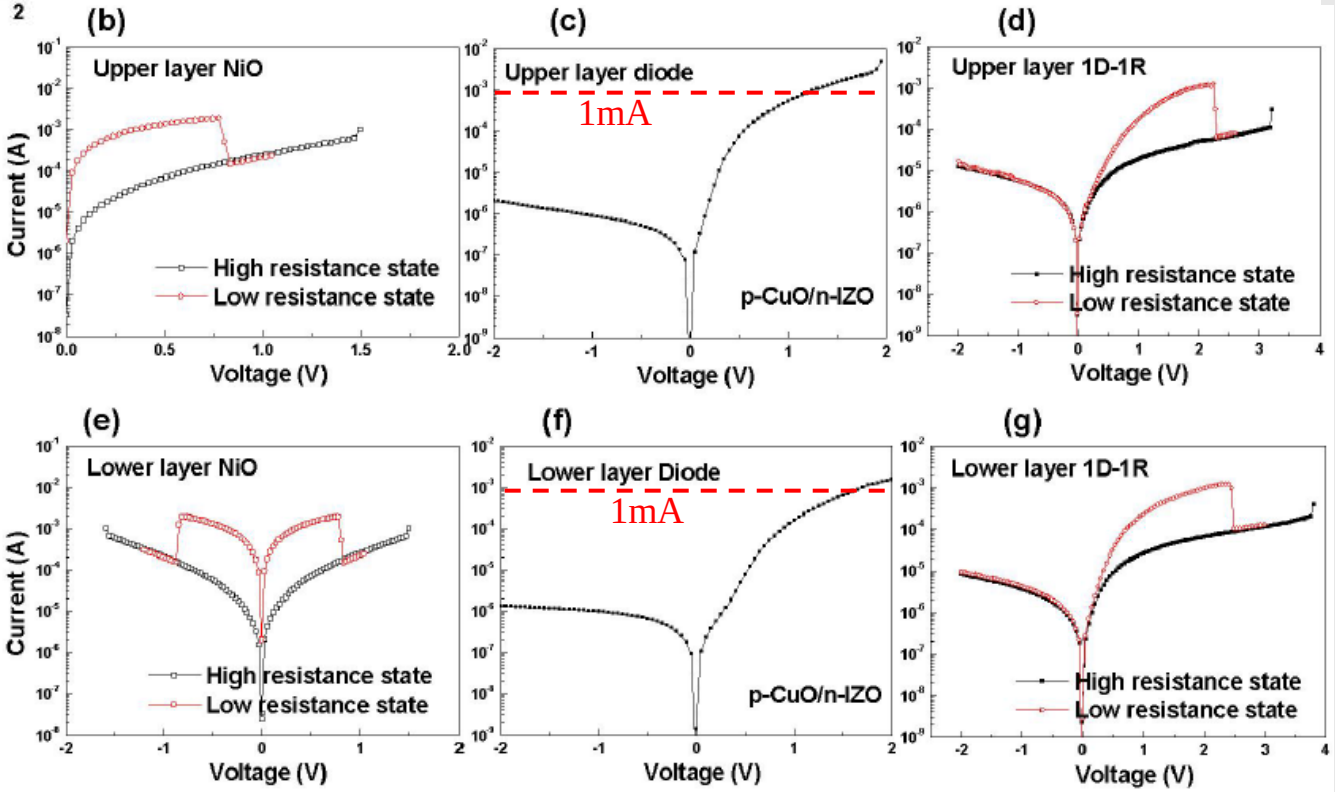
← 10^5 A/cm^2

10×10 nm^2 size with J = 1MA/cm^2
$\Rightarrow$ I = 1μA

Forward current:
NiO/TiO < NiO/ZnO < NiO/InZnO < CuO/InZnO

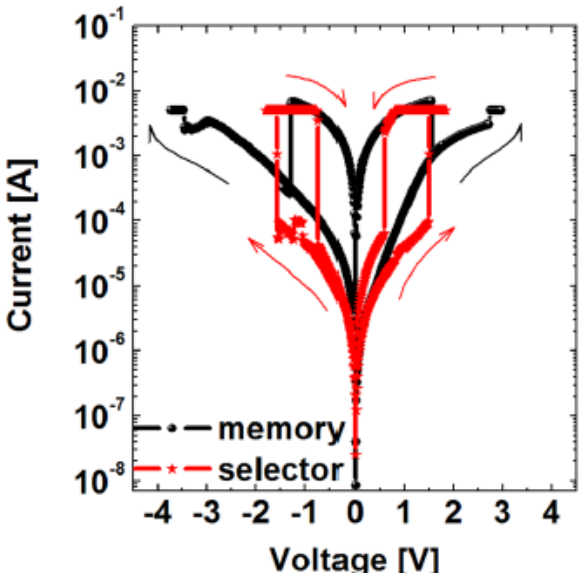
Cell size: 0.5μm × 0.5μm





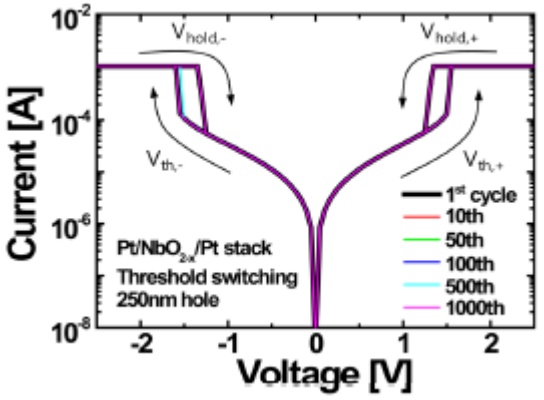
Samsung: IEDM 771 (2007)

Volatile Threshold Switch Selectors



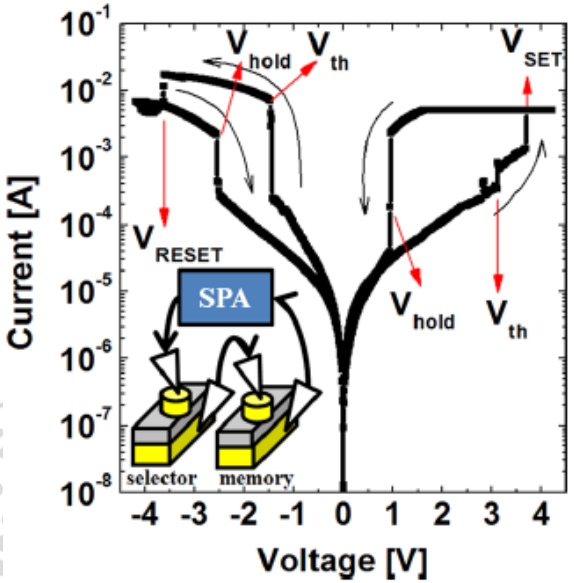
Si-As-Te switch

*APL **100**, 123505 (2012)*

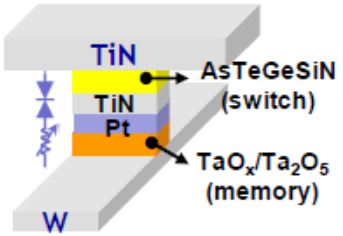


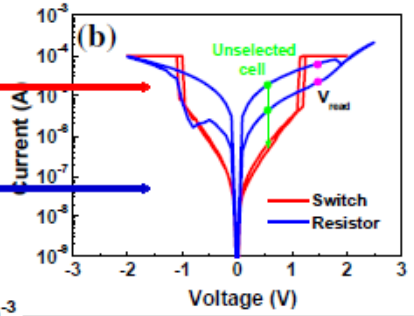
NbO_{2-x} switch

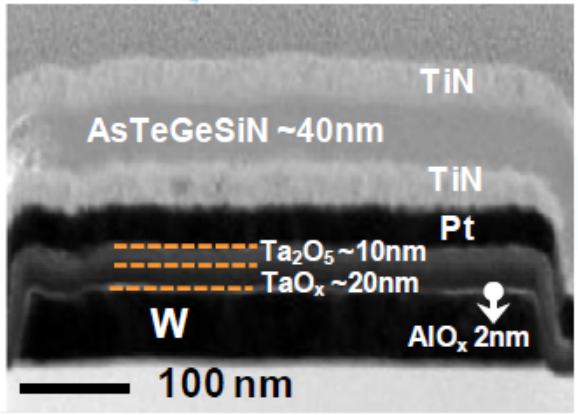
VLSI Tech (2012)

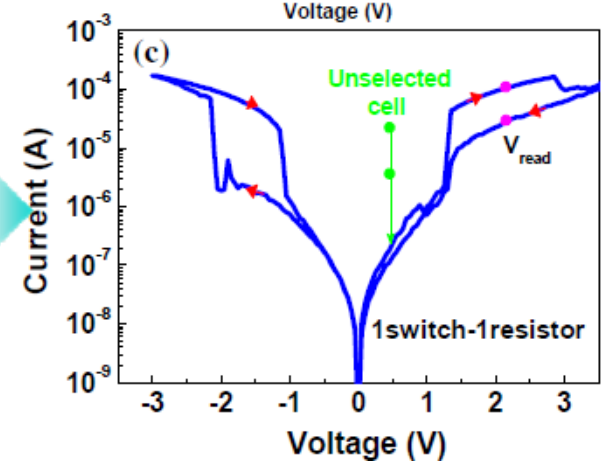


AsTeGeSi switch





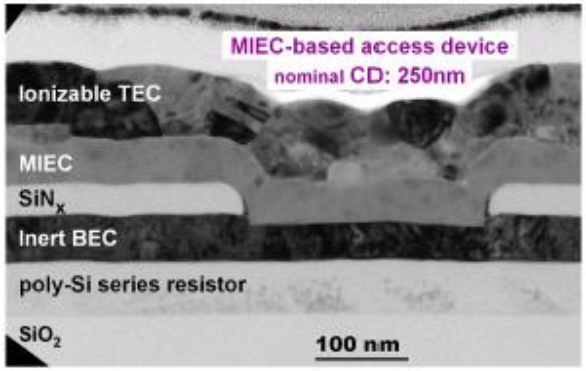




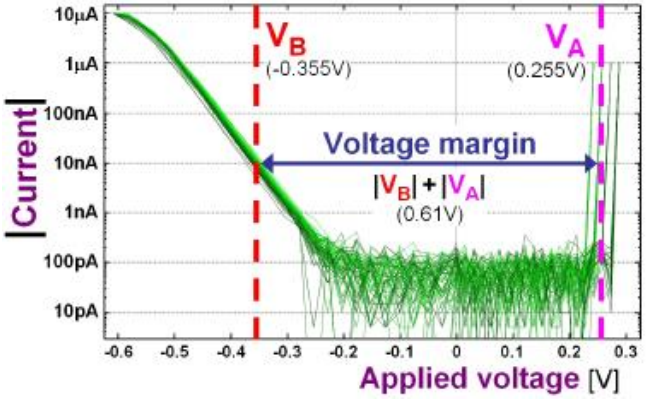
Samsung: IEDM 2.6.1 (2012)

MIEC: Mixed Ionic Electronic Conduction

Structure

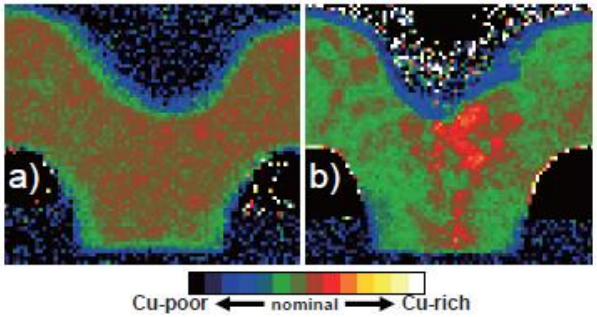


I-V characteristics

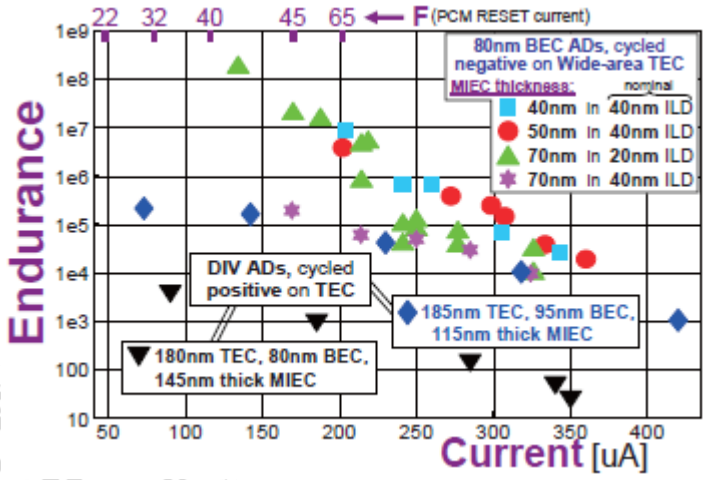


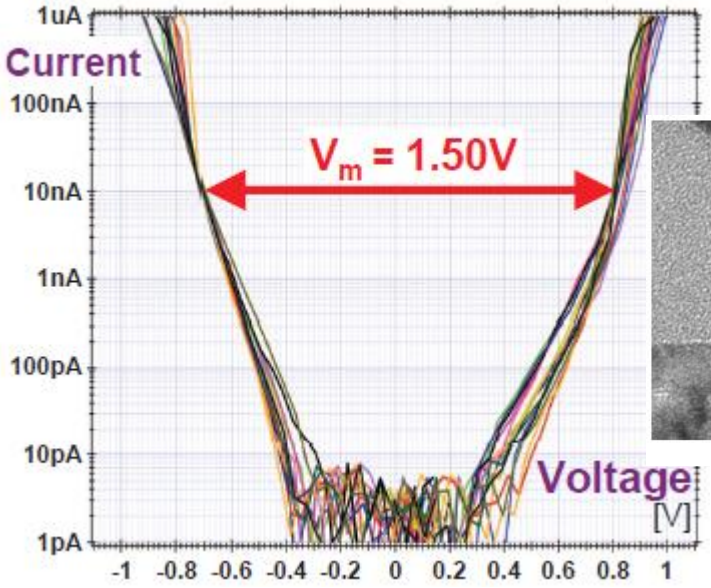
Local stoichiometry

As-fabricated After-cycling

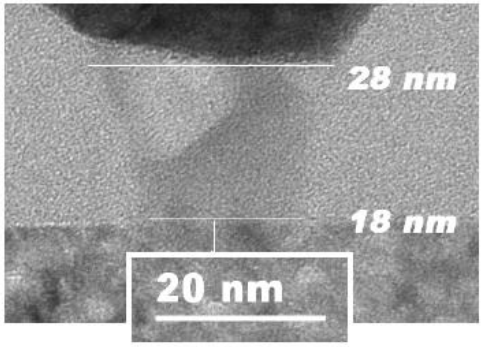


>10^8 endurance





<30nm size



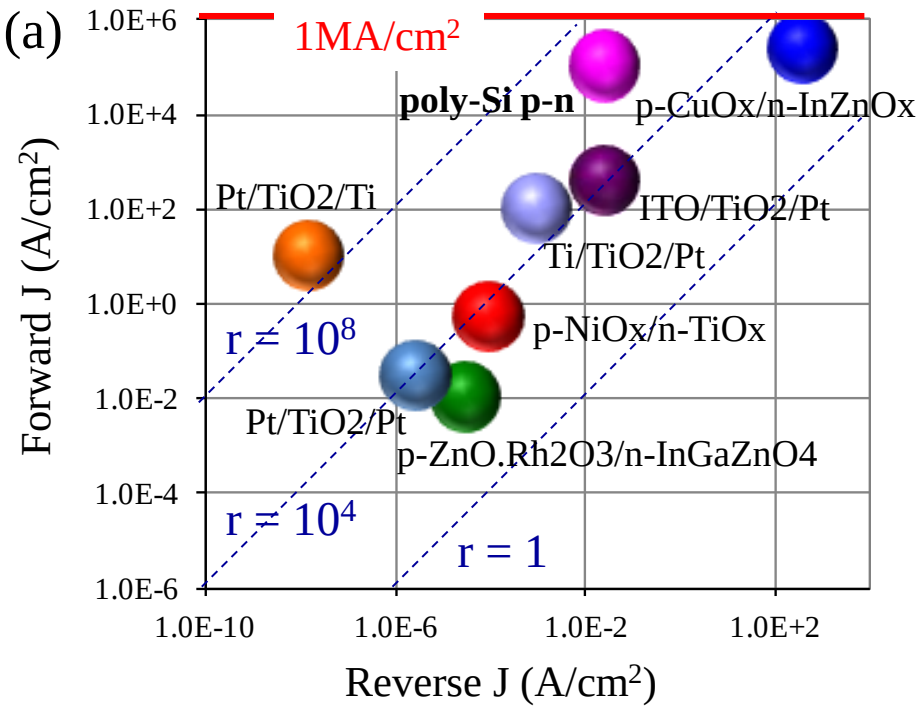
IBM: VLSIT (2010), VLSIT 94 (2011), IEDM, 36 (2012)

Selector Device Parameters and Requirements

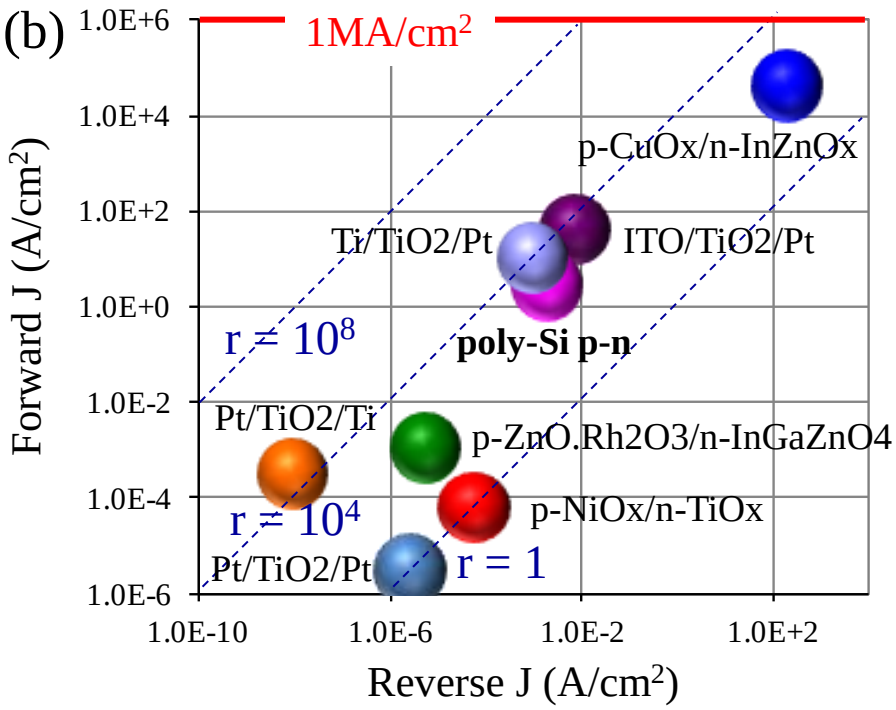
Parameters	**Requirements**
On/off ratio (or rectification ratio, nonlinearity ratio)	Sufficiently high for given memory element characteristics and array size
Maximum **on-current**	Sufficiently high for memory operation
Threshold voltage	Needs to be minimized
Scalability	Comparable with memory elements
Operation polarity	
Speed	
Endurance	
Manufacturability	Compatible with memory and CMOS processing

Examples of Reported Oxide Diodes

Current density at ± 1V

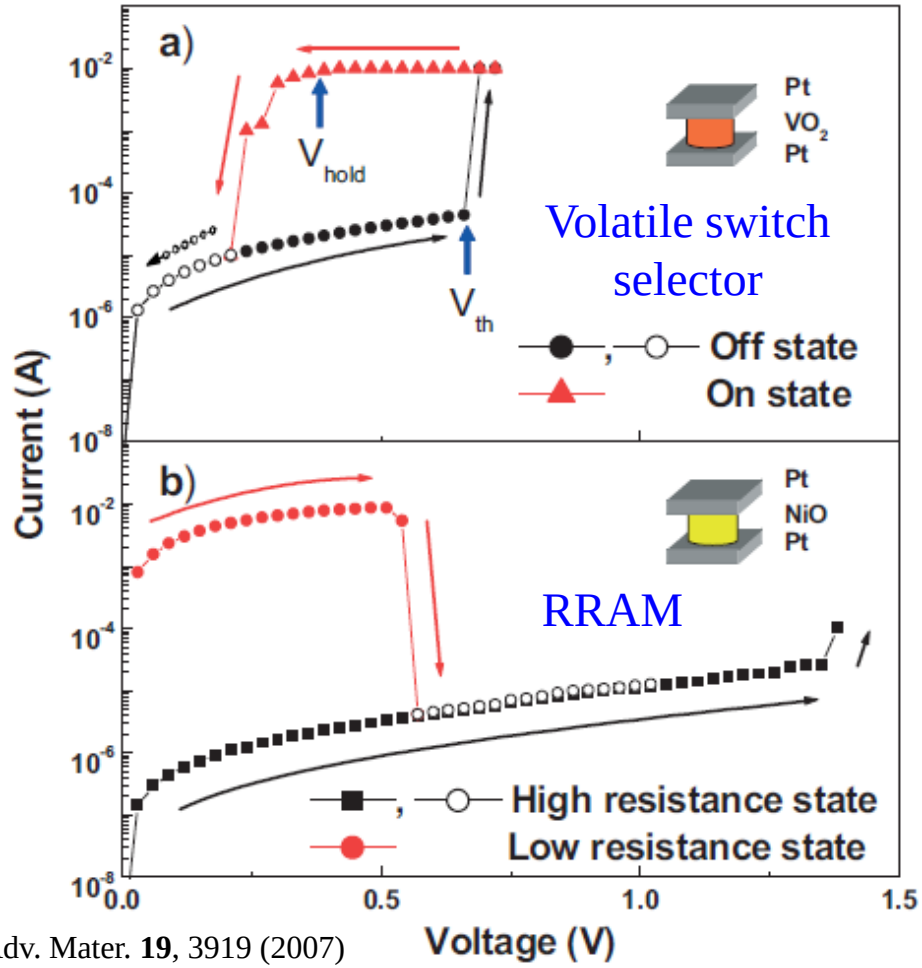


Current density at ± 0.5V

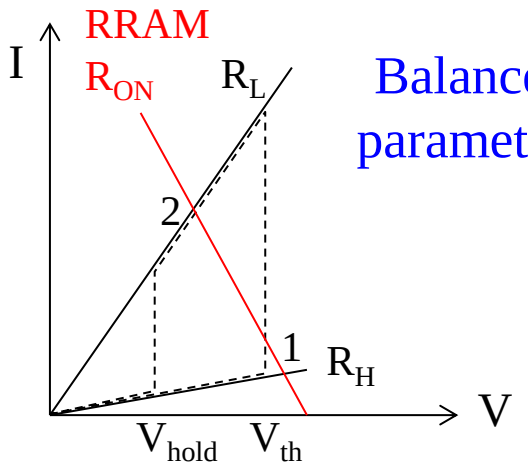


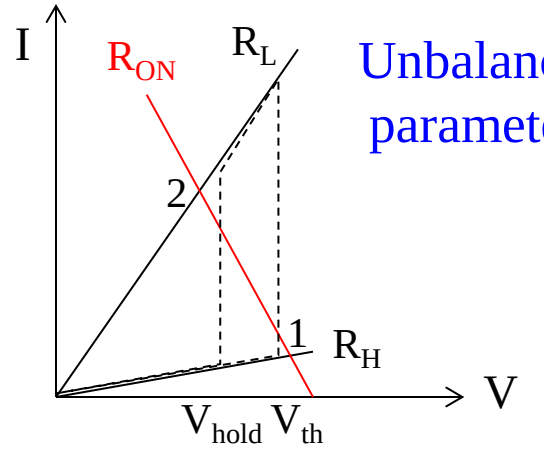
Ref: Adv. Mater. ***19****, 73 (2007); IEDM 771 (2007); Adv. Mater.* ***15****, 1409 (2003); Nanotech.* ***21****, 1 (2010); APL* ***92****, 162904 (2008); VLSI Tech. 24 (2009); APL* ***94****, 082905 (2009); APL* ***96****, 262901 (2010).*

Selector-Memory Parameter Balance



Adv. Mater. **19**, 3919 (2007)





Threshold switch parameters:
V_{hold}, V_{th}, R_L, R_H

RRAM parameters:
V_{set}, V_{reset}, R_{on}, R_{off}

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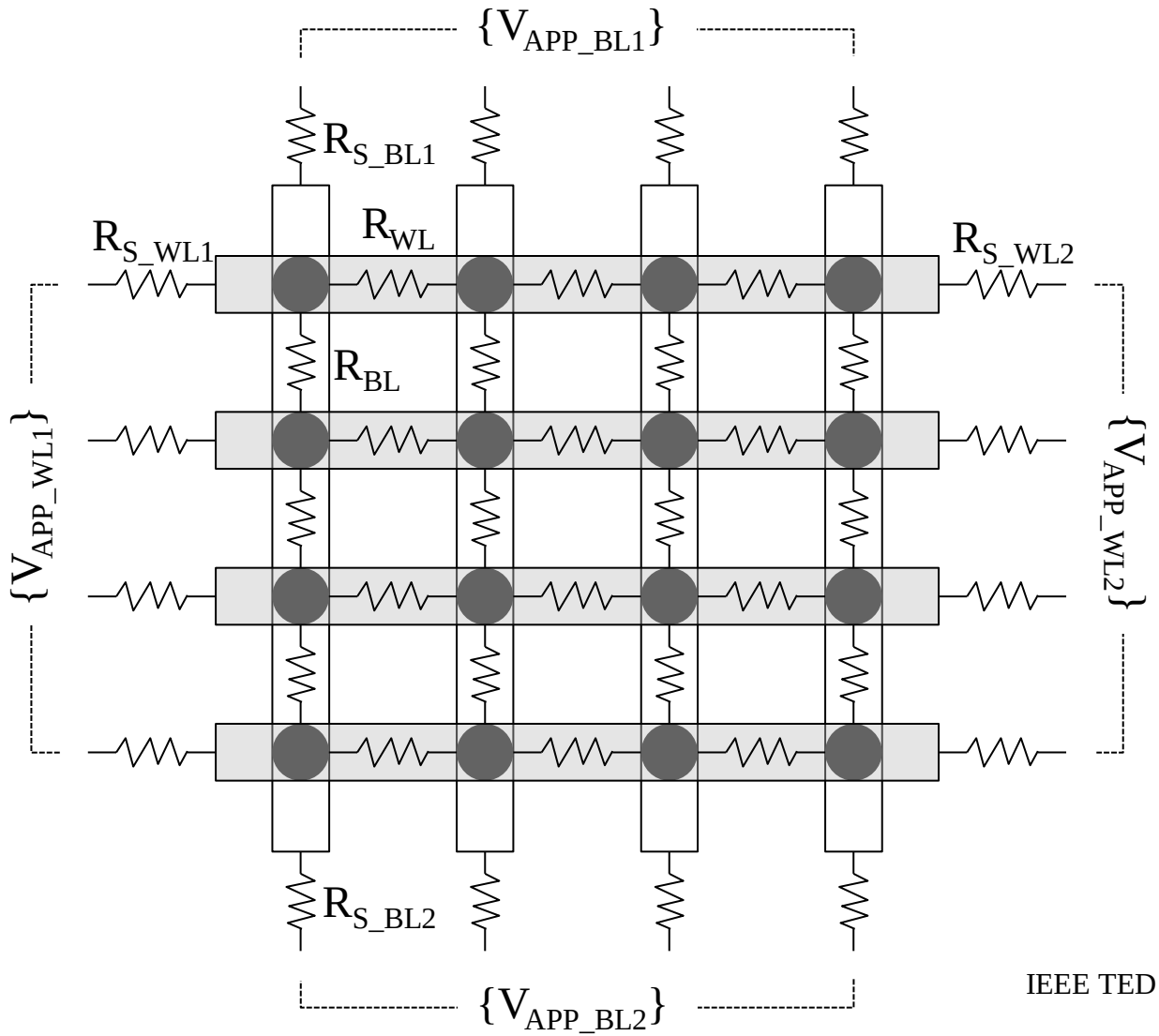
A Crossbar Array Model and Solution



IEEE TED **60**, 1318 (2013)

Crossbar Array Parameters

Technology

Memory element
- Switching I, V
- R_{LRS}, R_{HRS}, on/off ratio
- Variation

Selector devices
- Nonlinearity
- Asymmetry
- Contact resistance

Design

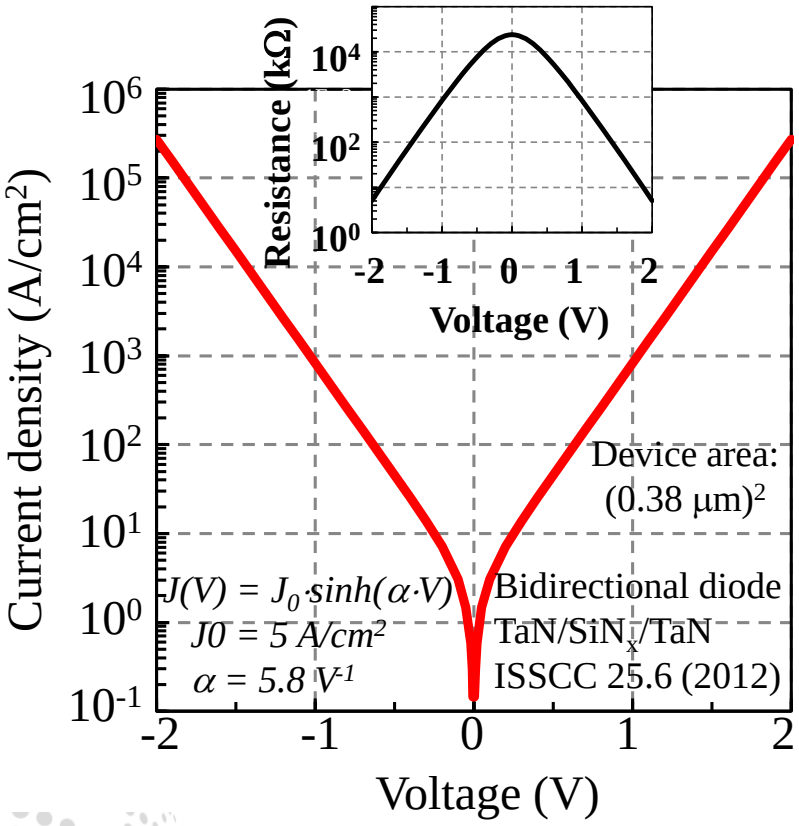
Array parameters
- Size (m×n)
- Line resistance
- Single- or dual-bias

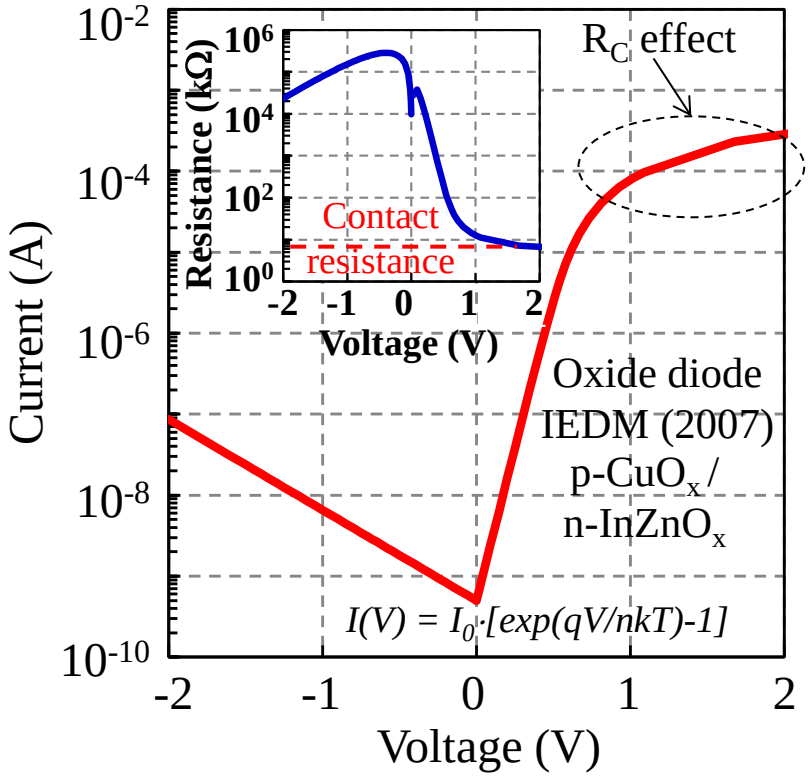
Array operation
- Supply voltage (V_{dd})
- Sensing/bias schemes
- Parallel access

- ➢ Sensing margin
- ➢ Writing voltage margin
- ➢ Power efficiency

Nonlinear and Rectifying Selectors

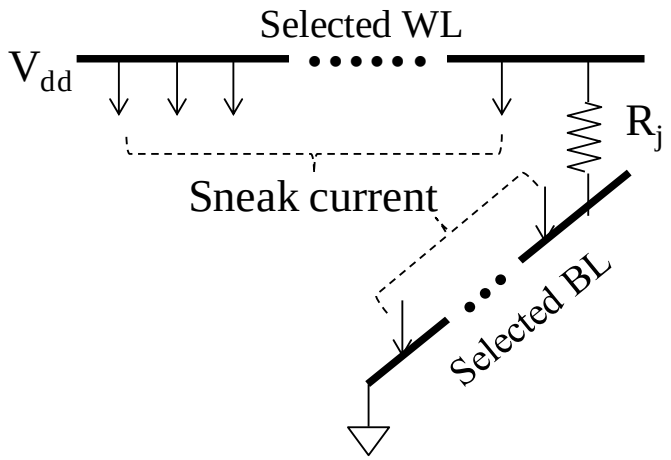
- A typical nonlinear characteristics is from tunneling transport mechanisms
- Rectifying selectors can be p-n junction, heterojunction, or Schottky diode
- I-V characteristics well described by hyperbolic or exponential functions
- Maximum current may be limited by contact resistance

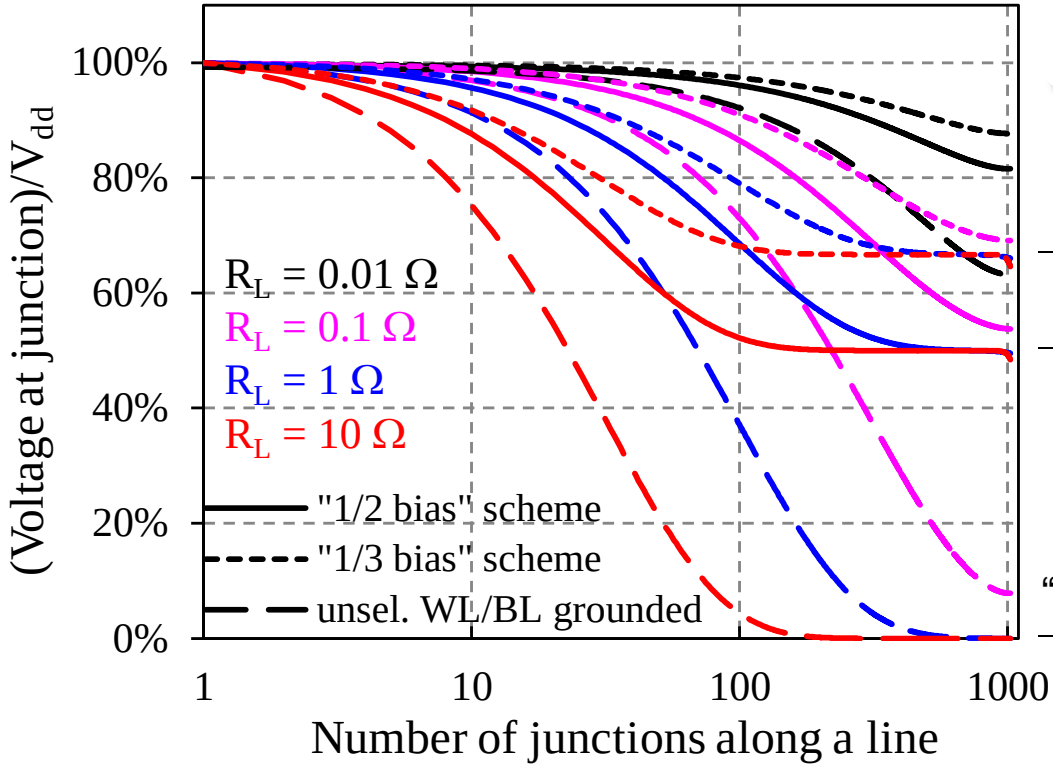




Line Resistance Induced Voltage Decay

$$V_{Rj} = V_{dd} - \sum I_{WL} \cdot R_{WL} - \sum I_{BL} \cdot R_{BL}$$





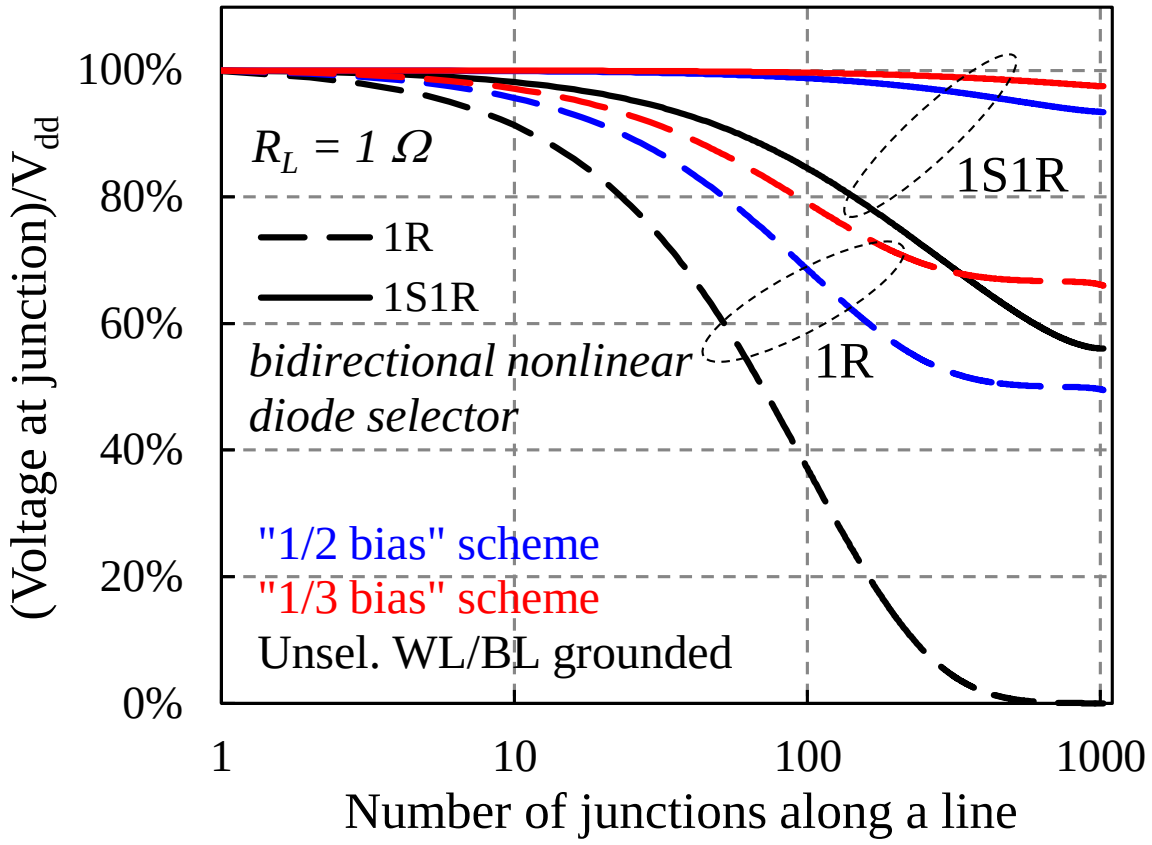
"1/3 bias": V drops to $2V_{dd}/3$

"1/2 bias": V drops to $V_{dd}/2$

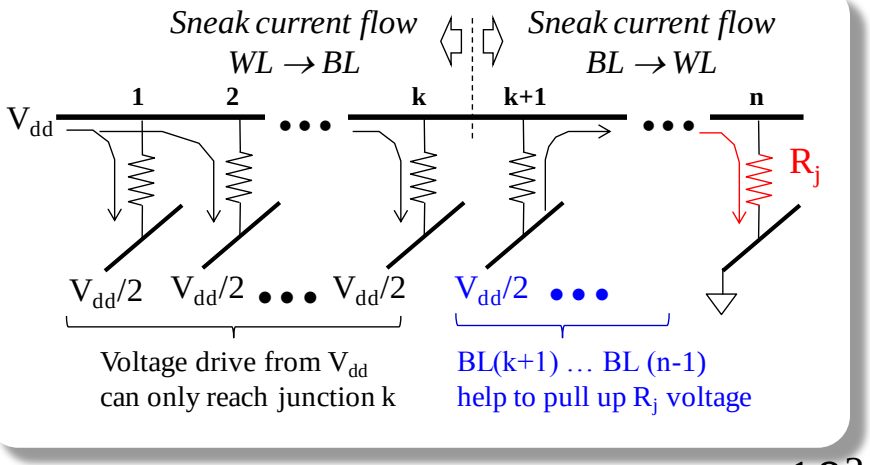
"ground": V drops to 0

Selector Reduces Voltage Degradation

- Integrating nonlinear selector devices significantly reduces line resistance induced voltage decay

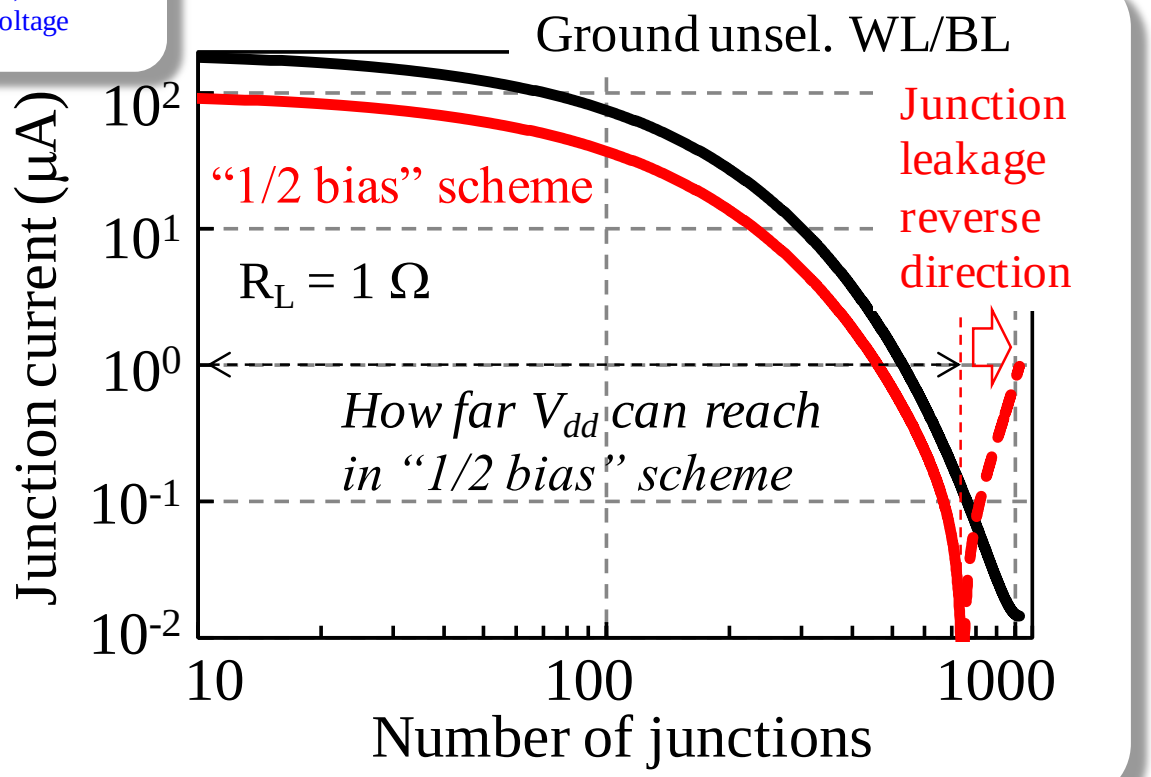


Sneak Leakage Reversal with Partial Bias



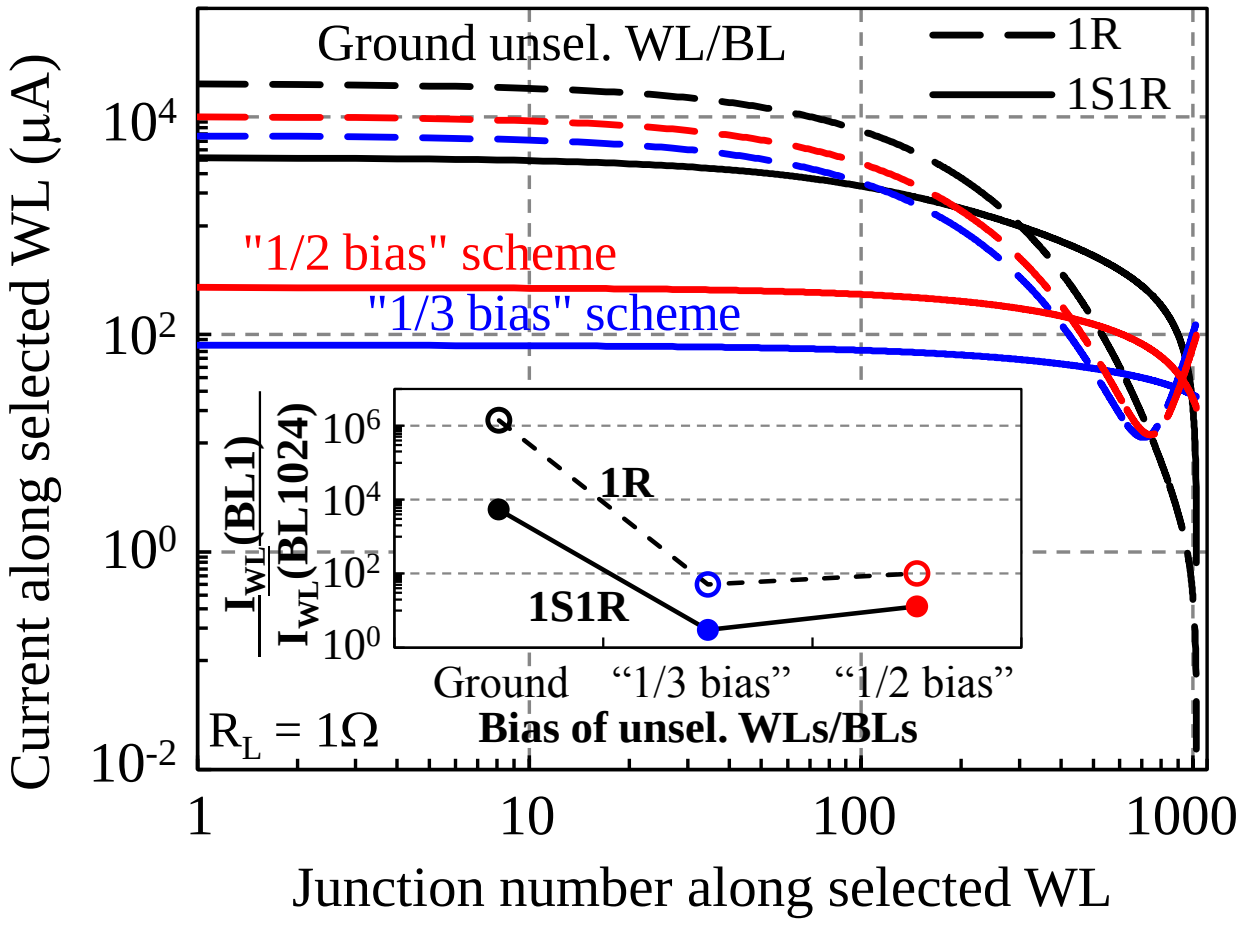
- With selected $V_{WL} = V_{dd}$ and selected $V_{BL} = 0$, sneak path leakage is usually WL → BL

- Reverse leakage occurs in partial bias schemes
- After reversal, the device at the end of WL is driven by partial biased BLs instead of V_{WL}



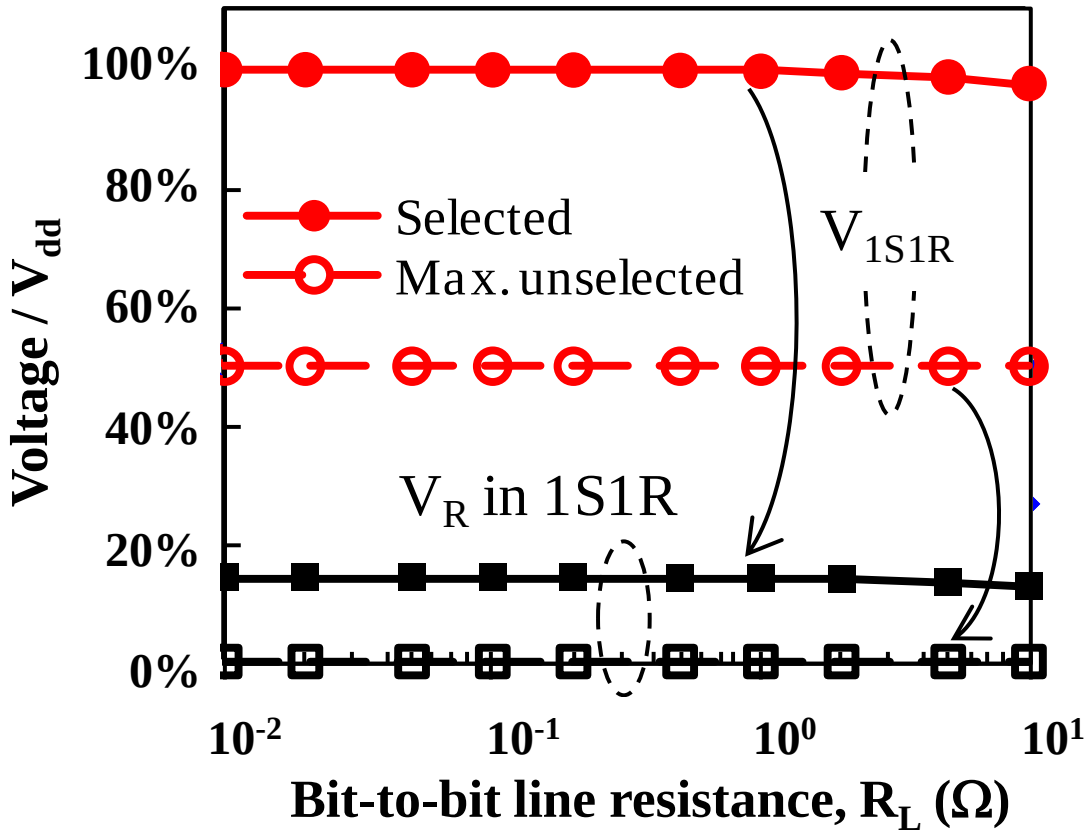
Selector Reduces Leakage and Line Current

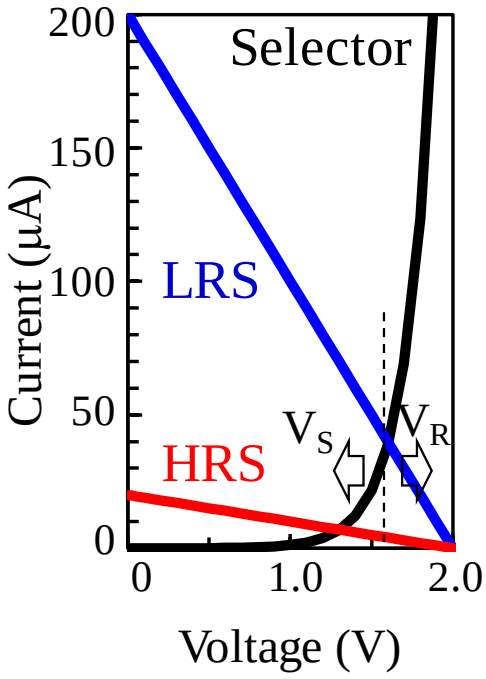
- Selector devices reduce both the sneak leakage through unselected junctions and the access line current



Writing Voltage Margin of a 4kb Array

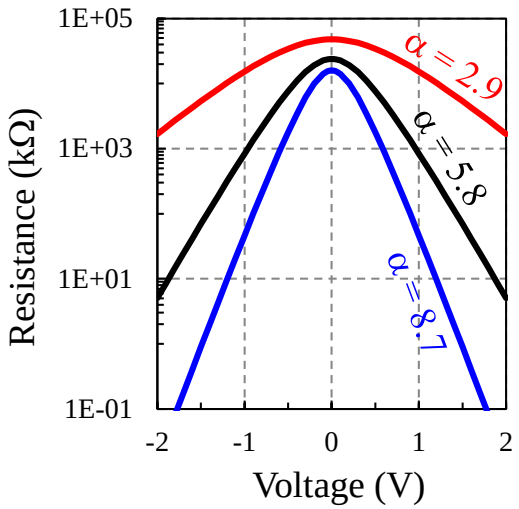
- Selectors helps to maintain nearly constant junction voltage margin
- However, only a portion of junction voltage drops on the memory element

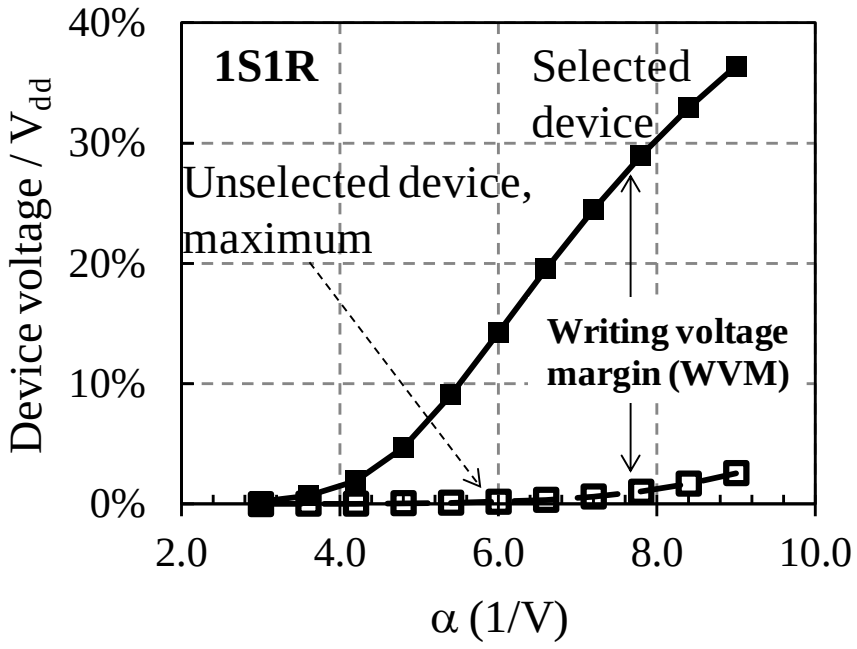


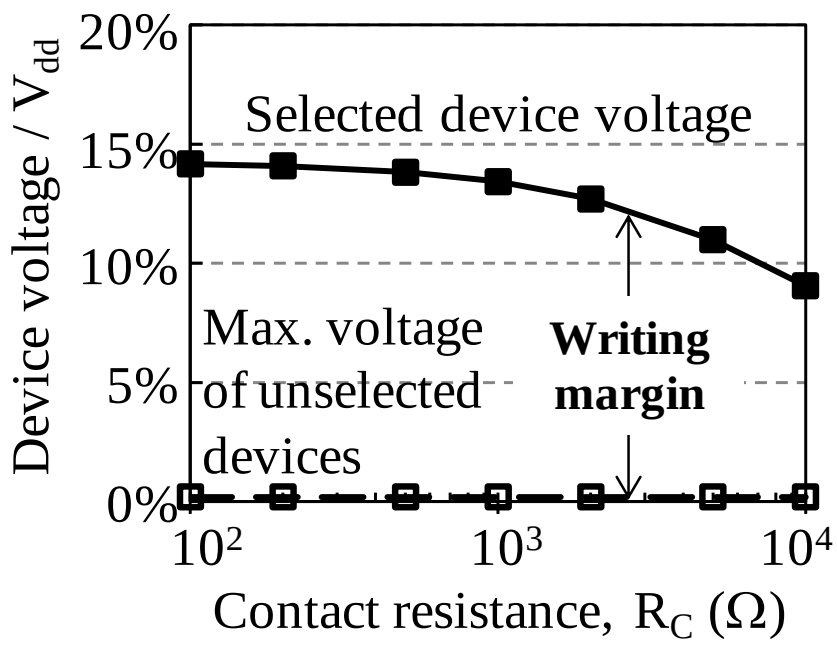


Effect of Selector Properties

- Higher exponential factor α of selectors (stronger nonlinearity) improves writing voltages and margin
- Contact resistance reduce writing voltages and margin

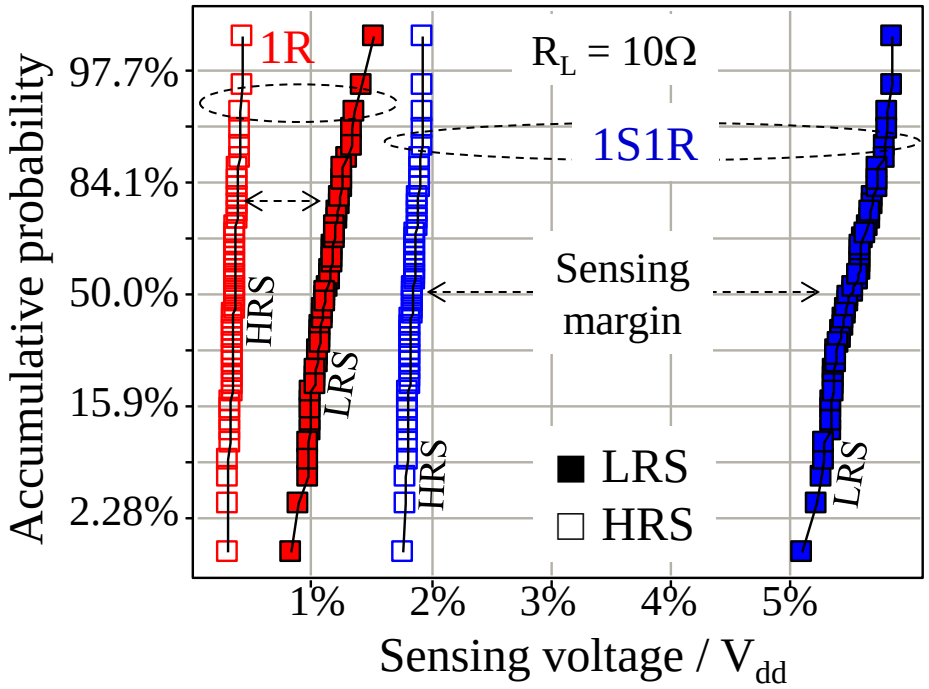


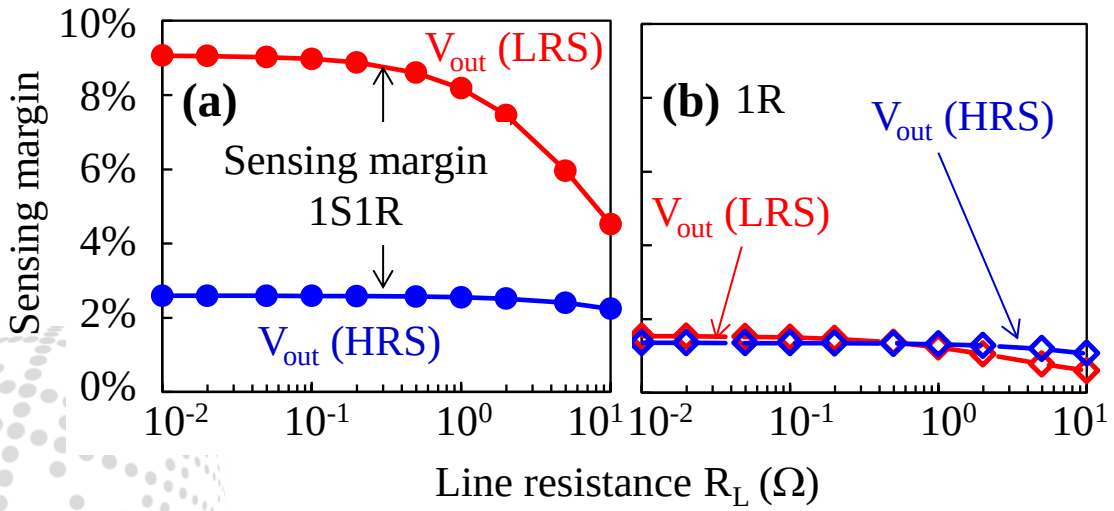


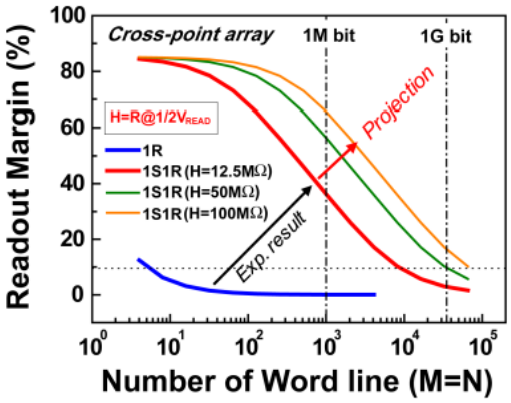


Sensing Margin of a 4kb Array

- Worst-scenario sensing margin is nearly zero without selector
- Selector greatly improves the sensing margin
- Analytical solutions ignoring line resistance and selector I-V may over-estimate sensing margin







Symp. VLSI Tech. 37 (2012)

Summary

- Two terminal selector with good scalability is essential for high-density crossbar memory arrays.
- Nonlinearity and asymmetry in device characteristics can enable device selection functions. Rectifying diodes, volatile switches, and nonlinear devices can be used as selectors.
- Selectors reduce sneak leakage and voltage/current decay, which helps to ensure sufficient operating voltage/current.
- Voltage dividing effect of selectors reduce disturbance but also requires higher array V_{dd} for CBA operation.
- Selectors with stronger exponential dependence are more effective in improving operation margins.
- CBA design and optimization have to consider the balance between memory elements and selector devices.