Non-Volatile Memory Technology: Directions Beyond Floating Gate Devices

Bob Gleixner and Chandra Mouli

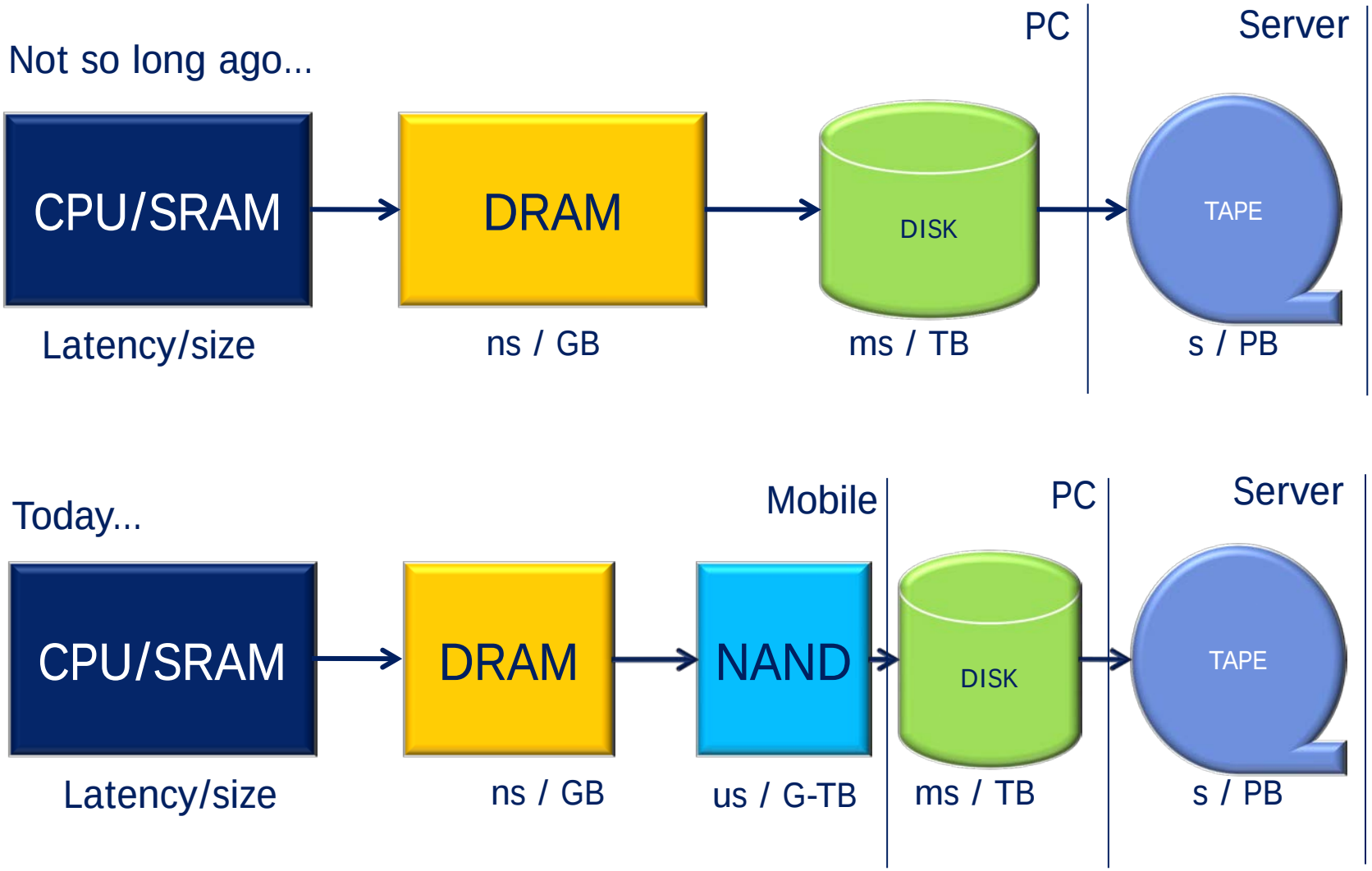
Micron Technology

Two question to ask (for a new NVM)…

- What are the cost/performance characteristics required to add *significant* value in computing devices?

- For the leading emerging NVM's, what materials improvements are needed to realize this value?

Computing memory hierarchy



Where could a new memory add value?

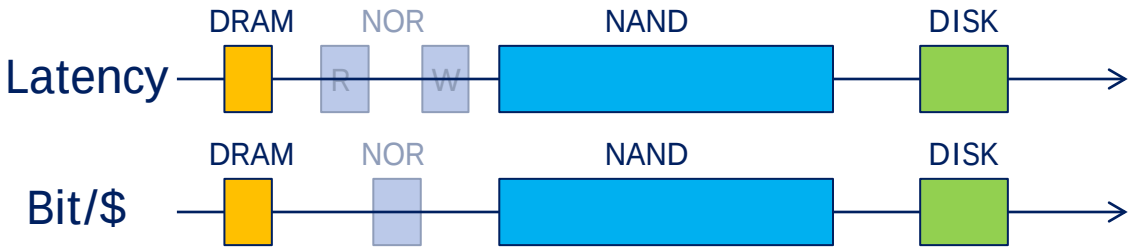
(Assumption – you find a niche to grow)

NAND had a big “hole to fill” in 2009

Normalized Parameters	DRAM	NAND	HDD
Latency	1x	~500x	~100,000x
$/Bit	1x	~0.1x	~0.01x

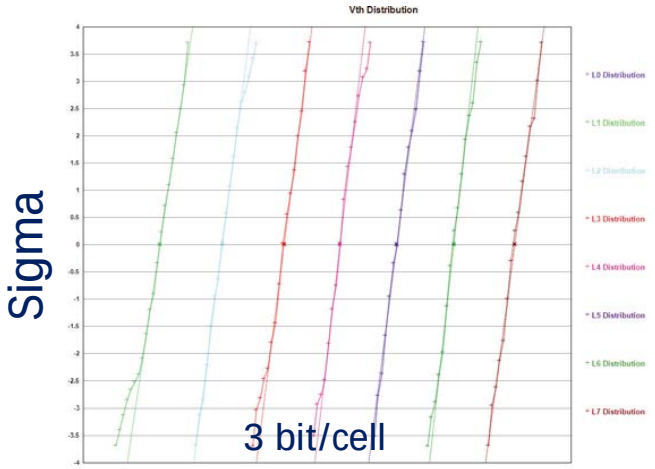
A. Fazio, IEDM 2009

What do the holes look like today?



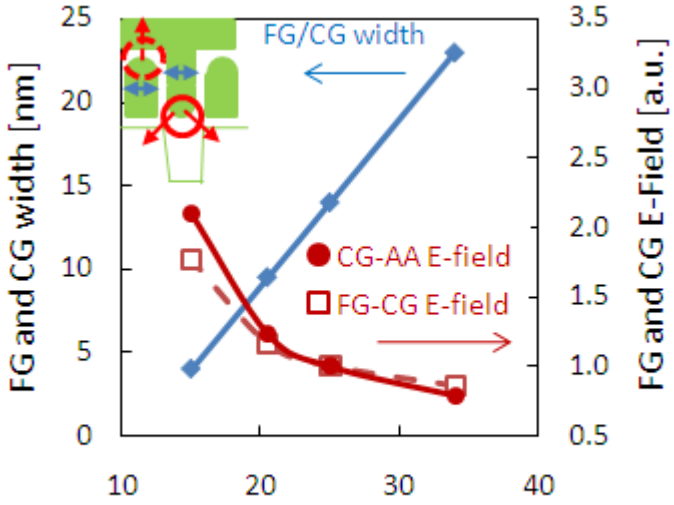
More importantly, what does this look like in 3-5 years?

Planar NAND is getting tough to scale...

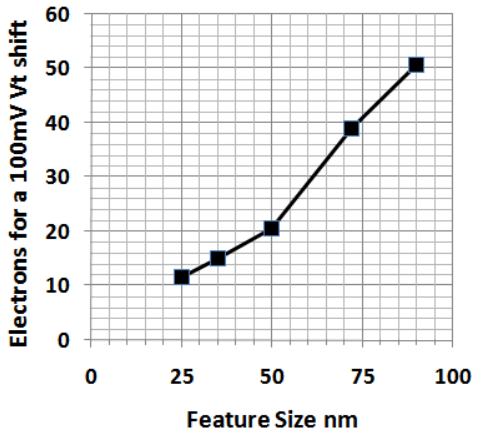


Threshold Voltage

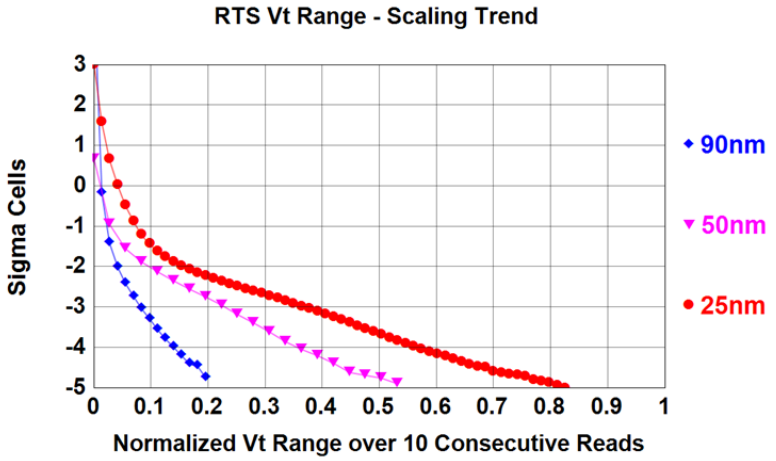
G. Naso, ISSCC 2013 – 128Gb 20nm NAND



Goda and Parat, IEDM 2012



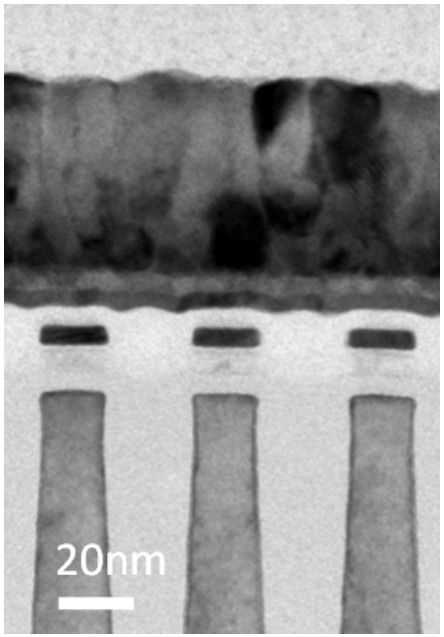
Prall and Parat, IEDM 2010



Prall and Parat, IEDM 2010

...but continues to find solutions

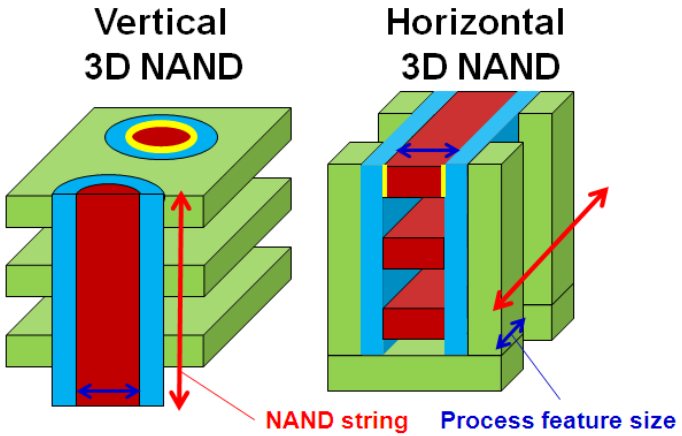
Planar floating gate cell



Goda and Parat, IEDM 2012

16nm NAND announced

3D NAND



Goda, VLSI-TSA 2013

Samsung Starts Mass Producing Industry's First 3D Vertical NAND Flash

Seoul, Korea on Aug. 6. 2013

www.samsung.com

CNET › News › Business Tech › Micron customers won't have to wait long ...

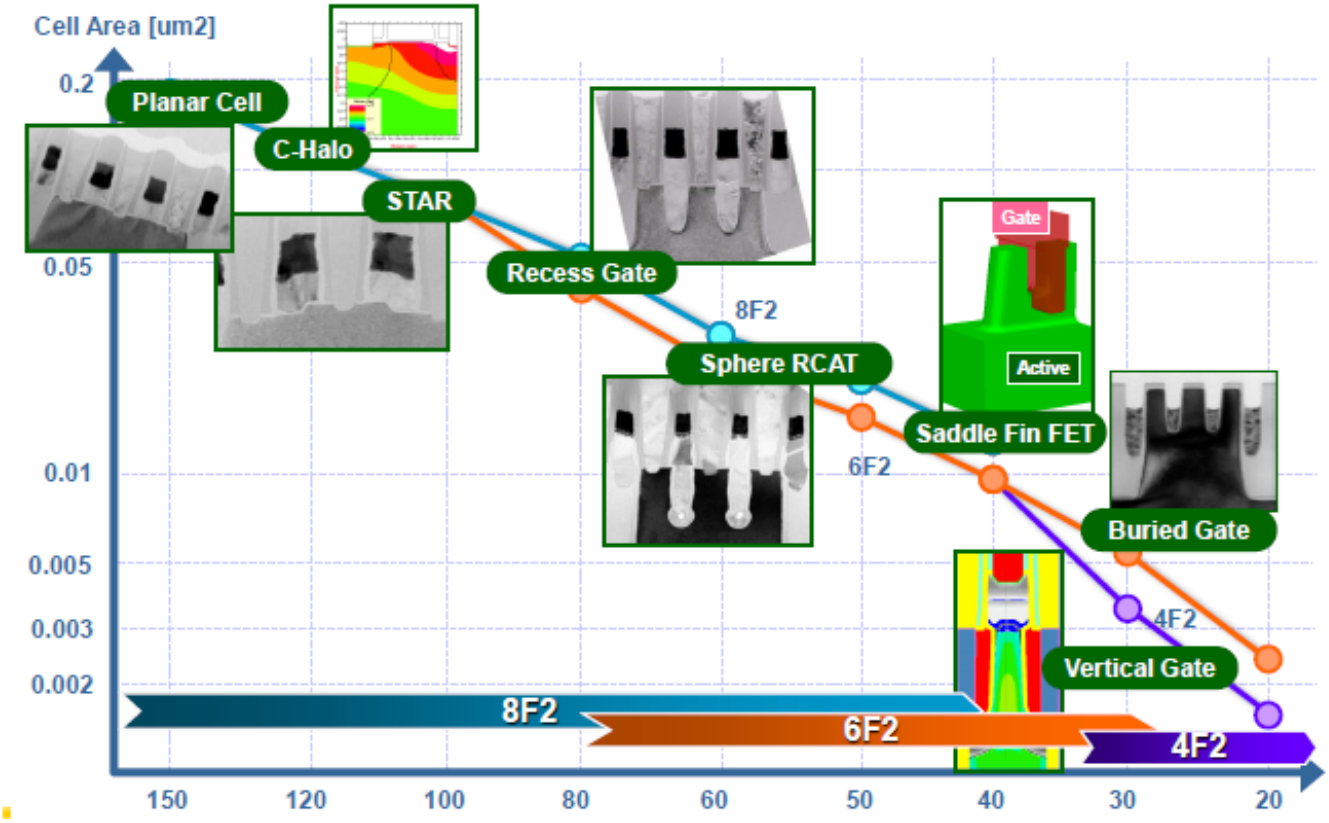
Micron customers won't have to wait long for 3D flash memory

CEO Mark Durcan tells CNET that the company will start providing samples of the advanced memory technology to customers in the first quarter of 2014.

www.cnet.com

Represents a breakthrough in overcoming NAND scaling limit; ushers in new 3D memory era

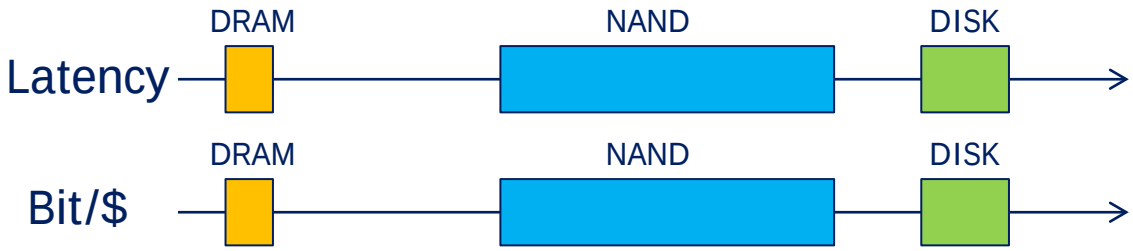
While DRAM continues to scale



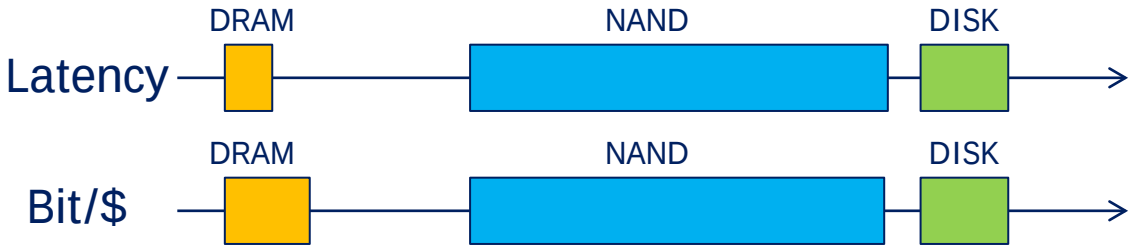
Seon Yong Cha, IEDM short course, 2011

Main vector in DRAM/NAND: Cost reduction

Today:



3 Years? :

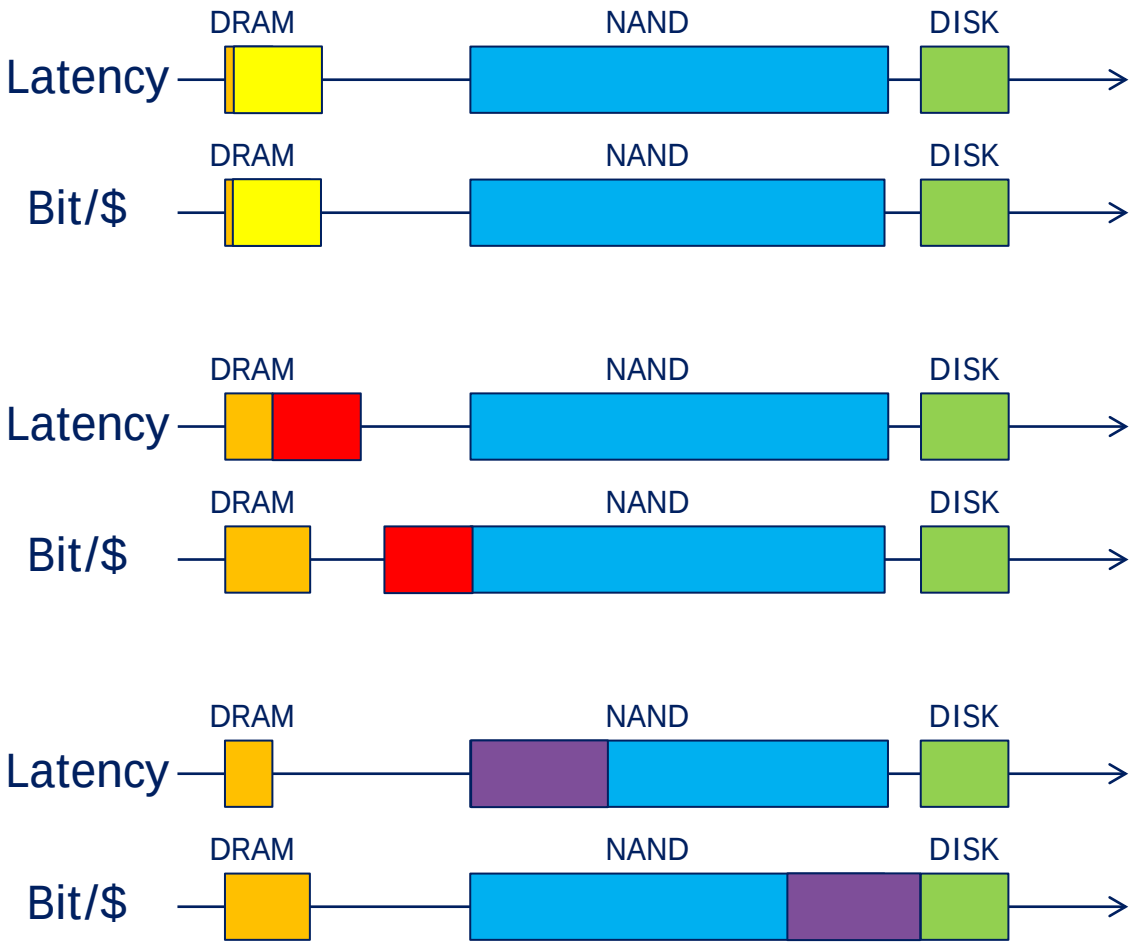


Where can an emerging memory fit in?

NVDRAM
(Non-Volatile DRAM)

SCM
(Storage class memory)

NAND
REPLACEMENT
(STORAGE)



Consider the “top 4” emerging memories

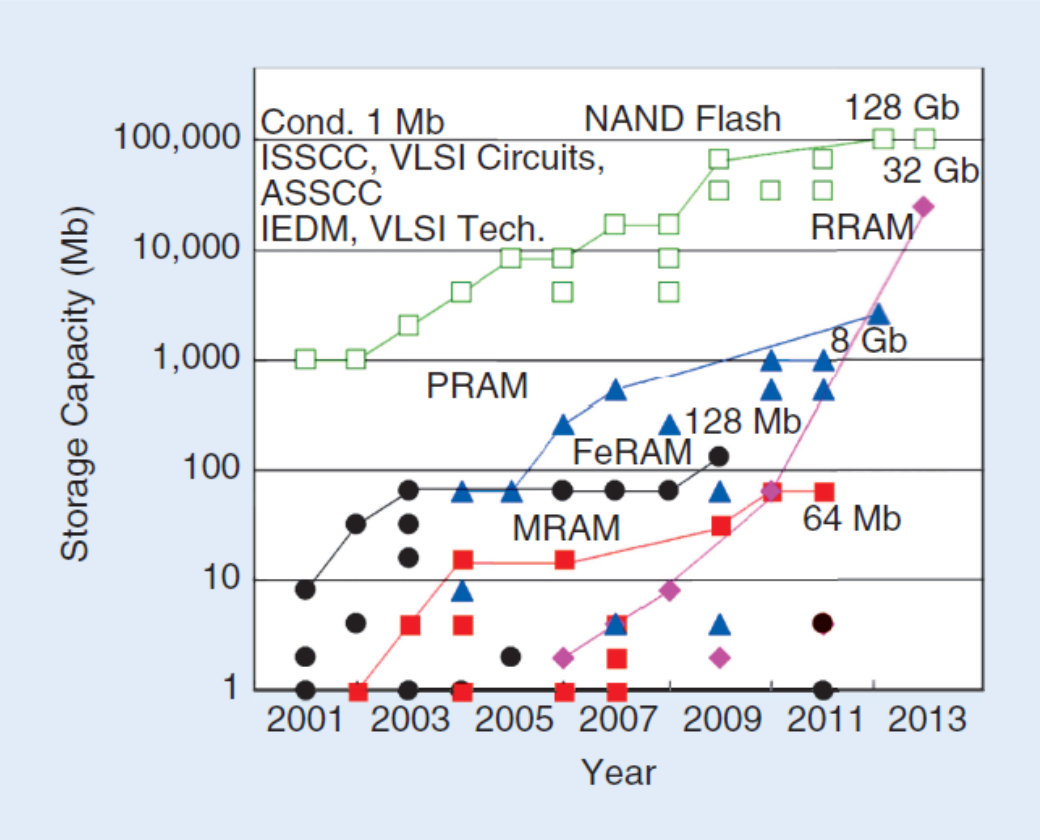


FIGURE 15: Memory capacity of emerging nonvolatile memories.

IEEE Solid-State Circuits Mag. Spring 2013

Technology	Company	Niche
RRAM	Adesto	EEPROM Replacement
MRAM	Everspin	Ultra high Reliability BBSRAM replacement
STRAM	Crocus	Embedded Security
FERAM	TI	Embedded
FERAM	Ramtron	Low Density – Power Meters
PCM	Samsung Micron	NOR replacement- Wireless applications

Prall, IMW 2012

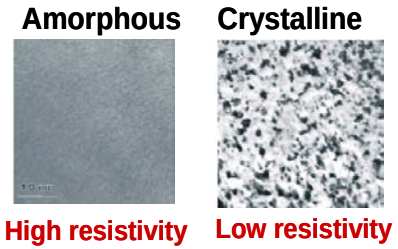
Memory “scorecard”

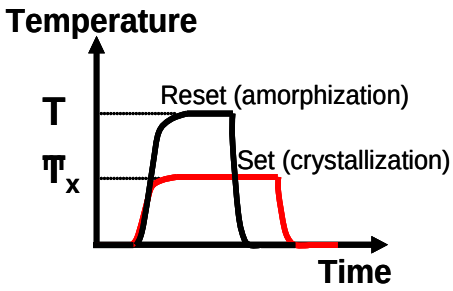
- Cost / bit
  - Small bit cell
  - Low programming energy
  - Multi-level or multi-layer
- Latency
  - Fast read (large signal + memory window)
  - Fast / deterministic writes
  - Write endurance

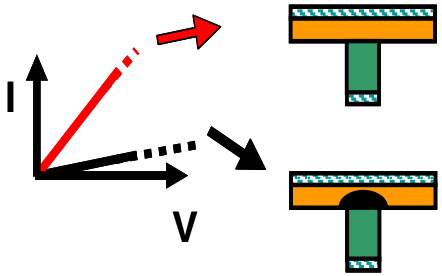
	Planar NAND	DRAM
Cost		
Cell size	$4F^2$ 16nm	$6F^2$ 2x nm
Programming energy	Low	(Refresh)
Multi-level / layer	1-3 BPC	None
Latency		
Fast read	10uS (page)	~10ns
Fast write	1mS (page)	~10ns
Endurance	1-100k	>1e15

Phase Change Memory (PCM)

- Storage mechanism
  - Amorphous/poly-crystal phase of chalcogenide alloy ($Ge_2Sb_2Te_5$ – GST)
- Writing mechanism
  - Current-induced Joule heating
- Sensing signal
  - Resistance change of the GST
- Cell structure
  - 1 transistor, 1 resistor (1T/1R)



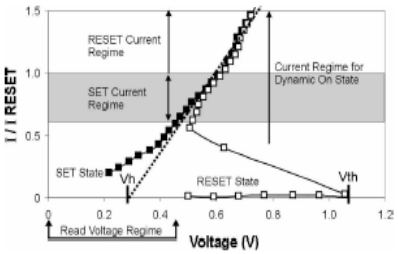




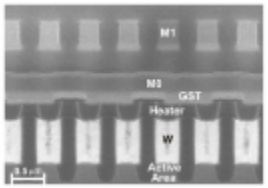
History of PCM Silicon Development

PCM cell

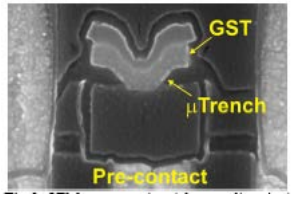
S. Lai and T. Lowrey,
IEDM 2001
180nm



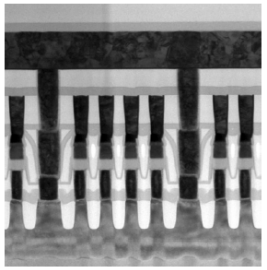
F. Pellizzer et al.,
VLSI 2004
180nm



F. Pellizzer et al.,
VLSI 2006
90nm

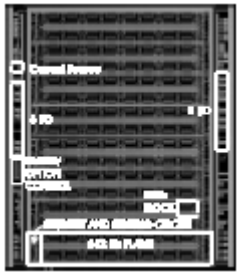


G. Servalli,
IEDM 2009
45nm

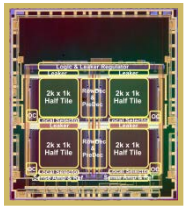


PCM array & chip

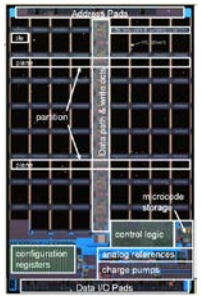
M. Gill et al.,
ISSCC 2002
180nm



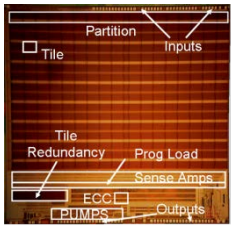
G. Casagrande et al.,
VLSI 2004
180nm



Bedeschi et al.,
ISSCC 2008
90nm 128Mb (256Mb MLC)



C. Villa et al.,
ISSCC 2010
45nm 1Gb



2001 2003 2005 2007 2009 2011

Concept Demonstration

Technology Validation

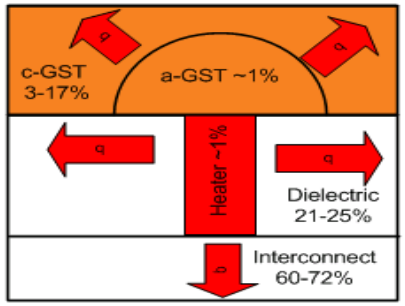
Product Manufacturing

PCM Scorecard

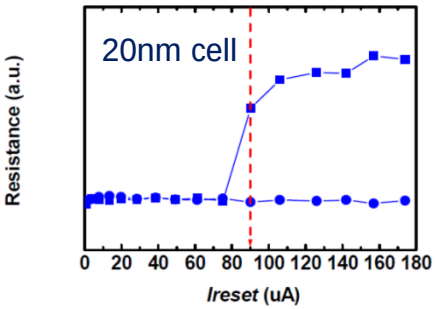
	Planar NAND	DRAM	PCM
Cost Overall			
Cell size	$4F^2$ 16nm	$6F^2$ 2x nm	$4F^2$ 20nm
Programming energy	Low	(Refresh)	~High I
Multi-level / layer	1-3 BPC	None	Level/Layer
Latency Overall			
Fast read	10uS (page)	~10ns	<100ns
Fast write	1mS (page)	~10ns	>100ns
Endurance	1-100k	>1e15	1e8

PCM Cell Challenges

- High programming current

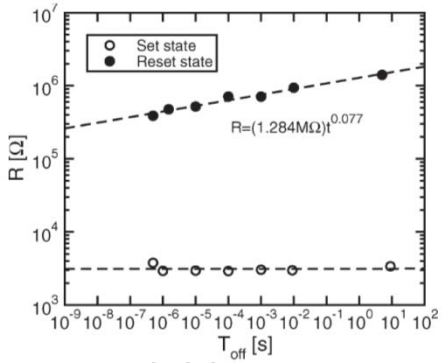


Sadeghipour, ITHERM 2006



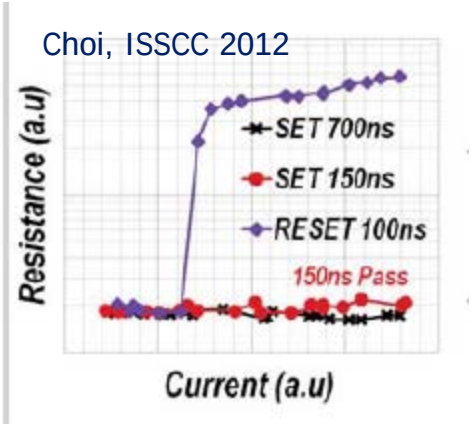
Kang, IEDD 2011

- Resistance drift (MLC)

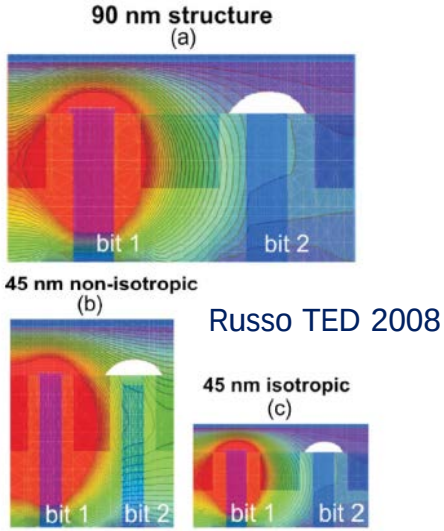


Ielmini TED 2007

- Programming speed to SET/crystallized state

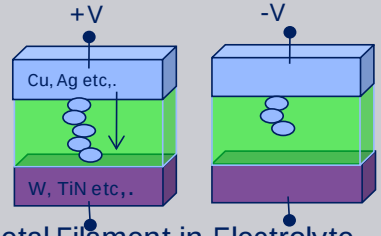
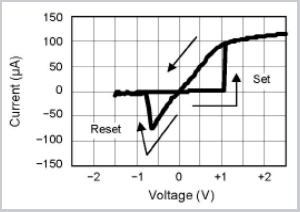
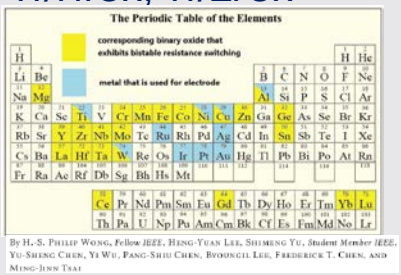
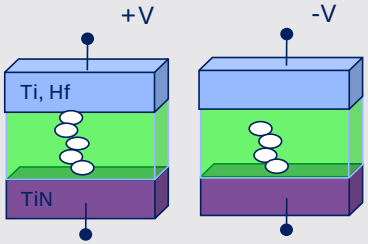
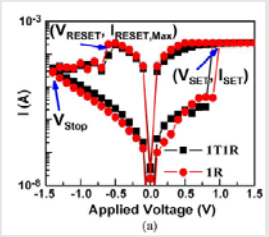
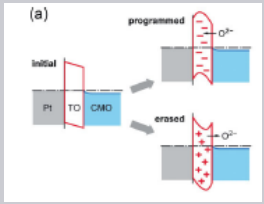
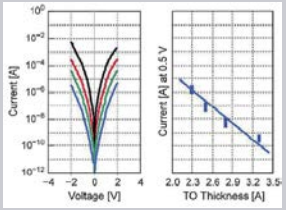


- Thermal disturb



Russo TED 2008

RRAM

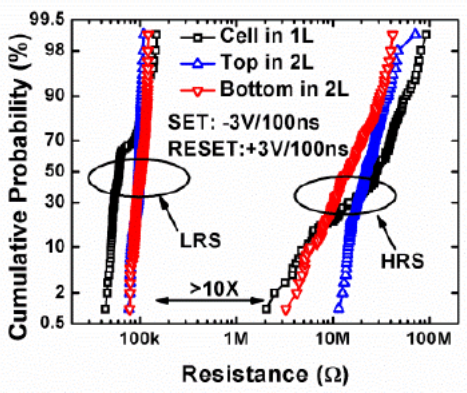
RRAM	Material Systems	Switching mechanism	Comments
RRAM-M (CBRAM)	Cu/GdO_x Ag/SiO_2 Ag/GeS	 Metal Filament in Electrolyte	K.Aratani etal, IEDM 2008  Ion/Ioff ~ 1000
Bipolar RRAM-Ox	Ti/HfOx, Ti/ZrOx 	 Oxygen vacancy filament in dielectric TiOx, ZrOx, TaOx etc,.	H.Y.Lee etal, IEDM 2008  Ion/Ioff ~ 10
RRAM-MVO	Mixed Valence Oxides SrTiOx, PCMO etc,.	 Uniform oxygen movement	Meyer etal, NVMTS 2008  Ion/ Ioff ~10

RRAM Scorecard

	Planar NAND	DRAM	RRAM
Cost Overall			
Cell size	$4F^2$ 16nm	$6F^2$ 2x nm	$4F^2$ 20nm
Programming energy	Low	(Refresh)	Low - Med
Multi-level / layer	1-3 BPC	None	Level/Layer
Latency Overall			
Fast read	10uS (page)	~10ns	<100ns
Fast write	1mS (page)	~10ns	~10nS
Endurance	1-100k	>1e15	1e8 ??

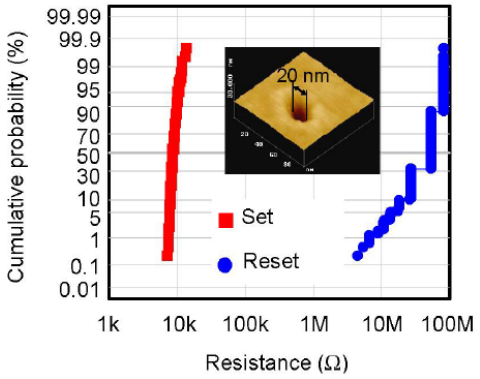
RRAM Cell Challenges

- Window for MLC



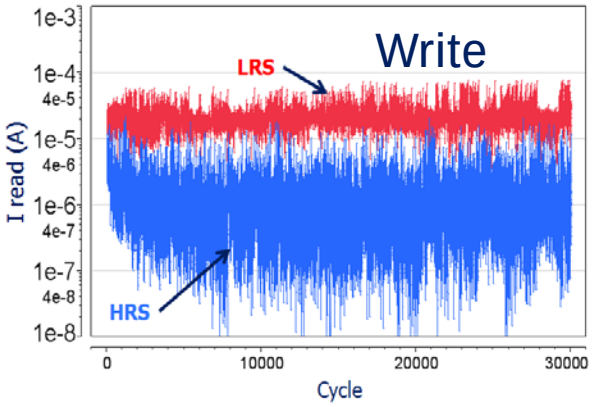
Chen IEDM 2012 – HfOx

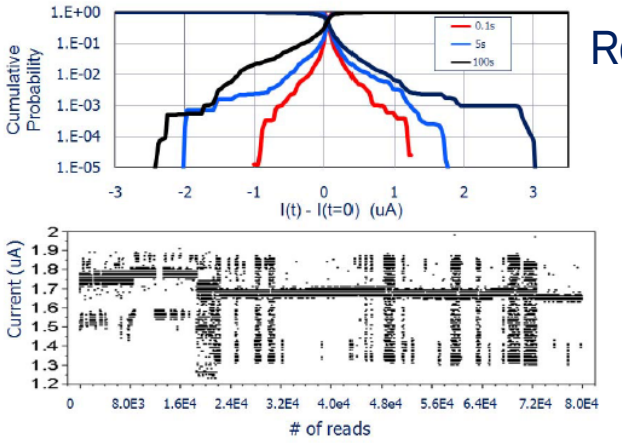
- Write current scalability?



Aratani IEDM 2007 -- CBRAM

- Noise





Read

Prall IMW 2012 – HfOx

MRAM

- Fast switching could enable DRAM replacement

EVERSPIN TECHNOLOGIES
The MRAM Company™

MR4A16B

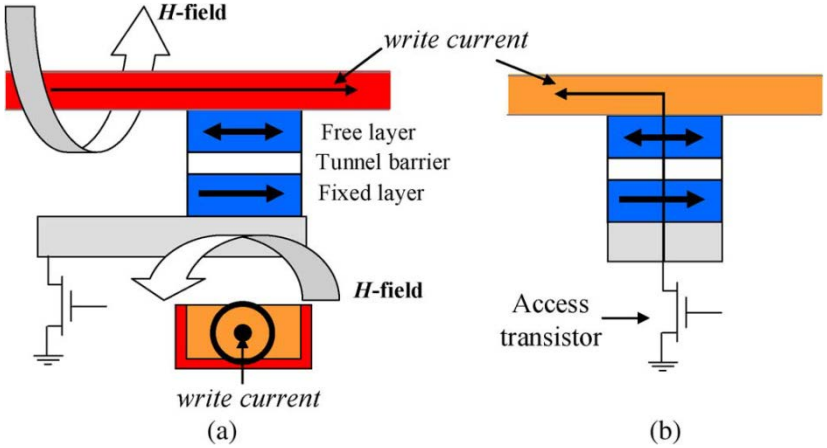
1M x 16 MRAM

FEATURES

- +3.3 Volt power supply
- Fast 35 ns read/write cycle
- SRAM compatible timing
- Unlimited read & write endurance
- Data always non-volatile for >20 years at temperature
- RoHS-compliant small footprint BGA and TSOP2 package
- AEC-Q100 Grade 1 option in TSOP2 package.

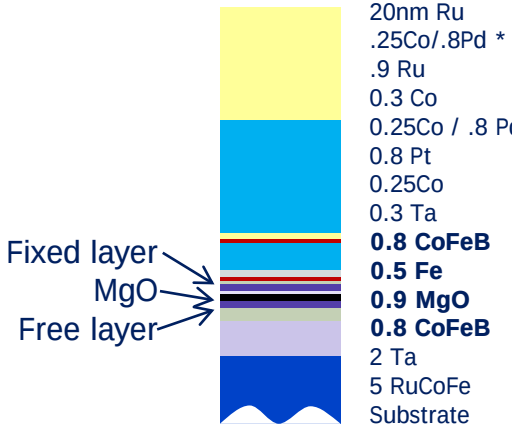
MR4A16B Datasheet, www.everspin.com

- But field / toggle MRAM cell too large → STT-MRAM

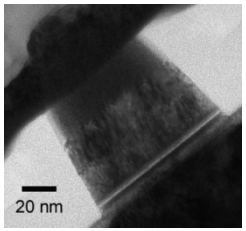


Rizzo, IEEE Trans Mag 2013

PMA Stack



20nm Ru
.25Co/.8Pd * 14
.9 Ru
0.3 Co
0.25Co / .8 Pd * 4
0.8 Pt
0.25Co
0.3 Ta
0.8 CoFeB
0.5 Fe
0.9 MgO
0.8 CoFeB
2 Ta
5 RuCoFe
Substrate



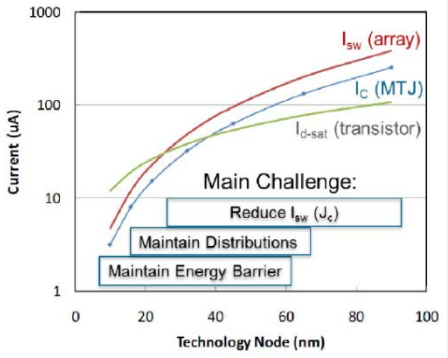
Sun, IEEE DRC 2011

STT-MRAM Scorecard

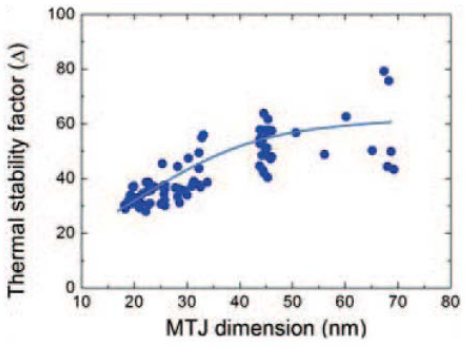
	Planar NAND	DRAM	STT-MRAM
Cost Overall			
Cell size	$4F^2$ 16nm	$6F^2$ 2x nm	$6F^2$ 20nm
Programming energy	Low	(Refresh)	Med I
Multi-level / layer	1-3 BPC	None	Layer
Latency Overall			
Fast read	10uS (page)	~10ns	<30ns
Fast write	1mS (page)	~10ns	~10ns
Endurance	1-100k	>1e15	>1e15

STT-MRAM Cell Challenges

- Writing current vs. stability

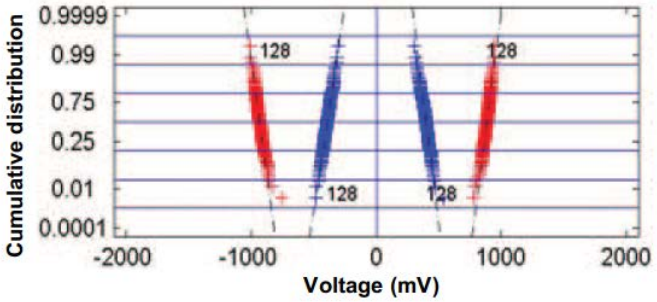


Slaughter, IEDM 2012



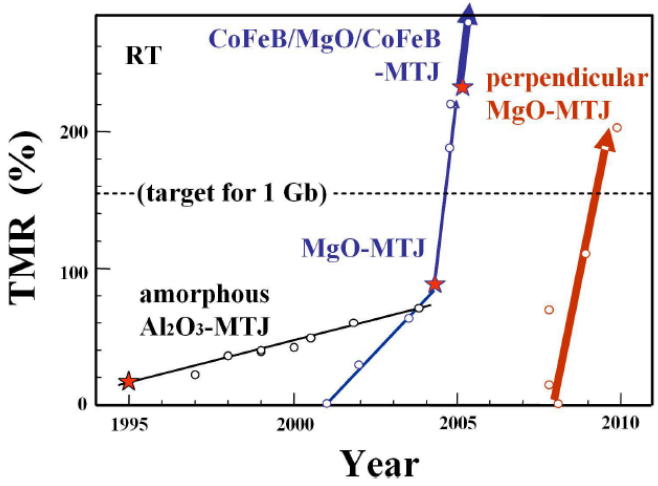
Park, VLSI 2012

- Tunnel junction reliability

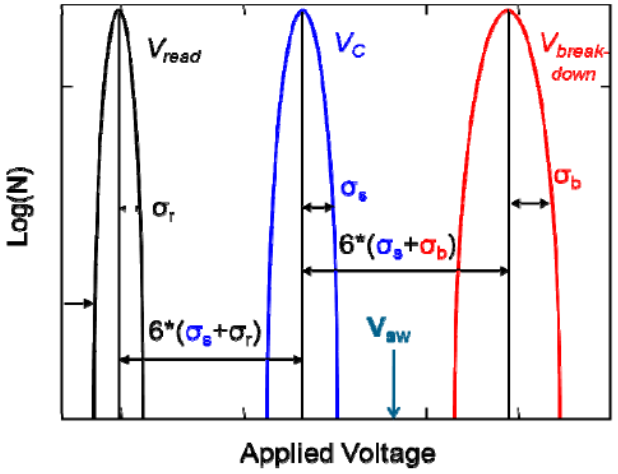


Gallagher, ICSICT 2012

- Operating window



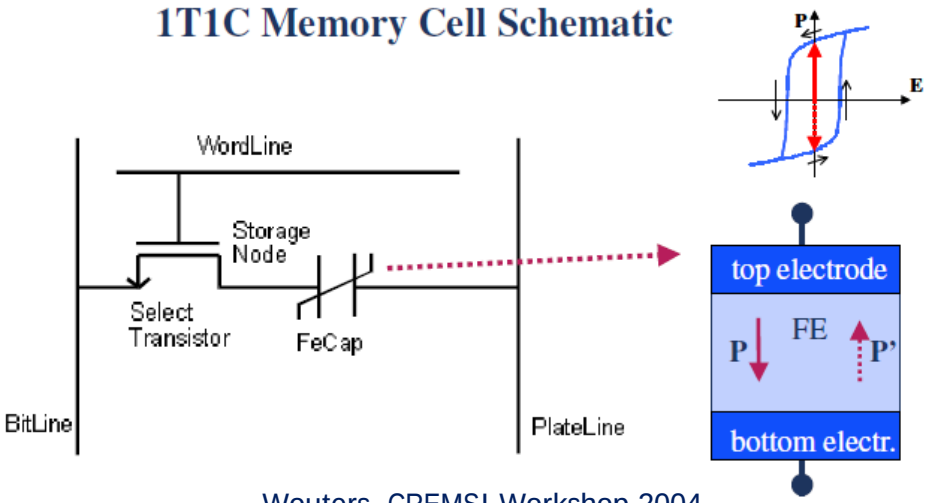
Ando, NVMTS 2011



Slaughter, IEDM 2012

FERAM

- Stores “charge” in a polarizable material
  - Typically PZT



Wouters, CREMSI Workshop 2004

- As with field/toggle MRAM, performance is similar to DRAM

FM23MLD16
8Mbit F-RAM Memory

RAMTRON

Features

8Mbit Ferroelectric Nonvolatile RAM
- Organized as 512Kx16
- Configurable as 1Mx8 Using /UB, /LB
- High Endurance 100 Trillion (10^{14}) Read/Writes
- NoDelay™ Writes
- Page Mode Operation to 33MHz
- Advanced High-Reliability Ferroelectric Process

SRAM Compatible
- JEDEC 512Kx16 SRAM Pinout
- 60 ns Access Time, 115 ns Cycle Time

Advanced Features
- Low V_{DD} Monitor Protects Memory against Inadvertent Writes

Superior to Battery-backed SRAM Modules
- No Battery Concerns
- Monolithic Reliability
- True Surface Mount Solution, No Rework Steps
- Superior for Moisture, Shock, and Vibration

Low Power Operation
- 2.7V – 3.6V Power Supply
- 14 mA Active Current

Industry Standard Configuration
- Industrial Temperature -40° C to +85° C
- 48-pin “Green”/RoHS FBGA package

http://www.cypress.com/

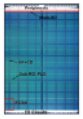
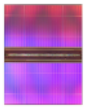
FERAM Scorecard

	Planar NAND	DRAM	FERAM
Cost Overall			
Cell size	$4F^2$ 16nm	$6F^2$ 2x nm	>100nm
Programming energy	Low	(Refresh)	Low
Multi-level / layer	1-3 BPC	None	Layer?
Latency Overall			
Fast read	10uS (page)	~10ns	~10ns
Fast write	1mS (page)	~10ns	~10ns
Endurance	1-100k	>1e15	>1e14

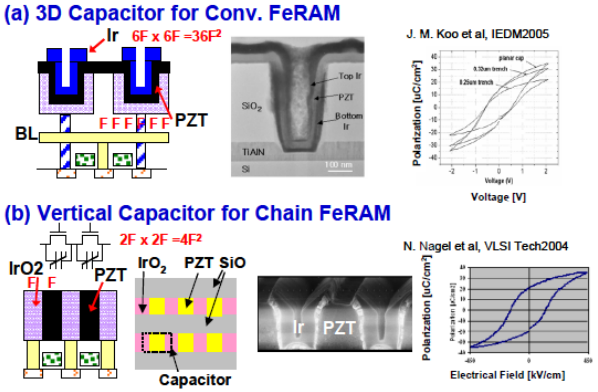
FERAM Cell Challenges

- Need to reduce cells size – limited by polarization / bitline cap ratio

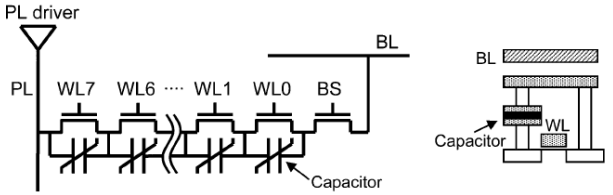
D. Takashima et al., MRS Spring Meeting 2011

Design Rule		0.5µm	0.25µm	0.2µm	130nm	130nm+DualOx
Capacity		16Kb	8Mb	32Mb	64Mb	128Mb
Chip		 ISSCC1999	 ISSCC2001	 ISSCC2003	 ISSCC2006	 ISSCC2009
Cell Structure		Offset Cell	Offset Cell	Stacked Cell	1-Mask Cell	Adv. Twin Cell
Capacitor		Sputter PZT	Sputter PZT	Sputter PZT	MOCVD PZT	MOCVD PZT
Cap. Size		3.24µm^2	0.855µm^2	0.49µm^2	0.194µm^2	0.098µm^2
Cell Size	Ave.	15.8µm^2	5.2µm^2	1.875µm^2	0.719µm^2	0.32µm^2
	Pure	13.3µm^2	4.2µm^2	1.539µm^2	0.612µm^2	0.25µm^2
Process		2Metal	2Metal	3Metal	3Metal	4Metal Dual Ox
Chip Size		1.9mm^2	76mm^2	96mm^2	87.5mm^2	87.7mm^2
R/W Cycle		80ns	70ns	75ns	60ns	75ns
Page/Burst		80ns	40ns	25ns	10ns	1.25ns
R/W Bandwidth		12.5MB/s	50MB/s	80MB/s	200MB/s	1.6GB/s
Vdd		3.3V	3.3V	3.3V/2.5V	3.3V/2.5V	1.8V

- Considering cell / array architecture solutions



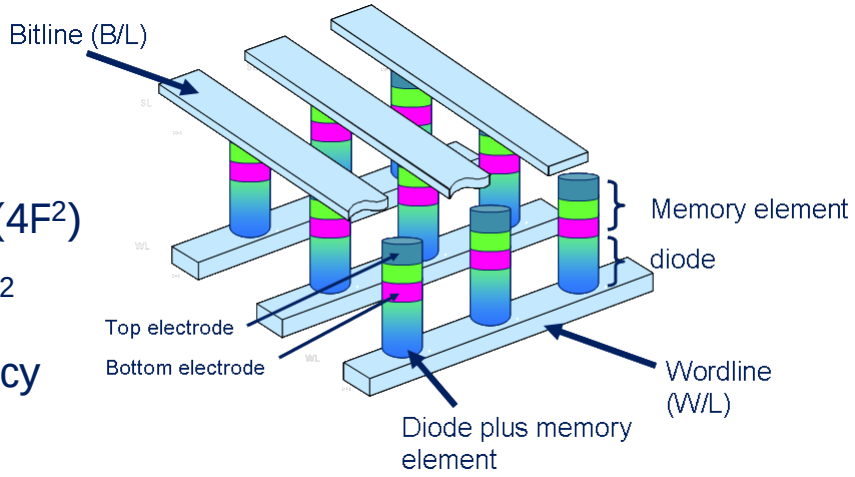
Takashima NVMTS 2011



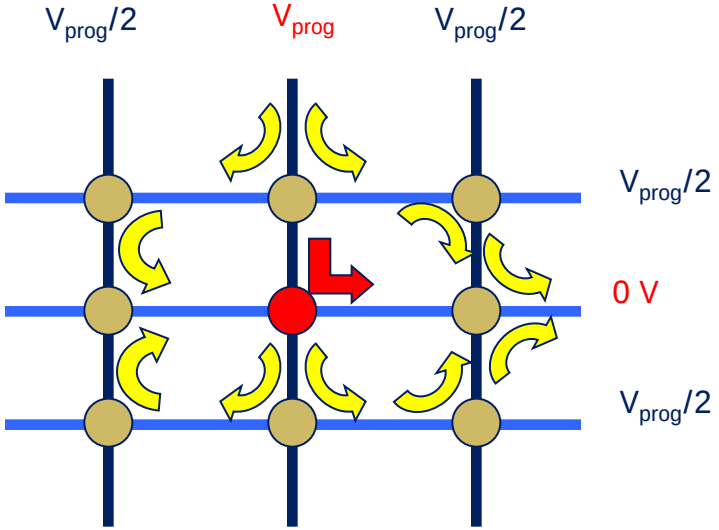
Shiga JSSC 2010

Multi-*Layer* Memory

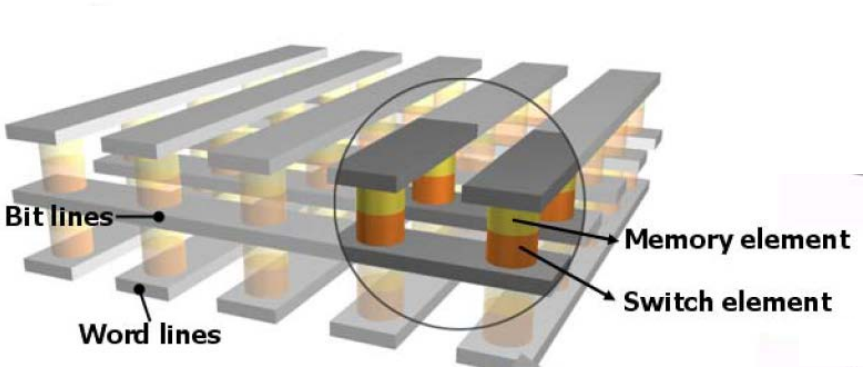
- Crossbar memory very attractive
  - "Simple" structure and minimum cell size ($4F^2$)
  - Suitable for 3D stacking → cell size $(4/n)F^2$
  - Array over circuitry → better array efficiency



- The basic cell architecture requires a selector structure to be integrated in the BEOL
  - Parasitic paths exist through neighboring cells
  - Programming (and also reading) can perturb the array



A Wide Range of Material Choices



For the selector structure several devices have been proposed so far, none have been “proven”

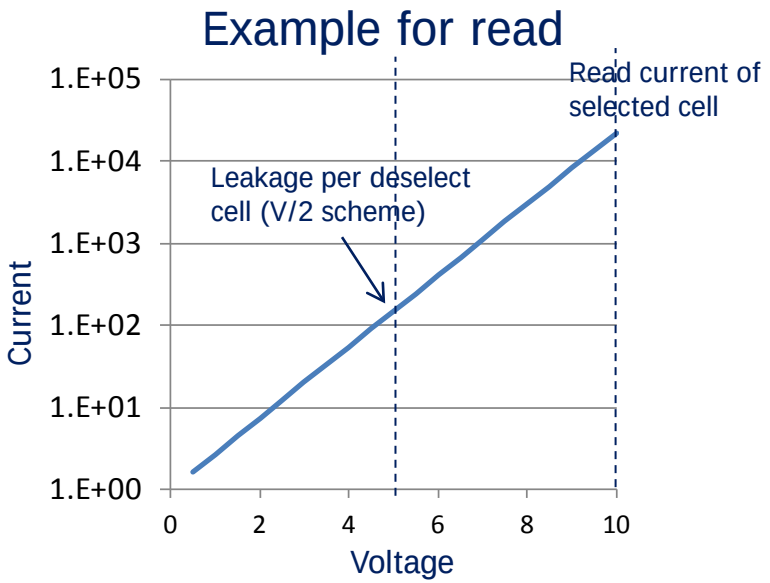
Selector device options

- Homojunctions → polySi p/n junctions
- Heterojunctions → p-CuO/n-InZnO
- Schottky diode→ Ag/n-ZnO
- Chalcogenide Ovonic Threshold Switching (OTS) materials
- Mixed Ionic Electronic Conduction (MIEC) materials

Cross-Point Switch Requirements

- Very high forward bias current
  - Greater than the switching current
- Low leakage through unselected cells
  - Steep IV characteristic
- Bipolar operation may be required
  - Necessary for bipolar RRAM

Cell Type	~20nm Cell Current	Current density
PCM	100uA	10 MA/cm^2
RRAM	10uA	1 MA/cm^2



Array size < $I_{LRS}(V) / I_{LRS}(V/2)$

Summary Scorecard

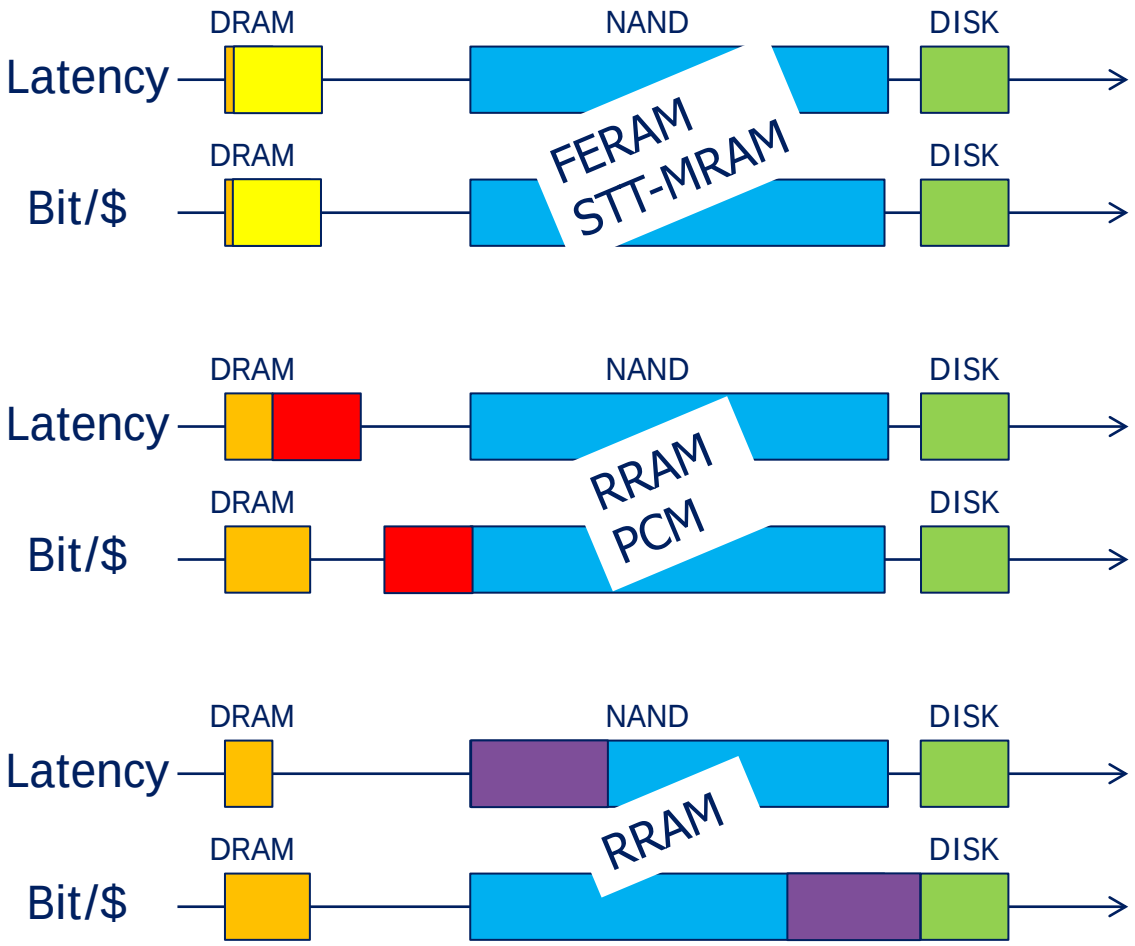
	Planar NAND	DRAM	PCM	RRAM	STT-MRAM	FERAM
Cost Overall						
Cell size	$4F^2$ 16nm	$6F^2$ 2x nm	$4F^2$ 20nm	$4F^2$ 20nm	$6F^2$ 20nm	>100nm
Programming energy	Low	(Refresh)	~High I	Low - Med	Med I	Low
Multi-level / layer	1-3 BPC	None	Level/ Layer	Level/ Layer	Layer	Layer?
Latency Overall						
Fast read	10uS (page)	~10ns	<100ns	<100ns	<30ns	~10ns
Fast write	1mS (page)	~10ns	>100ns	~10nS	~10ns	~10ns
Endurance	1-100k	>1e15	1e8	1e8 ??	>1e15	>1e14

Where can an emerging memory fit in?

NVDRAM
(Non-Volatile DRAM)

SCM
(Storage class memory)

NAND
REPLACEMENT
(STORAGE)



Summary

- Many new NVM technologies are attempting to gain a foothold in the computing devices
- While they have cost *or* performance advantages over NAND or DRAM, none beat the performance of DRAM or the cost of NAND
- The most direct fit would be a NAND/DRAM “blend” / SCM, but the system implementation for this type of memory is not yet established
- We need a few more advances in materials to make these a reality!

- Acknowledgments: Thanks to the Micron R&D team and the work of the authors presented here.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