



# **Interfacial Engineering in ReRAMs based on Strongly Correlated Electron Systems**

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# Summary



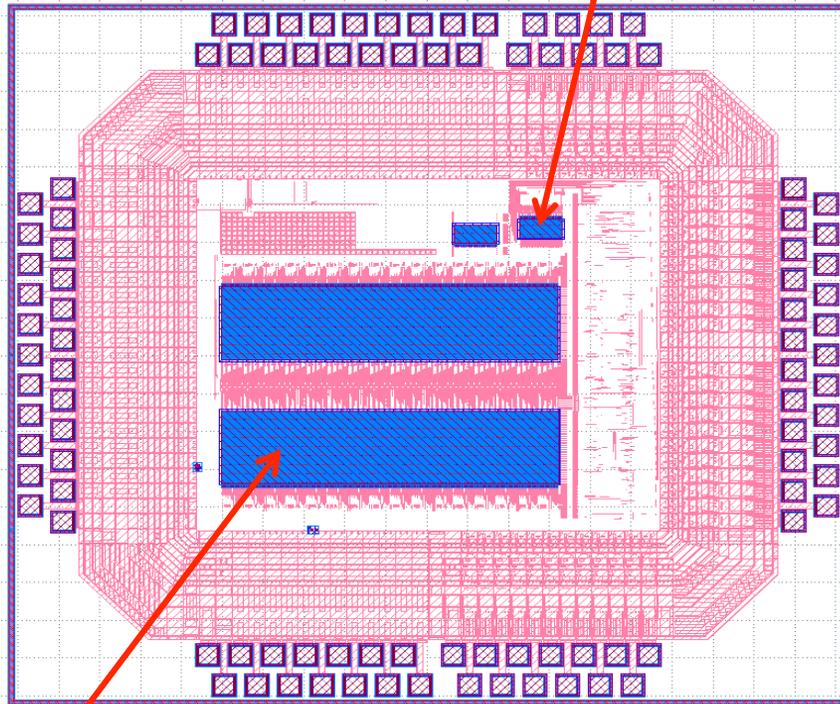
- 4DS has developed a robust ReRAM system, (MOHJO™) based on Strongly Electron Correlated Systems such as  $\text{Pr}_{1-x}\text{Ca}_x\text{MnO}_3$  (PCMO)
- Technology attributes include: low power operation, high-speed switching, scalable down to 10 nm and below, high cycle endurance and long retention time
- MOHJO™ is implemented as a back end process atop standard CMOS flow
- MOHJO™ is based on Mott metal-insulator transition driven by field-induced non-linear transport of oxygen vacancies across the hetero-junction

# 4DS TEST CHIP 16kb

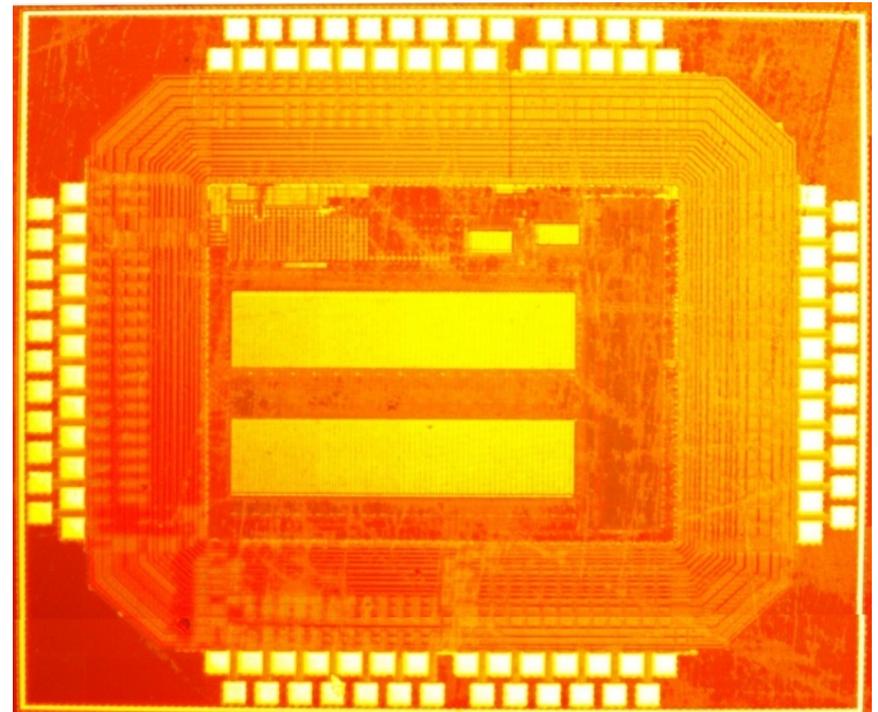


Two mini-arrays

Die Layout

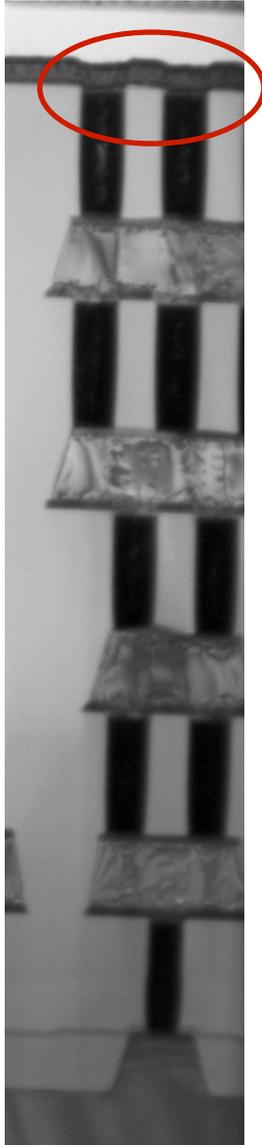


Die Picture



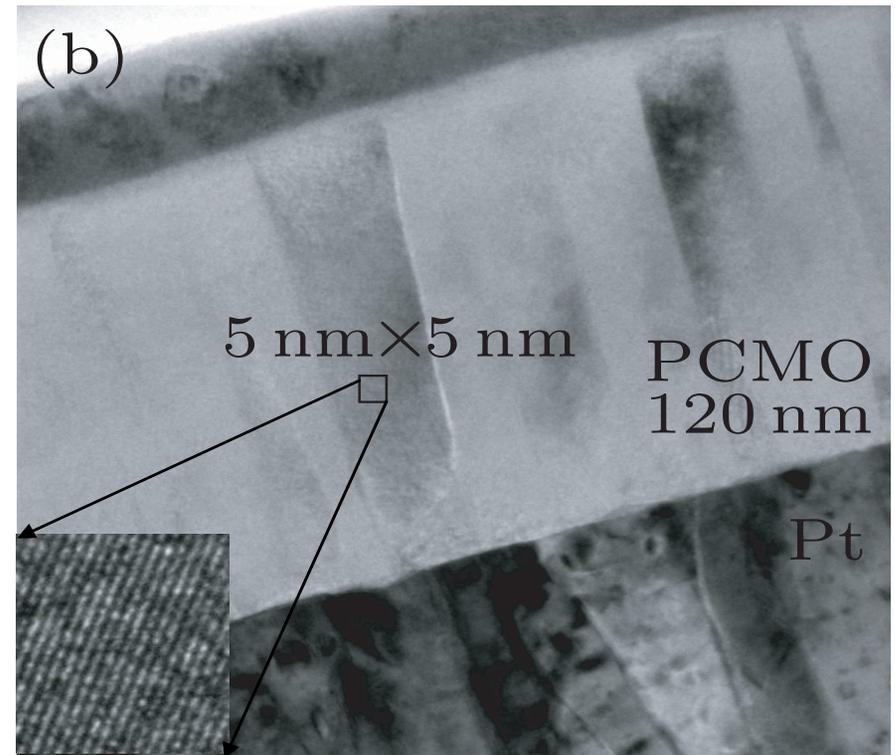
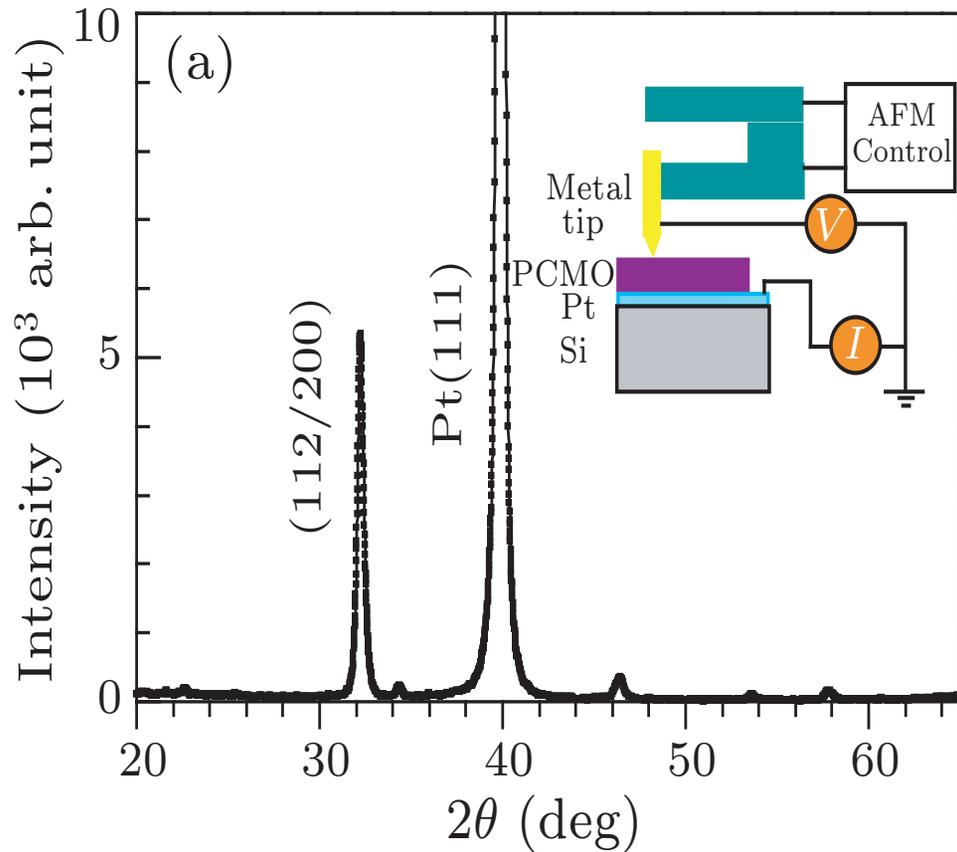
Two Full Banks of 8kb Each

# Cross-Sectional View of Test Chip

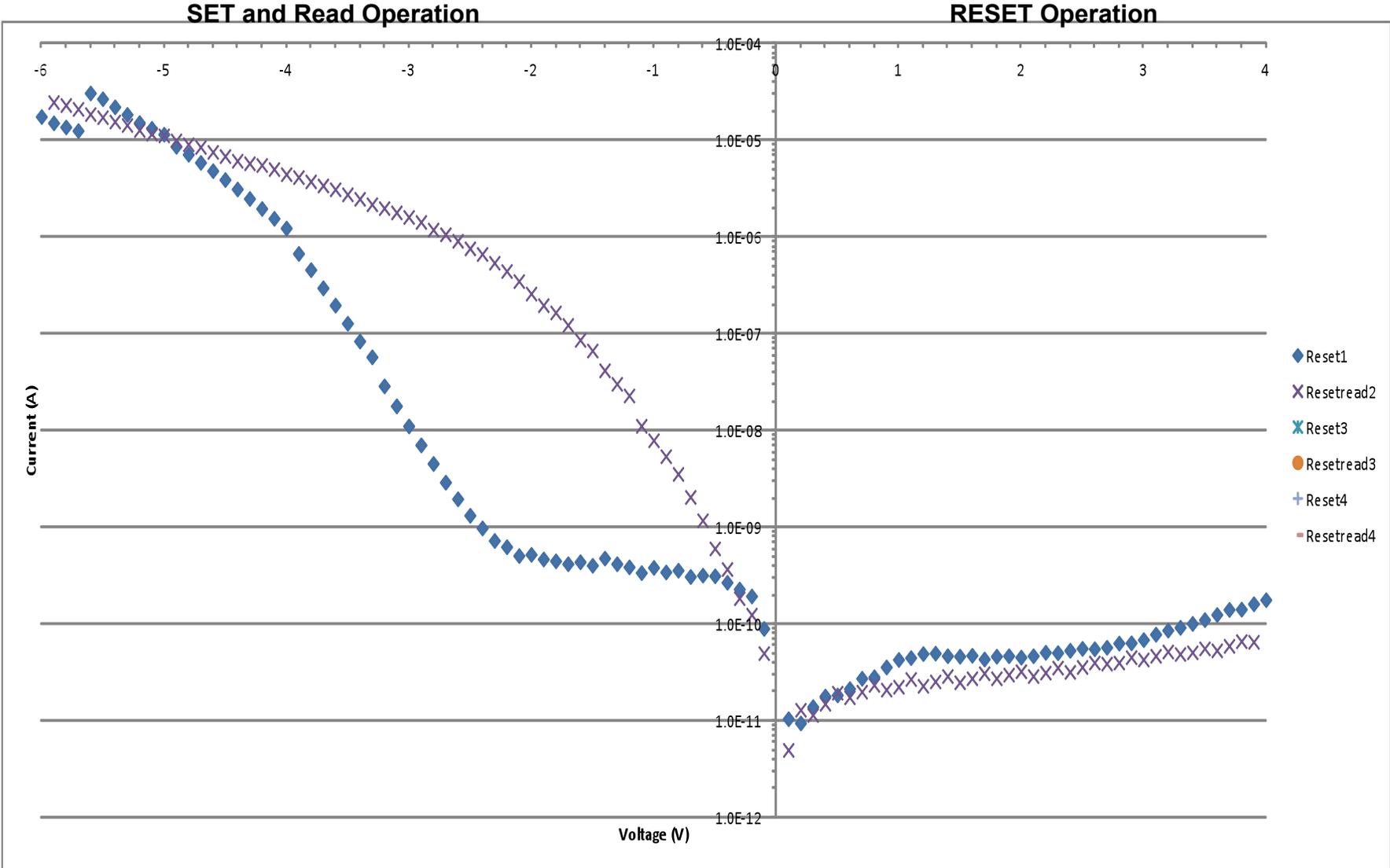


- TEM of core area
- Base process is a friendly 0.18um 4 metal layers, 5 via layers for ease of implementation, while we have single cell data proving scaling down to 30nm.
- Resistor process is entirely contained above the top via layer.
- Resistor process is low temperature, metal/via process friendly, with no visible or measureable negative impact to the lower interconnect layers.

# Highly-oriented, Stoichiometric, Crystalline Material



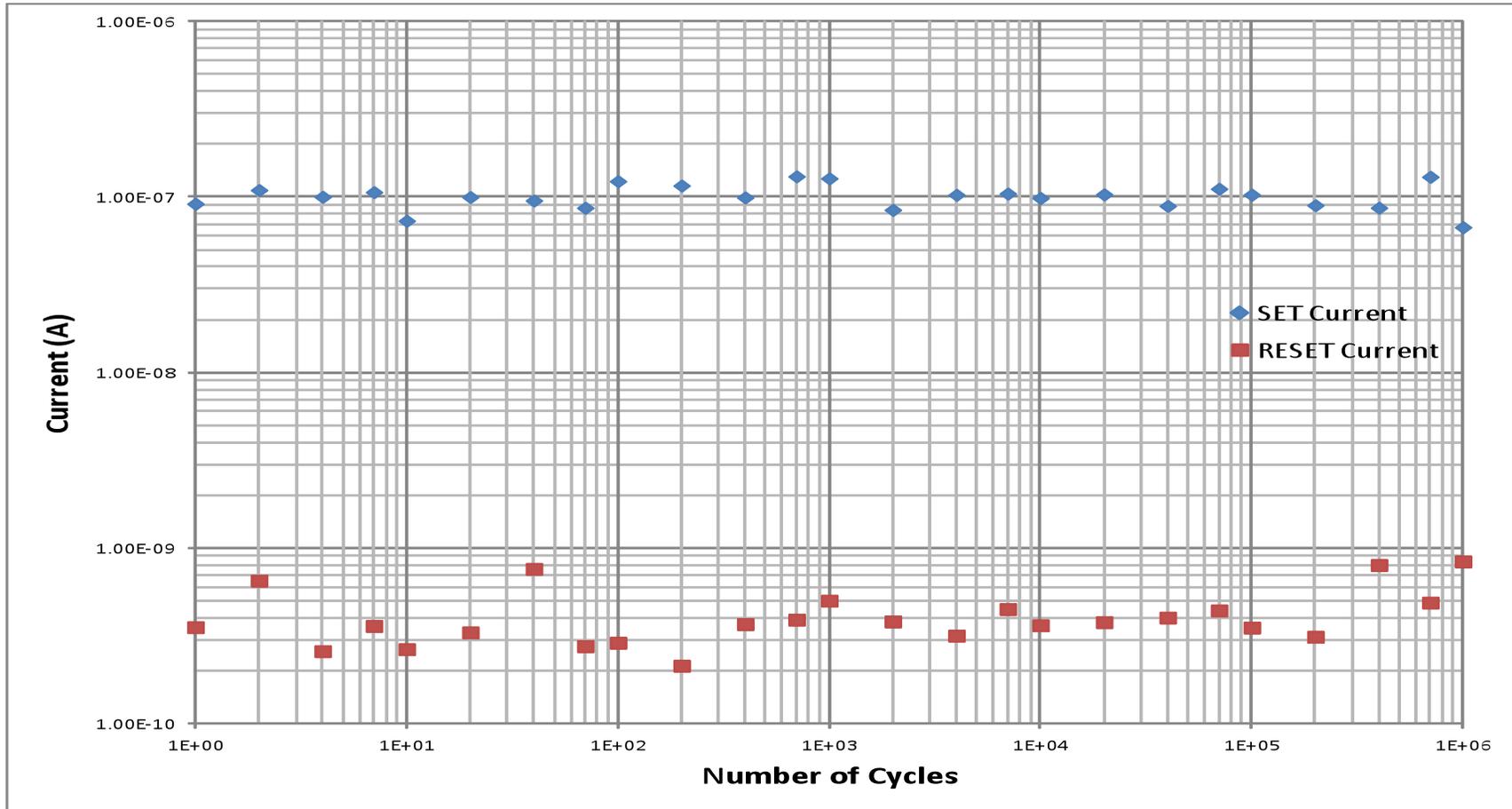
# Typical Device Hysteresis is Asymmetric



# Advantages of Asymmetric Hysteresis

- **Extra low power operation on the reset side and low power operation on the set side.**
- **Low power operation enables a bulk or block erase optional feature.**
  - Low power bulk erase is also a highly desirable feature in security applications where the data may need to be wiped out quickly.
  - The bulk erase is a feature and not a requirement as in many current nonvolatile memories.
- **Both the Set (Program) and Reset (Erase) operations can be performed on a byte by byte basis.**

# Typical Cycling Data



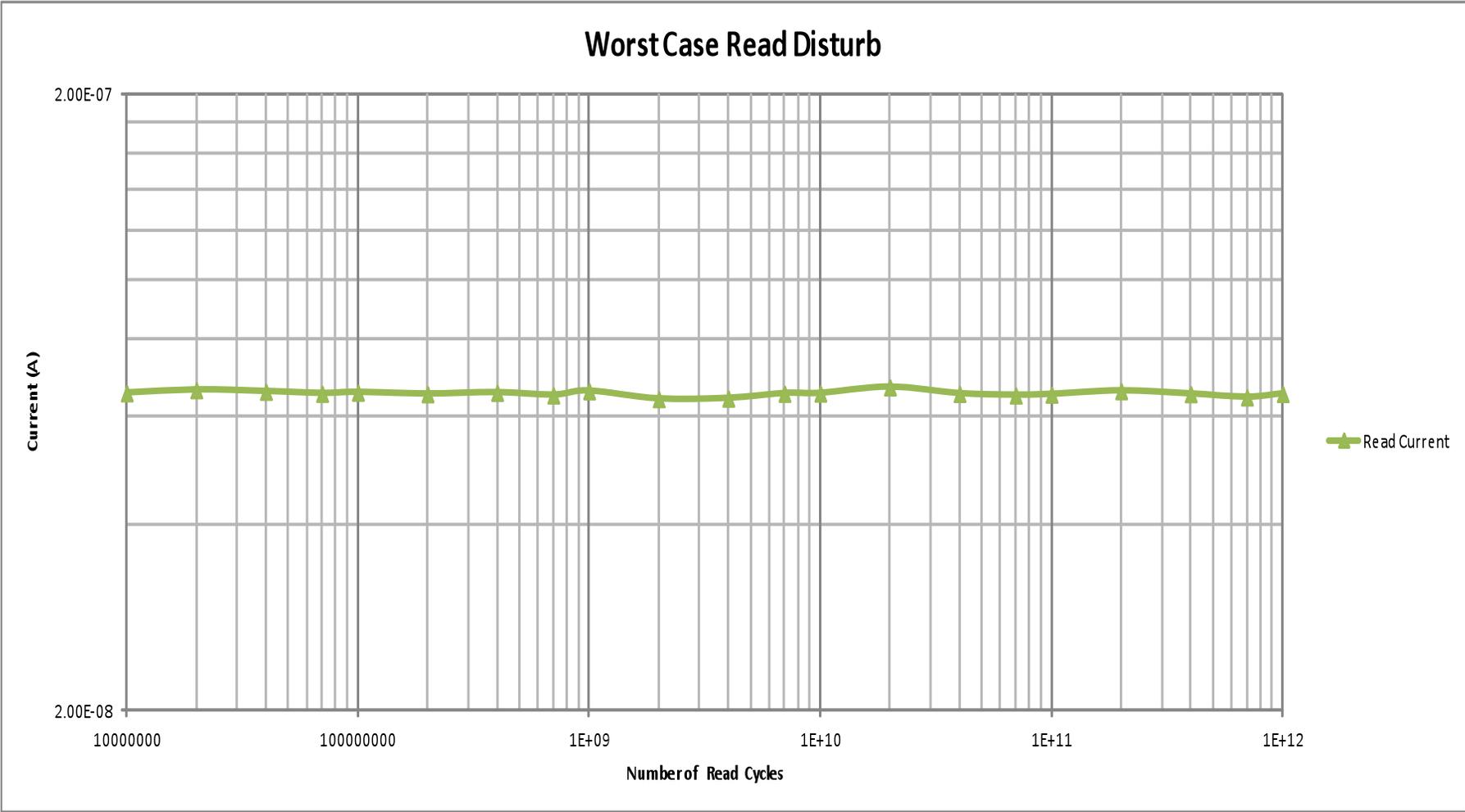
- The cycling for this type of memory is very stable, with good results up to  $10^9$  using dumb cycling. With a smart algorithm including verify and field modification much higher endurance is expected

# More than 10 year Data Retention at 85 °C



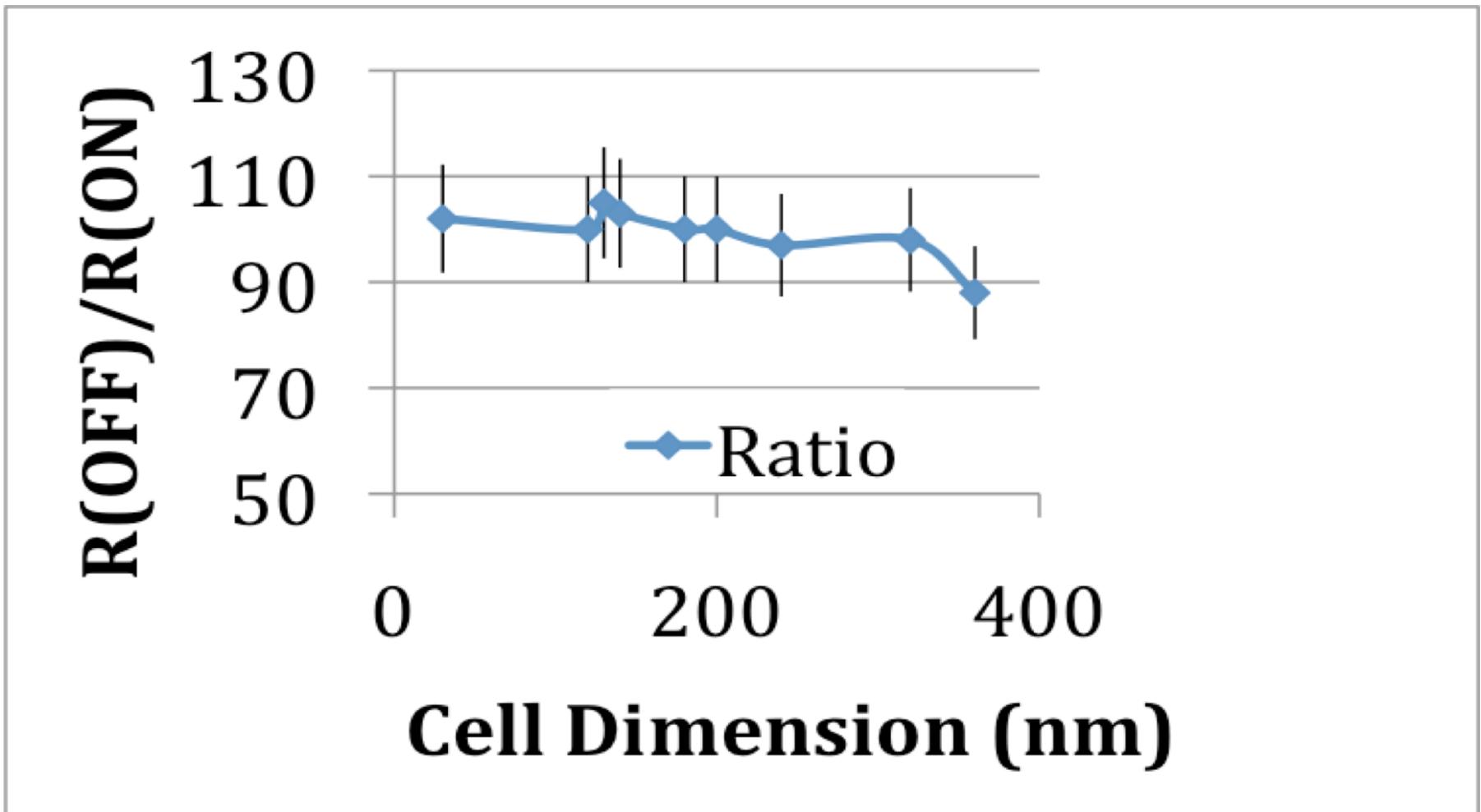
<b>T (°C)</b>	<b>T (K)</b>	<b>Relaxation Constant (sec)</b>
<b>27</b>	<b>300</b>	<b>1.4 X 10<sup>9</sup></b>
<b>50</b>	<b>323</b>	<b>9.4 X 10<sup>8</sup></b>
<b>85</b>	<b>358</b>	<b>5.8 X 10<sup>8</sup></b>
<b>90</b>	<b>363</b>	<b>5.5 X 10<sup>8</sup></b>
<b>130</b>	<b>403</b>	<b>3.6 X10<sup>8</sup></b>

# Typical Read Disturb Data



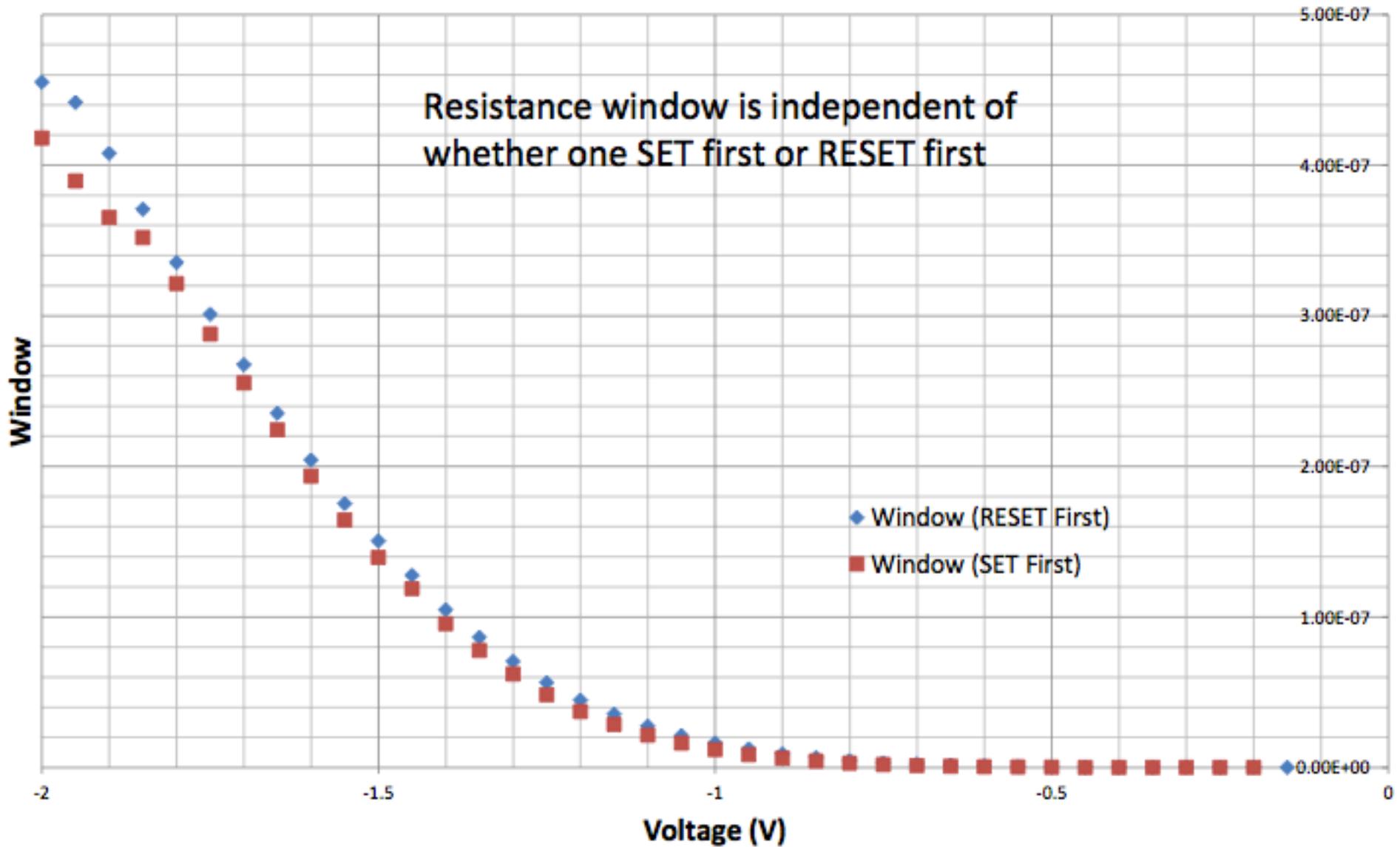
- The graph shows the disturb of the reset condition, due to the asymmetrical hysteresis of this material the read is always done in the set direction so the worst case disturb would be of reset data shown here with no noticeable read disturb at  $10^{12}$  reads

# Scalability data down to 30 nm (projected < 10nm)

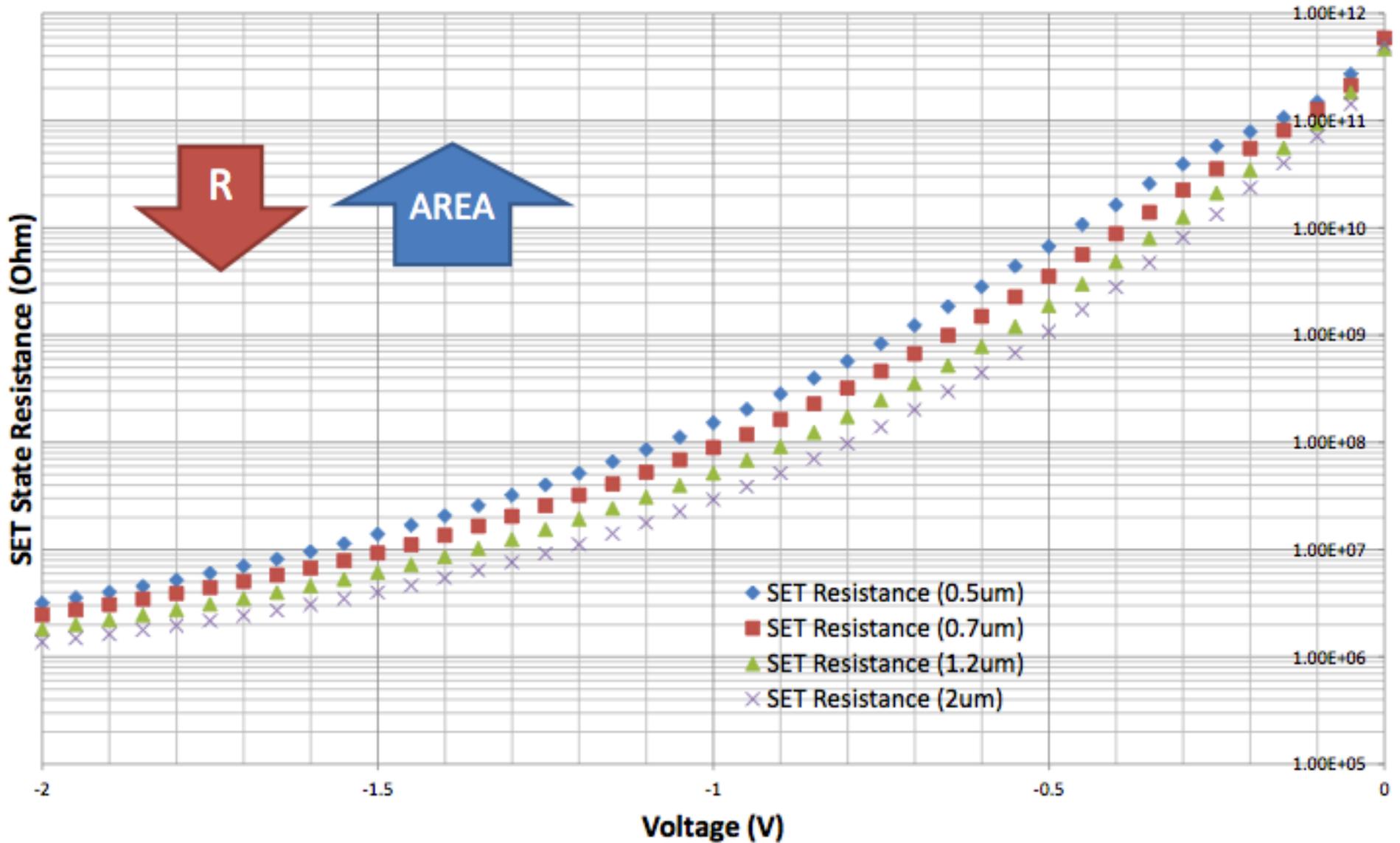


**MOHJO™ IS NOT BASED ON  
FILAMENTARY PROCESS**

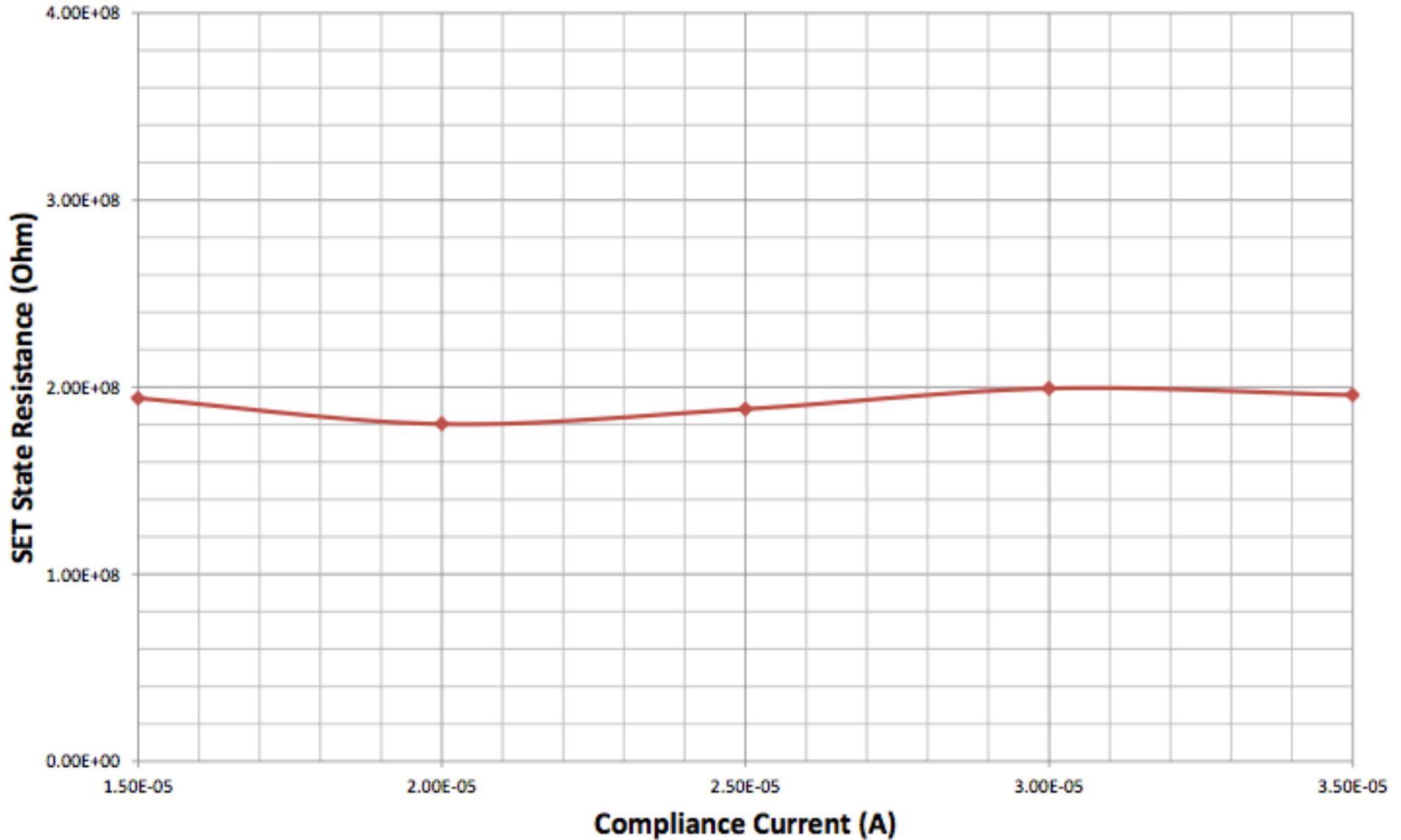
# Forming is not Required for 4DS Resistors



# 4DS ON State Resistance is Area Dependent

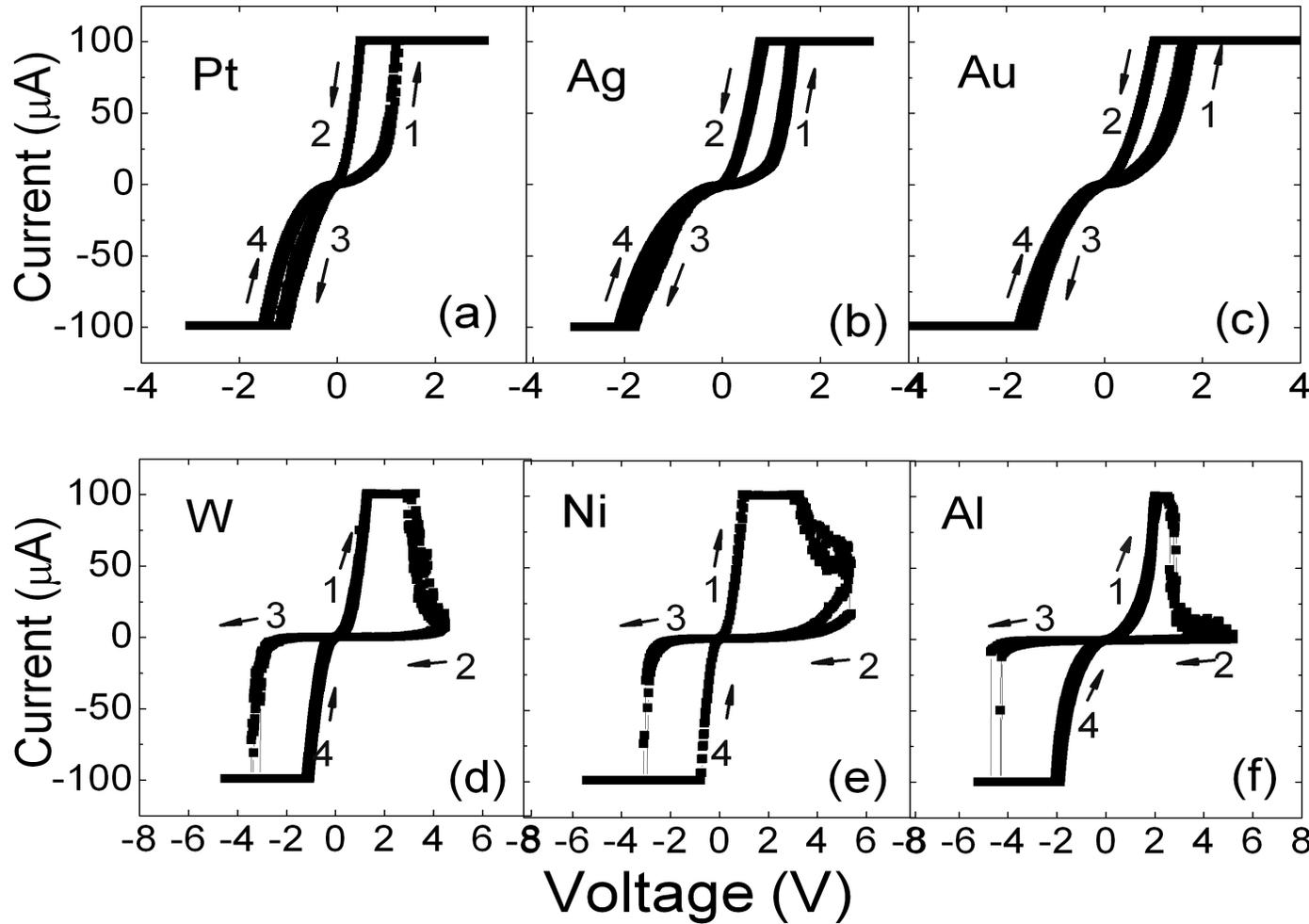


# 4DS ON Resistance is a Weak Function of Compliance Current

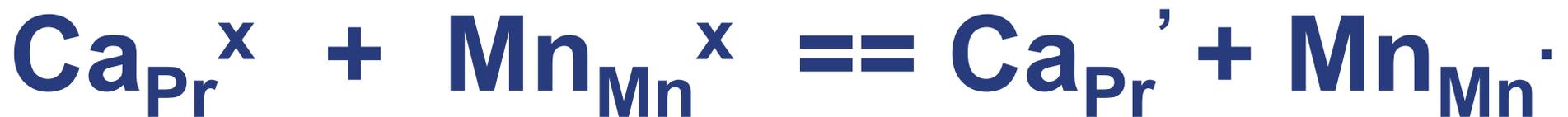


**OXIDATION OF TOP ELECTRODE  
(TE) IS SEEN IN MOHJO™**

# Clock wise and Counter Clock wise Loops



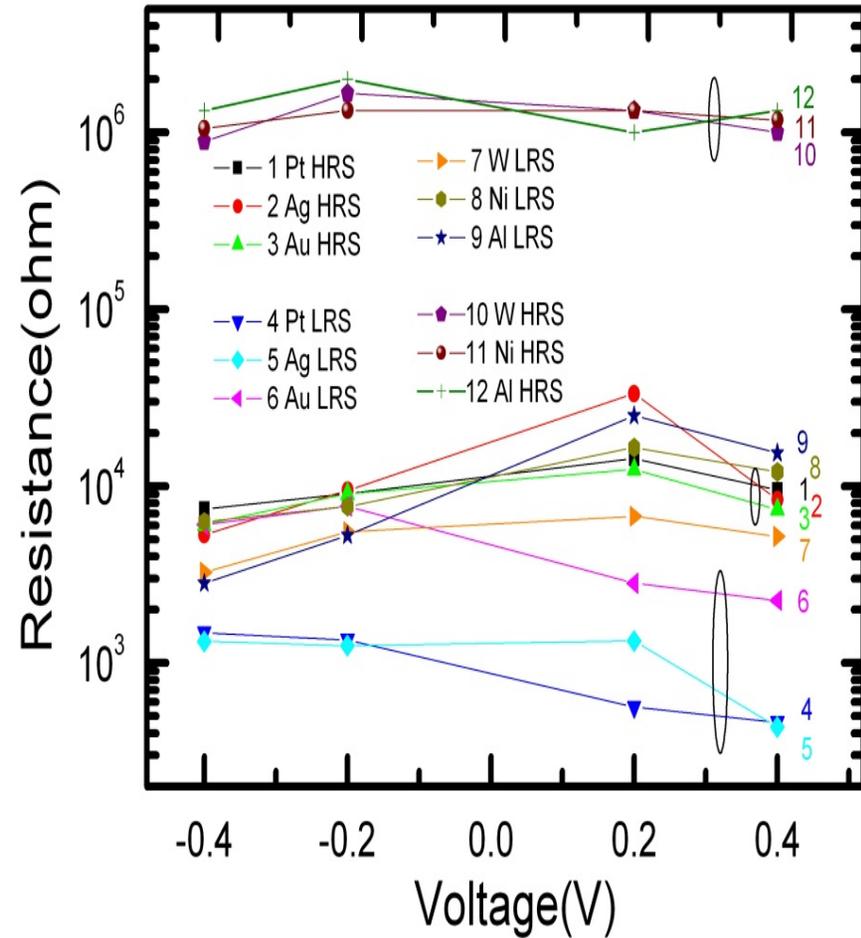
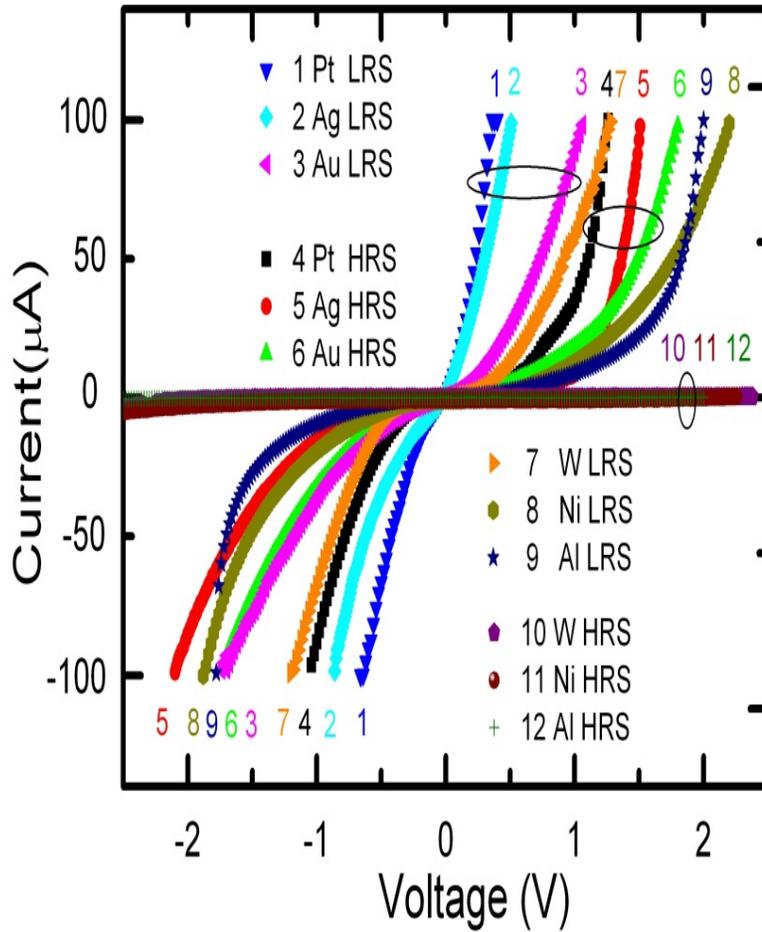
# Ca is an Acceptor in PCMO



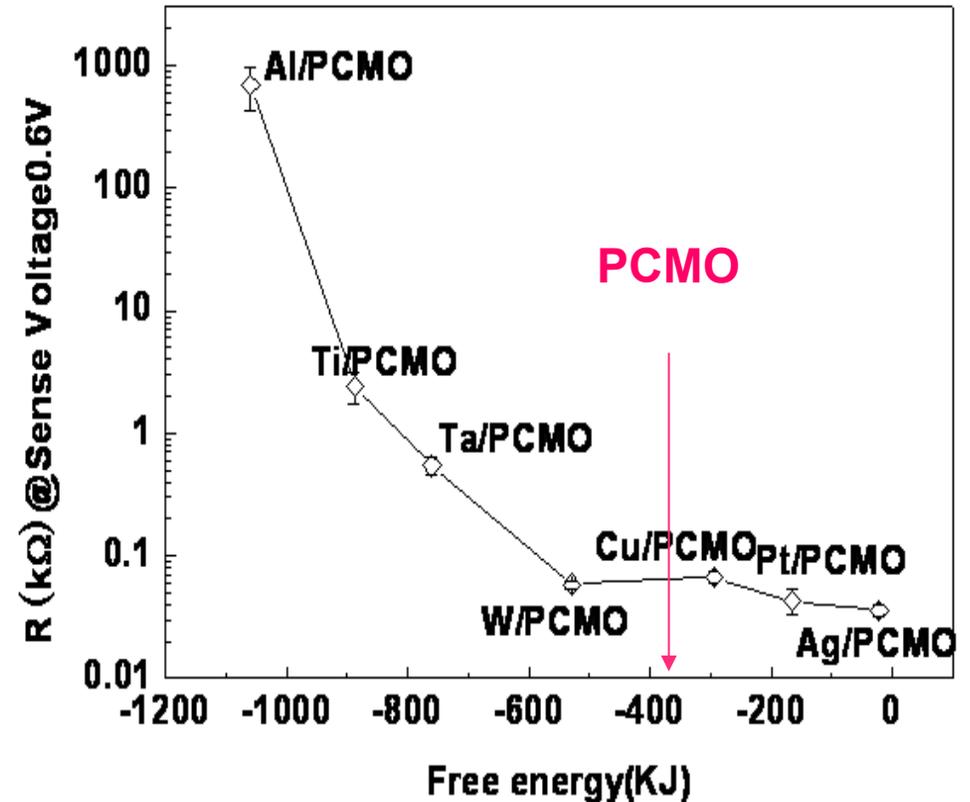
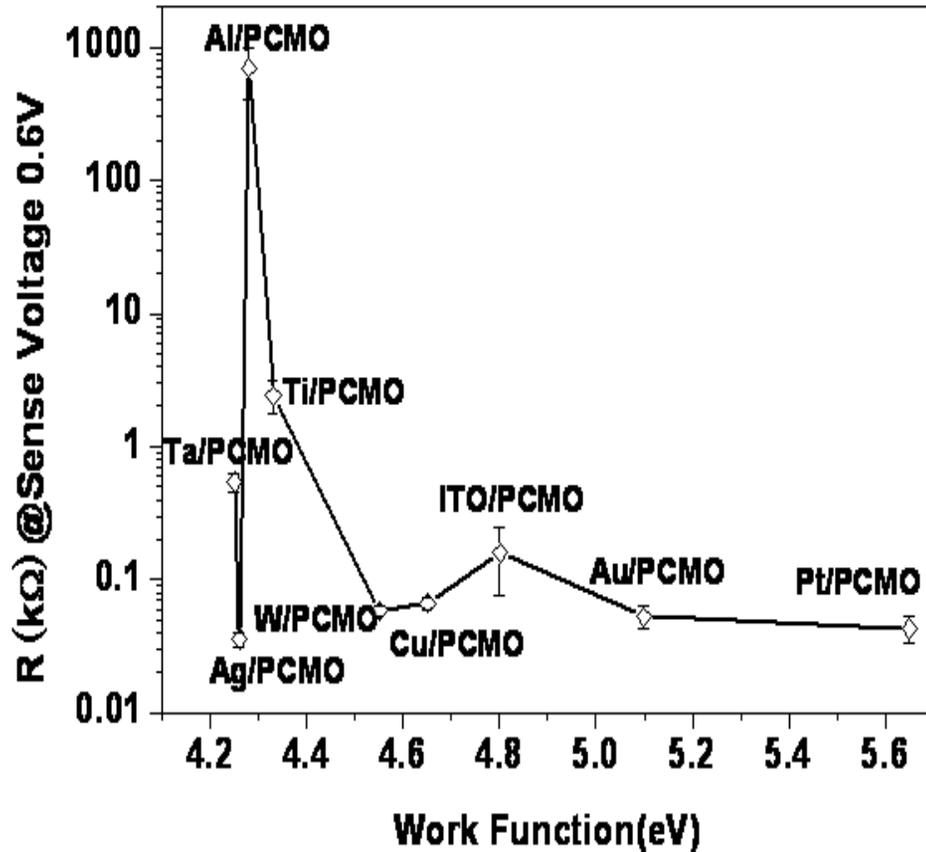
# Oxygen Vacancy is a Donor



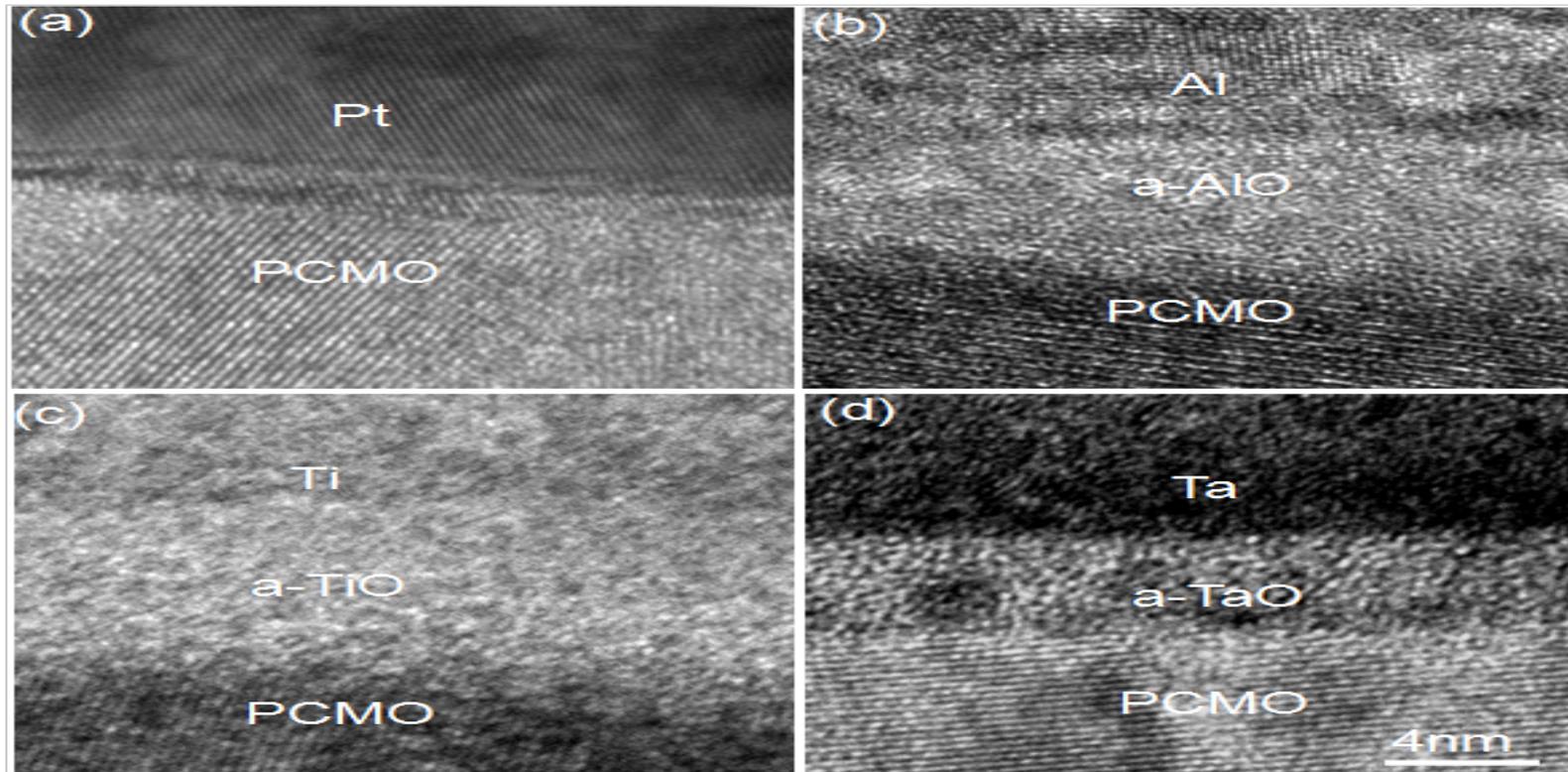
# Variation of I-V for various TEs



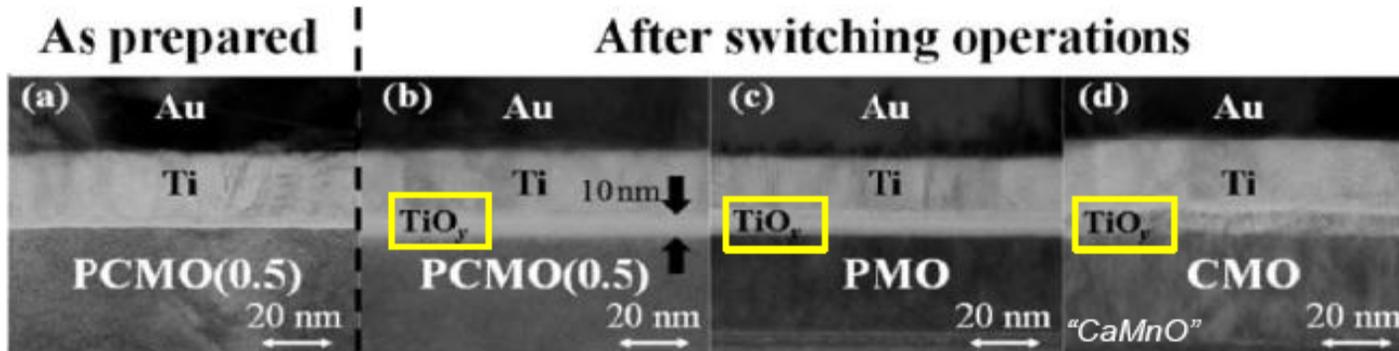
# Gibbs Free energy of oxidation of TE is important



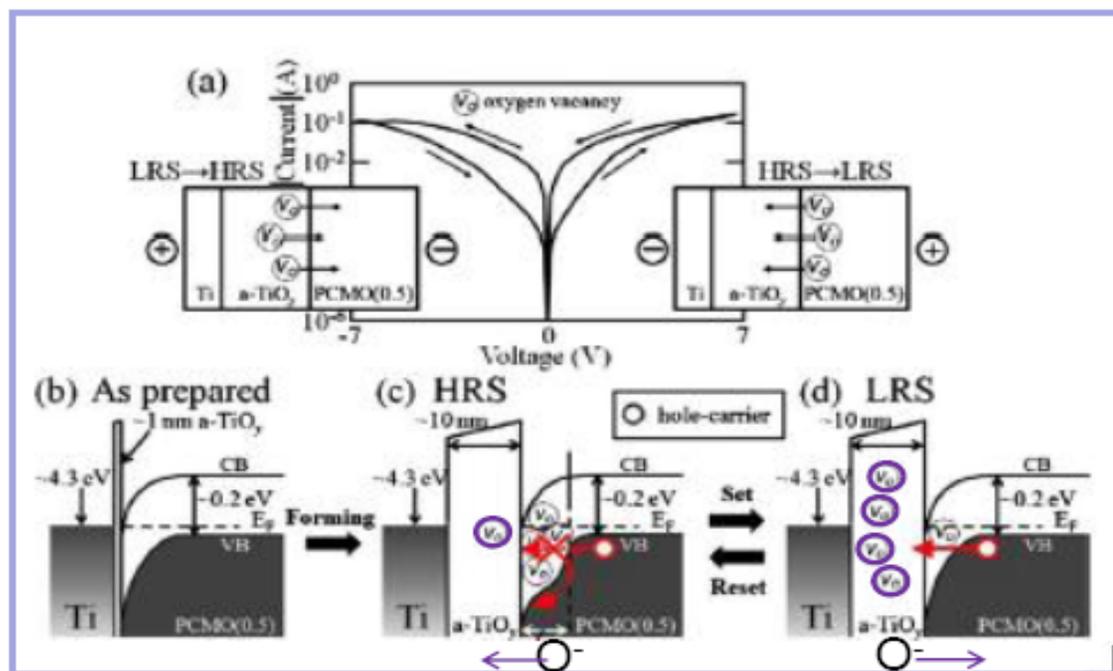
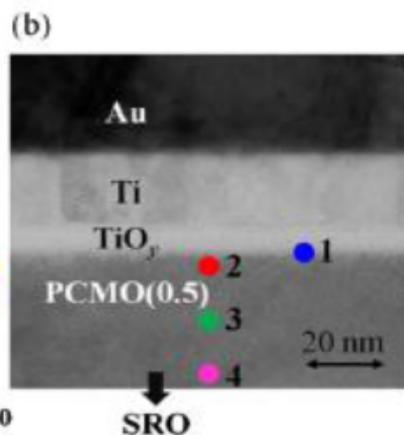
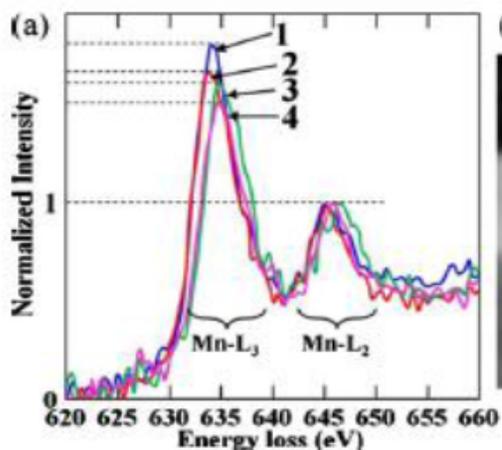
# Oxidation of reactive Top Electrodes (TE)



# Oxygen Migration

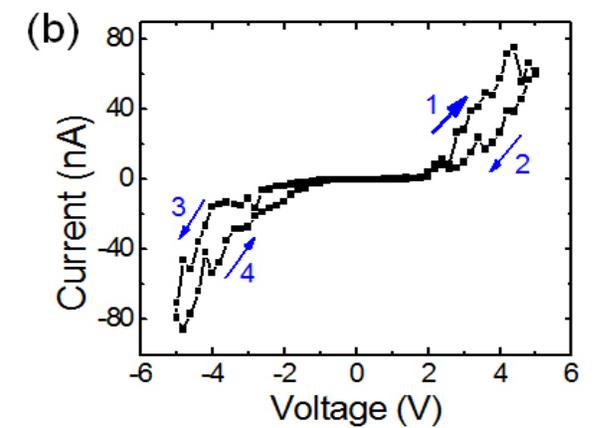
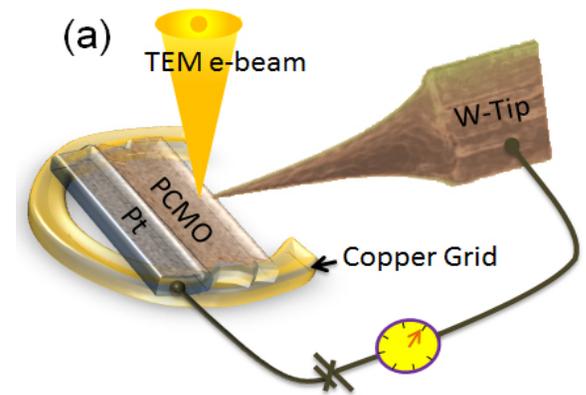
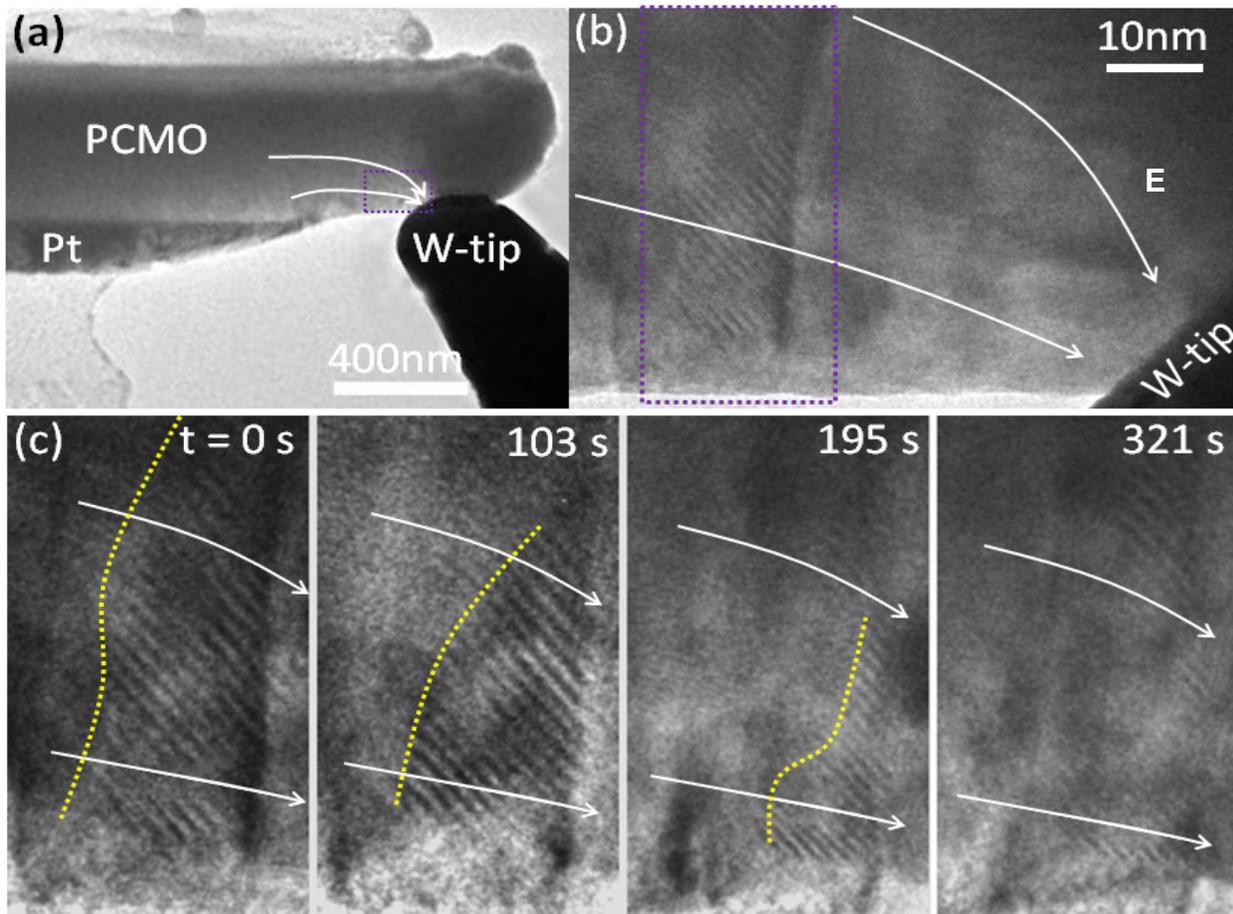


1. Interface Oxidation-Revealed by TEM



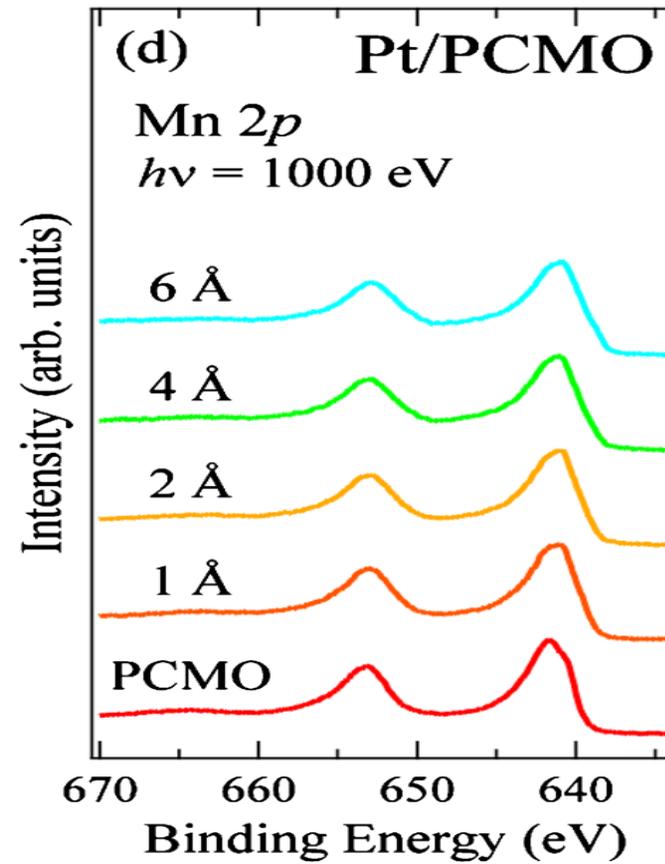
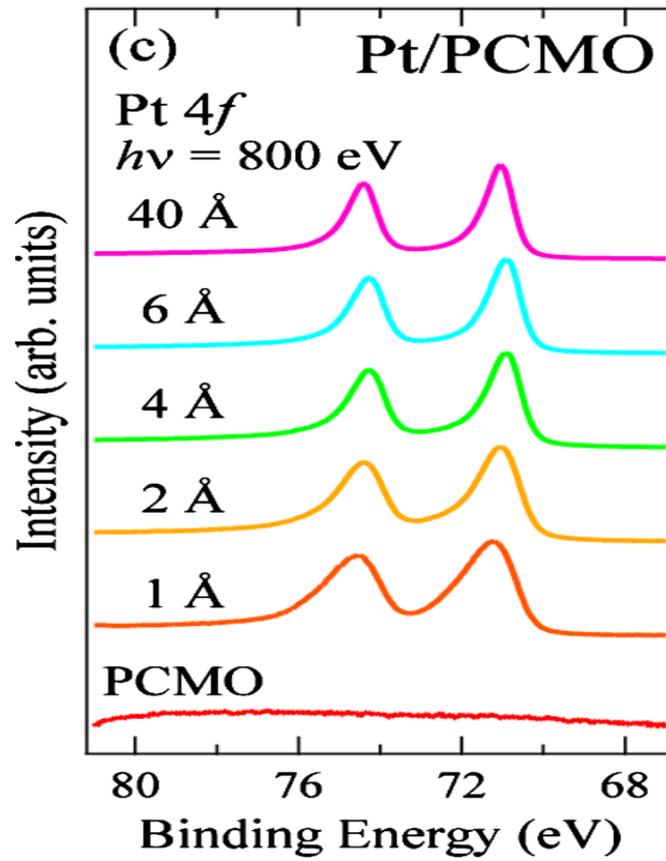
1. Oxygen migration → Change Band structure and Fermi Level

# In situ TEM Observation of Oxygen Vacancy Motion

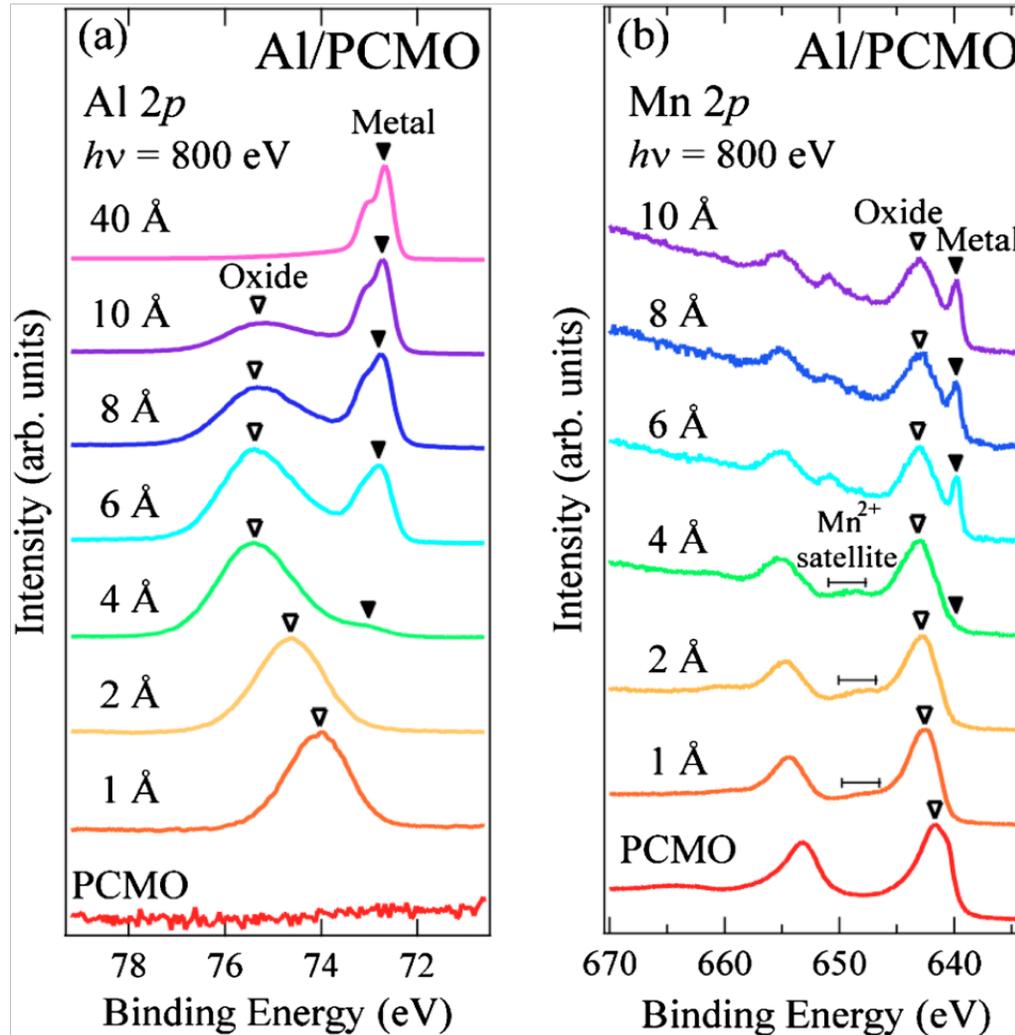


# CHANGES IN MANGANESE OXIDATION STATES ARE SEEN IN MOHJO™

# No interaction with noble metals



# Both Oxide Formation and Oxidation State Changes are Seen



R. Yasuhara, et al., APL 97, (2010)

<b>Metal Oxide Heterojunction</b>	<b>P-N Junction</b>
Gibbs Energy	Fermi energy
Space vacancy formation	Space charge formation
Ion migration	Drift of electrons/holes
Temperature sensitive	Temperature sensitive
Field dependent	Field dependent

**METAL-INSULATOR TRANSITION  
IS SEEN AT THE INTERFACE IN  
MOHJO™**

# 4DS Oxides are Correlated Electron Systems

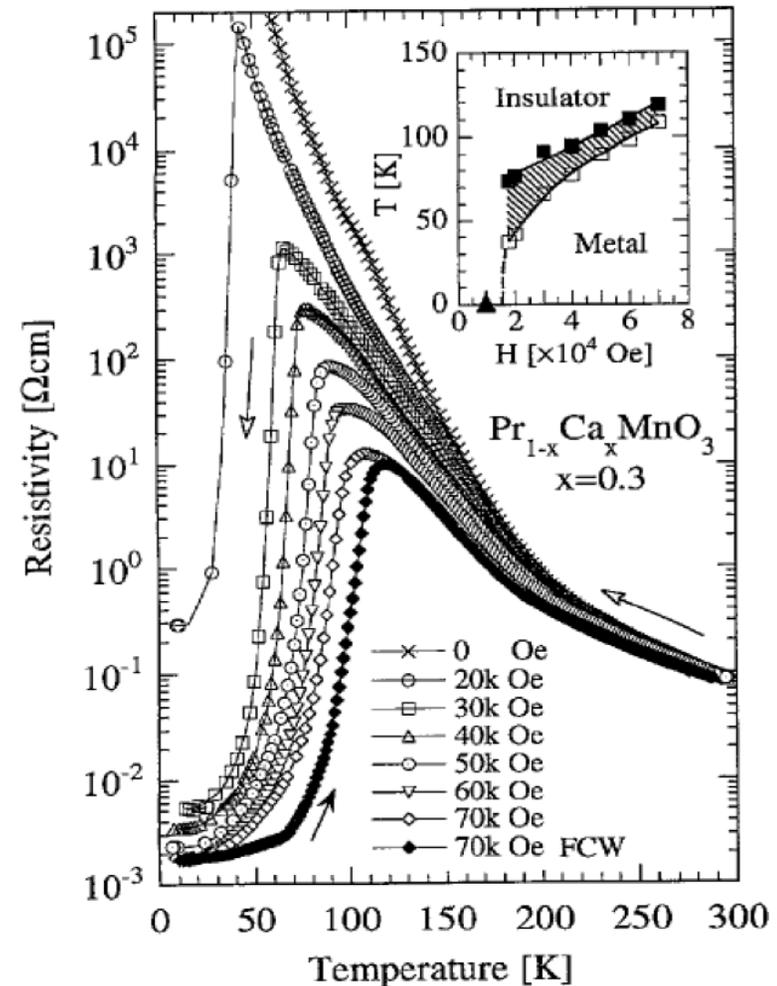
■ Resistivity modulations in the bulk can be induced by:

Magnetic field

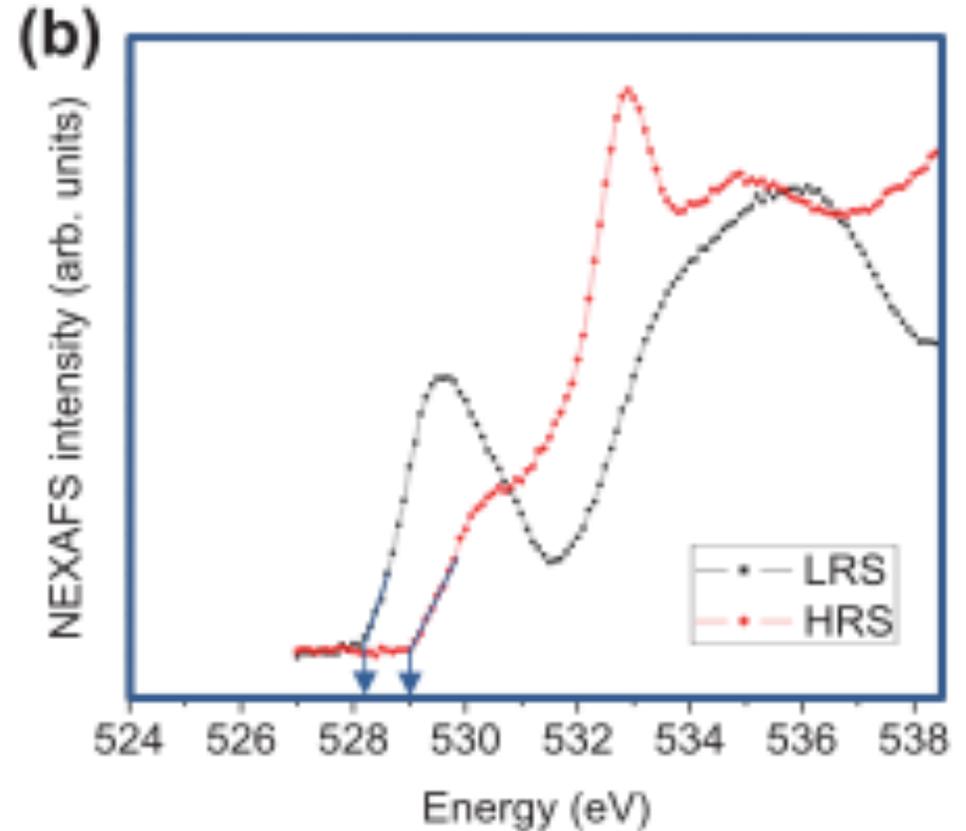
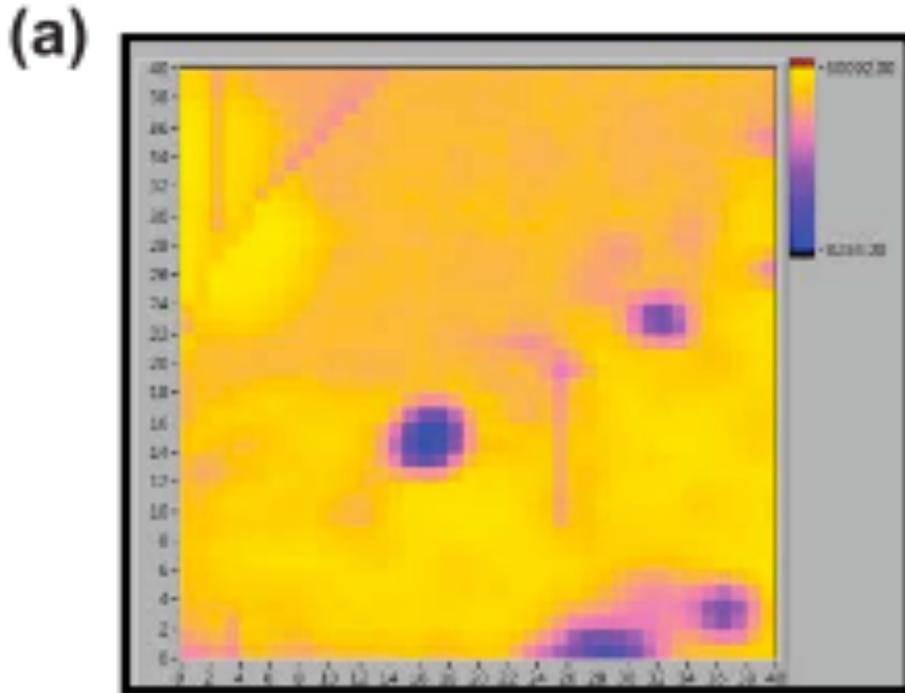
Electric field

Charge particle bombardment

■ Resistivity modulation in the bulk is attributed to the Metal to Insulator transition



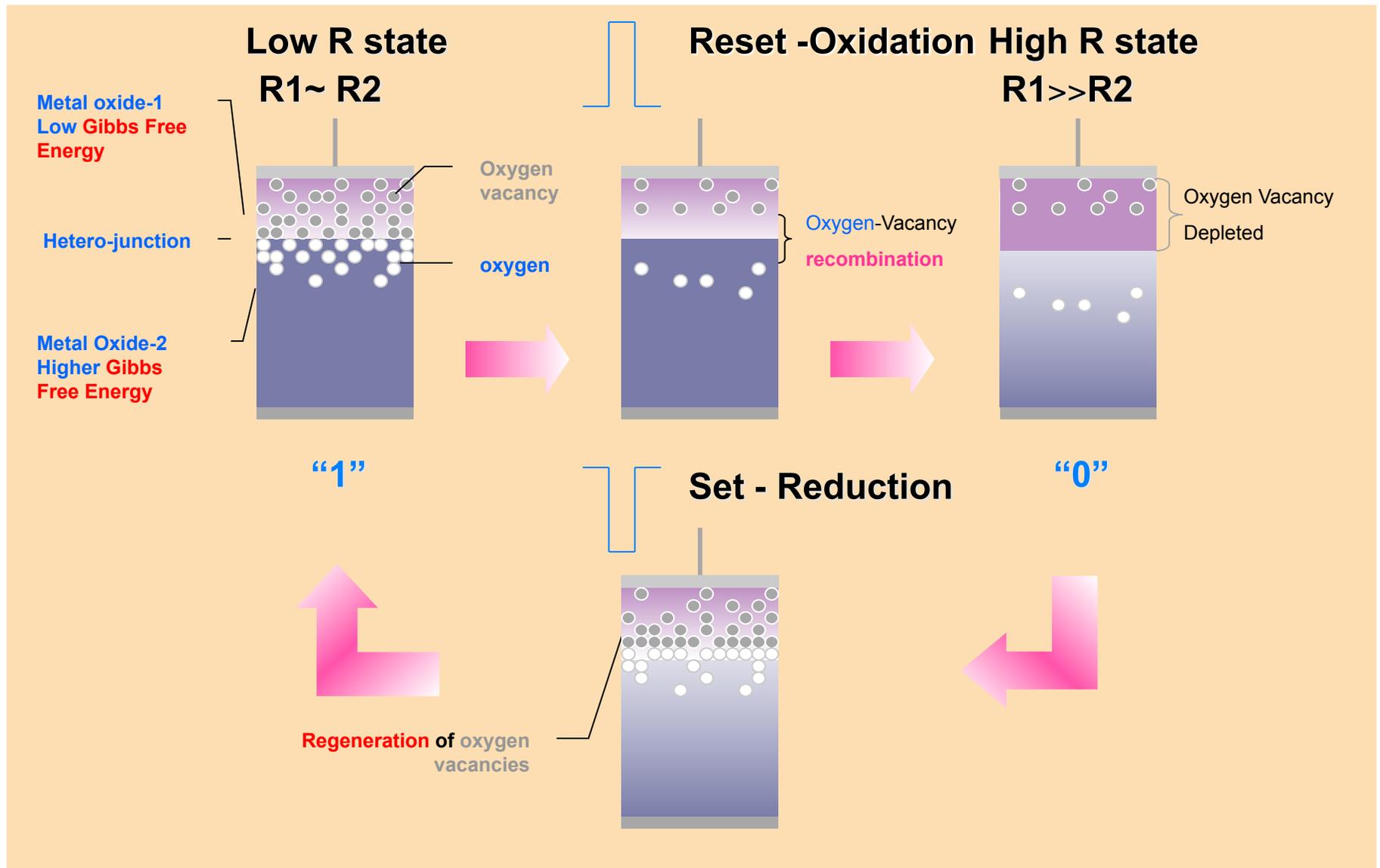
# Spectro-Microscopy Image and NEXAFS (Near Edge X-Ray Absorption Fine Structure)



**Conduction band edge for LRS = 528 eV**  
**Conduction band edge for HRS = 528.7 eV**

**Mott gap = 0.7 eV**

# Metal Oxide Heterojunction Operation (MOHJO™)



# Technology – Key Attributes

**4DS' MOHJO™ memory is high speed, non-volatile, low power, low cost and is able to be produced using existing semiconductor manufacturing equipment**

<b>LOW COST</b>	<ul style="list-style-type: none"> <li>Produced using +1 to 4 mask steps when combined with standard CMOS process (as compared to +16 to 20 mask steps for FLASH) for the memory core.</li> <li>Scalable and repeatable proprietary wafer process for mass production.</li> </ul>	<b>EXISTING FAB EQUIPMENT / PROCESSES</b>	<ul style="list-style-type: none"> <li>Simple integration into fabs, process steps utilizes established fabrication equipment and processes.</li> <li>Proprietary process is implementable as customized modules on existing fabrication tools.</li> </ul>
<b>LOW POWER</b>	<ul style="list-style-type: none"> <li>Low voltage operation and low current, making it attractive for a variety of applications</li> </ul>	<b>DENSITY</b>	<ul style="list-style-type: none"> <li>High density: 4F<sup>2</sup> with diode/6F<sup>2</sup> with transistor</li> </ul>
<b>LOW TEMPERATURE</b>	<ul style="list-style-type: none"> <li>The memory is formed in the back end metal layers with a proprietary low temperature process.</li> </ul>	<b>LONG CYCLE LIFE</b>	<ul style="list-style-type: none"> <li>10<sup>9</sup></li> </ul>
<b>HIGH SPEED</b>	<ul style="list-style-type: none"> <li>Fast Read/Write</li> </ul>	<b>RELIABILITY</b>	<ul style="list-style-type: none"> <li>10 year data retention</li> </ul>
<b>SCALABILITY</b>	<ul style="list-style-type: none"> <li>Tested at 30nm, projected down to 10nm and below.</li> </ul>	<b>CMOS COMPATIBLE</b>	<ul style="list-style-type: none"> <li>Process is CMOS compatible.</li> </ul>

Thanks for your attention