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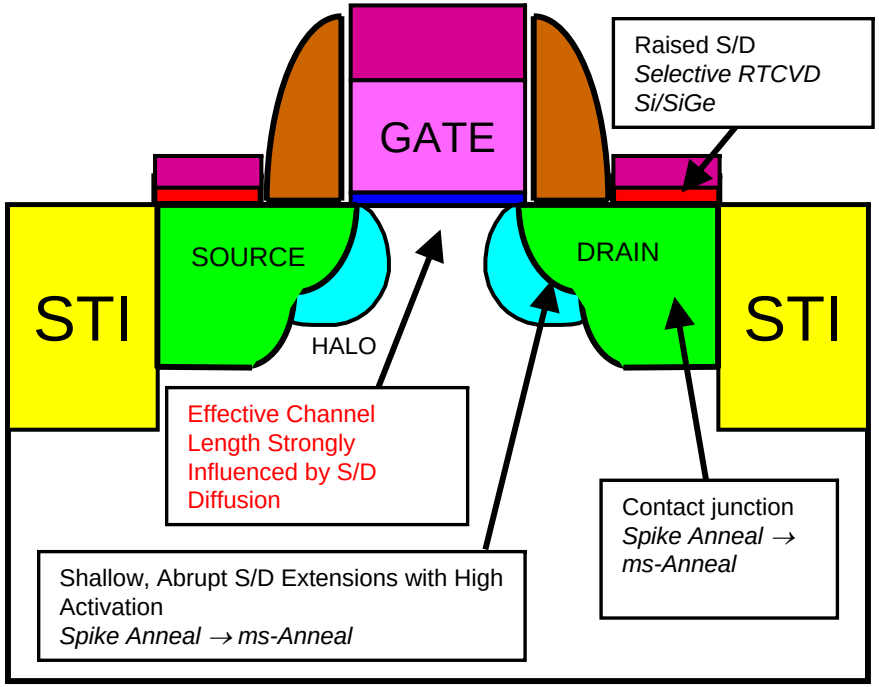
# Pattern Effects in Thermal Processing

P. J. Timans & Y. Lee

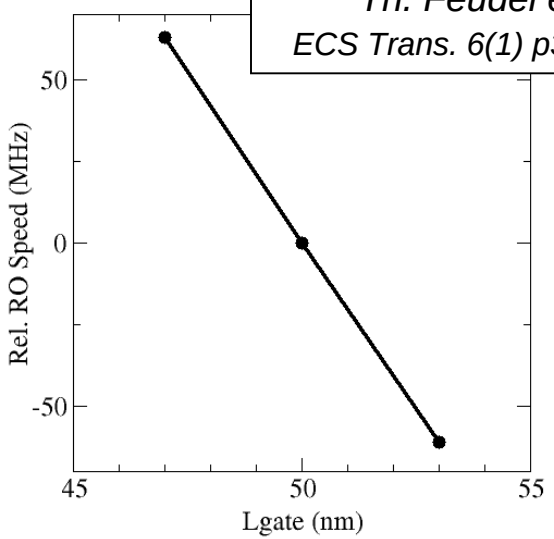
# Outline

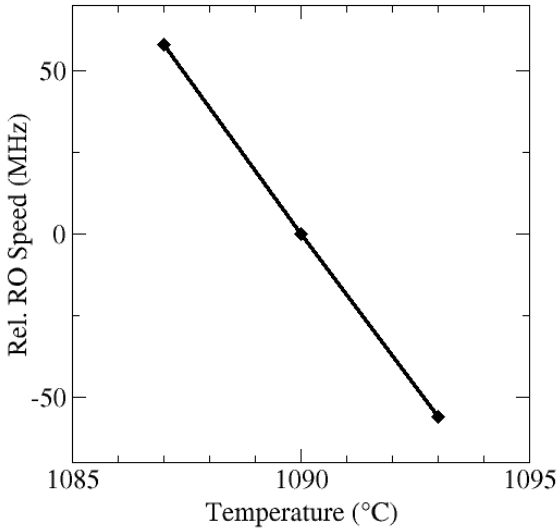
- Pattern effect impact on devices
- Physics of the pattern effect
- Solutions for the problem
- Conclusions

# Spike RTA: Critical for Device Performance



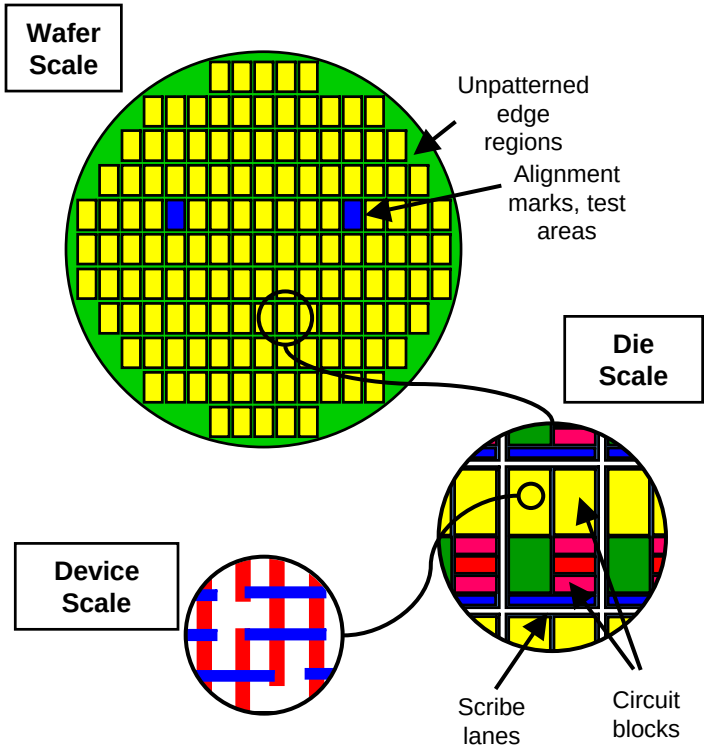

*Th. Feudel et al.*
*ECS Trans. 6(1) p373 (2007)*




- Spike RTA is a critical step:
  - Activation / Defect Annealing / Diffusion
  - Typically ~1000-1050°C for ~ 1.5 s
- 1K variation in peak T ≡ 1nm variation in gate length (at ~ 45nm node)

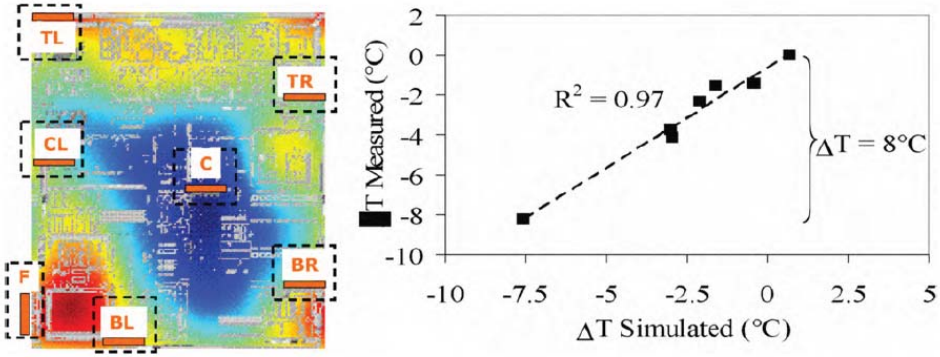
# The RTP Pattern Effect is Caused by Non-Uniform Optical Properties




- Optical properties vary with
  - Films / materials
  - Lateral structures (patterning)
- There are many length scales of non-uniformity
  - Wafer (cm)
  - Die (mm)
  - Device (μm/nm)

- Experiments & theory show that the pattern effect arises from two types of variation
  - Variation in **absorption** of heating lamp power
  - Variation in **emission** of radiant heat from the wafer

*P. Morin et al., ESSDERC 2009, p288*

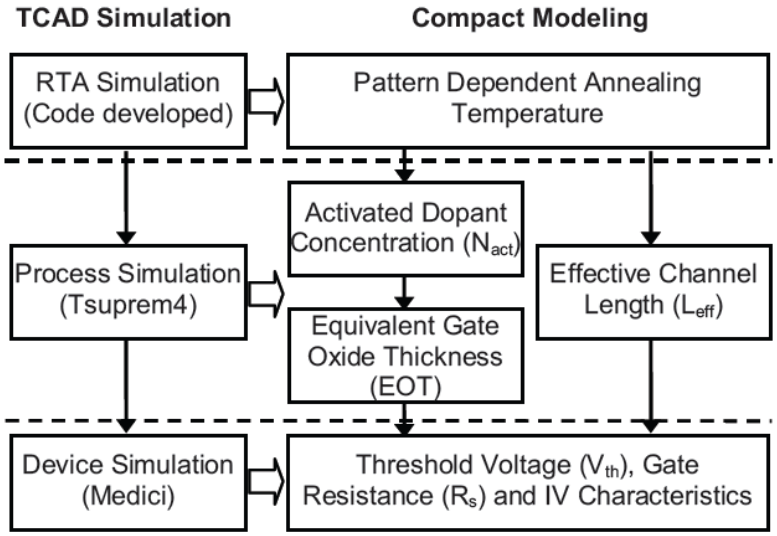


# Modelling Impact at Device Level

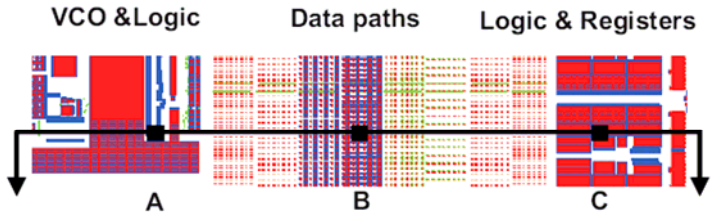
## Variability Analysis under Layout Pattern-Dependent Rapid-Thermal Annealing Process

Yun Ye[1], Frank Liu[2], Min Chen[1], Yu Cao[1]
[1]Department of Electrical Engineering, Arizona State University, Tempe, AZ 85287
[2]IBM Austin Research Laboratory, Austin, TX 78758

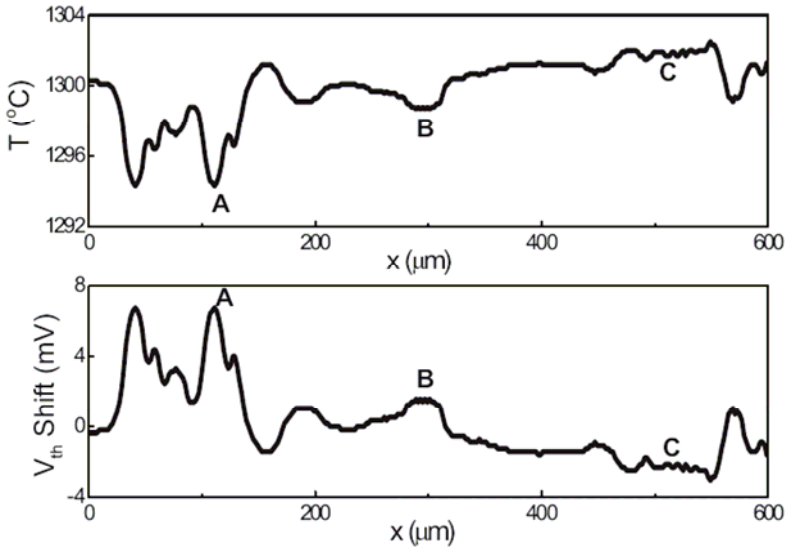
DAC'09, July 26-31, 2009, San Francisco, California, USA




- Models predict optical, thermal, process & device characteristics

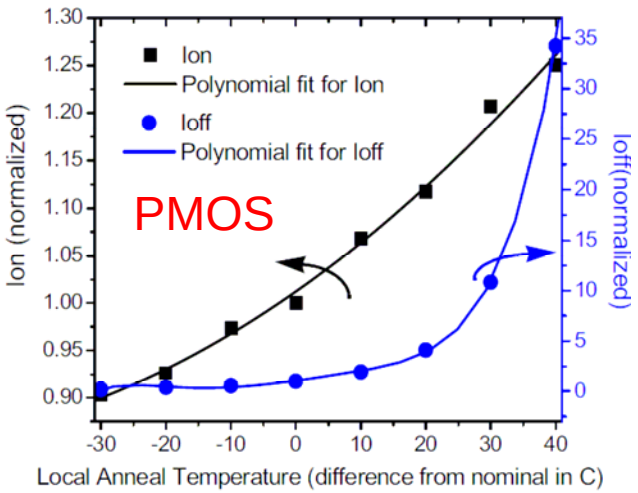


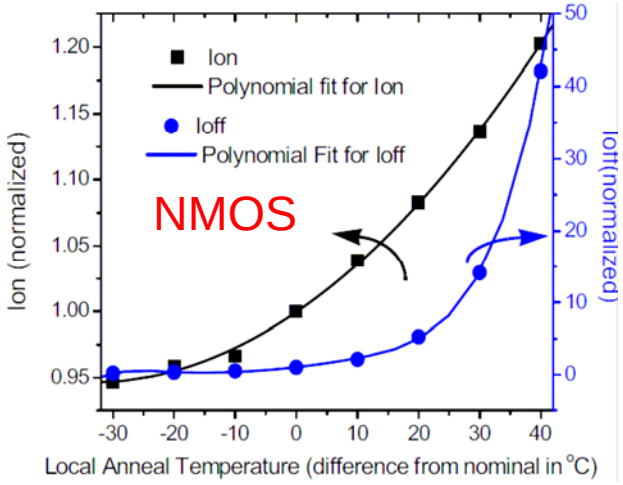

(a) Partial layout of a 45nm test chip.




(b) T and $V_{th}$ variations predicted by simulations.

# Within-Die Uniformity Predictions



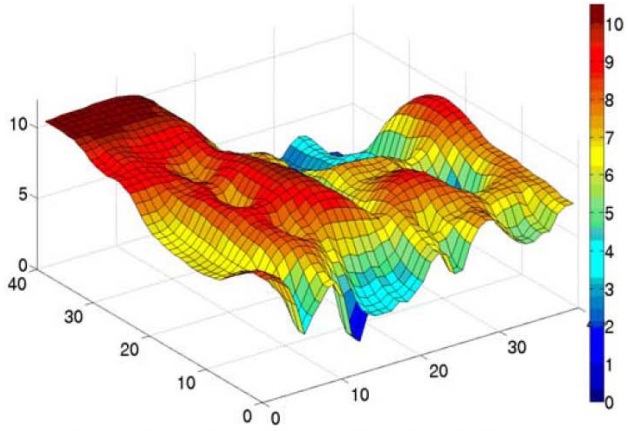



Figure 10. Local anneal temperature distribution for the 45nm chip.

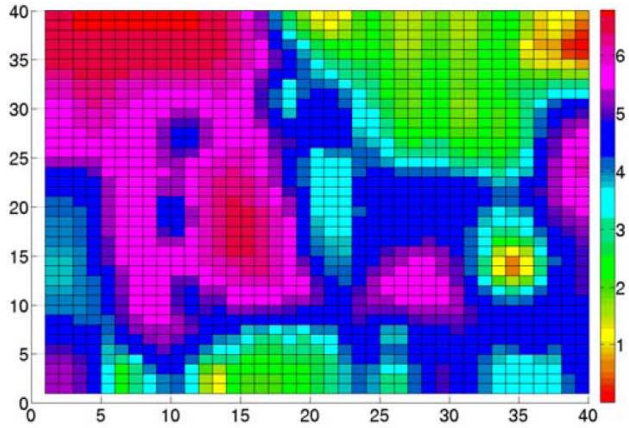


Figure 11. Ion map for the 45nm chip.

*Vivek Joshi et al., Univ. Michigan*
*Analyzing electrical effects of RTA-driven local anneal temperature variation*
*The 15th Asia and South Pacific Design Automation Conference (2010)*

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# RTP Pattern Effect: The Early Days

WAFER STRESS DURINlG RAPID THERMAL ANNEALING
DUE TO SURFACE GEOMETRICAL PATTERNS

Yasuo Ohno, Sakae Kitajo* and Ichiro Moriyama
Microelectronics Research Labs.,
and R&D Planning and Technical Service Division*,
NEC Corporation

Y. Ohno et al.: *1985 Symp. VLSI Technol. Dig. Tech. Papers* (1985), p. 86

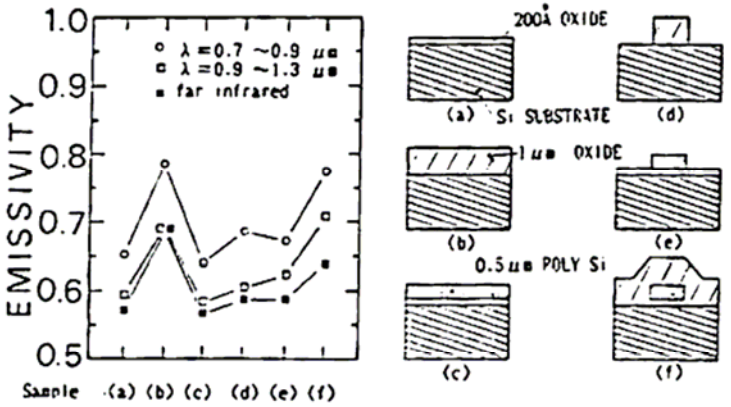
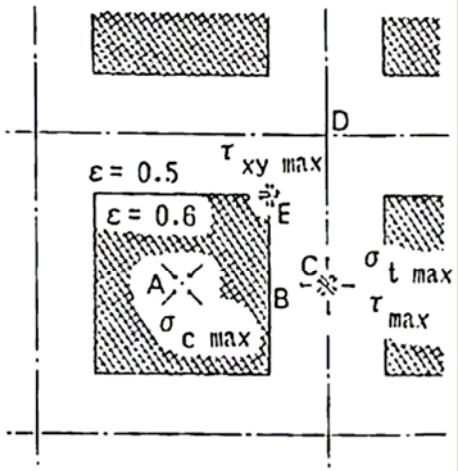
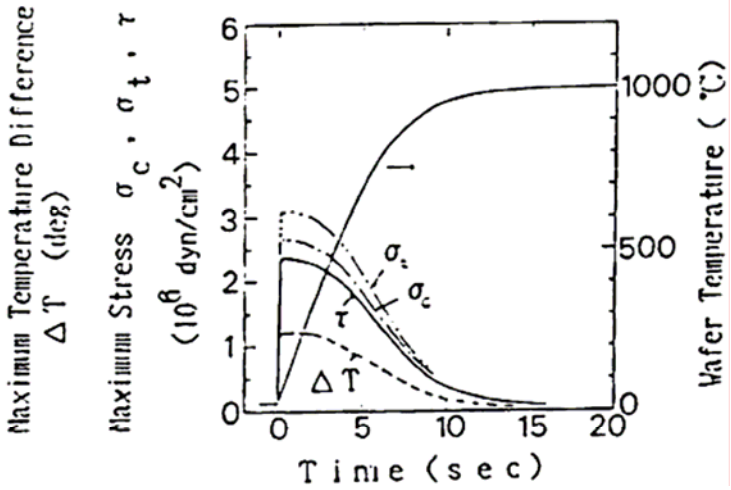


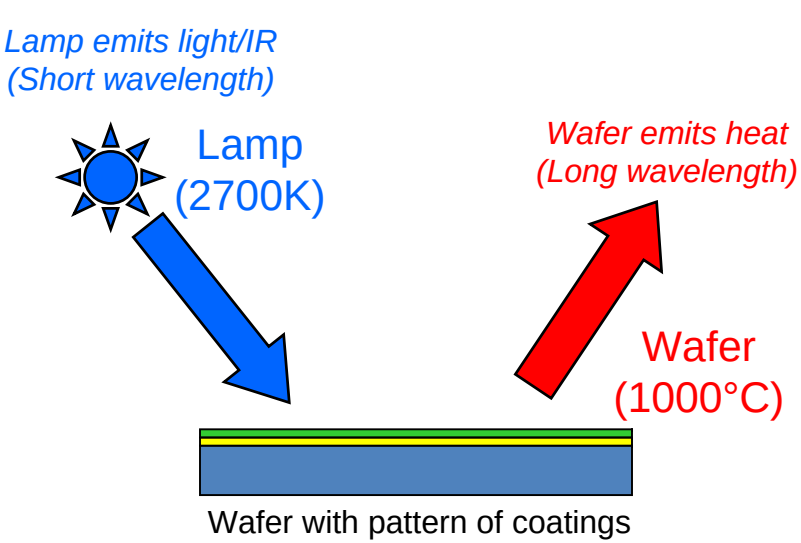

Fig.1 Surface emissivity for silicon wafers with different structures.

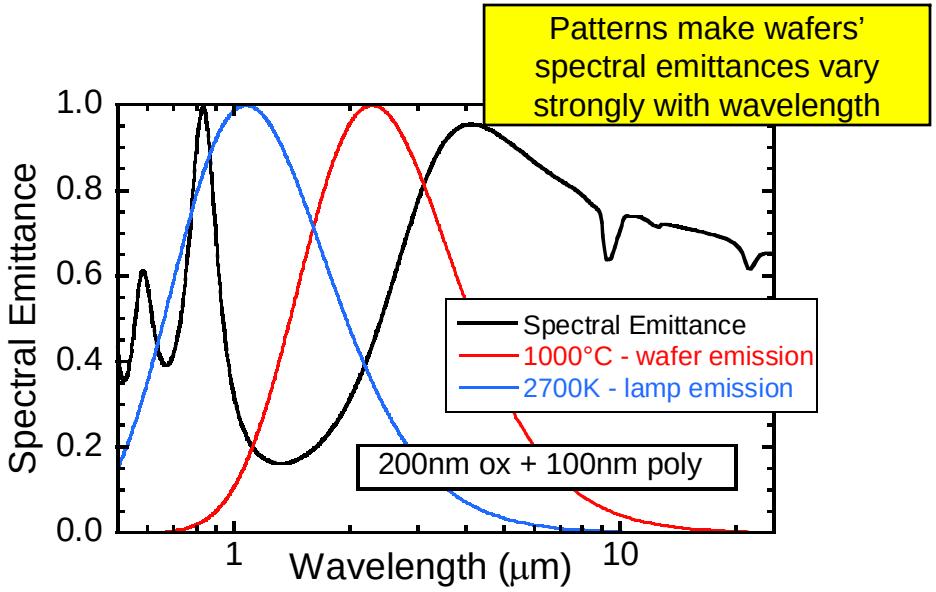



- The problems of patterns in RTP were recognized early in the development of commercial RTP

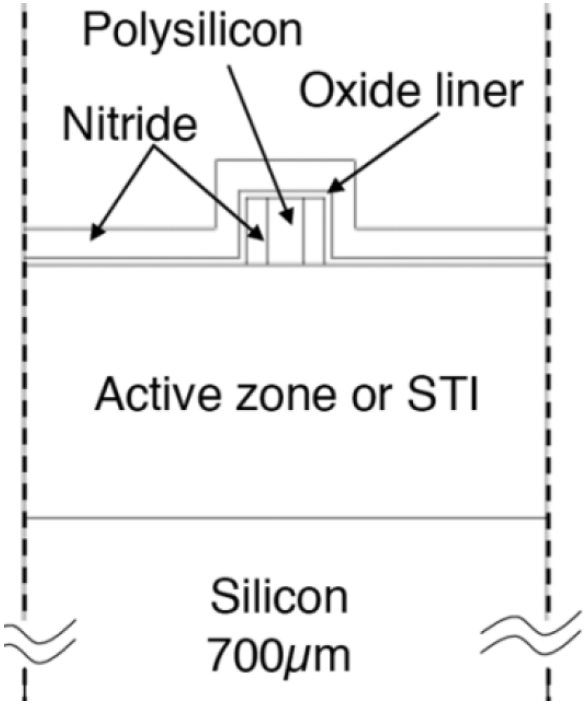
# Effect of Surface Optical Properties on Heat Transfer

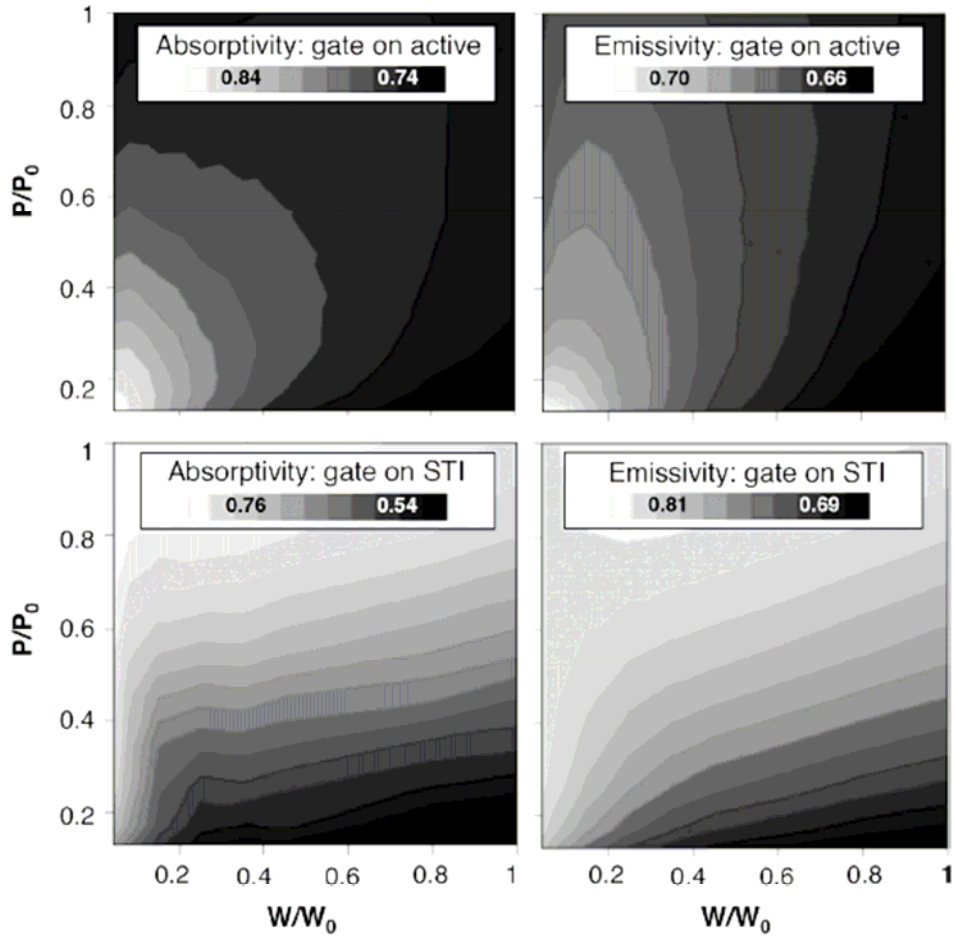



- Spectral emittance affects the energy emitted or absorbed at any given wavelength
  - $\varepsilon(\lambda) = a(\lambda)$ (Kirchhoff's law)
  - On wafers, patterns & films make $\varepsilon(\lambda) \neq$ constant
- To calculate total lamp power absorbed
  - Integrate $\varepsilon(\lambda)$, weighted by lamp spectrum (short $\lambda$) $\Rightarrow$ Total Absorptance, $a_{tot}$
- To calculate total heat radiated
  - Integrate $\varepsilon(\lambda)$, weighted by wafer's thermal emission spectrum $\Rightarrow$ Total Emittance, $\varepsilon_{tot}$

# Wafer Coatings and Patterning Affect Optical Properties

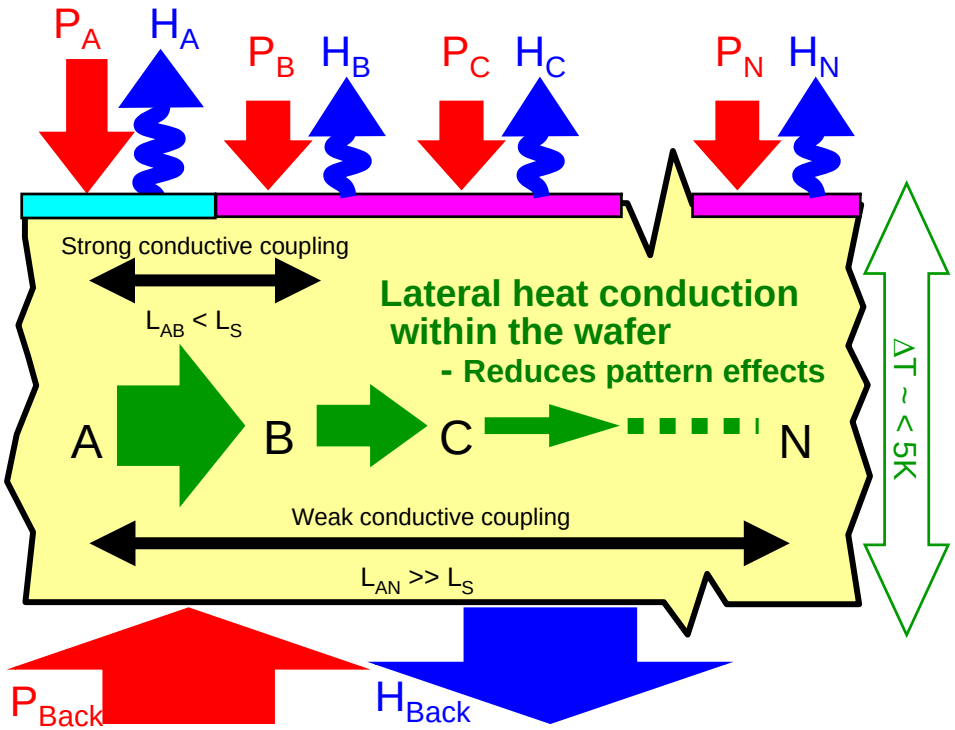


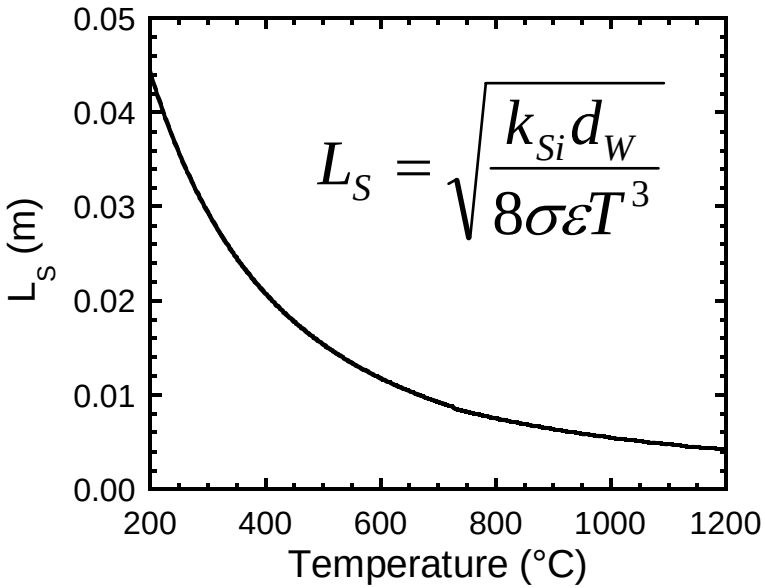




- Data from "*Investigation of Pattern Effects in Rapid Thermal Processing Technology: Modeling and Experimental Results*", F. Cacho et al., IEEE Trans. On Semiconductor Manufacturing, 23(2), 2010
- Parametric study of effect of gate width (W) and space between gates (P) covers wide range of conditions

# Lateral Heat Flow Limits the Magnitude of Pattern-Induced ΔT

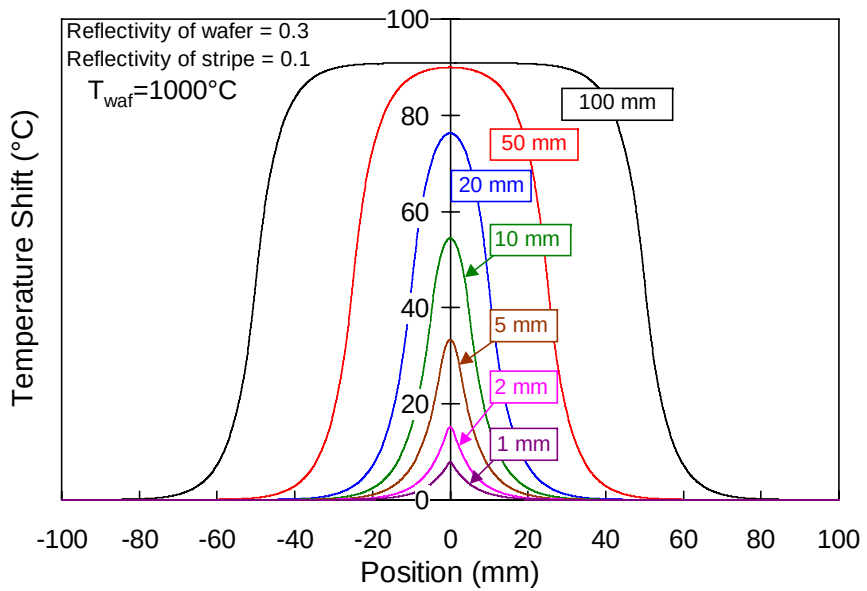
**Energy flows into and out of the surfaces of the wafer**
**⇒ Non-uniformity causes pattern effects**

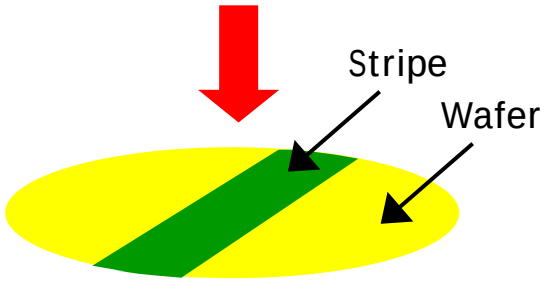


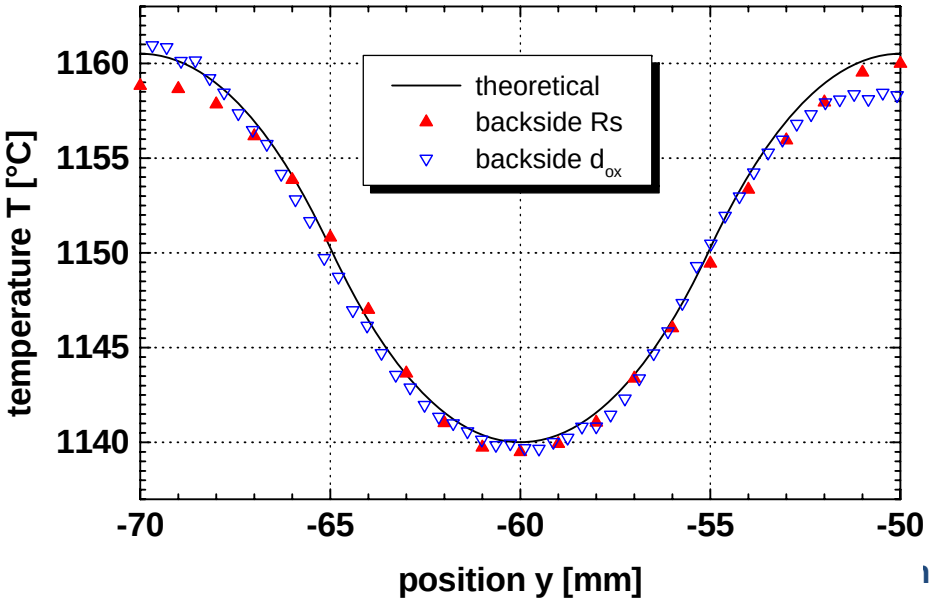

- A characteristic length-scale, $L_S$, defines the minimum size of pattern that causes significant ΔT
- $L_S$ depends on:
  - Rate of lateral heat transfer
  - Heat flow through surfaces

# The Effect of a Stripe of Absorbing Material on ΔT



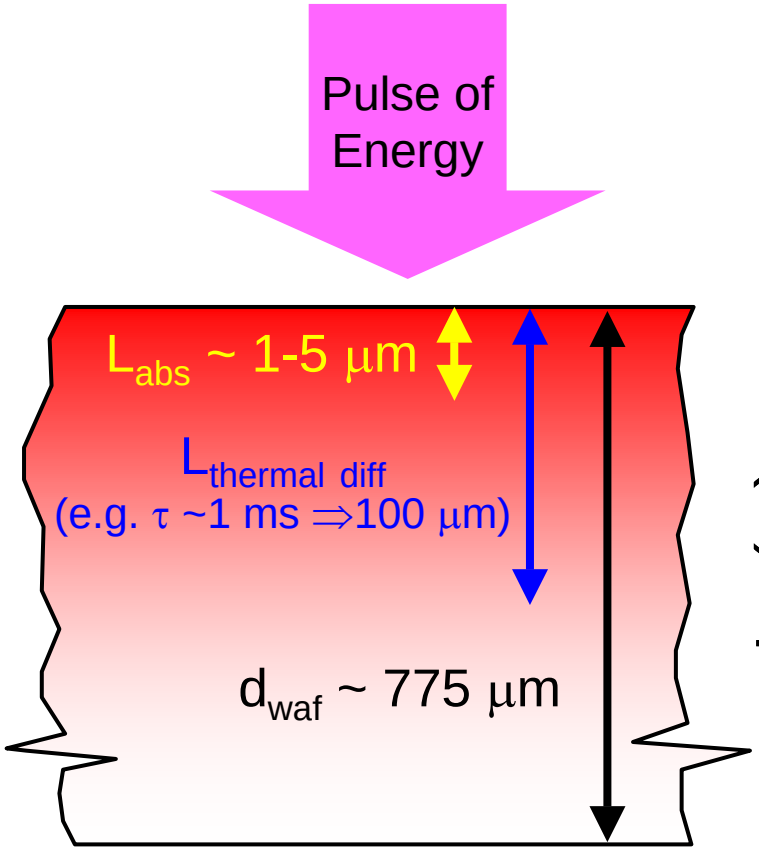




- ΔT caused by a stripe of material with higher lamp power coupling
- Thermal conduction makes ΔT decrease with feature size
- For large feature sizes thermal conduction has no effect on ΔT
- Experimental RTO & RTA studies show good agreement with the theory



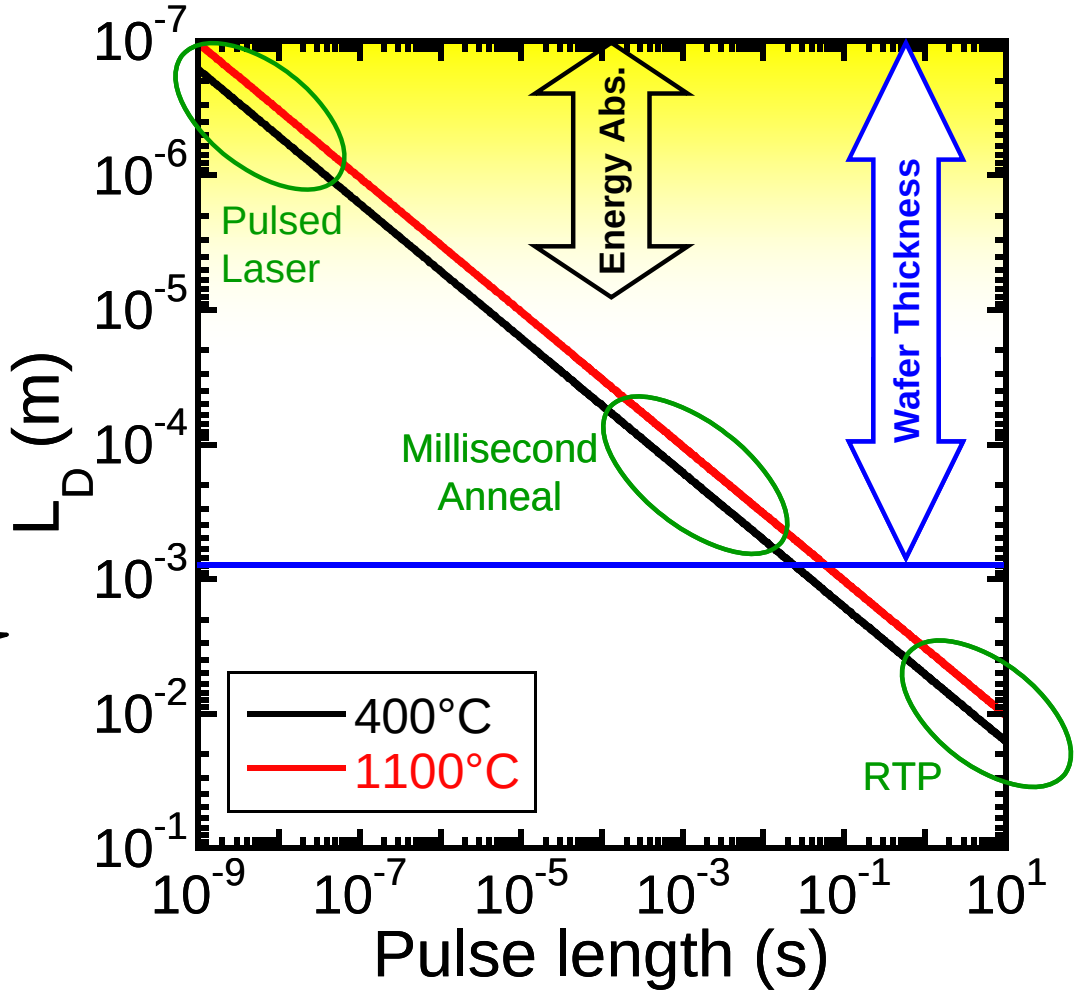

"Pattern Effects and how to Explore Them", J. Niess et al., in *10th International Conference on Advanced Thermal Processing of Semiconductors*, p. 49 (2002)

# Pulsed Heating: Surface Heating Regime
# ⇒ Length Scale << Wafer Thickness

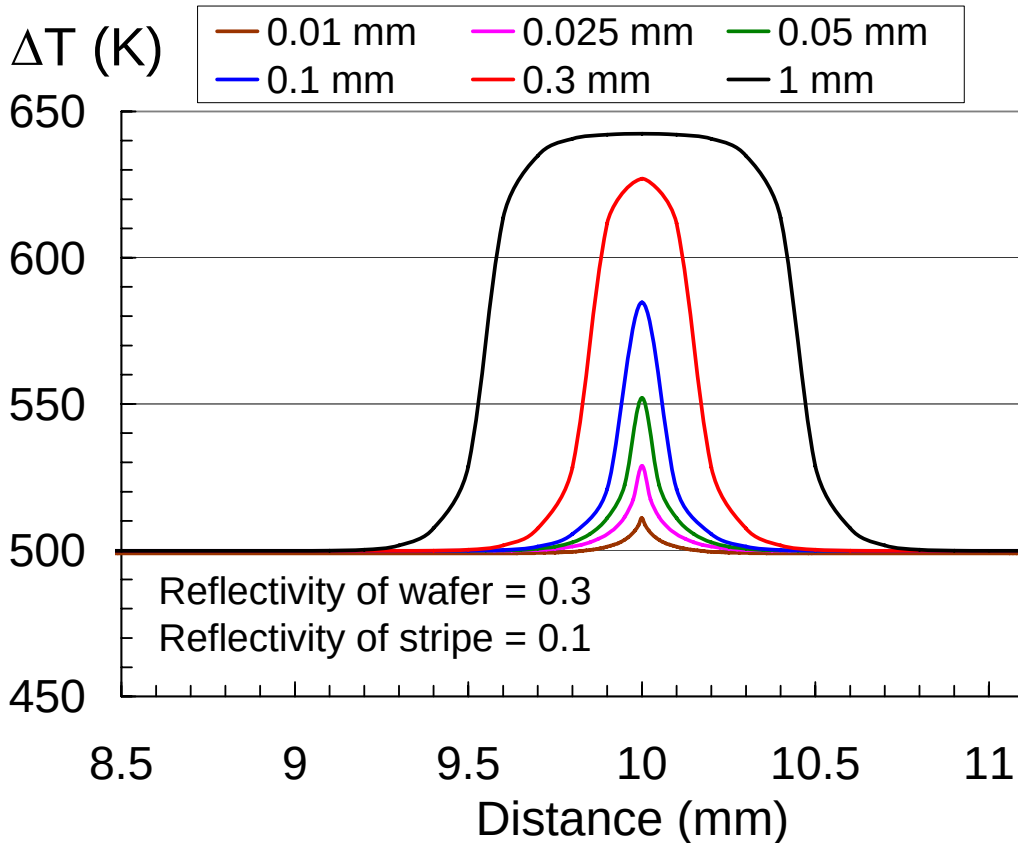


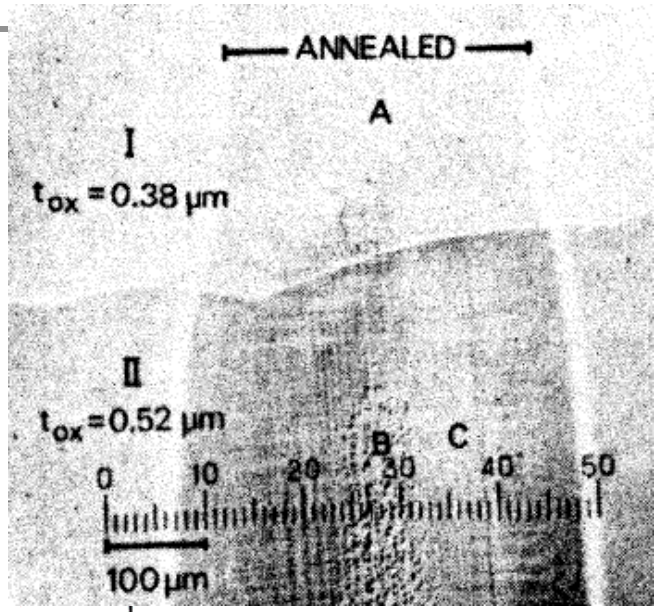

**Three Key Length-Scales**

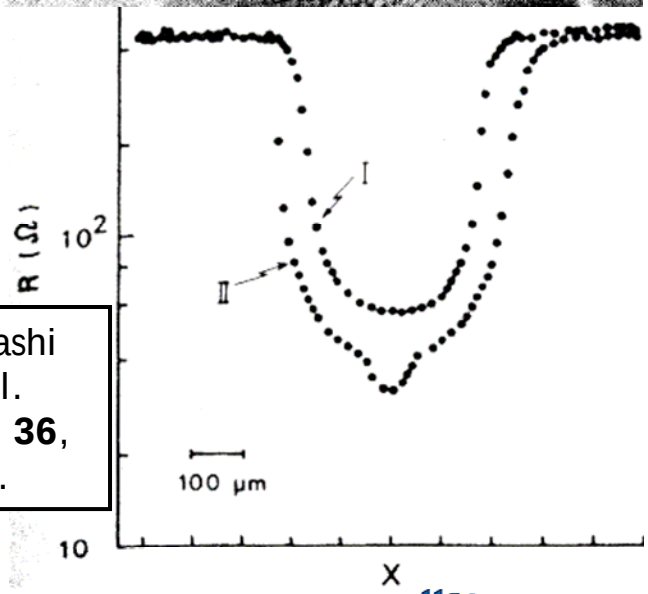
$$L_D = \sqrt{Dt_{pulse}}$$



# Short $L_D$ in ms ⇒ Large ΔT Over Short distance



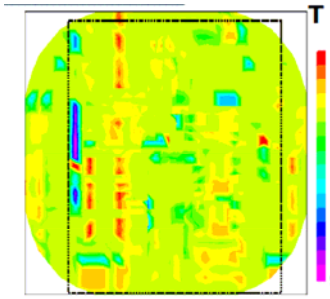




Heat has less time to diffuse in ms-anneal than in RTP

⇒ pattern effects emerge at shorter length scales: ~ 10 μm

H. Okabayashi et al., Appl. Phys. Lett. **36**, (1980) 202.

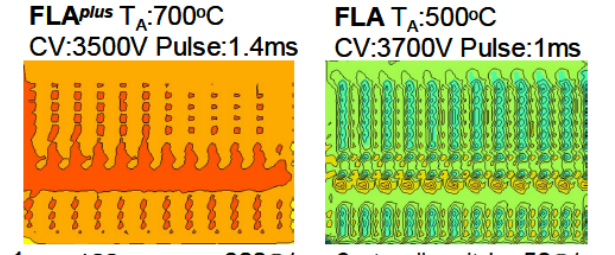
# Pattern Effects in Millisecond Annealing

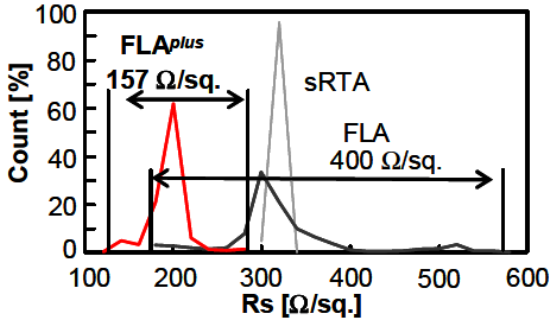



**Main remarks**
- **Cold line = cut way**
- **Local hot spots with temperature close to 1300°C → high stress**
- **not perfect technique need more accuracy (measure step 1mm)**

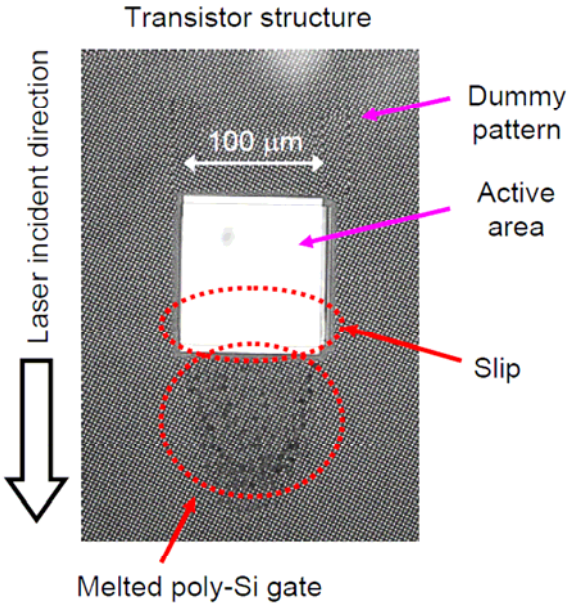
**Intradie temperature variation around 250°C**

*R. Beneyton et al., ST Microelectronics - RTP2008*




*S. Kato, SELETE - IWJT 2010*




After annealing at about 1350 °C by LSA

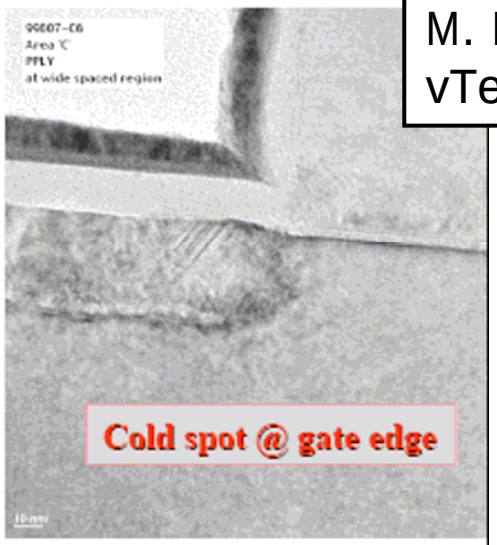
*T. Kubo., Fujitsu - RTP2008*

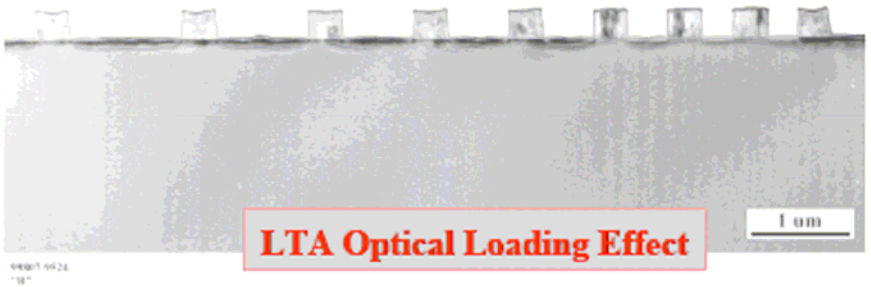
- High powers & short pulse lengths can cause large lateral ΔT in MSA
- Laser scanning pattern effects can also depend on scan direction
- Fortunately, in MSA, the process window tends to be large (very small amount of dopant diffusion)

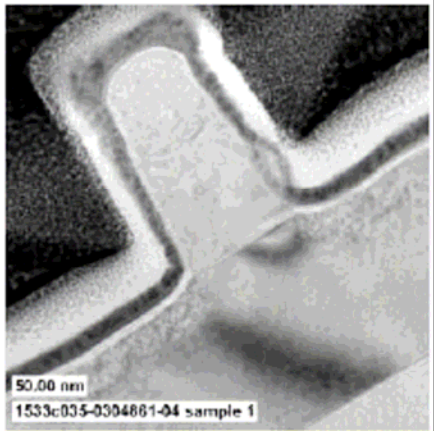
# Pattern Effects in Pulsed Laser Anneal

- At very short time-scales (sub-μs), $L_D < L_{abs}$: "Adiabatic" heating
- $\Delta T$ evolves where energy is absorbed (in all 3 dimensions)


M. Mansoori, vTech 2002

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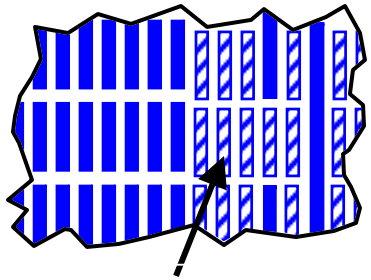
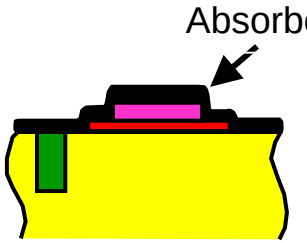
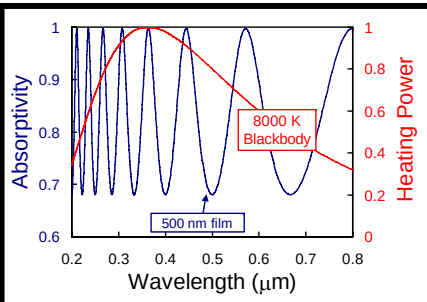
# How to Manage the Pattern Effect?

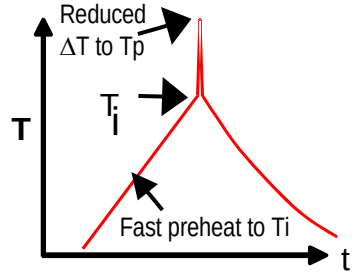


Dummy features

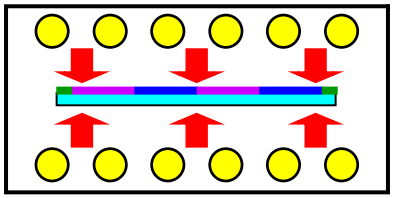


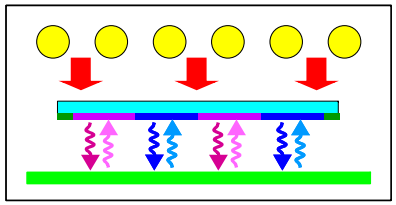

Spectral Averaging



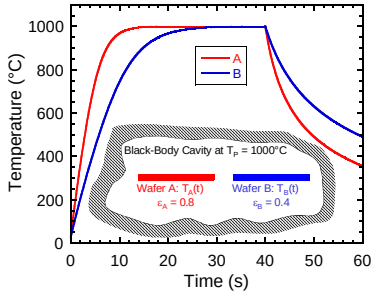

New processing methods



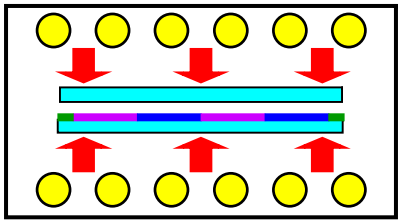
Double-sided Heating (& Asymmetric heating)



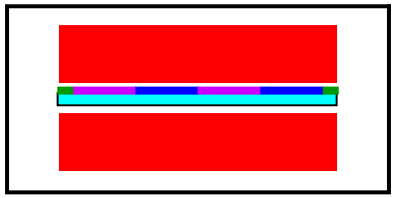
Reducing heat transfer through patterned surface



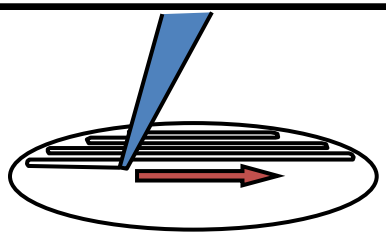

≅ Radiative Equilibrium



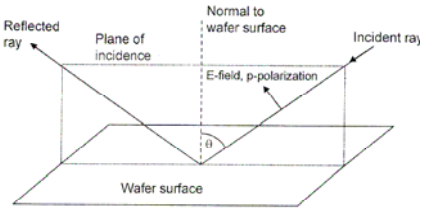
"Hot Shielding"



Conductive Heating



Non-Optical Energy Beams

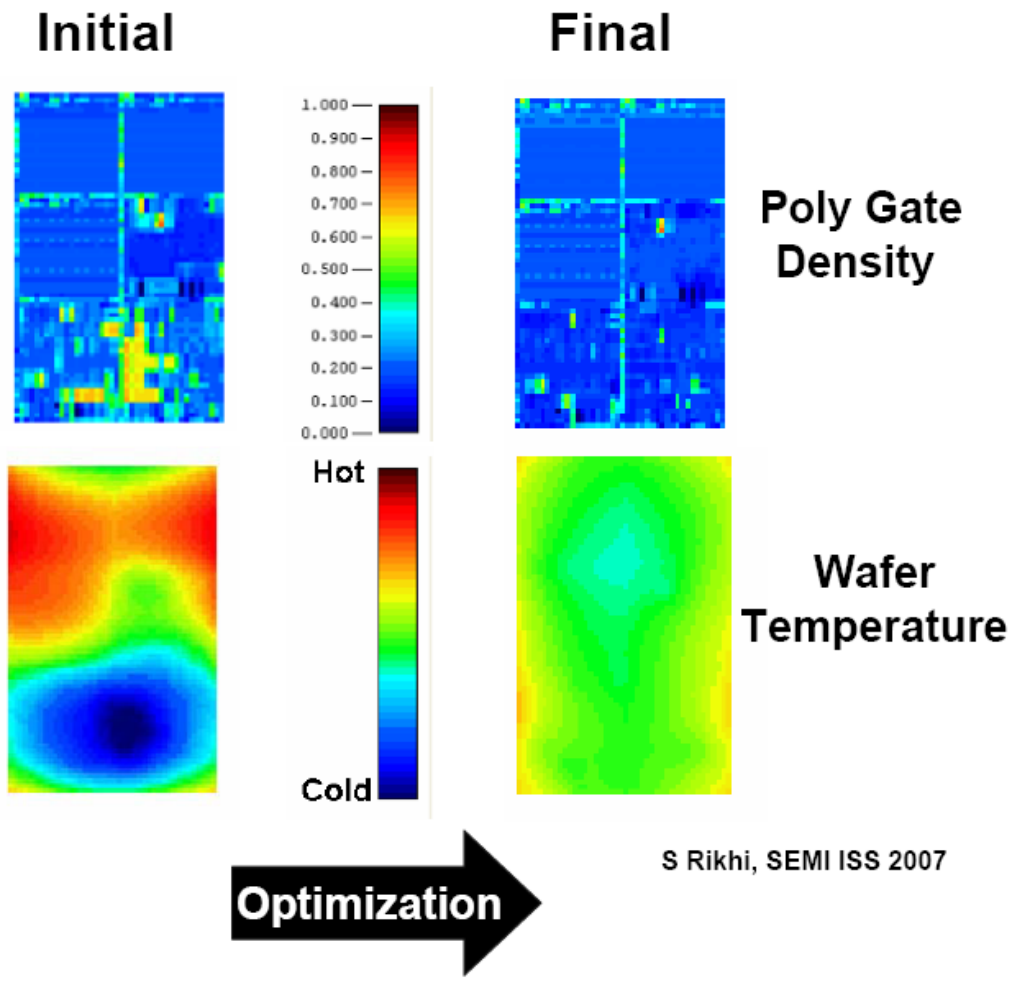



Special Illumination Conditions: θ, pol.

- There are many possible paths!

# Intel: Reducing Pattern Effects with Poly-Dummies

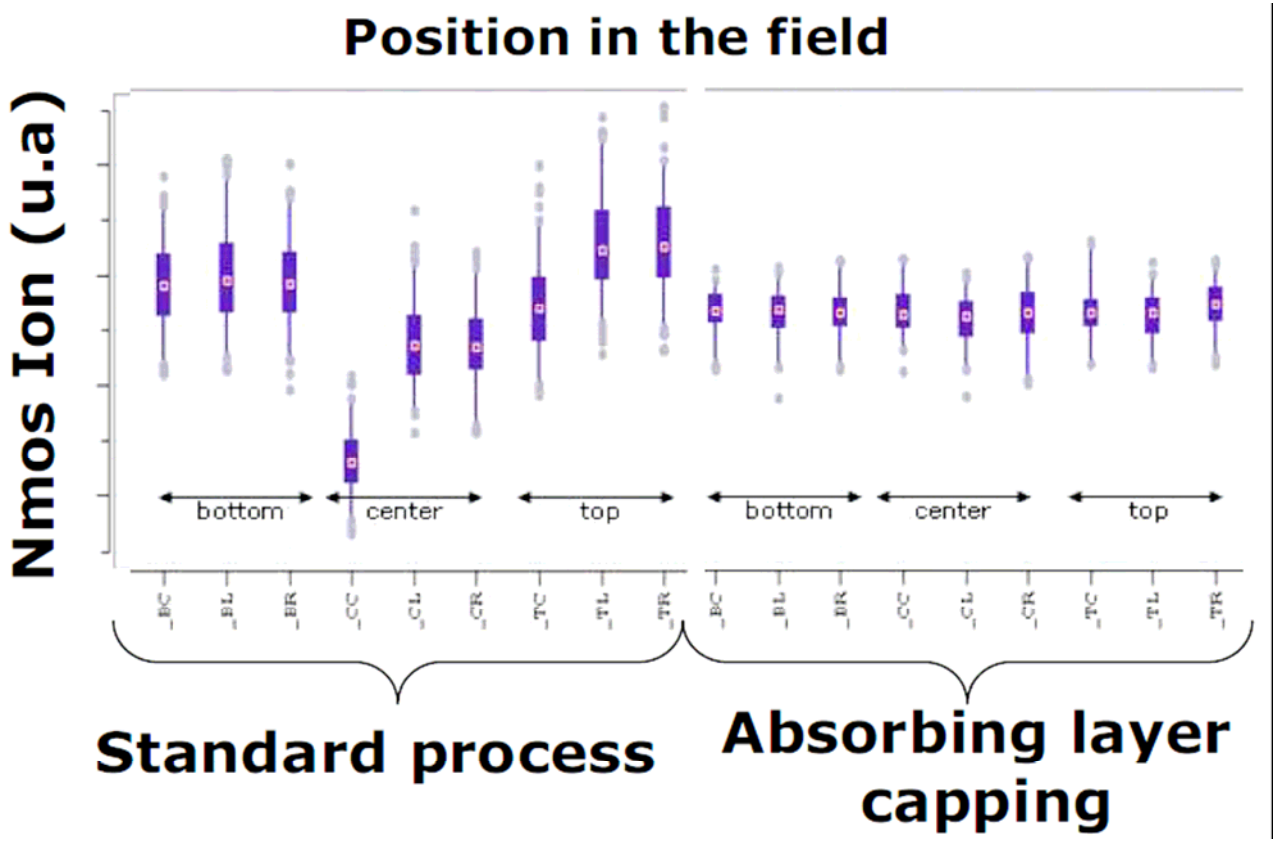
- Temperature non-uniformities can directly impact Le
- Similar effects can be seen for other process steps such as deposition and polish
- Adds to device variation
- Modeling effects critical to correct optimization




S Rikhi, SEMI ISS 2007

- From: IEDM 2007 Short Course on CMOS Boosters (Paul Packan, Intel)

# An Absorber Layer Can “Hide” the Pattern




*R. Beneyton et al., ST Microelectronics*
*Origin of local temperature variation during spike anneal and millisecond anneal*
*16th IEEE International Conference on Advanced Thermal Processing of Semiconductors - RTP2008*

# The Process Recipe Could Be Modified

*I. Ashan et al., Advanced Semiconductor Manufacturing Conference, 2009. ASMC '09. IEEE/SEMI*

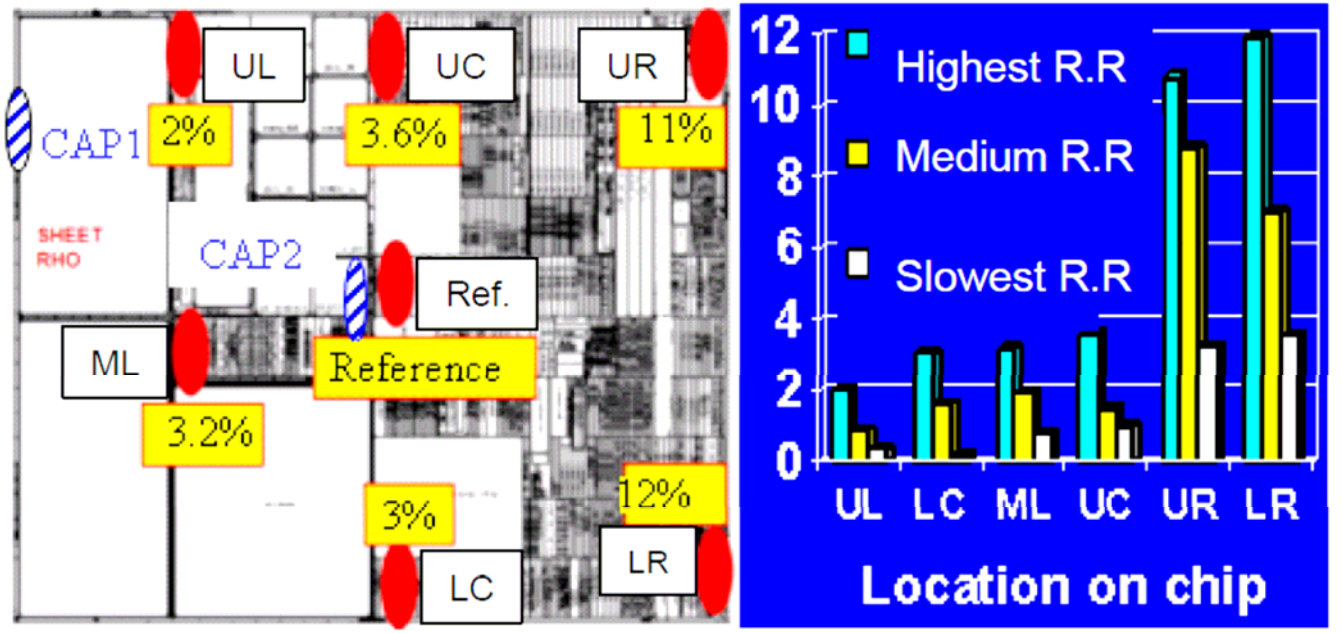
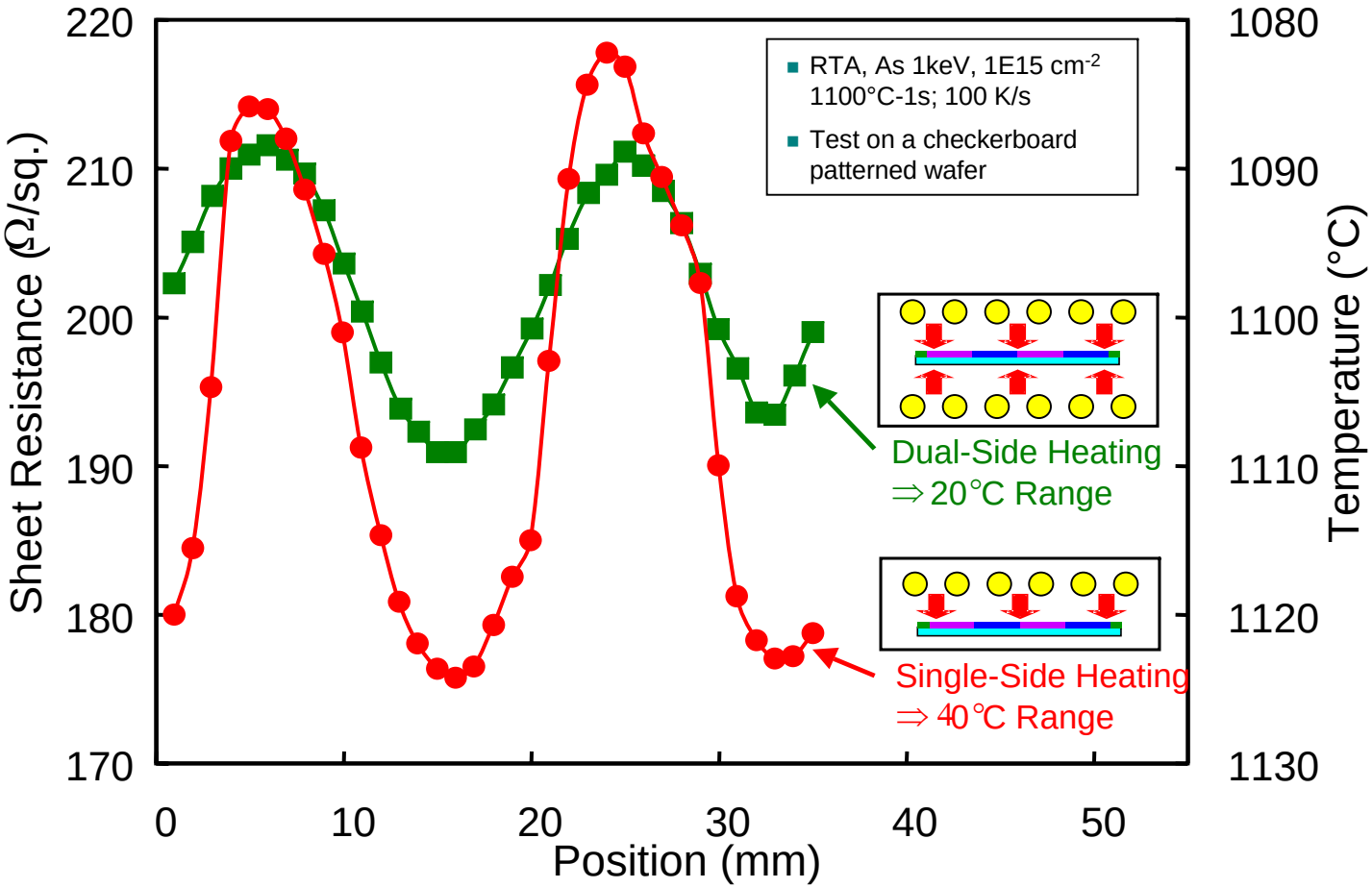



Fig. 2. Description of the test-structures in the test-chip and the degree of poly-silicon RS variation due to thermal variation

- By reducing the spike anneal ramp rate, the effect of variations in absorbed lamp power is reduced

# RTP Configuration Determines Pattern Effect ΔT




– Single-sided illumination of patterned surface
  - All the lamp power is incident on the pattern ⇒ **Maximum ΔT**

– Dual-sided illumination
  - Split the lamp power between the surfaces ⇒ **Significantly reduced ΔT**

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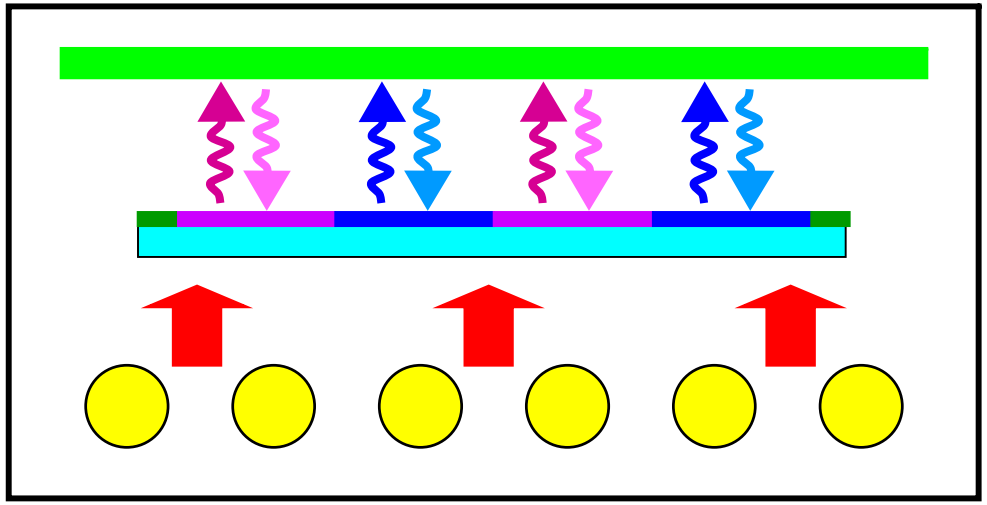
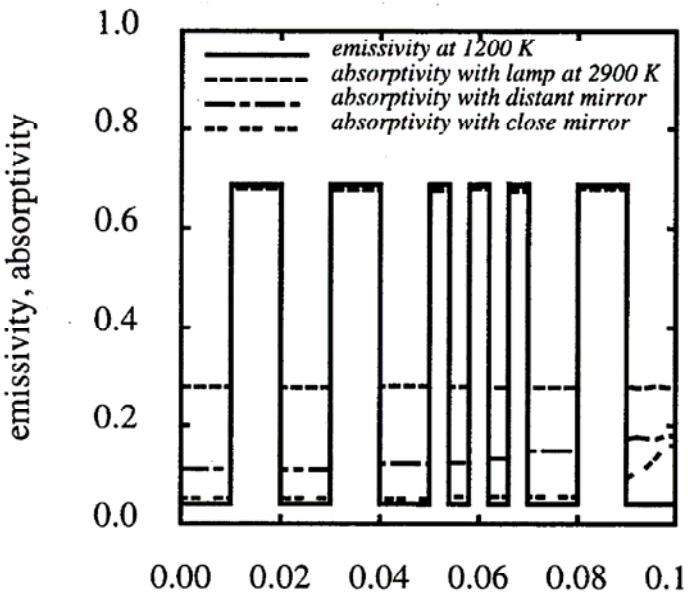
# Backside Heating & Frontside Radiative "Insulator"

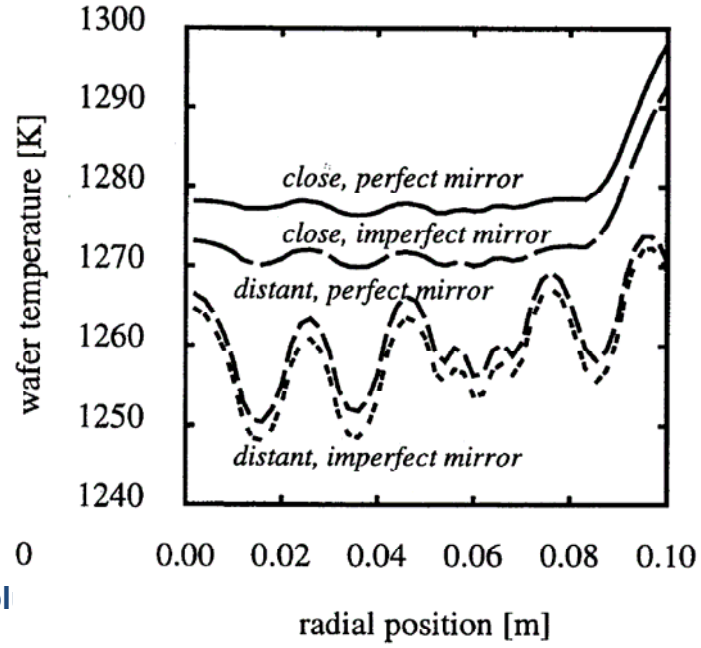




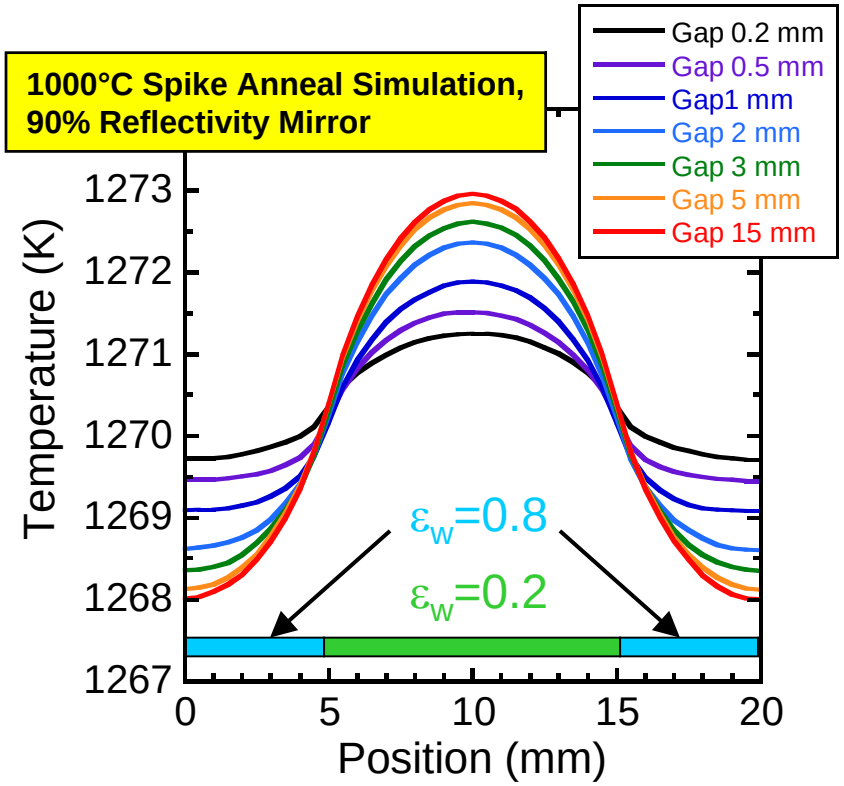

Limitations:

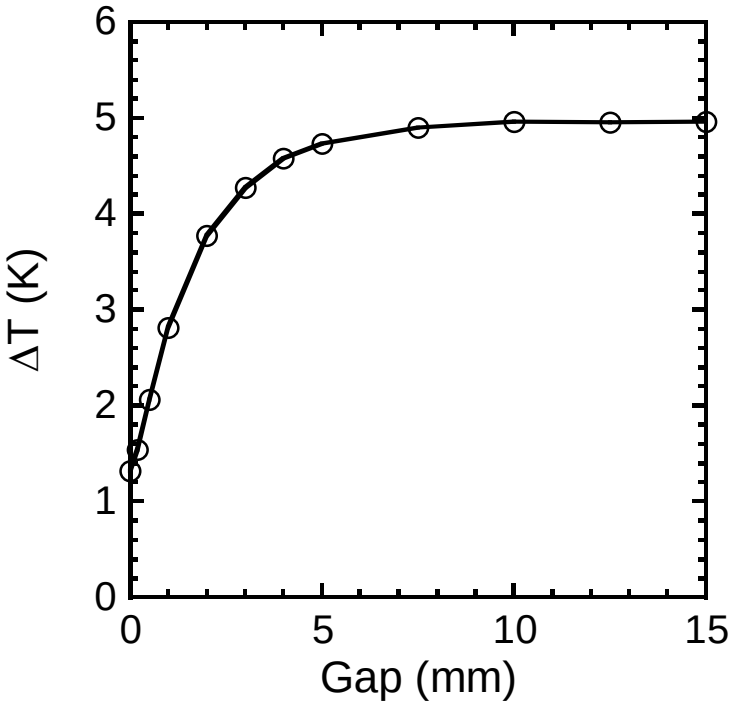
- –Only works with mirror very close to wafer
- –Cooling rate decreases
- –T measurement integration
- –Wafer support is a difficult challenge

*A. Kersch et al., MRS Symp. Proc. 429 (1996), p. 71*



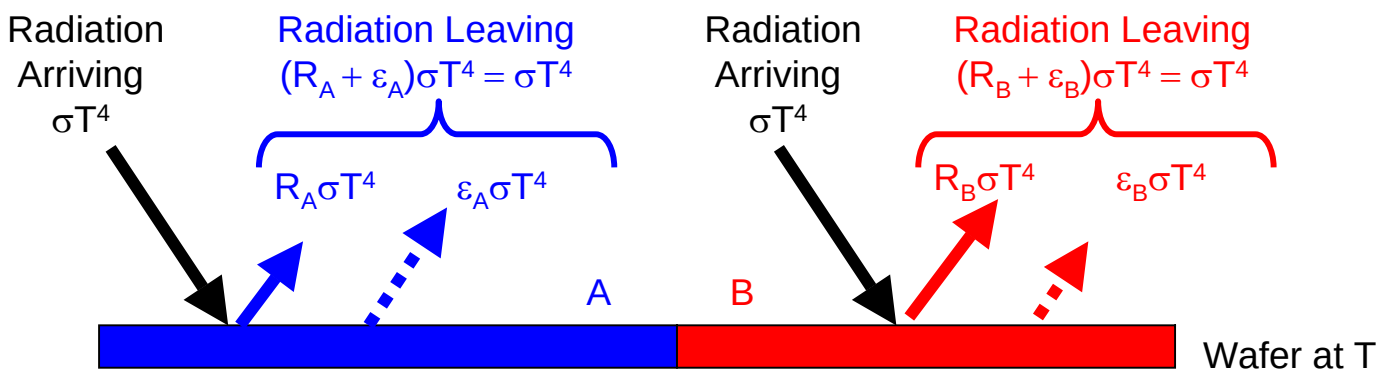
# Limitation of Front-Side Mirror Approach



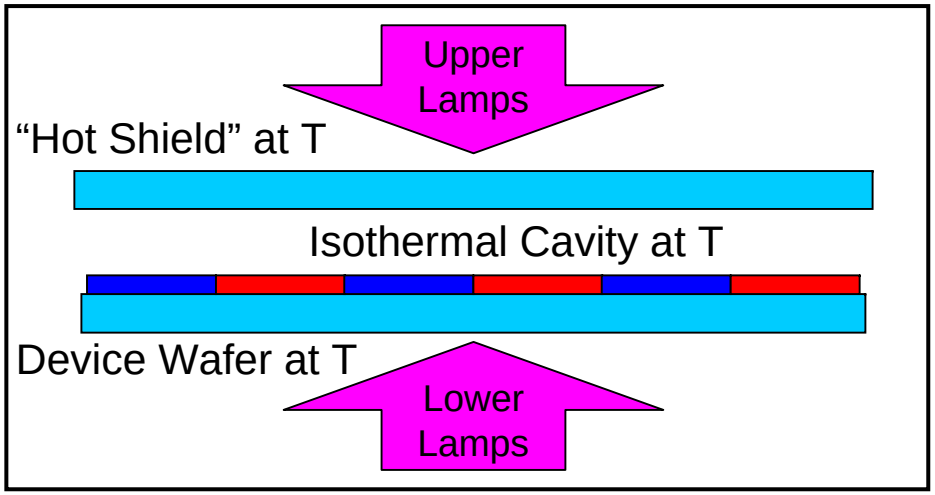




- Pattern effect suppression becomes less effective once the mirror is further away than the length scale of the pattern on the wafer
- However, bringing the mirror closer than ~ 3 mm risks wafer warping from conduction-driven thermal runaway

# Hot-Shielding: Creating a Dynamic "Hot Wall"

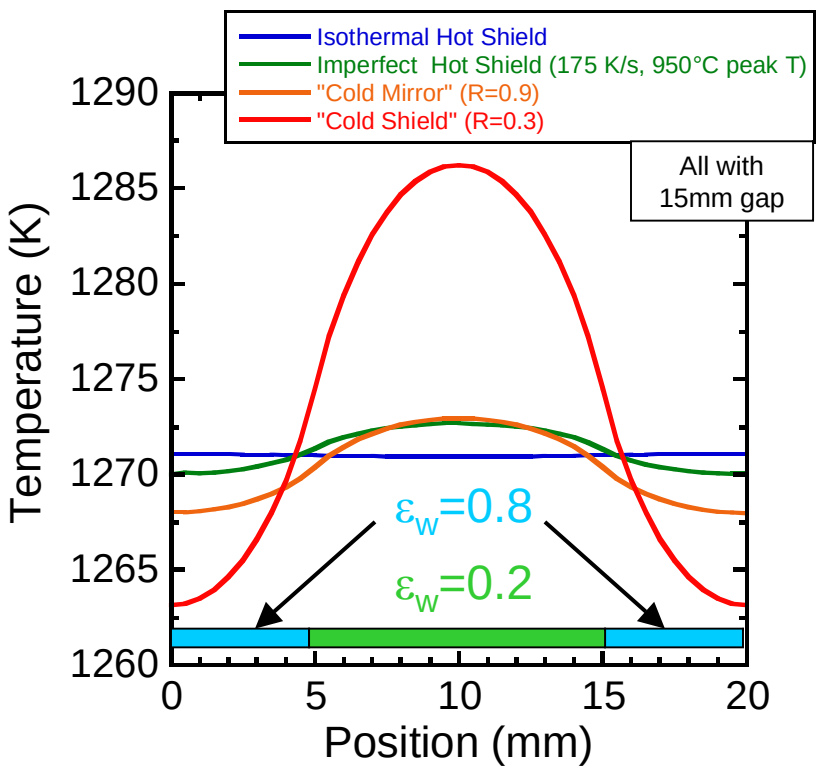


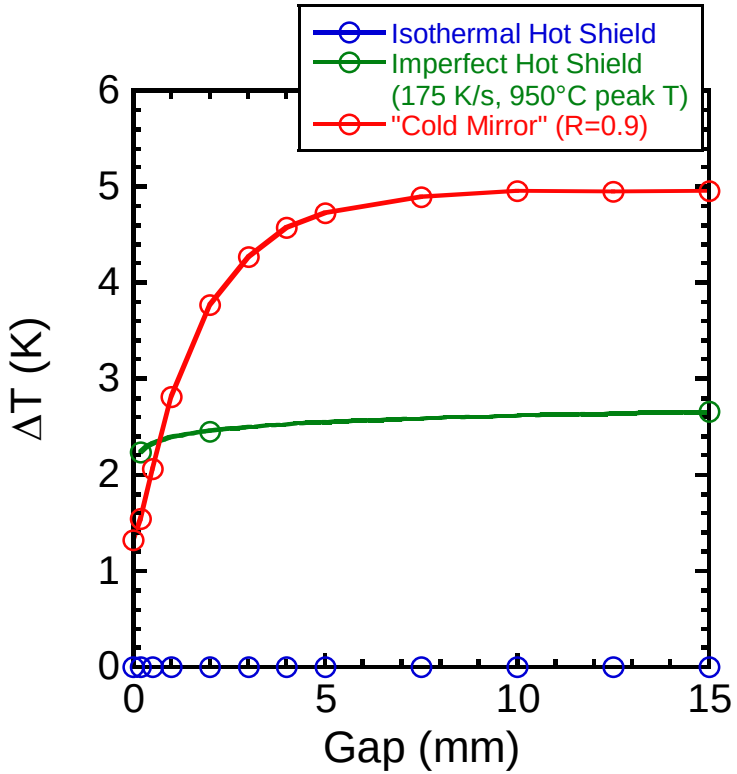

**For an isothermal cavity ("hot wall" environment):**
Radiation Arriving = Radiation Leaving = Blackbody radiation
**Regardless of Optical Properties**




Hot Shield + Device Wafer form isothermal cavity
⇒ Pattern effects vanish

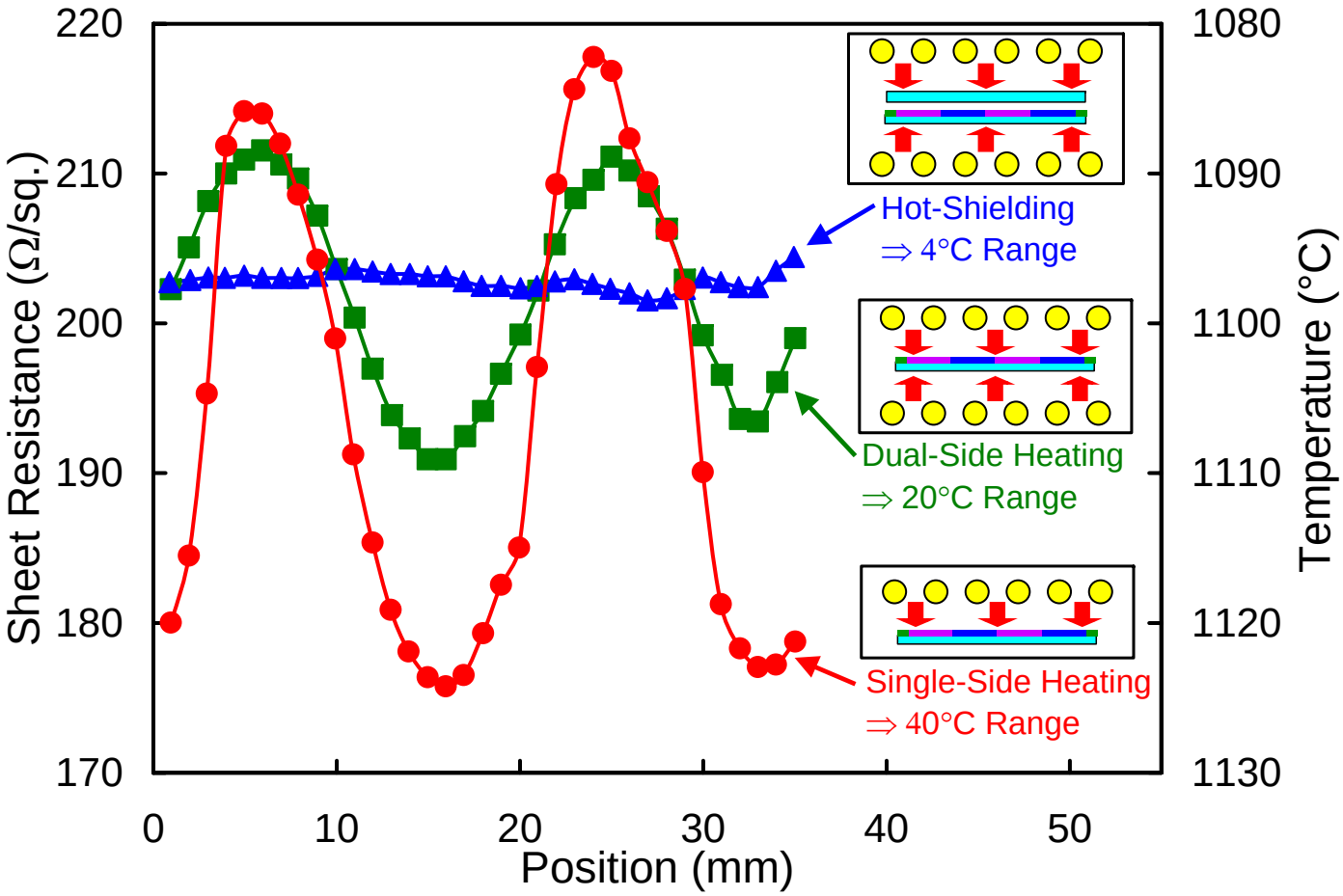
# Hot-Shielding: Isothermal Cavity Robustly Eliminates Effects of Optical Properties & Geometry




- Spike Anneal Simulations (200K/s from 600 to 1000°C)
- Perfect Hot Shield ⇒ **No Pattern Effect**
  - If the Hot Shield only reaches 950°C (when wafer is at 1000°C) then ΔT ~ 2.5 K
- Hot Shield Operation is independent of gap size

# “Hot Shielding” – A Uniquely Flexible Approach for Eliminating the Pattern Effect

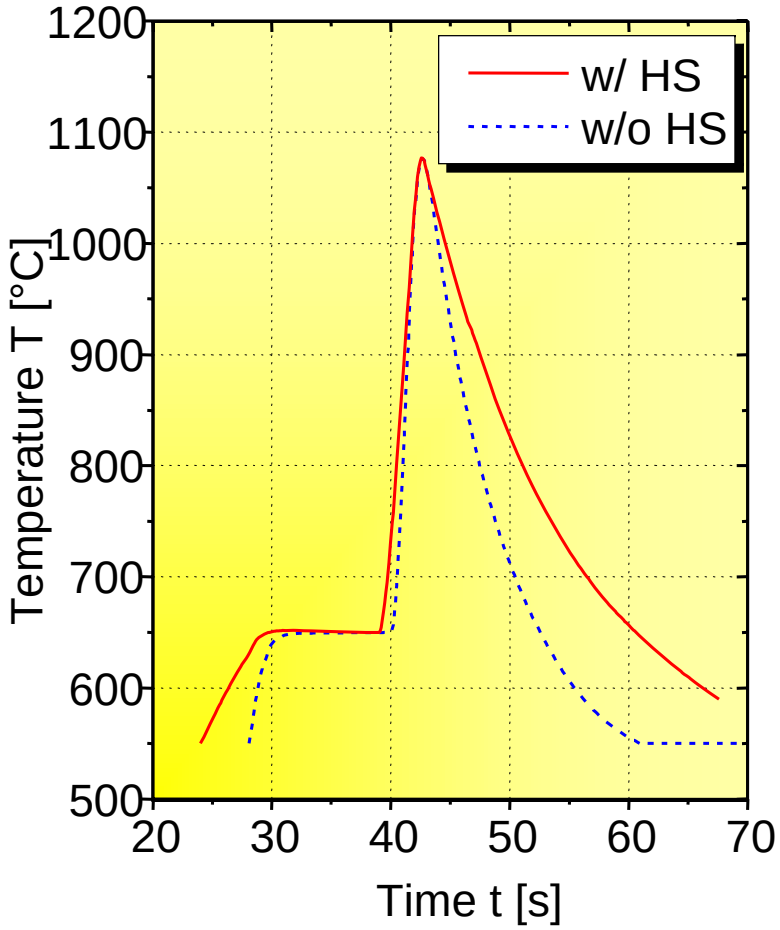


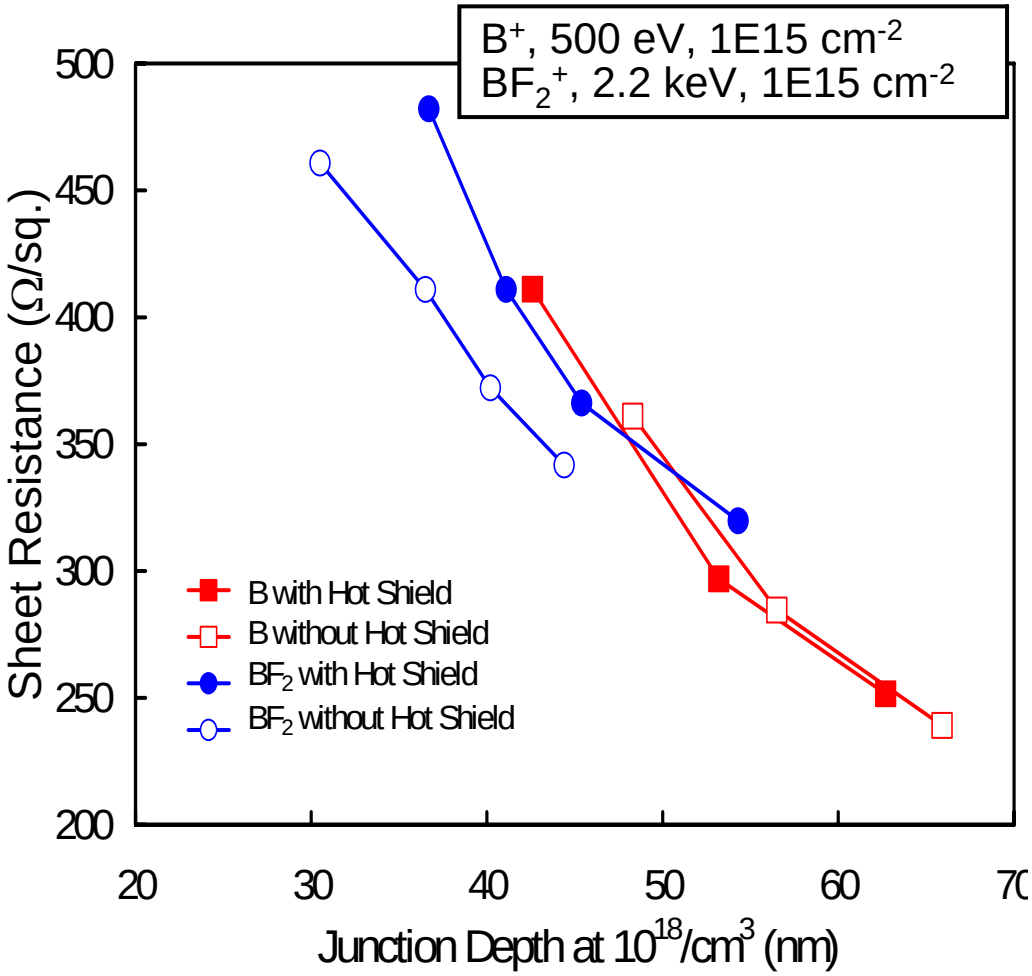

*“Logic in RTP”*, L. H. Nguyen, W.Dietl, J. Niess, Z. Nenyei, S.P. Tay, G. Obermeier, D.F. Downey, RTP’99, Colorado Springs (1999), p. 26

Hot Shield ⇒ Local thermal equilibrium between wafer and “dynamic hot wall”

**⇒ No pattern effect + Preserves Full Flexibility of RTP**

# Effect of Hot-Shielding on Spike Profiles & Process Results



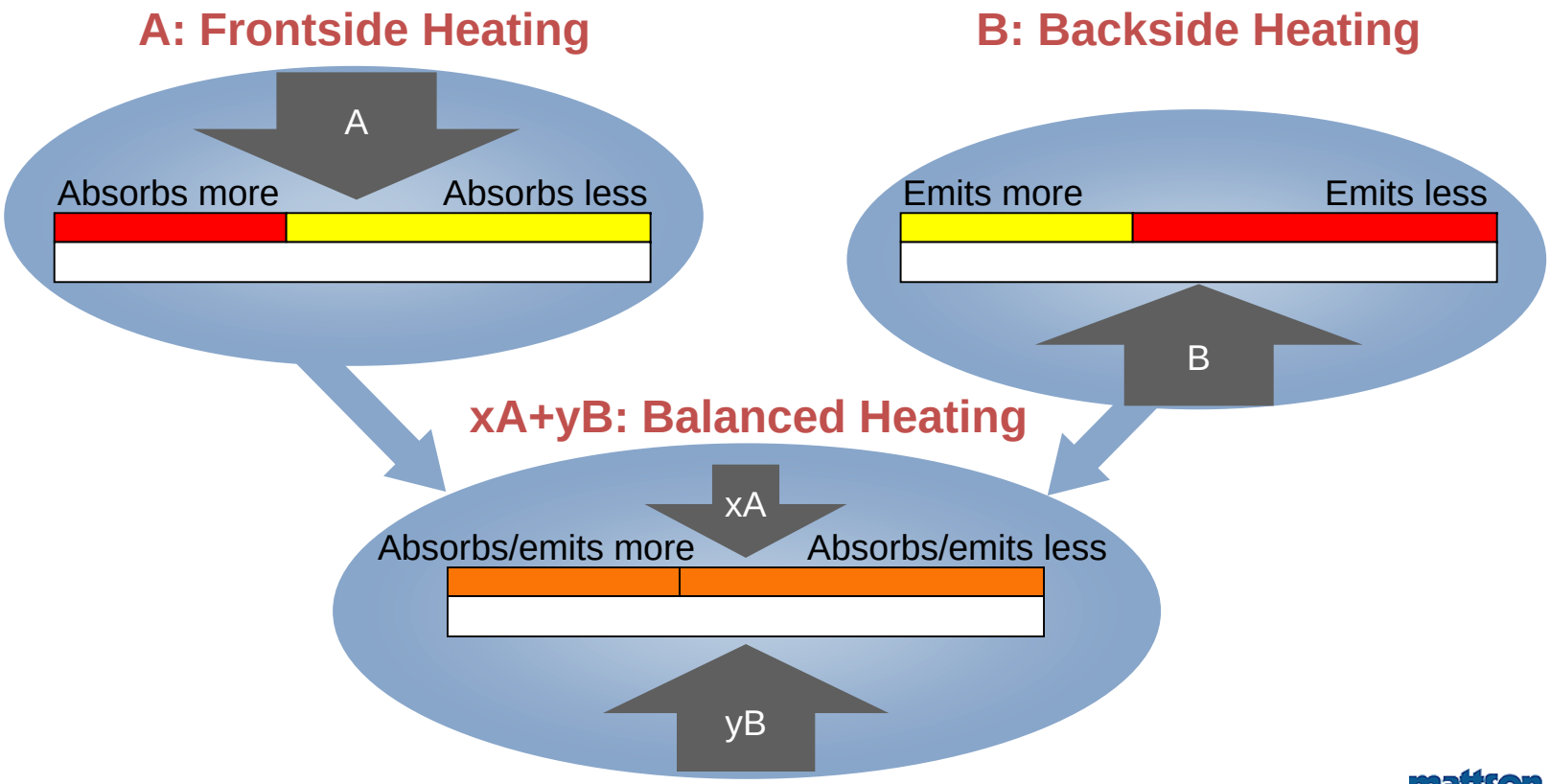




**Hot-Shielding has a rather small effect on $X_J$-$R_S$ trade-off**

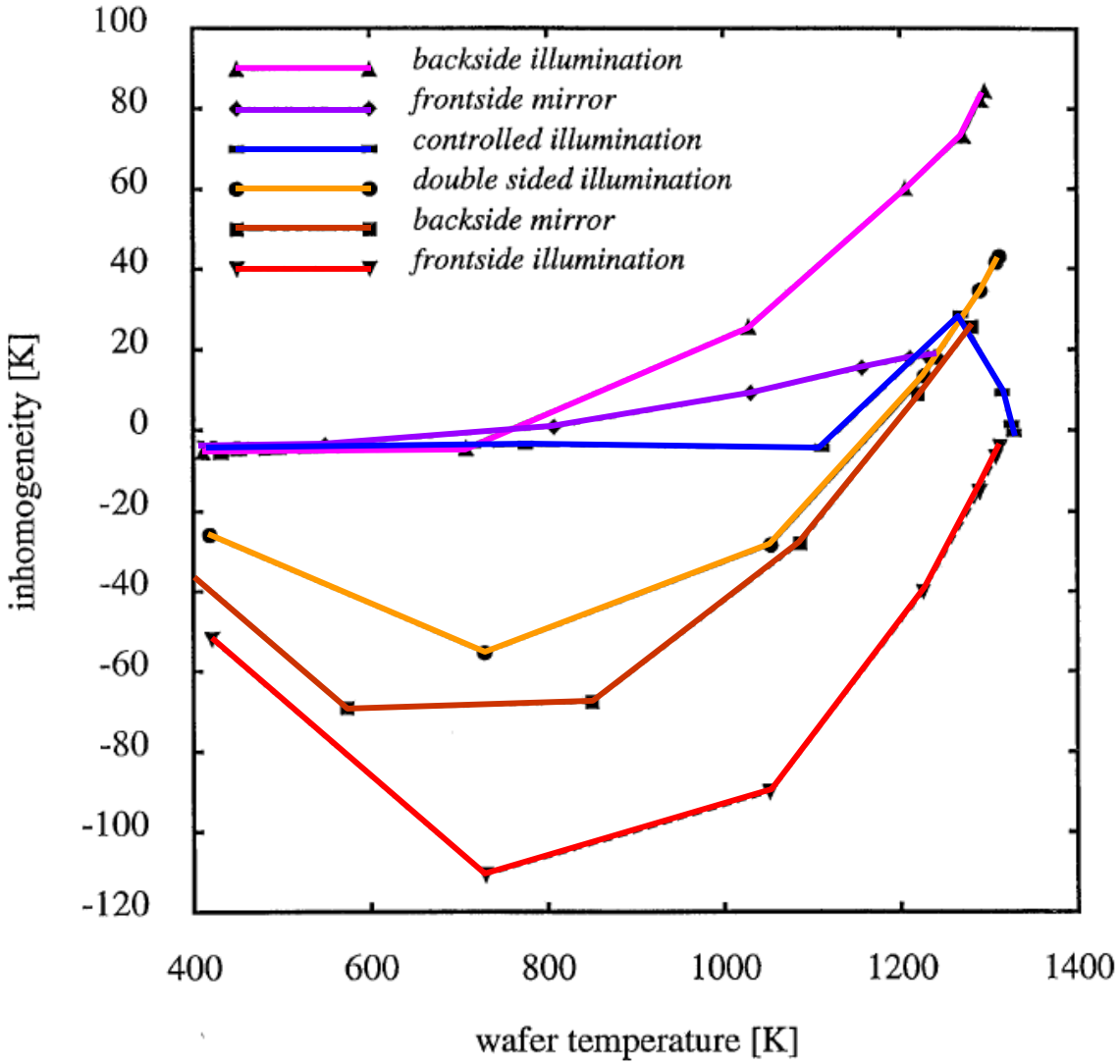
*"Pattern effects during spike annealing of ultra-shallow implants", J. Niess, Z. Nényei, W. Lerch and S. Paul, in Advanced Short-Time Thermal Processing for Si-Based CMOS Devices, p.11 (2003)*

# Combining Front and Backside Heating can Suppress $\Delta T$ from both $a_{tot}$ AND $\varepsilon_{tot}$ Variations

- Dual side heating: Optimal ratio of $P_{Front}$:$P_{Back}$ minimizes pattern effects
  - Frontside-only heating $\Rightarrow$ $\Delta T$ from power absorption variations
  - Backside-only heating $\Rightarrow$ $\Delta T$ from heat loss variations
  - Optimized ratio of front-side to back-side heating $\Rightarrow$ **Balance out the non-uniformity**



# Simulations Have Shown Unique Capability of Lamp Ratio Control




- "Controlled illumination" concept simulated by A. Kersch in 1996
- Plot is for non-uniformity during ramp to ~1050°C (Open-loop)
- Adjusting $P_F$:$P_B$ ratio allows $\Delta T$ to be minimized
- Device results have confirmed that this approach gives excellent suppression of pattern effects at < 45nm

*A. Kersch et al., MRS Symp. Proc. 429 (1996), p. 71*

# Conclusions

- Non-equilibrium conditions enable rapid & flexible controlled heating & cooling on time-scales from ns to s
  - Pattern effects are a natural consequence of non-equilibrium heating
- Pattern-induced $\Delta T$ depends on the heating power and on the thermal & optical properties of the wafer
- There are many ways to manage the pattern effect for both conventional RTP & for the surface heating regime
  - Device & equipment manufacturers can work together to meet the challenge

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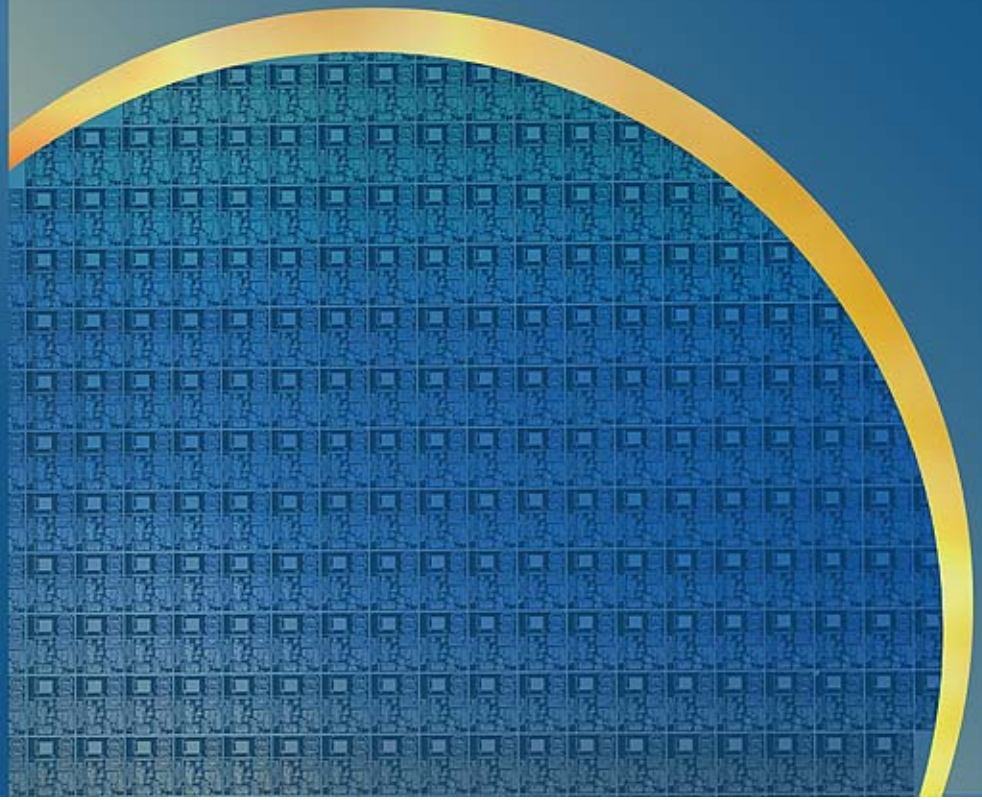

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