Nanowires for microelectronics: realistic perspectives for on-wafer Si –compatible growth and applications

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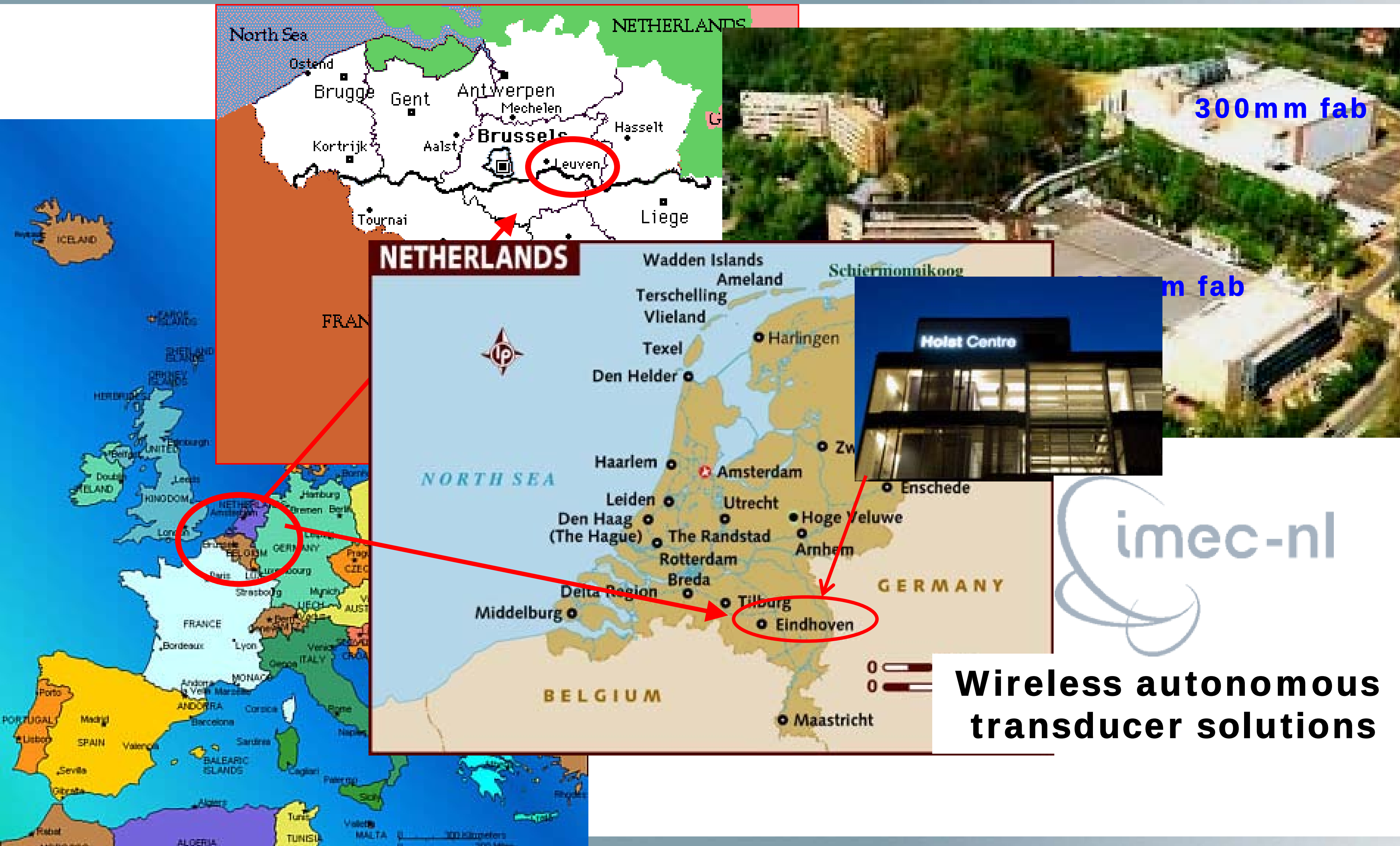
IMEC Inter-University Centre for Microelectronics



Wireless autonomous transducer solutions

Outline

1. Introduction: applications of NW

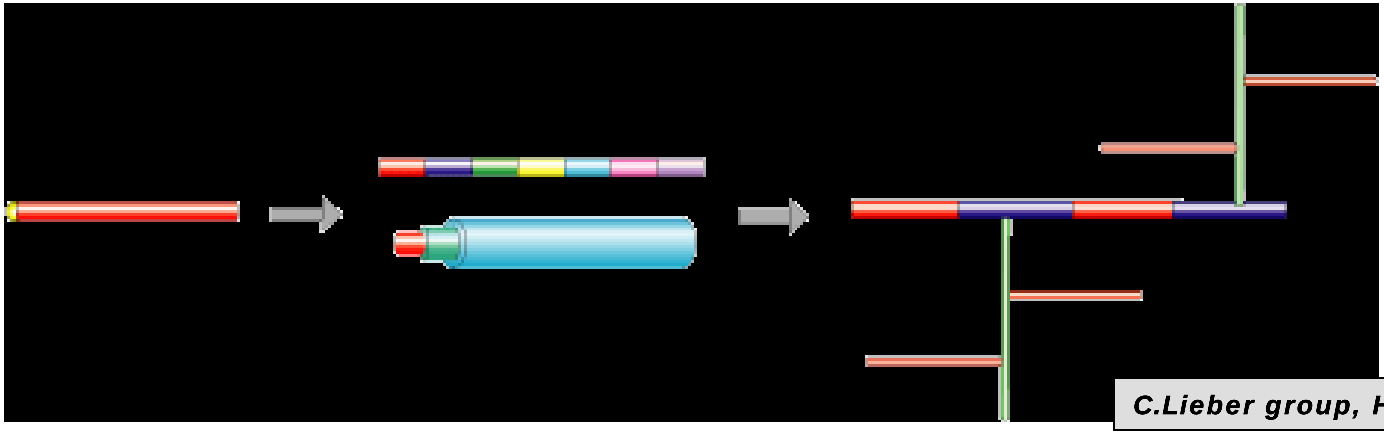
2. NW growth approaches
   - VLS, advantages and drawbacks

3. Problem ONE: Si-compatible catalyst
   - Plasma –enhanced catalytic growth with In
4. Problem TWO: direction control
   - Templated growth
5. Templated seedless growth
   - Selective epi growth of SiGe/Si and Ge/Si hetero-structures
6. Conclusions and perspectives

Characteristics / Applications

Characteristics of nanowires

1. 1D Vertical structure ➔ flexible architecture

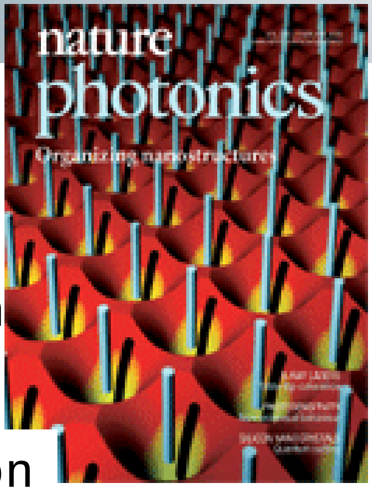


C.Lieber group, Harvard U.

2. Large surface-to-volume ratio

3. Eventually, quantum effects (ex.: e^- in Si➔ d<5nm)

Semiconductor NW applications…



- NanoPhotonics (waveguides, light sources, etc)
- Photovoltaics (multi-junction devices, radial collection,
  L.Samuelson- Lund U, H.Atwater –Caltech,
  S.Guha –IBM Watson

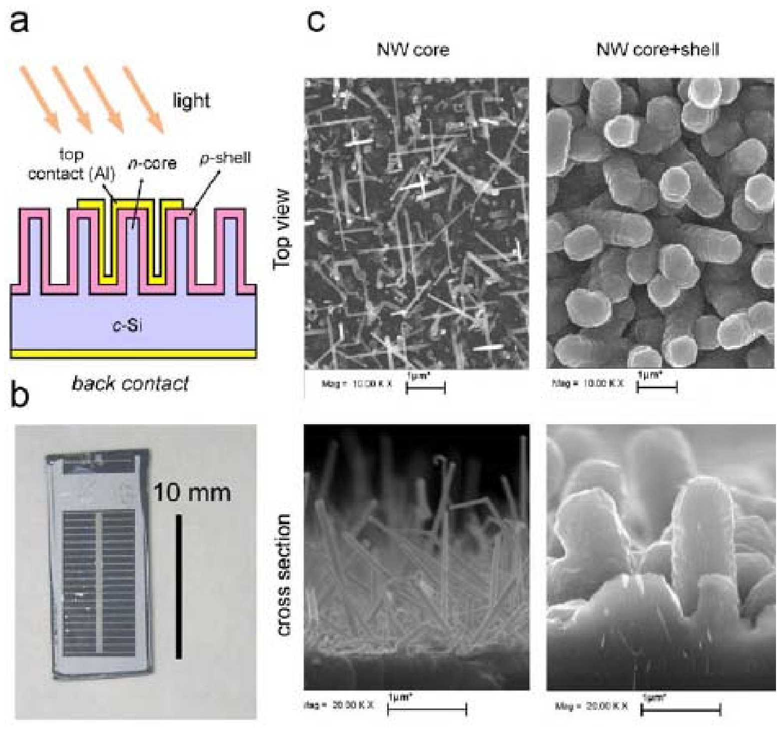
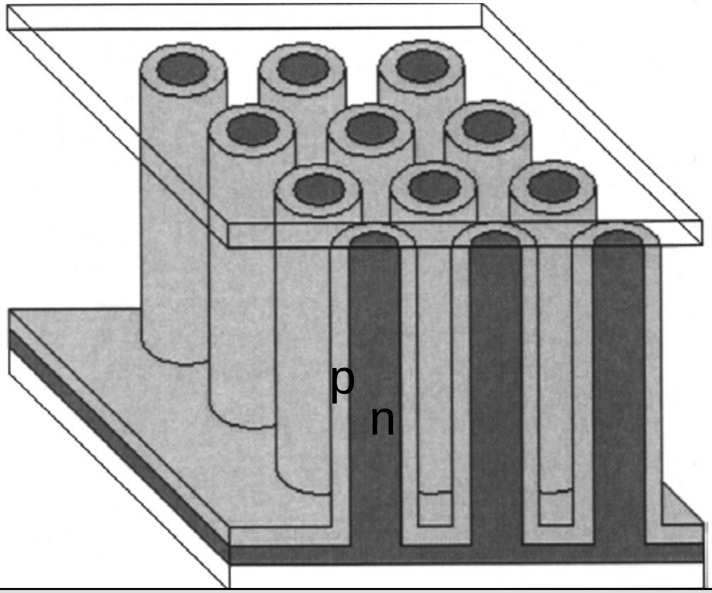


Fig. 1. (a) Schematic diagram of a radial p–n junction NW solar cell, (b) finished device and (c) SEM images of the NW, before and after the shell layer growth.

Efficiency ~1.8%

O.Gunawan, S.Guha, Solar Energy Materials &Solar Cells 93, 2009

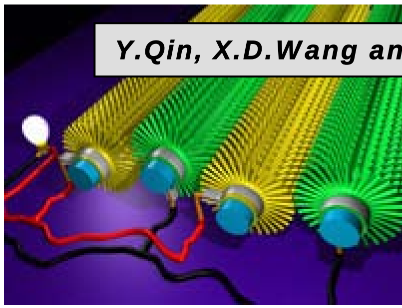
Radial n-p core-shell junction



B.M.Kayes et al, J.Appl.Phys. 97, 114302, 2005

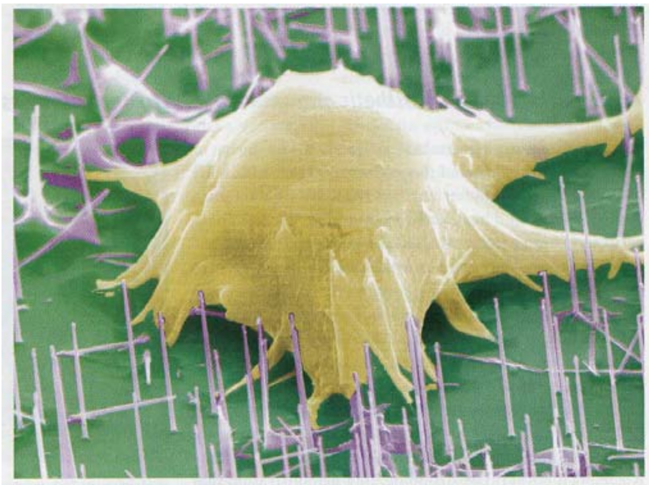
Semiconductor NW applications…

- sensors (JR Heath, Caltech)
- energy scavenging (piezo ZnO, ZLWang, GATech)



Y.Qin, X.D.Wang and Z.L.Wang, Nature, 451, 2008

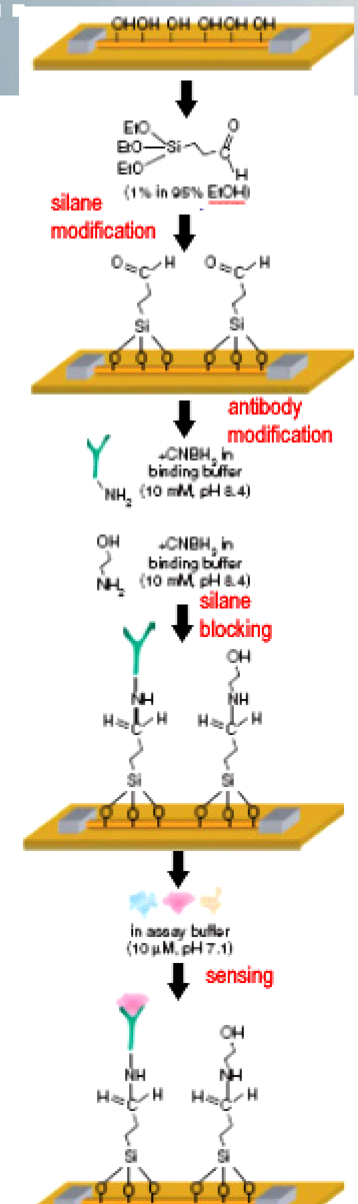
- medical applications (probes, etc, P.Yang- UCBerkeley, C.Lieber- Harvard)



Nanowires could deliver signals to prompt a stem cell to differentiate into another cell type.

Stem Cell control through NW
Scientific American 50, P.Yang

- thermo-electrics (JR Heath- Caltech, P.Yang- UCBerkeley)



http://www.vistatherapeutics.org/

Sensors @ imec-nl

- III-V NW gas sensors:
  - No catalyst, InAs NW on InP/SiO_2
  - surface functionalisation possible

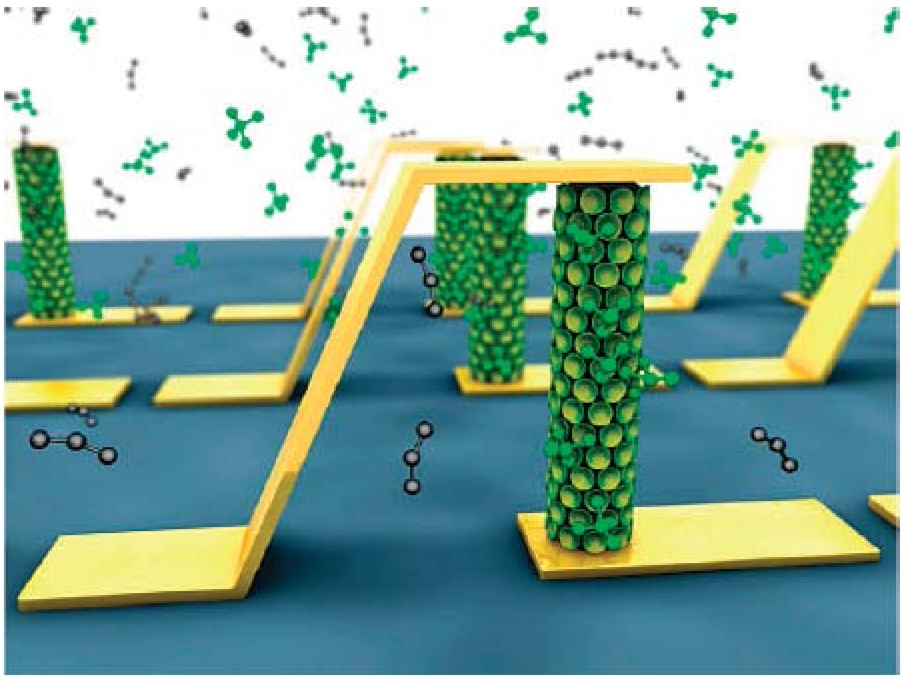
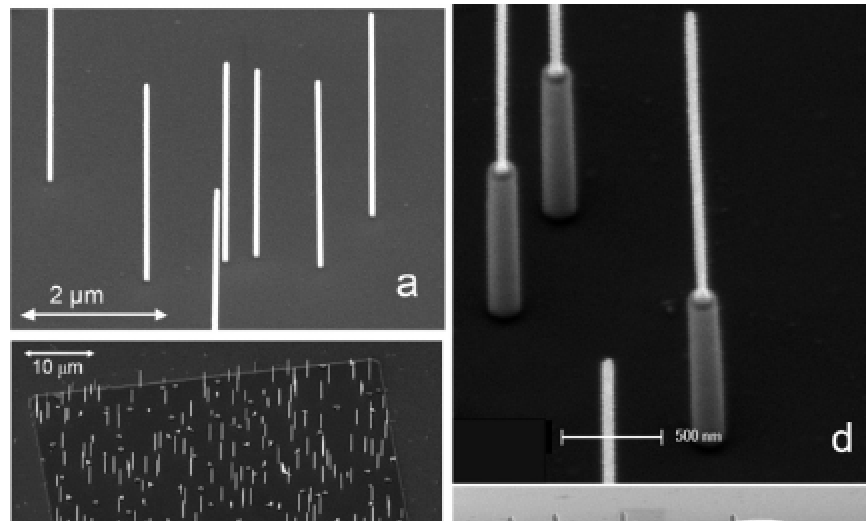


FIGURE 1. Schematic of nanosensor concept. Illustration of selective adsorption of gas molecules on a contacted vertical nanowire surface.



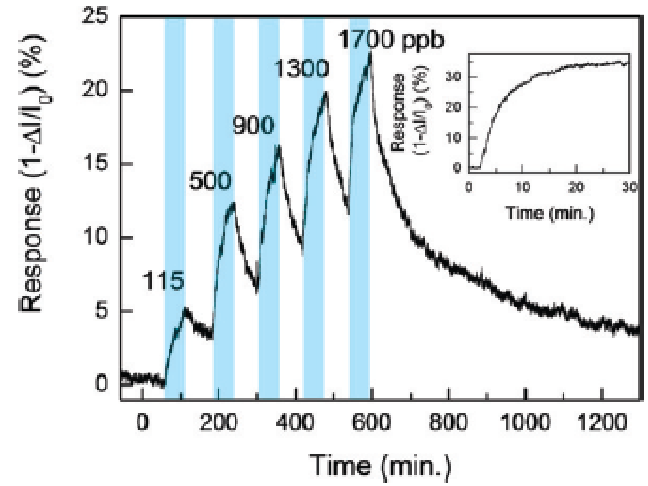
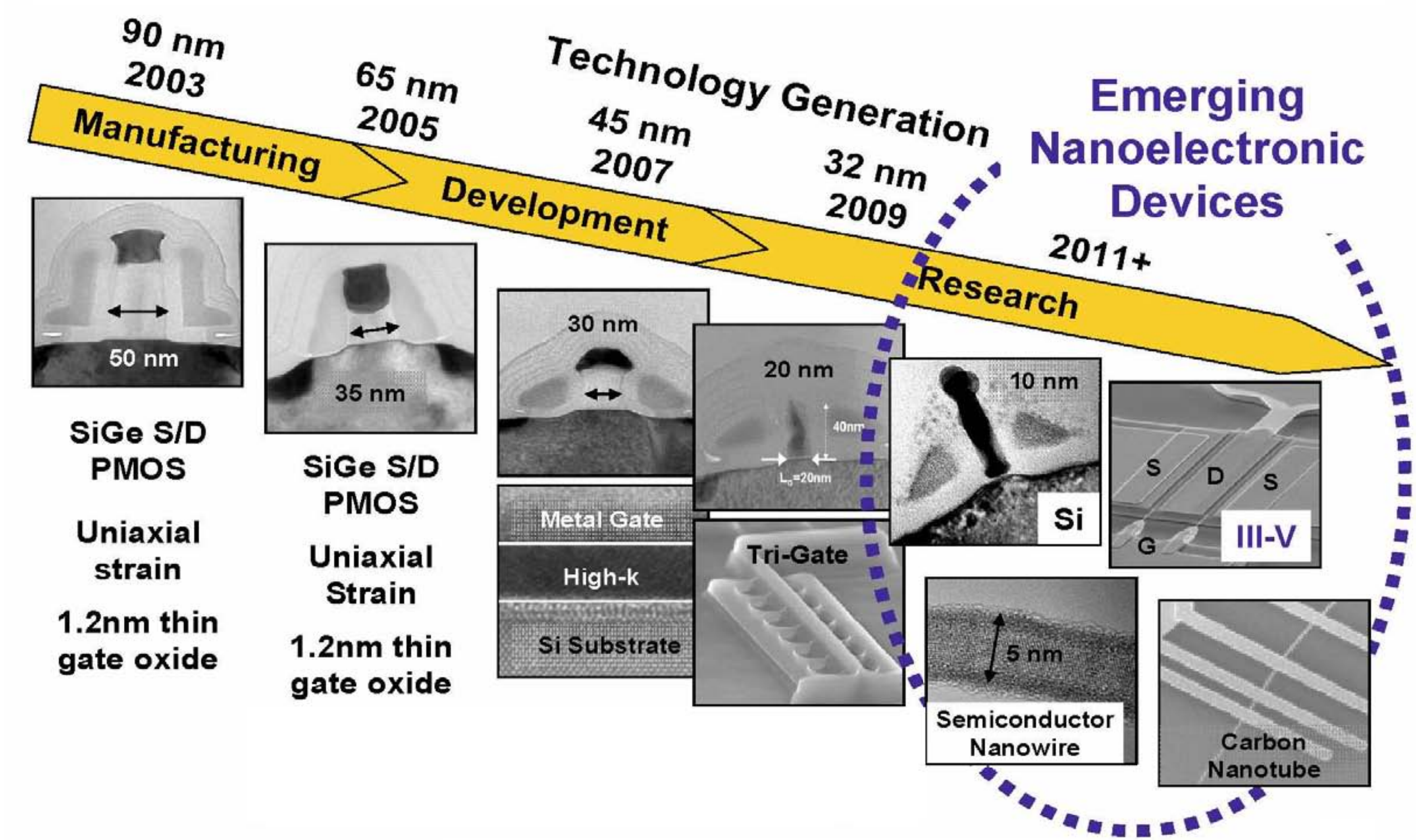


FIGURE 5. Gas detection with vertical InAs nanowire arrays. Response of a nanowire array with approximately 200 nanowires to varying concentrations of NO_2 in N_2. The inset shows a saturated response to 9 ppm NO_2/N_2.

P.Offermans et al., Nanoletters, in press, 2010

And microelectronics? Moore's future….



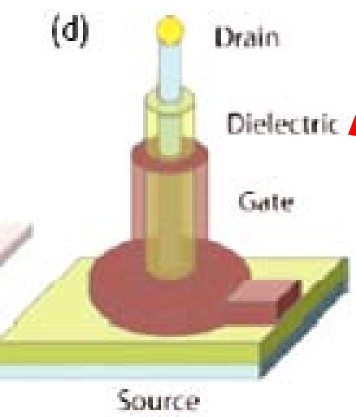
Ref: Robert Chau, *Role of High-K Gate dielectrics and Metal gate Electrodes in Emerging Nanoelectronic Devices*, Intel (2005)

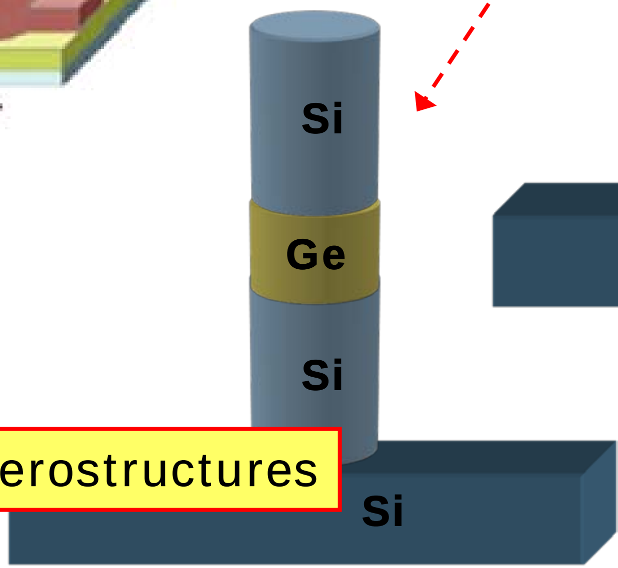
Expanding possibilities with NWs…

Vertical devices

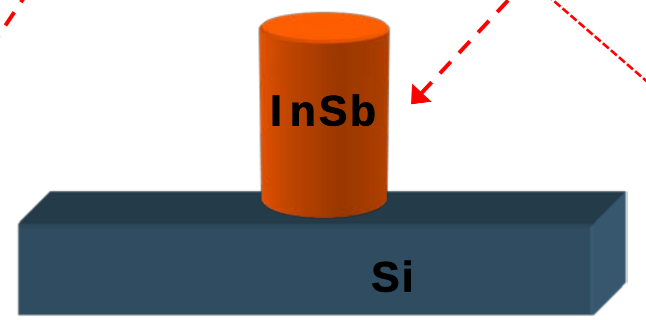
All-around gate

- Novel architectures
- possibility for **heterostructures**
- integration of **high μ materials** on Si
- possibility for devices in BEOL

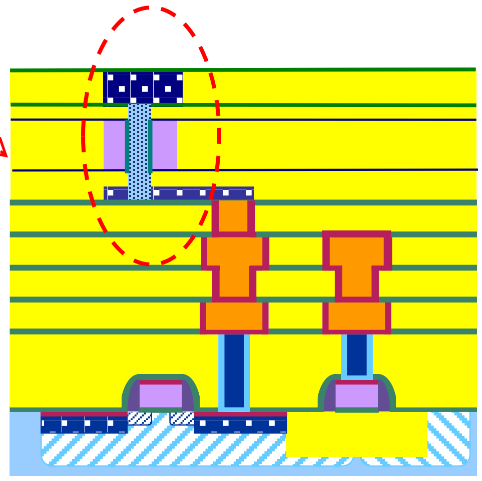




Heterostructures



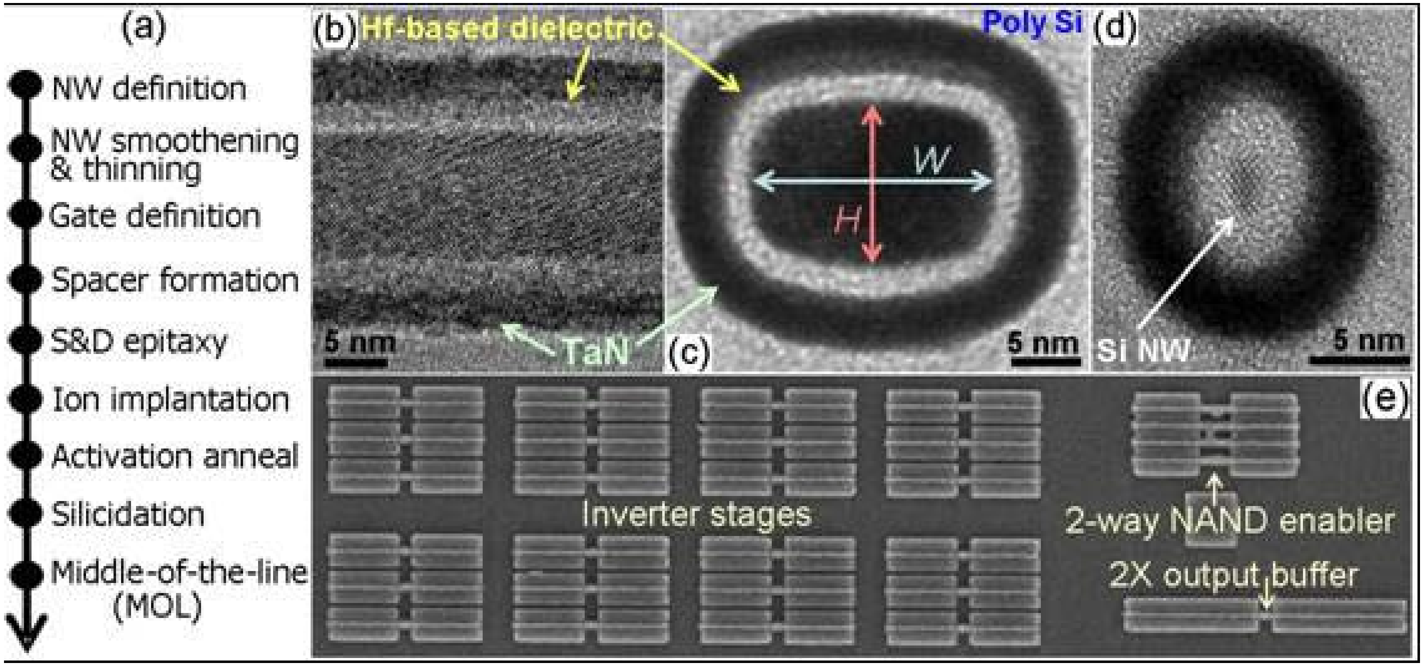
High μ on Si



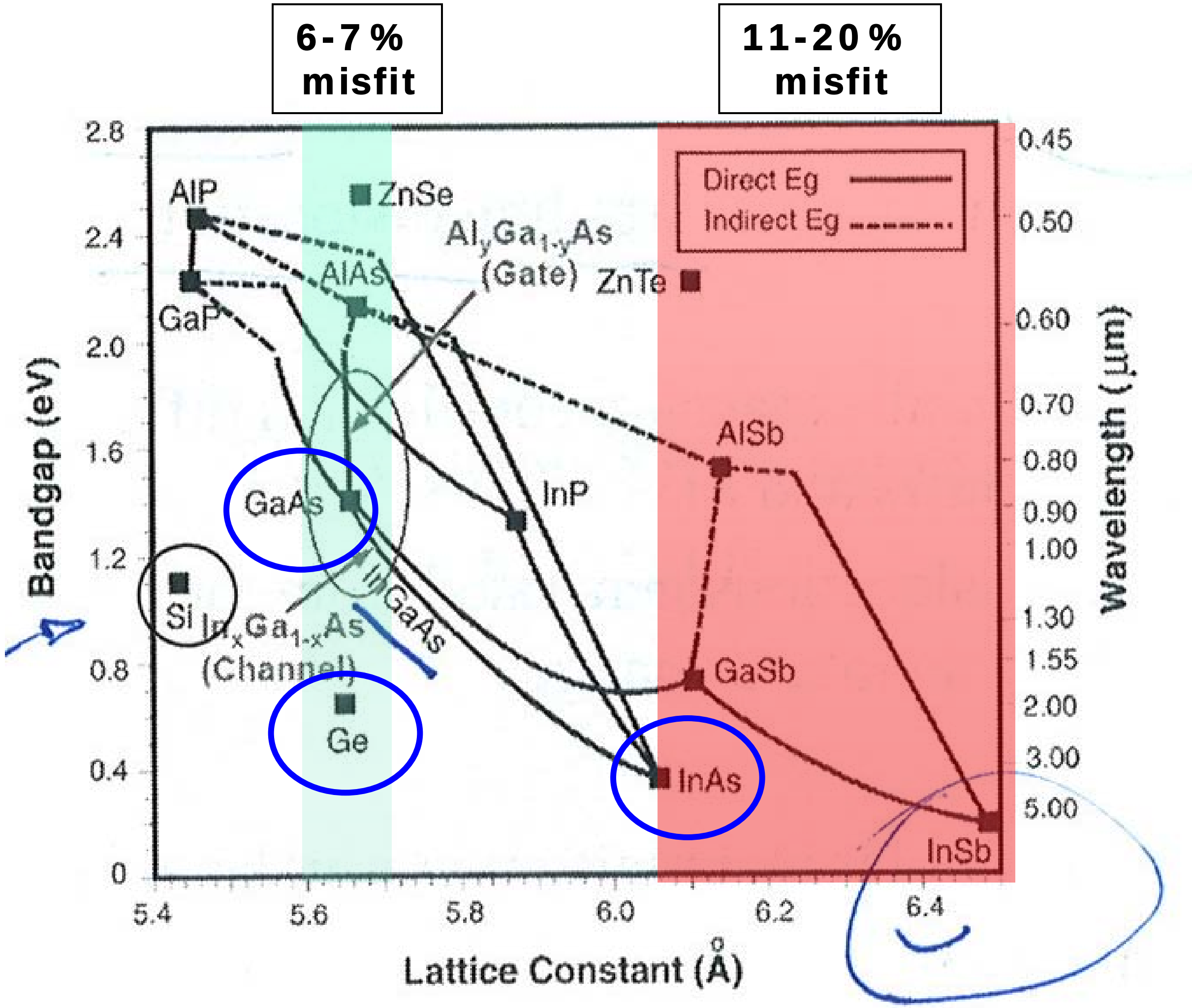
NODE EU 6th framework project
http://www.node-project.com/

Implementation of novel architectures...

VLSI Symp 2010, Hawaii
"Gate-all-around Silicon Nanowire 25-Stage CMOS Ring Oscillators with Diameter Down to 3 nm,"
Sarunya Bangsaruntip, et al., IBM T. J. Watson Research Center

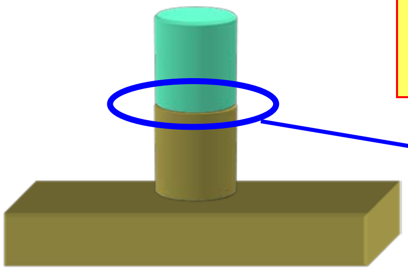


Semiconductor materials properties



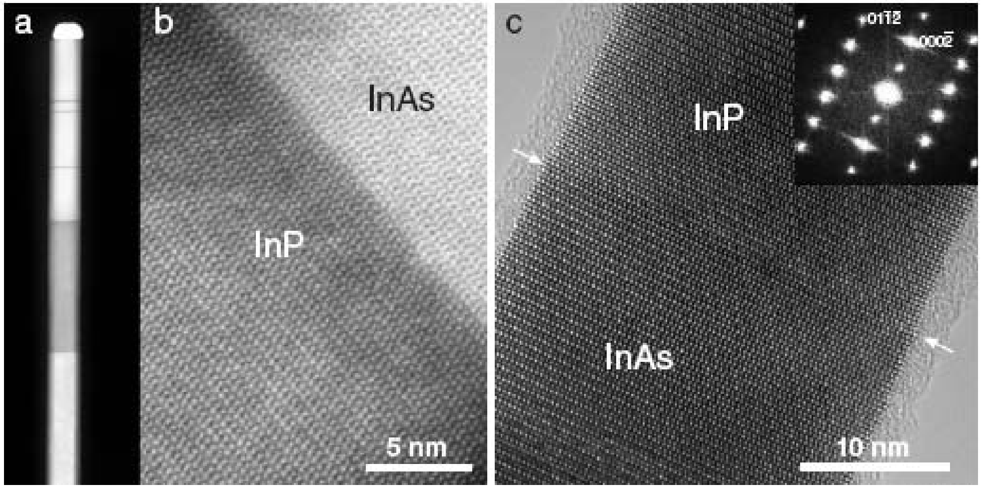
Relaxation @ nanoscale

$h_c \rightarrow \infty$ when $r < r_0$:
High strain sustained with no dislocations!



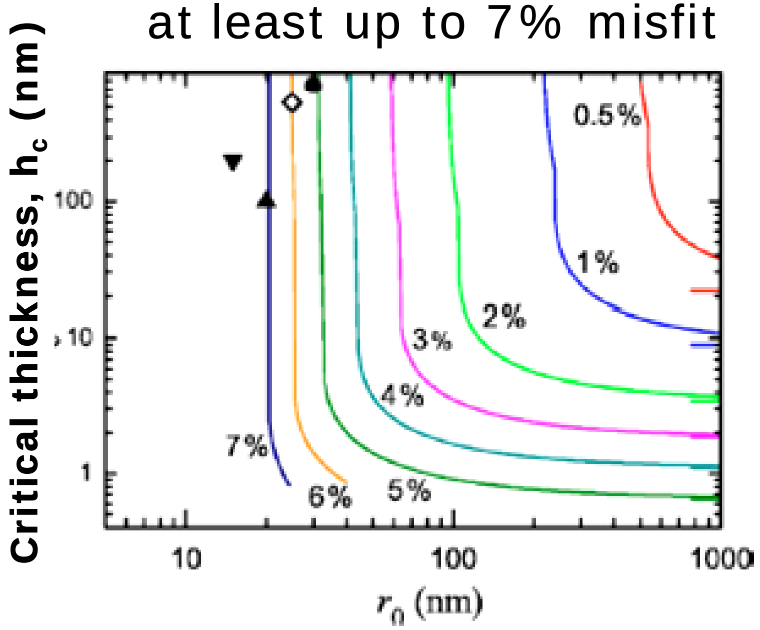
Dislocations inhibited!

Experiments:
3% misfit accomodated w/o dislocations



M.W.Larsson et al., Nanotechnology 18, 2007

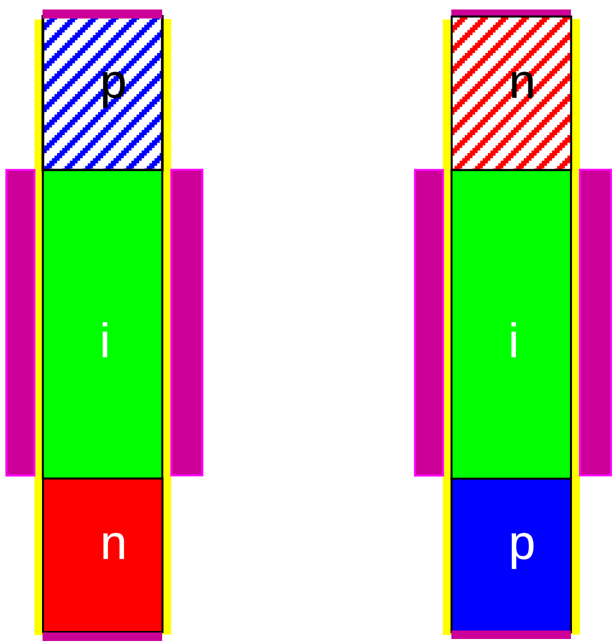
Calculations:
at least up to 7% misfit



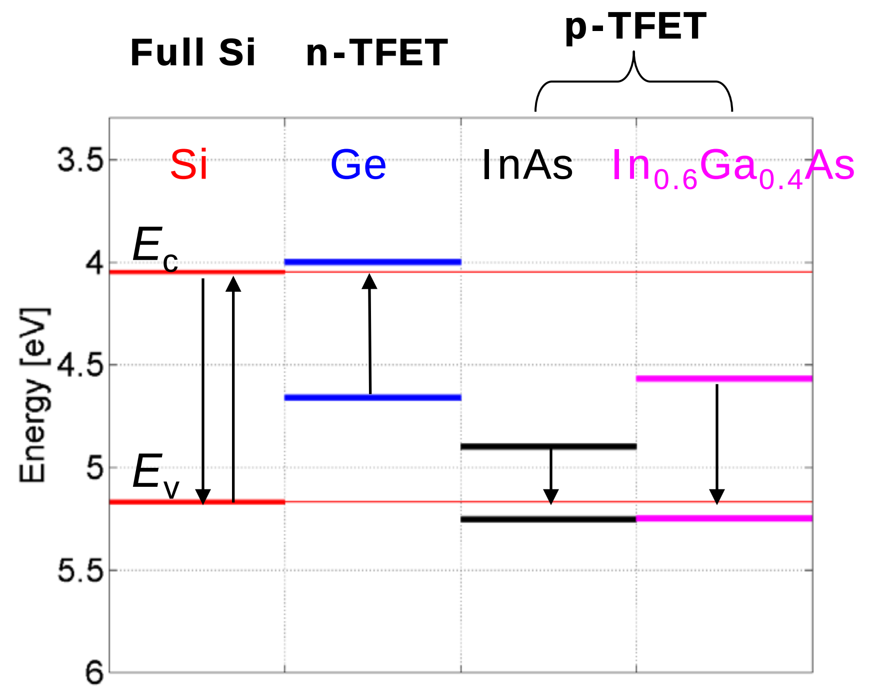
F.Glas, Phys Rev B 74, 505307, 2006

Hetero-wires for Tunnel -FETs

Ge-source n-TFET | InAs-source p-TFET



: silicon
: germanium
: indium-arsenide



Mismatch w/Si	Ge	InAs	$In_{0.6}Ga_{0.4}As$
Lattice	4.2%	11.6%	8.6%
Thermal	127%	74%	120%

A.S. Verhulst et al, IEEE EDL 29(12), 2008

NW growth strategy

PROBLEM:

What is suitable for large scale production?

- Microelectronics (logic, memory) and on-chip heterogeneous system integration (MEMS, sensors, etc..)

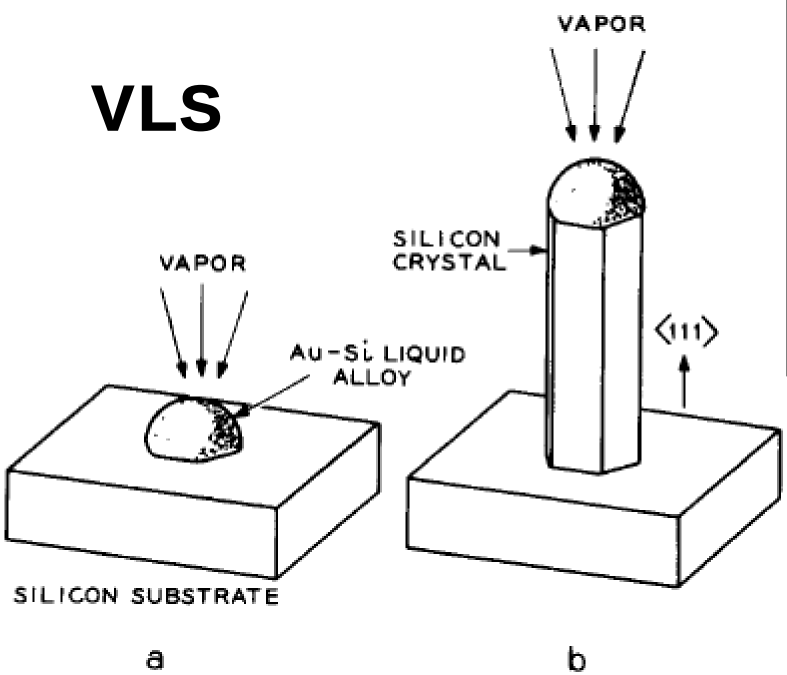
Requirements:

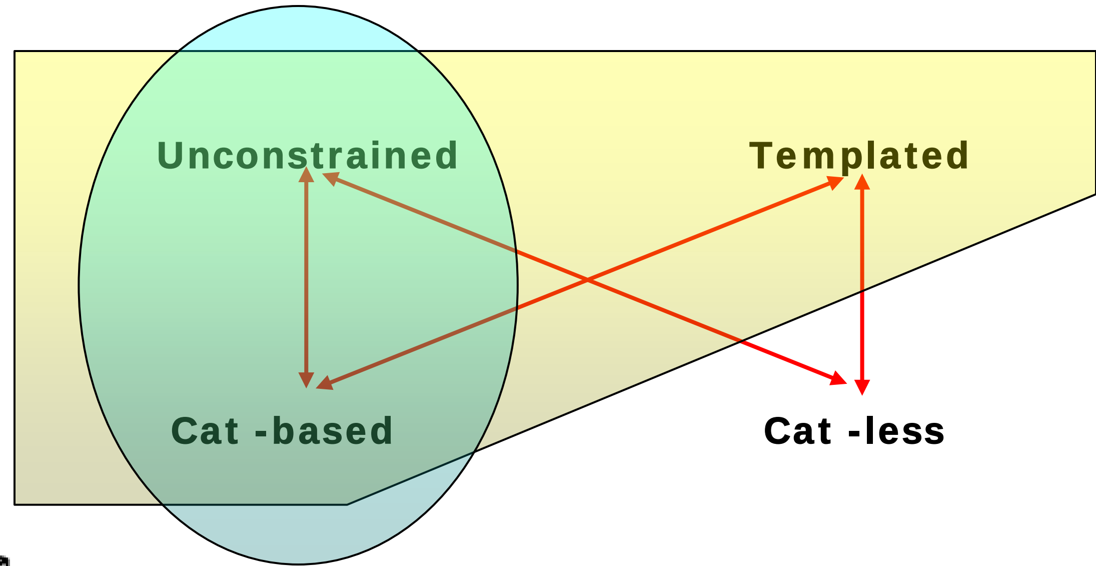
- **I. Compatibility with Si**
- **II. High yield**
- **III. Control on**
  - I. Location
  - II. size
  - III. Orientation
  - IV. Crystalline quality
  - V. Doping level/profile: channel and contacts
- **IV. Reproducibility at wafer –level**
- **V. Heterostructures: nm sharp interfaces**

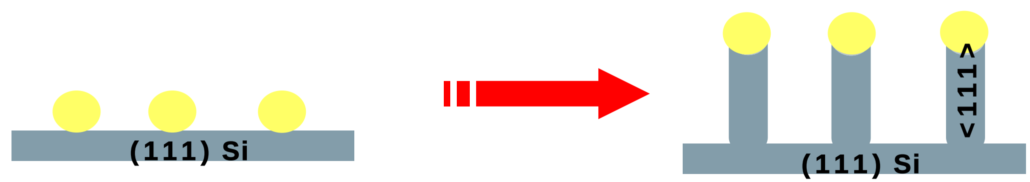
Vapor Liquid Solid growth

Wagner, Ellis, Appl.Phys.Lett.4(5), 1964

VLS







<u>Role of liquid nanoparticle:</u>

1. **chemical dissociation catalyst**
2. **high collection coefficient**
3. **E_a(L-S) < E_a(V-S)**

<u>Issues</u>:

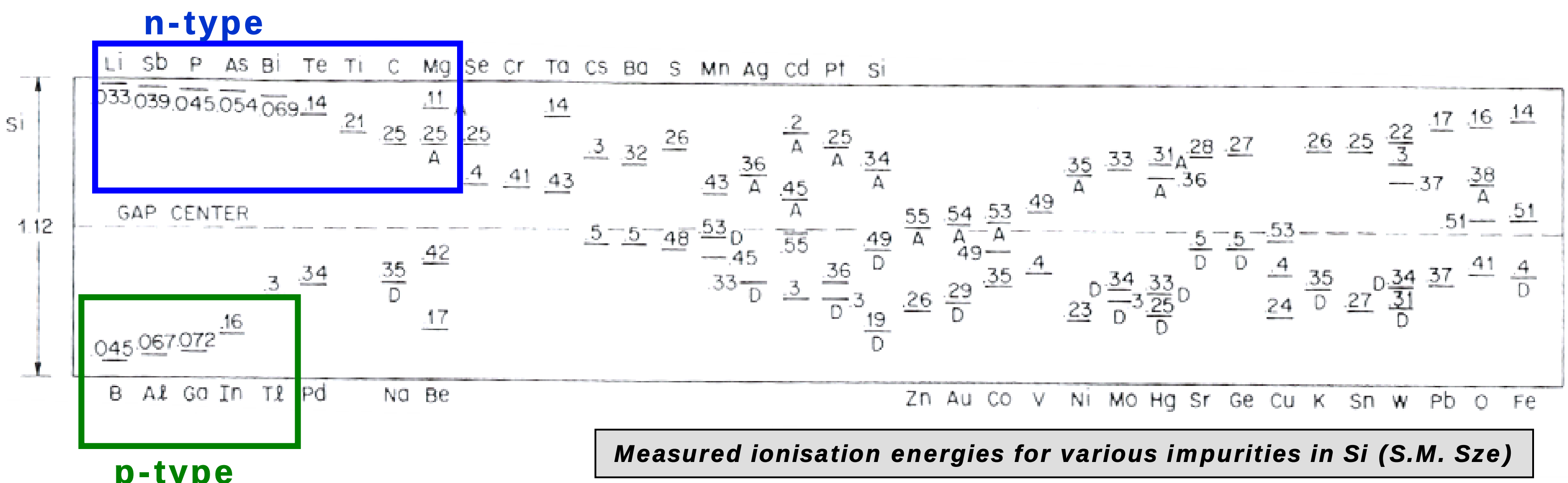
1. Si-compatibility: catalyst ≠Au
2. alignment:
   - use of (111)Si
   - does not work for small <d>

Problem one: impurities in Si

Au
- **chemical catalyst**
- **favourable Au-Si alloying properties**
- **noble metal, not reactive**

BUT

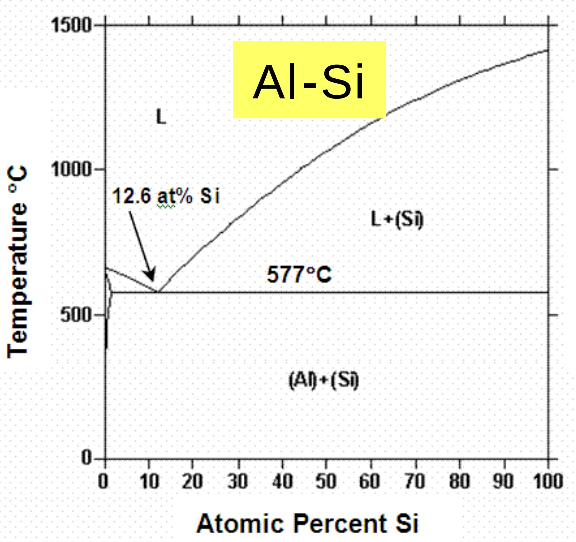
- Electrically active defects in Si: performance killers
  - Au, Ag, Cu ➔ mid-gap states, generation-recombination centers
- Electrically neutral, donors and acceptors: acceptable

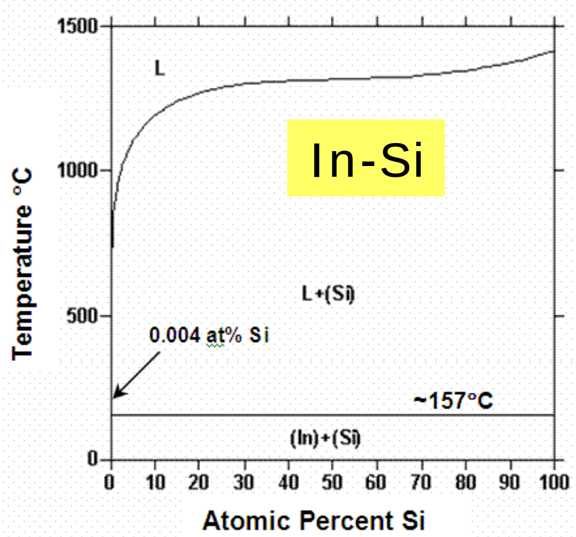


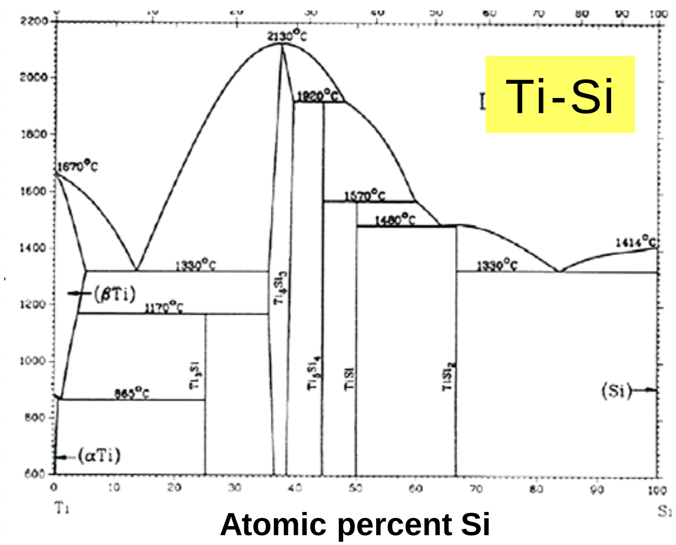
Measured ionisation energies for various impurities in Si (S.M. Sze)

Alternatives to Au for Si?

Earlier literature on Si NW growth (thermal CVD):







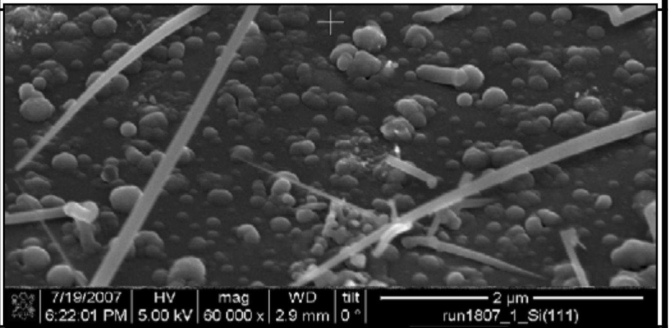
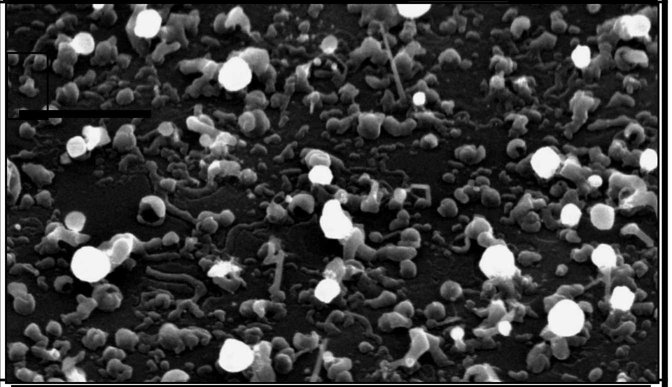
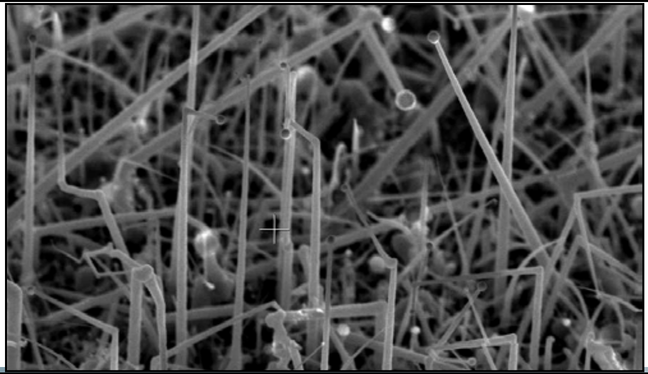
VSS growth <500°C
Wang et al., MPI Halle
Nature Nanotech Dec.2006

Not successful

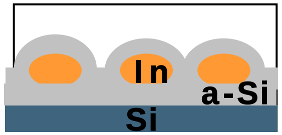
VSS growth @640°C
Kamins et al., JAP 89, 2001

Plasma –enhanced VLS growth with In

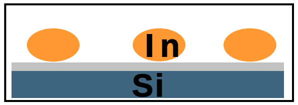
PE critical for Si NW growth with In

PRETREATMENT	GROWTH	RESULT
Thermal anneal	Plasma enhanced	
Plasma enhanced	Thermal growth	
Plasma enhanced	Plasma enhanced	

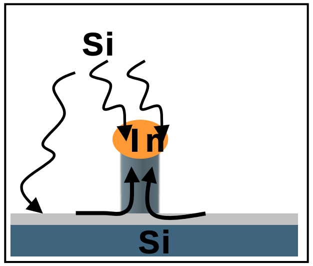
NO growth



NO growth

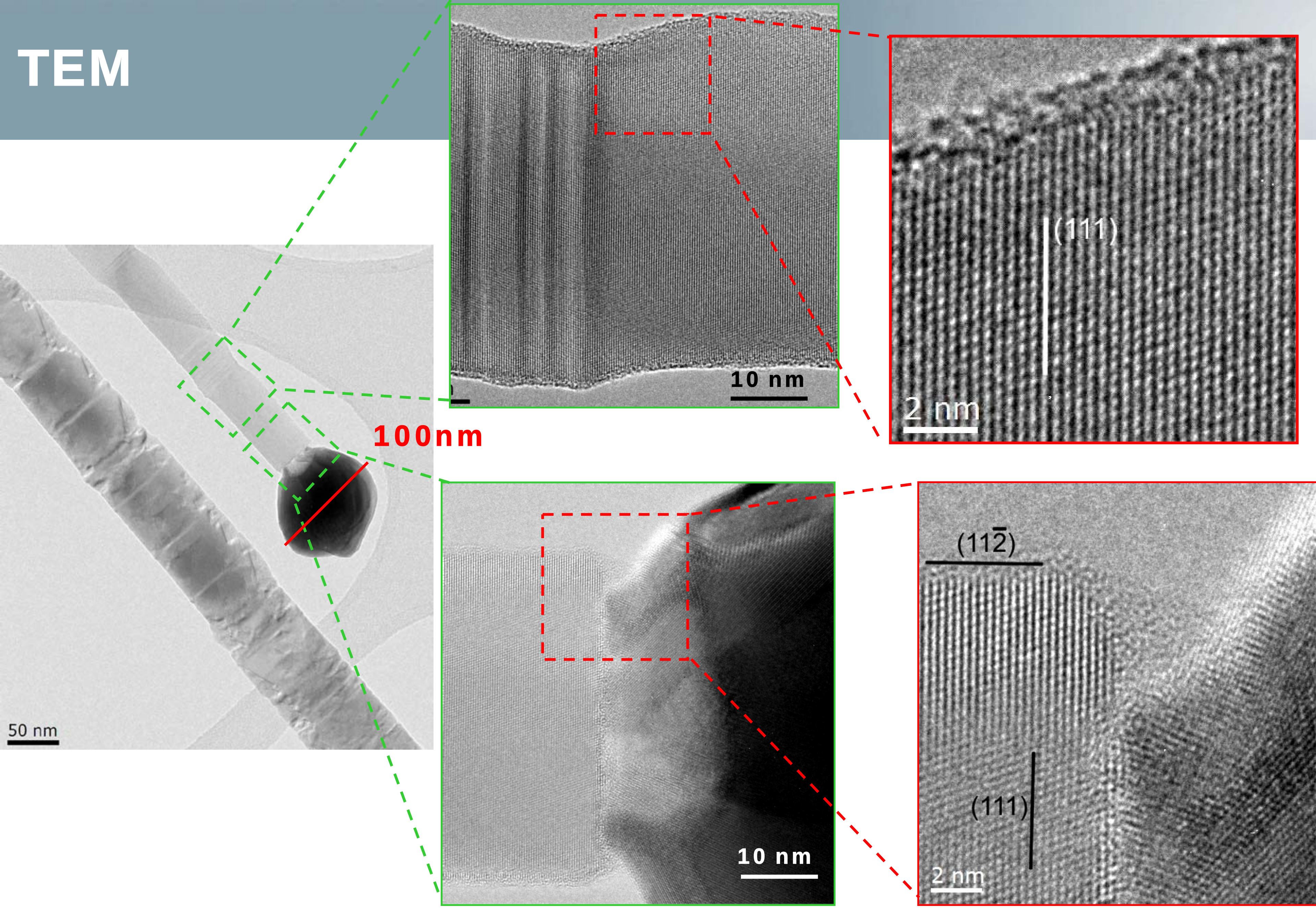


NW growth



F.Iacopi et al., Nanotechnology 18, 505307, 2007

TEM

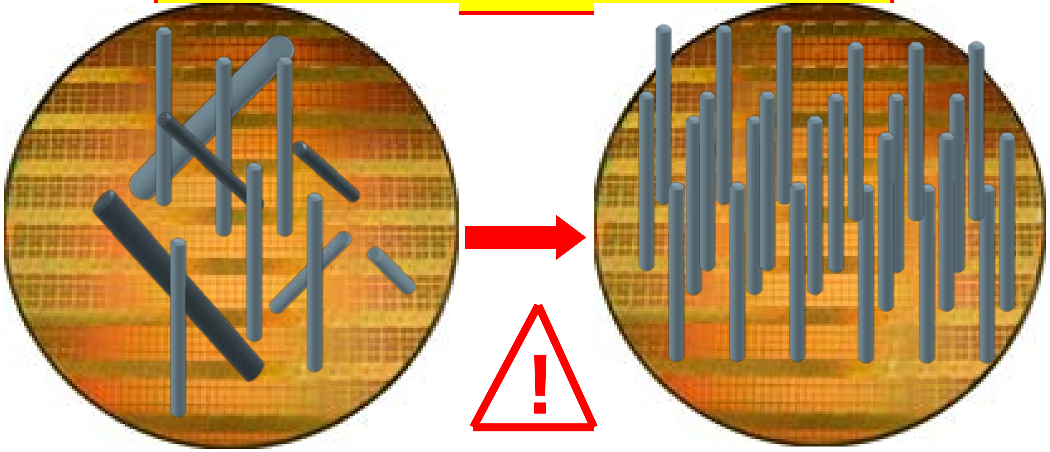


F.Iacopi et al., Nanotechnology 18, 505307, 2007

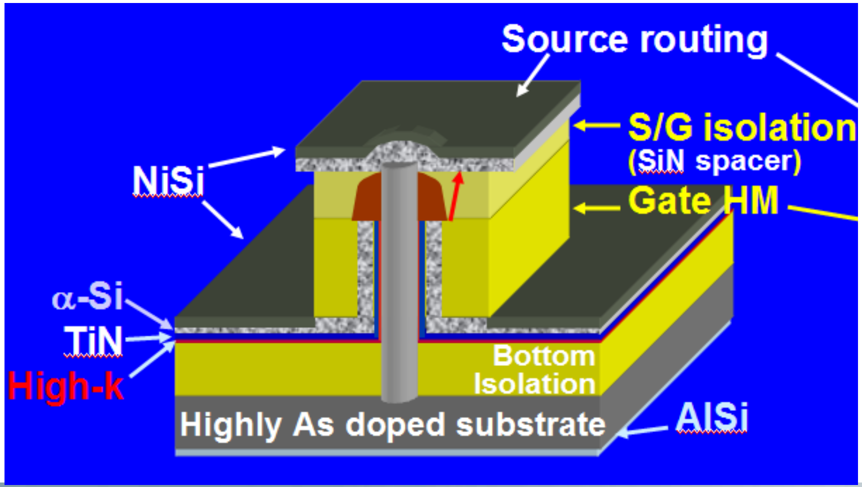
Problem 2: how about wafer-scale 1D growth??

www.intel.com

Pick and place: NO option

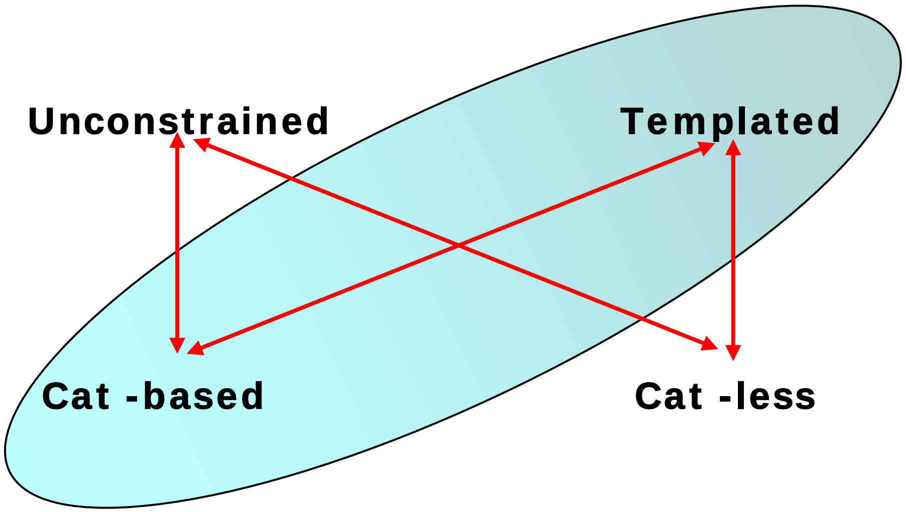


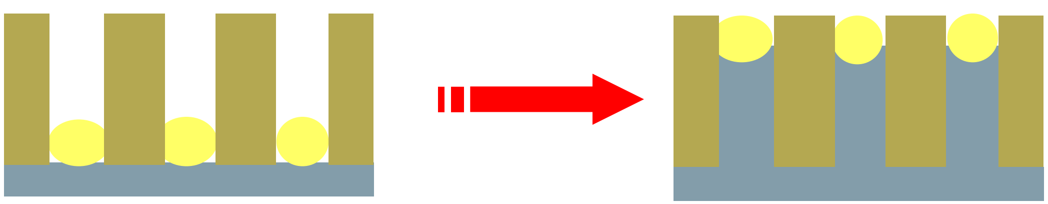
Control on position, size, orientation, etc.. over ~700 cm^2 ➔ ~10^{11} NW / wfr

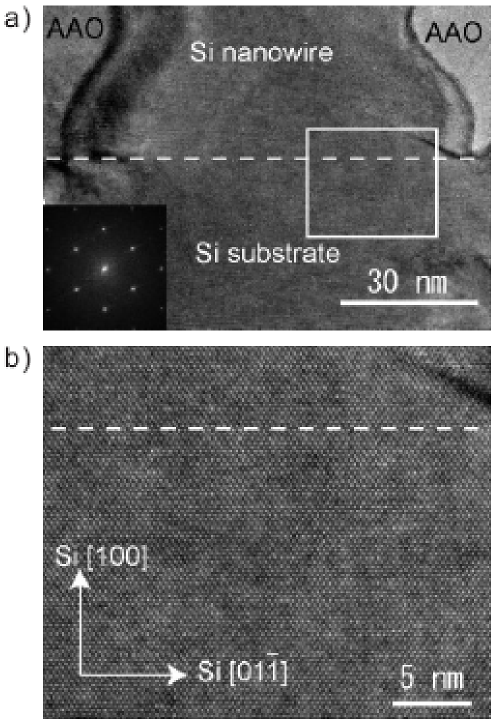


A.Vandooren et al, Nanoelectronics Workshop, Kyoto VLSI 2009

Templated VLS growth



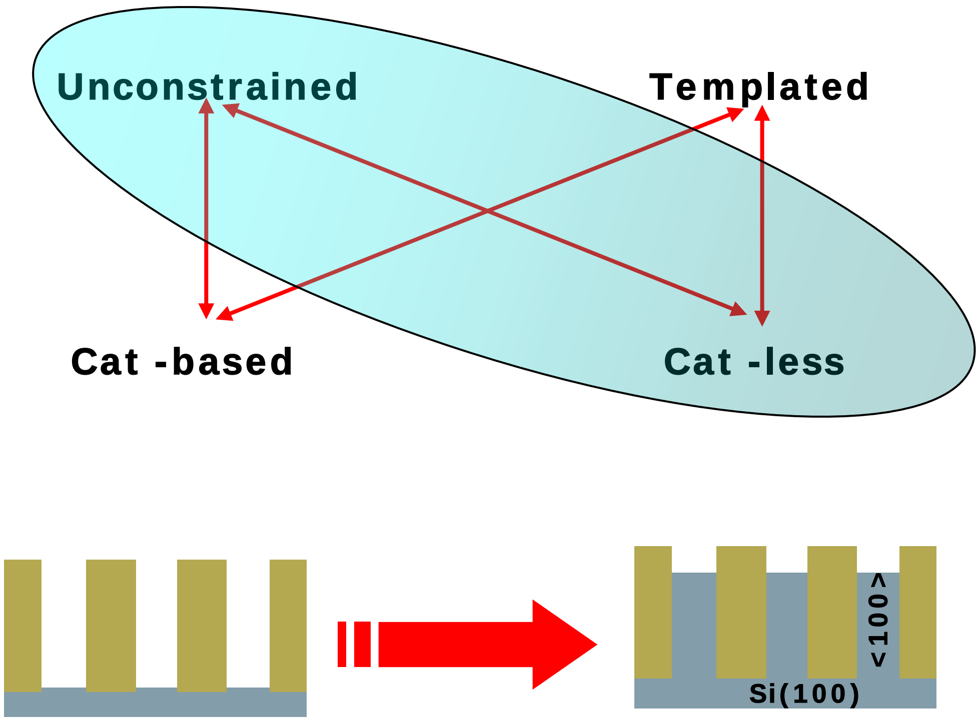




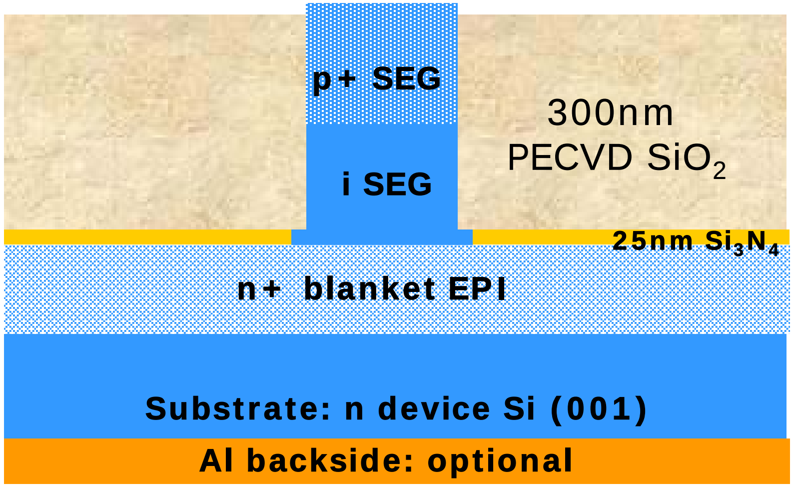
T.Shimizu et al., Advanced Materials, 2007

Direction control! But still catalyst –related issues...

Seedless templated growth



Selective Epitaxial Growth in via holes



..directed selective growth replaces catalyst –based growth!

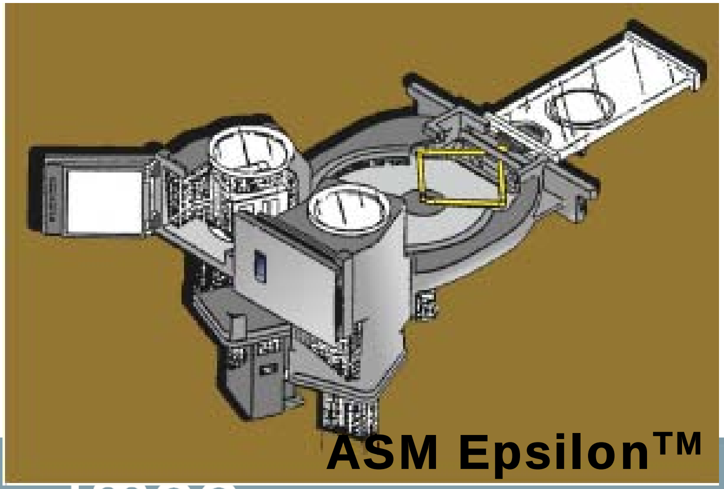
Seedless templated growth

Selective Epitaxial Growth

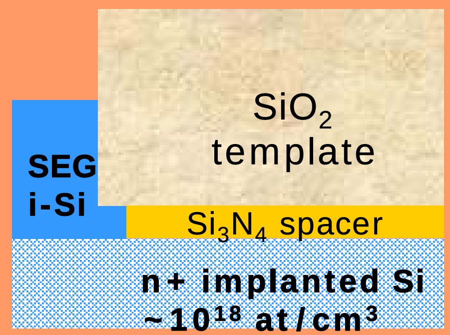
-
    - Growth rate:

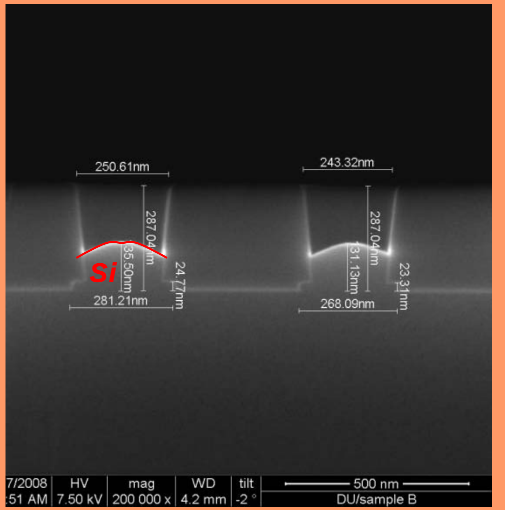
1) **i-Si** SE growth:
$SiCl_2H_2/HCl/H_2$ **@810°C**

2) **p+ $Si_{0.85}Ge_{0.15}$** SE growth:
$GeH_4/SiCl_2H_2/HCl/H_2/B_2H_6$ **@750°C**

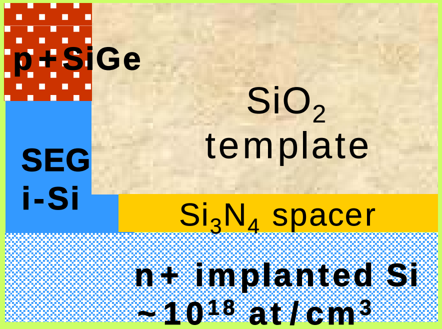


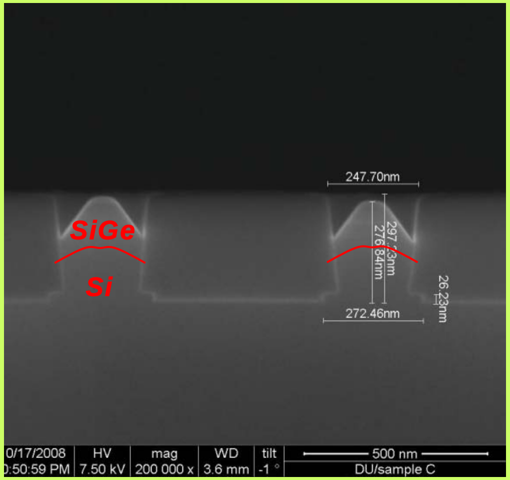
1 i-Si
~4nm/min



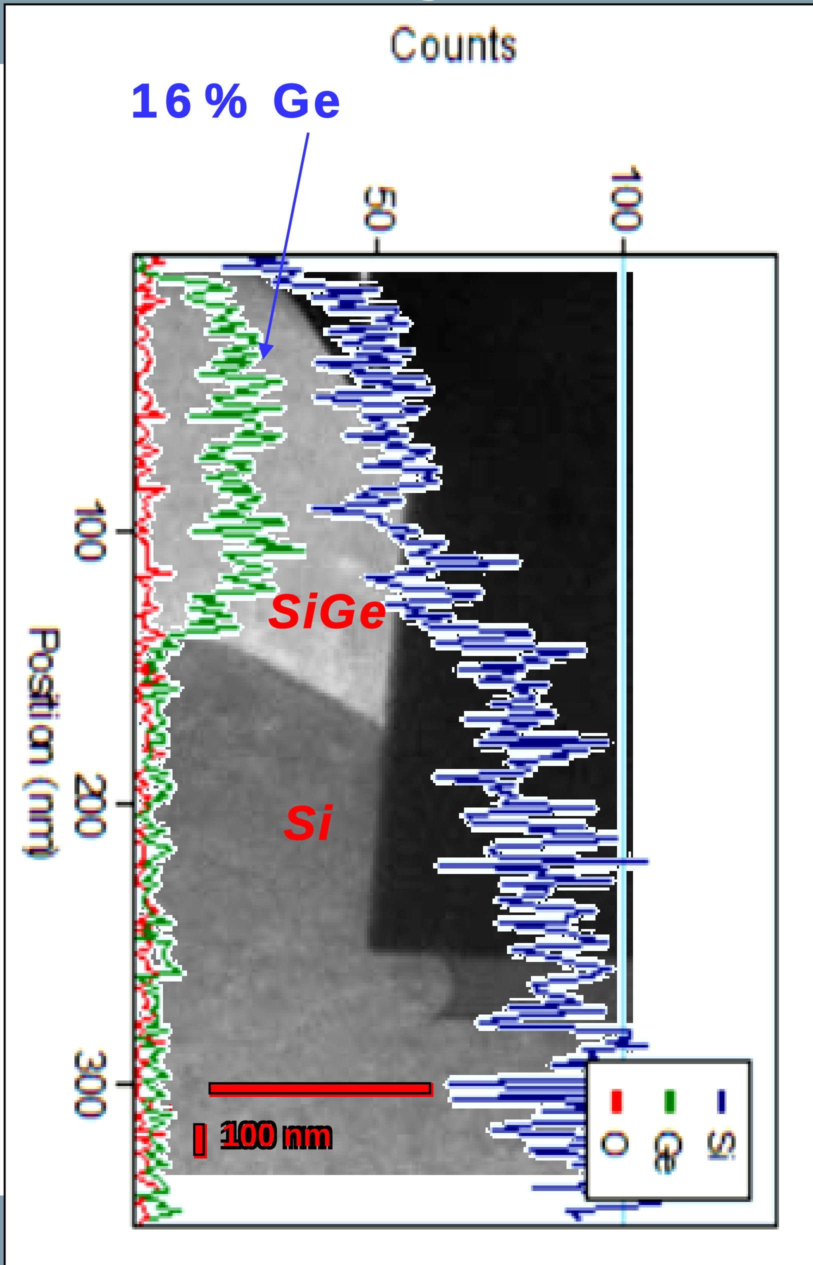


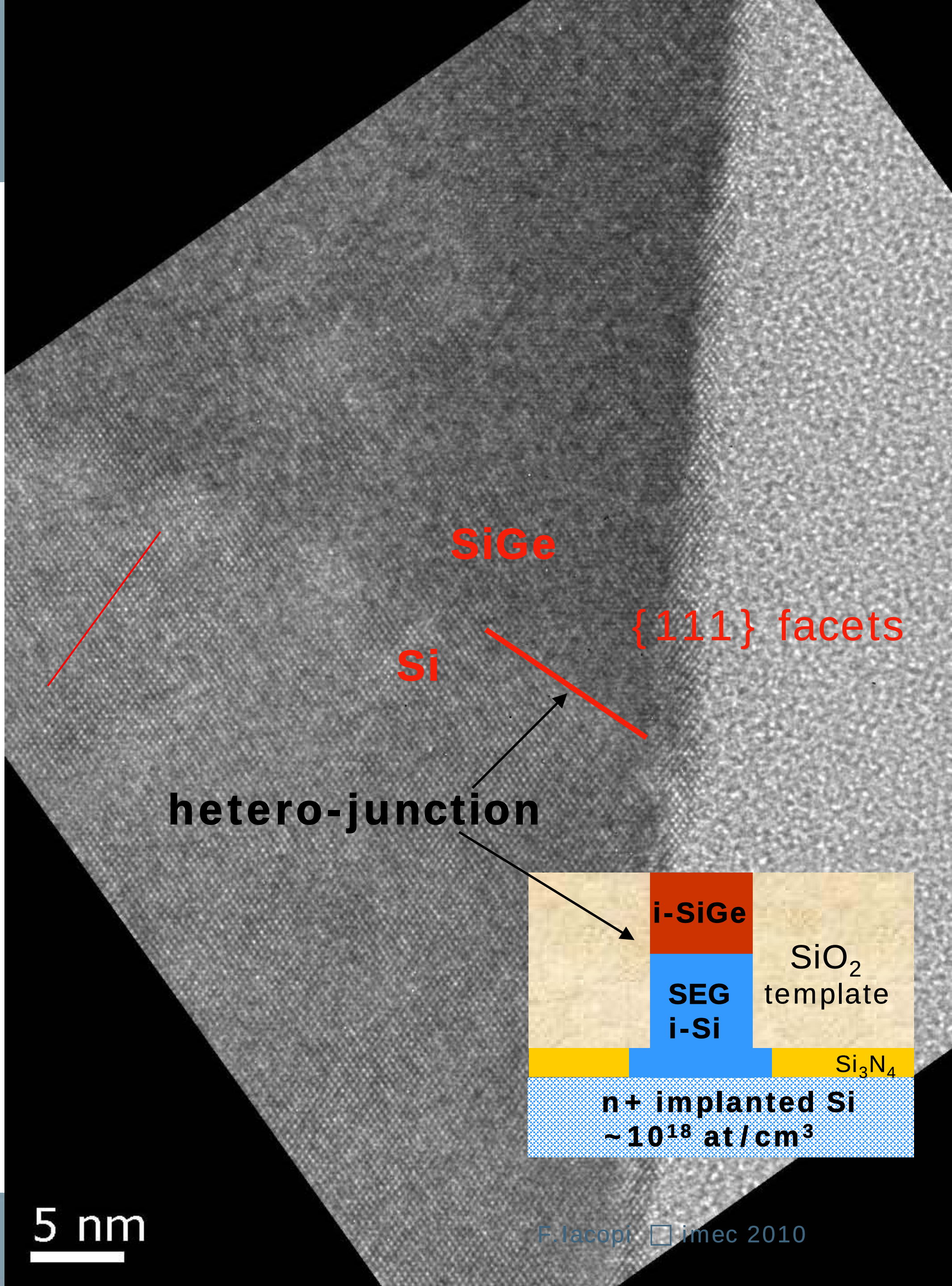
2 p+ SiGe 15%
~5nm/min



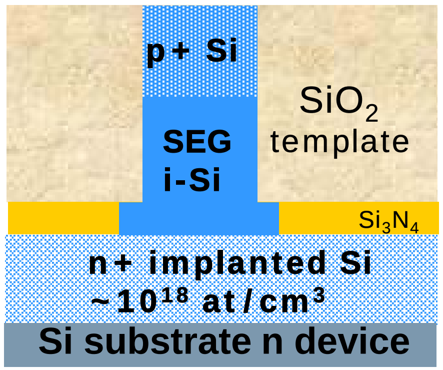


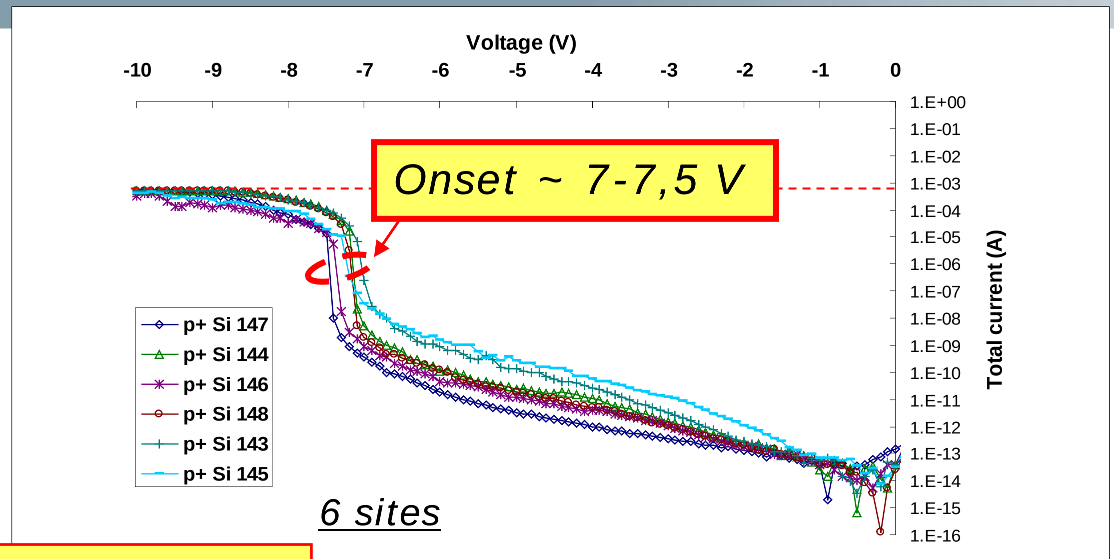
Hetero- junction



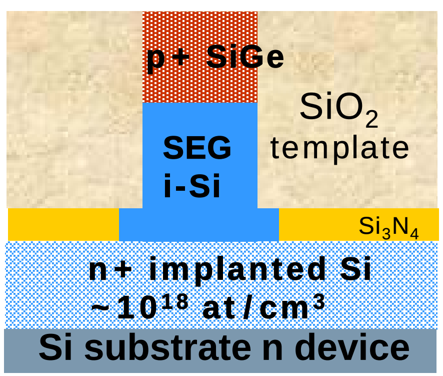


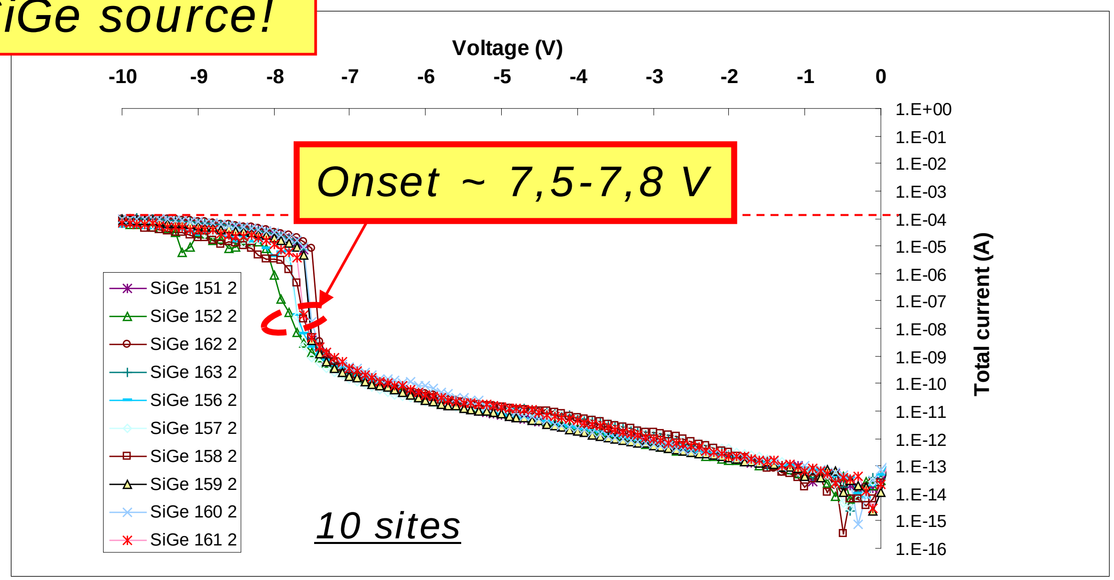
Reverse bias



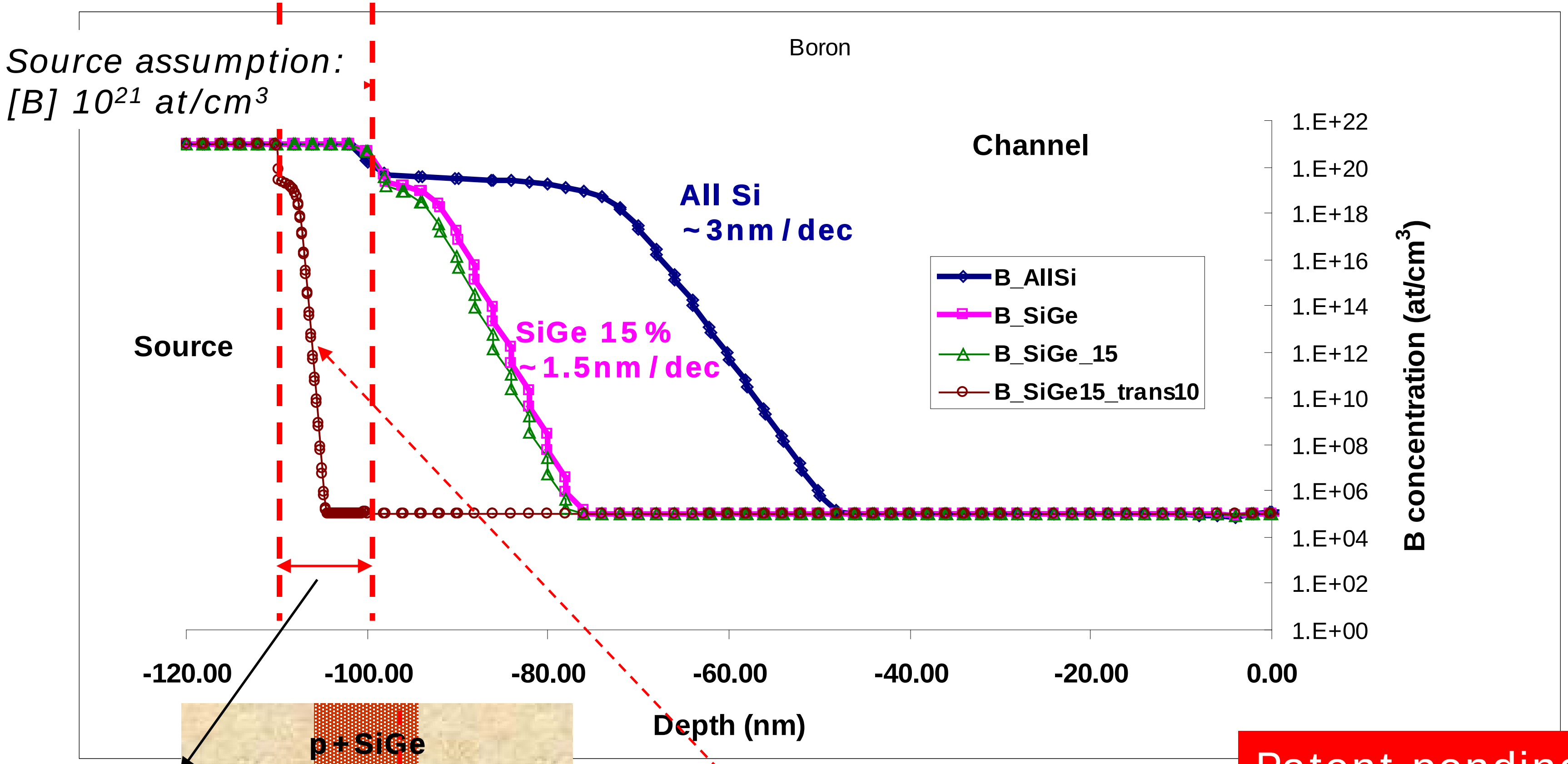


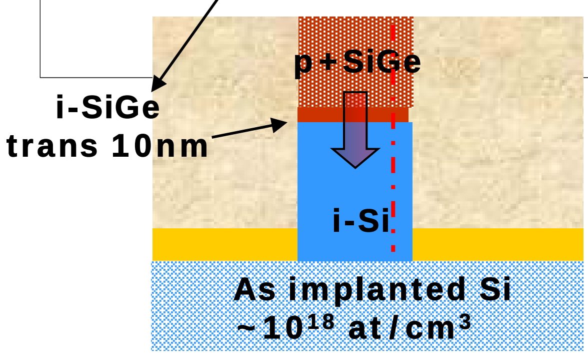
Onset is delayed for SiGe source!





Doping profiles?



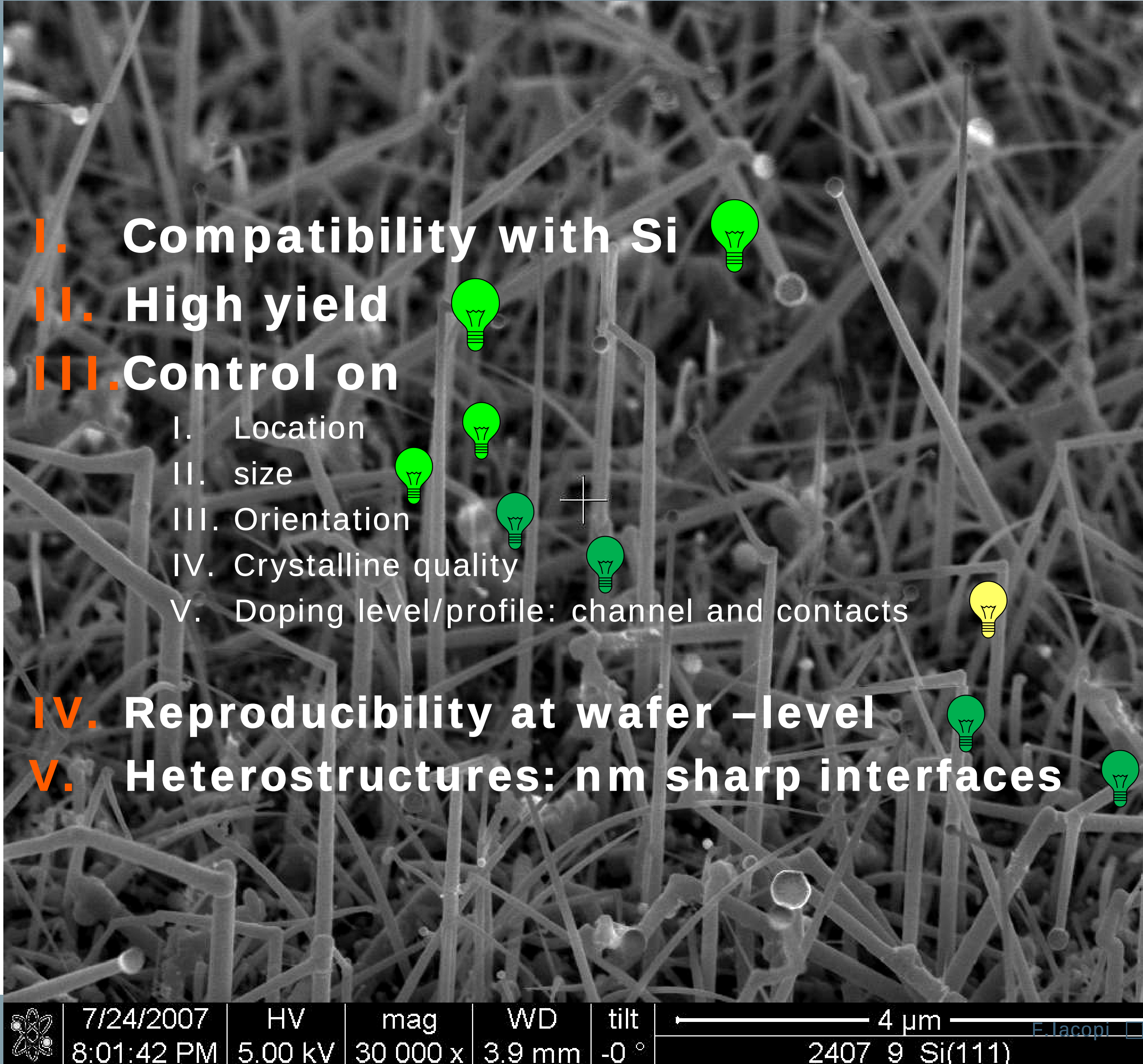


Patent pending

Steepest profile, 16 decades in ~6nm!!

I. **Compatibility with Si**
II. **High yield**
III. **Control on**
   I. Location
   II. size
   III. Orientation
   IV. Crystalline quality
   V. Doping level/profile: channel and contacts

IV. **Reproducibility at wafer –level**
V. **Heterostructures: nm sharp interfaces**



Summary and outlook

1. NW extremely promising and flexible

2. NW growth: issues for μ-electronics/ wafer –scale processing
    - Si –compatible catalyst ➔ Indium with PE CVD
    - NW orientation control ➔ templated growth

3. *Seedless templated growth*
    - Solve most of the problems linked to on-wafer manufacturing
    - Tunneling nano-hetero –junctions demonstrated on 300mm wafer

4. Conclusion
    - Wafer –scale growth and fabrication of vertical hetero devices possible ***combining top-down and bottom-up approaches***
    - If growth T an issue ➔ In-seed in template

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1) Nanowire-based OneDimensional Electronics
NODE FP 06 -015783

2) SEA-NET Pronano IST-027982