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Status and Challenges for Non-Volatile Spin-Transfer Torque RAM (STT-RAM)

Mohamad T. Krounbi
S. Watts, D. Apalkov, X. Tang, K. Moon
V. Nikitin , A. Ong, V. Nikitin, E. Chen
Grandis, Inc.

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Outline

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- **Grandis Corporation Overview**
- **STT-RAM Status**
  - **MTJ Write Current Density**
  - **STT-RAM Thermal Stability**
  - **STT-RAM Scalability**
  - **Test Chip results**
- **Latest Advances in write current performance**
  - **Dual MTJ Design**
  - **Partial perpendicular Anisotropy**
- **Conclusions**

***STT-RAM: Spin Transfer Torque Random Access Memory**

Grandis Corporation Update

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- **Joint Development Program with Hynix Semiconductor moving ahead fast**
  - Hynix has large team working on STT-RAM, expect fully-functional STT-RAM chips this year
  - Major paper on high-density STT-RAM chip operation accepted for presentation at IEDM 2010
- **Significant progress in MTJ development since last year**
  - 2x reduction in write current, 30% stability improvement, 10-20% TMR improvement
  - In-plane STT-RAM shows clear, scalable path to below 20 nm technology
- **Met Phase I targets on $15M DARPA contract six months ahead of schedule**
  - Demonstrated <0.25 pJ MTJ write energy, $8.6M Phase II begins in September 2010
- **Presented key papers at VLSI Symposium, IEEE IMW & other major conferences**
  - Covered latest advances in MTJ materials, scalability of in-plane STT-RAM technology, read disturb and write error rates, and design requirements for thermal stability and 1 Gb STT-RAM chips
- **Latest granted patents take U.S. patent total to 55**
  - Grandis now has 192 filed patent applications and 68 issued patents worldwide
- **Significant increase in worldwide interest in STT-RAM over past 12 months**
  - Strong interest from multiple parties in licensing and partnering with Grandis

Grandis Development Partners

The Need for a New Memory Technology

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- **All existing memory technology is greatly challenged beyond 45 nm**
  - SRAM: high power consumption, leakage increasing 10X with each technology node
  - DRAM: refresh current increasing, incompatible process for embedded applications
  - Flash: limited endurance, high write power, very slow write speed, MLC & aggressive scaling leading to reduced performance and complicated controller
- **Power consumption in both mobile and data center applications is now a real issue**
  - Incorporating STT-RAM in mobile applications can dramatically reduce standby power
  - Replacing DRAM with STT-RAM in data centers can reduce power by up to 75%
- **Memory performance is fast becoming the key bottleneck that limits system performance**
  - Critical applications are becoming more data-centric, less compute-centric
  - Instant-on is becoming a requirement for many applications
- **These problems create an opening for an alternative, high-density, high-speed, non-volatile random access memory**

STT-RAM versus Conventional MRAM

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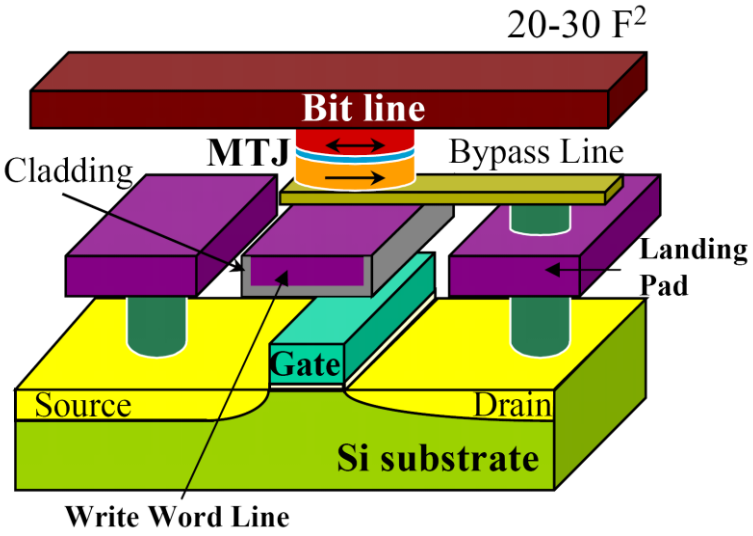
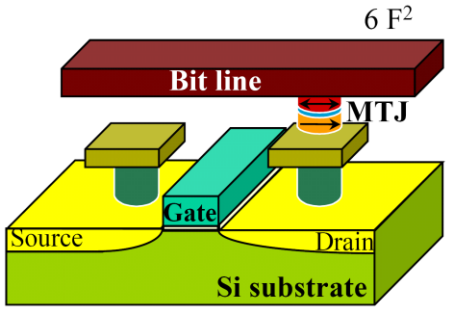
Conventional MRAM Cell



STT-RAM Cell



Write Current: $I_{sw} \sim 1 / Volume$

$I_{sw} \sim Volume$

Key Advantages over conventional MRAM:

- **Excellent write selectivity** <— Localized spin-injection within cell
- **High scalability** <— Write current scales down with cell size
- **Low power consumption** <— Low write current (<100 μA)
- **Simpler architecture** <— No write line, no by-pass line and no cladding
- **Faster operation** <— Multibit (parallel) writing compatible

The Solution: STT-RAM

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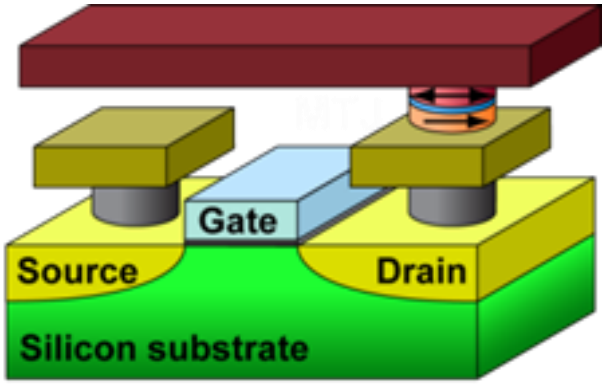
- **STT-RAM is an evolution in magnetic storage from hard disk drives to solid-state semiconductor memory**
  - Uses spin-polarized current ("spintronics") to write magnetic bits
  - Non-volatile, random-access memory with no moving parts
  - Key building block is the magnetic tunnel junction (MTJ)
  - MTJ is currently in high volume production as a Read sensor in HDD

- **STT-RAM has all the characteristics of a universal memory**
  - Non-volatile
  - Highly scalable
  - Low power consumption
  - SRAM read/write speed
  - Unlimited endurance
  - DRAM & Flash density (6 F^2)
  - Multi-level cell capability



- **STT-RAM uses existing CMOS technology with 2-3 additional masks and less than 3% cost adder**

MTJ Junction in Recording Head Technology

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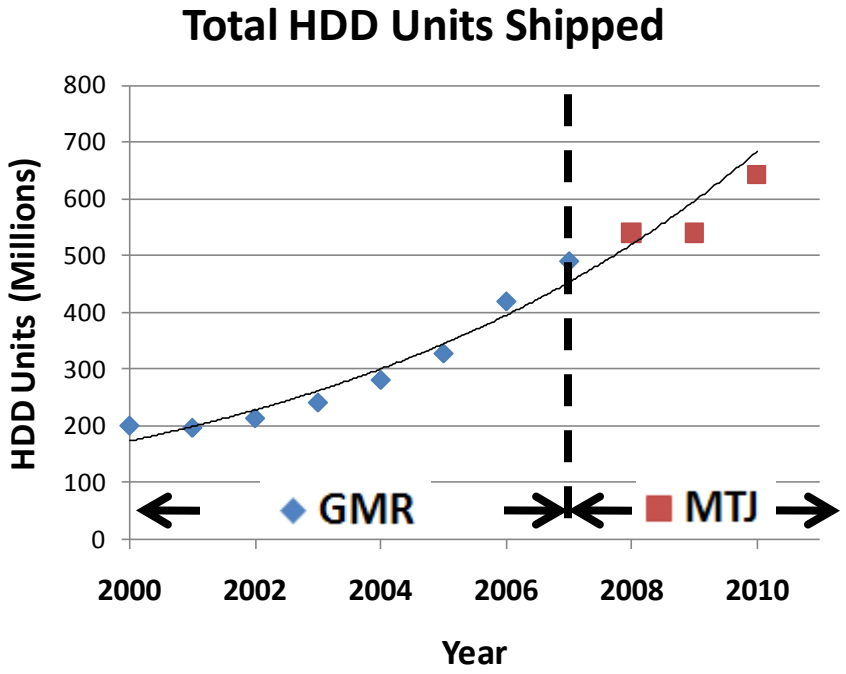
Critical Elements of the MTJ cell

- **MTJ material and stack** <— AFM pining, spin-injection, free layer properties
- **MTJ annealing** <— Time and temp. to form max TMR, low α, and high η
- **MTJ patterning** <— Damage free stack & CD control
- **Capping & post processing** <— Damage free stack

HDD Read Head Experience

- Average 3 MTJ junctions per 1 HDD
- Over 5 billion MgO-MTJ's shipped
- Current density in MTJ exceeds 5 MA/cm^2 (STT writing current ~ 1 MA A/cm^2)
- Manufacturability, reliability and endurance of MgO-MTJ is proven



STT-RAM Technology Acceptance

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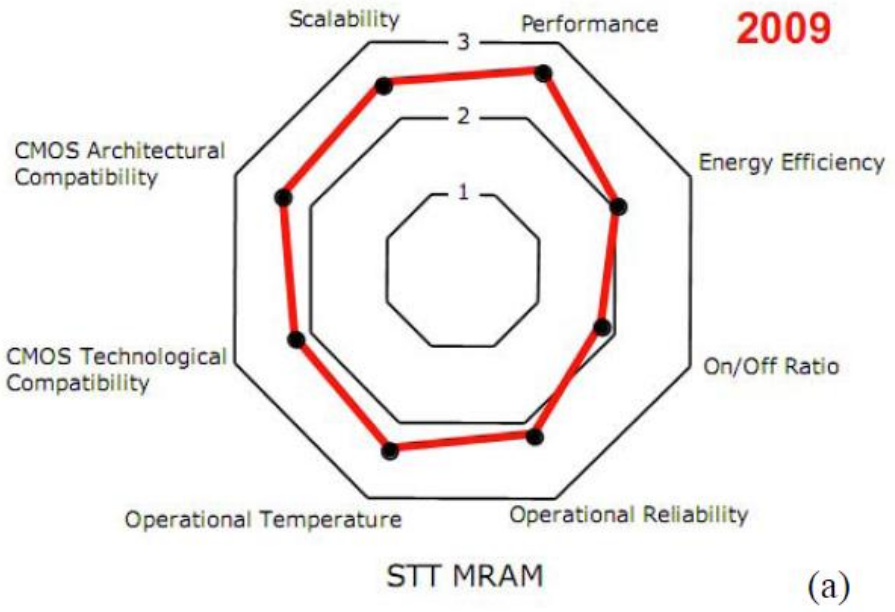
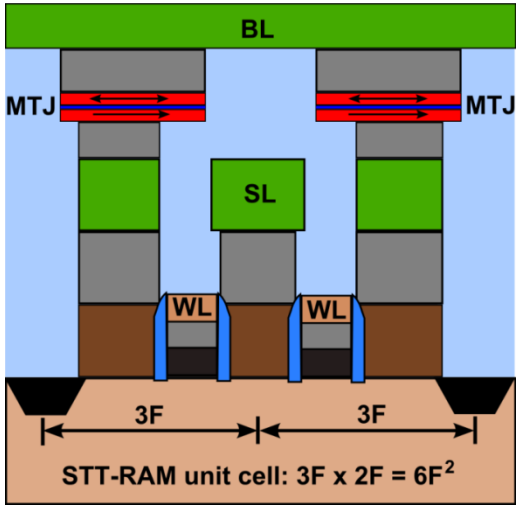
- **Experts and major companies across the semiconductor industry now accept that STT-RAM is the leading next-generation memory solution**
  - **ITRS 2009** roadmap includes STT-RAM table due to its closeness to production
  - **Samsung**, the world's largest memory manufacturer, publicly states that STT-RAM and PCM are the two viable next-generation memory technologies
  - **IBM** lists STT-RAM as a future storage class memory (in addition to PCM and RRAM)
  - Independent academic studies (e.g. from Carnegie Mellon University) show that STT-RAM is a viable technology even for replacing hard drives in the long term



Source: ITRS Roadmap for Semiconductors, Dec. 2009

STT-RAM leads all other memory technologies across the 8 ITRS key attributes



STT Write Mechanism

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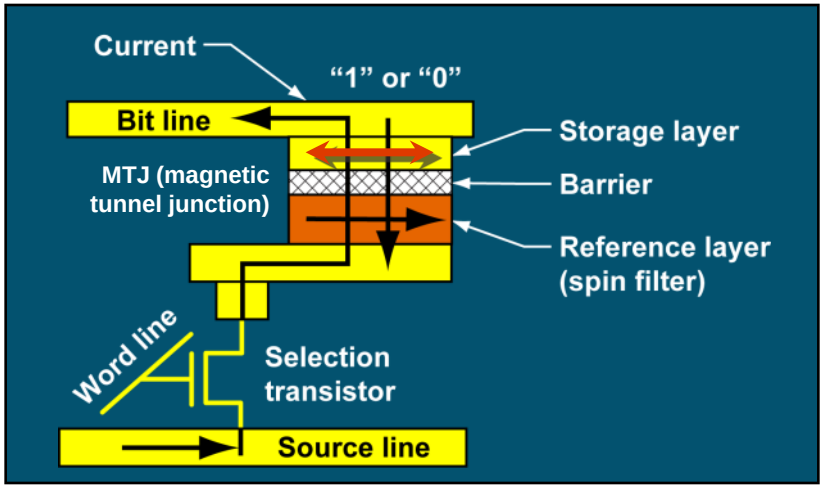
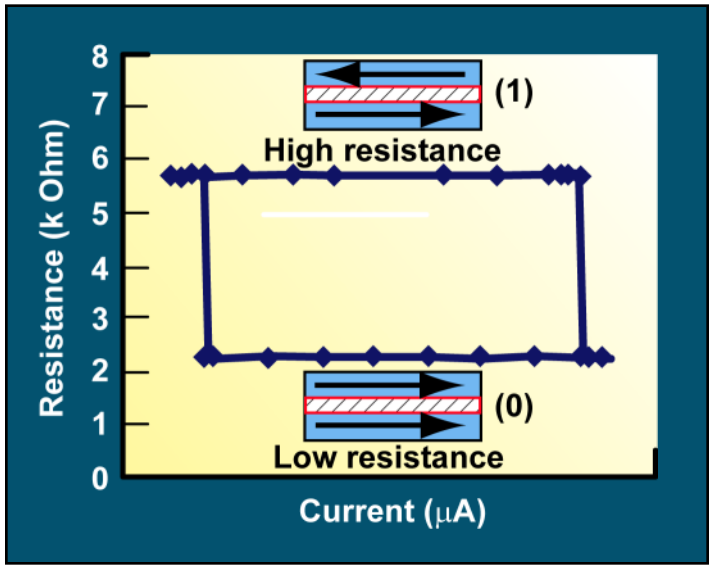
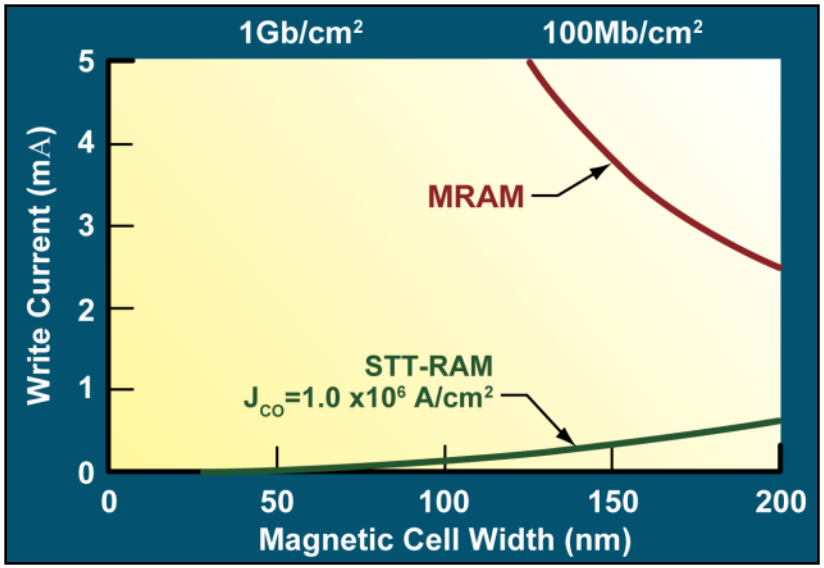
- **Spin-transfer torque writing**
  - Uses spin-polarized current instead of magnetic field to switch magnetization of storage layer
  - Has low power consumption and excellent scalability







Intensified Development of STT-RAM

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Nov. 2009: Korean Government updates on progress of $50M STT-RAM program with **Samsung** and **Hynix**, installs 300 mm STT-RAM facility at Hanyang University

Dec. 2009: **TSMC** and **Qualcomm** describe 45 nm low power embedded STT-RAM process and design at IEDM

Dec. 2009: Also at IEDM, **Hitachi** & Tohoku University present MTJ SPICE model, and **Intel** presents design space study and requirements for STT-RAM in embedded applications

Dec. 2009: France launches €4.2M SPIN project with 11 partners including LETI, Spintec & **Crocus**, one of project goals is to develop magnetic FPGAs

Feb. 2010: **Toshiba** describes a 64 Mb STT-RAM using perpendicular MTJs and 65 nm CMOS at ISSCC conference

Apr. 2010: **Everspin** takes MRAM to higher densities, begins sampling 16 Mb MRAM targeted at the aerospace, automotive, industrial and RAID storage markets, also continues to develop STT-RAM for future technology nodes

Jun. 2010: **Grandis**, **Hitachi** and **Fujitsu** all present papers on STT-RAM at VLSI symposium covering STT-RAM thermal stability, scalability and MLC

Dec. 2010: **Hynix** and **Grandis** to present joint paper on high-density STT-RAM chip operation at IEDM

Standalone STT-RAM Product Roadmap

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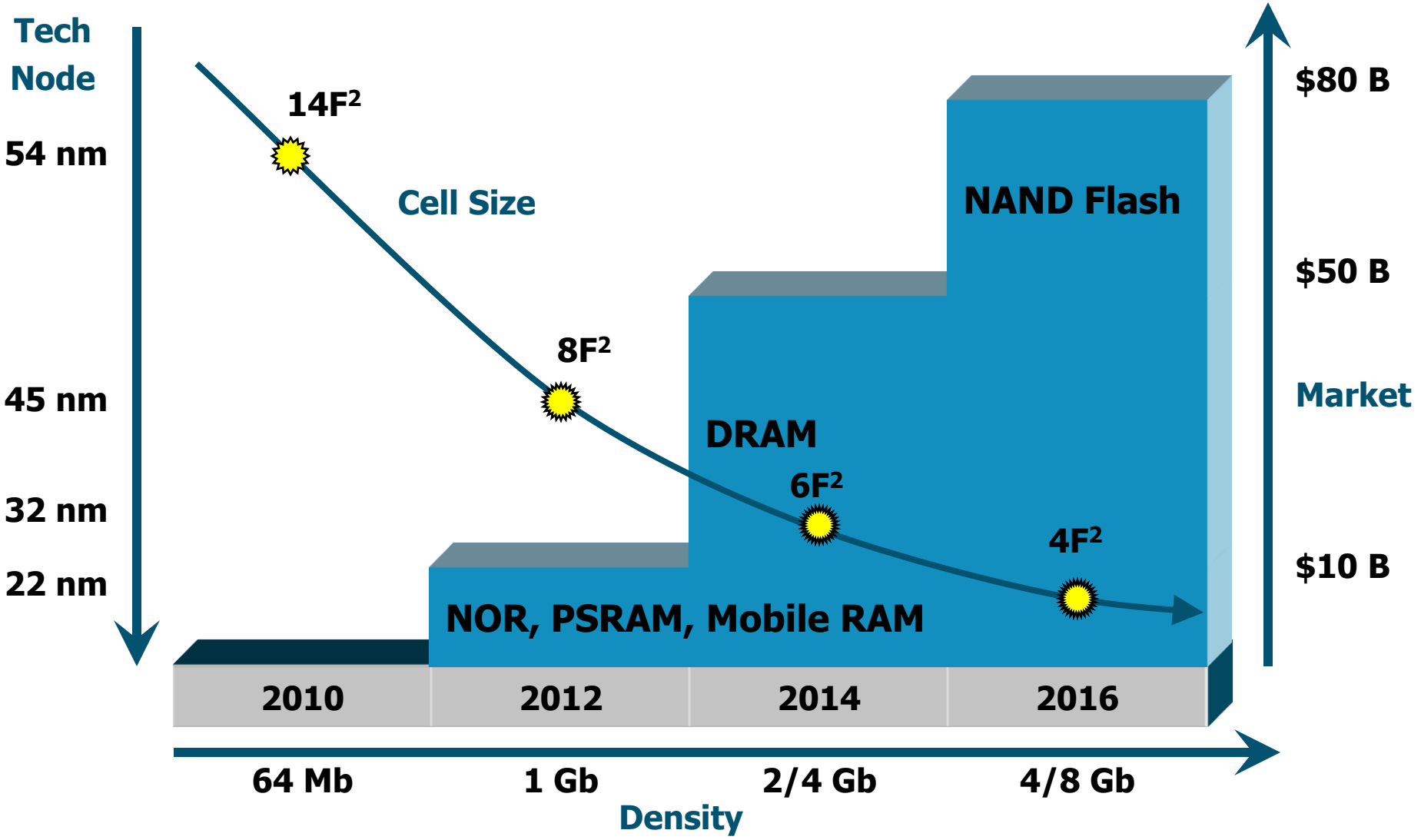

Embedded STT-RAM Product Roadmap

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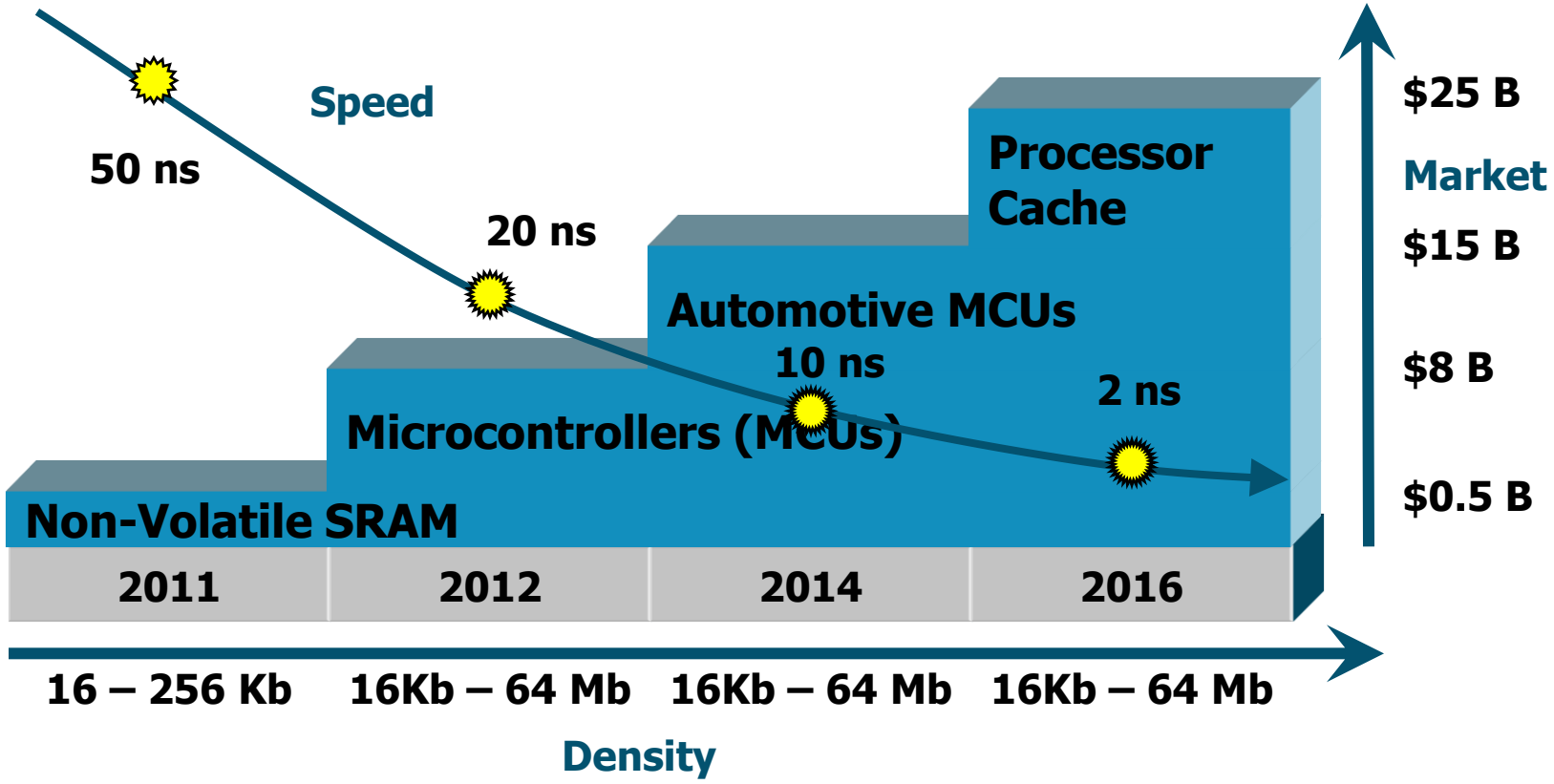
- **Initial applications: replace embedded non-volatile memory in industrial, medical, consumer and military microcontroller units**
- **STT-RAM is scalable alternative to existing MRAM solution**



 Proprietary and Confidential

STT-RAM Write Current Scalability

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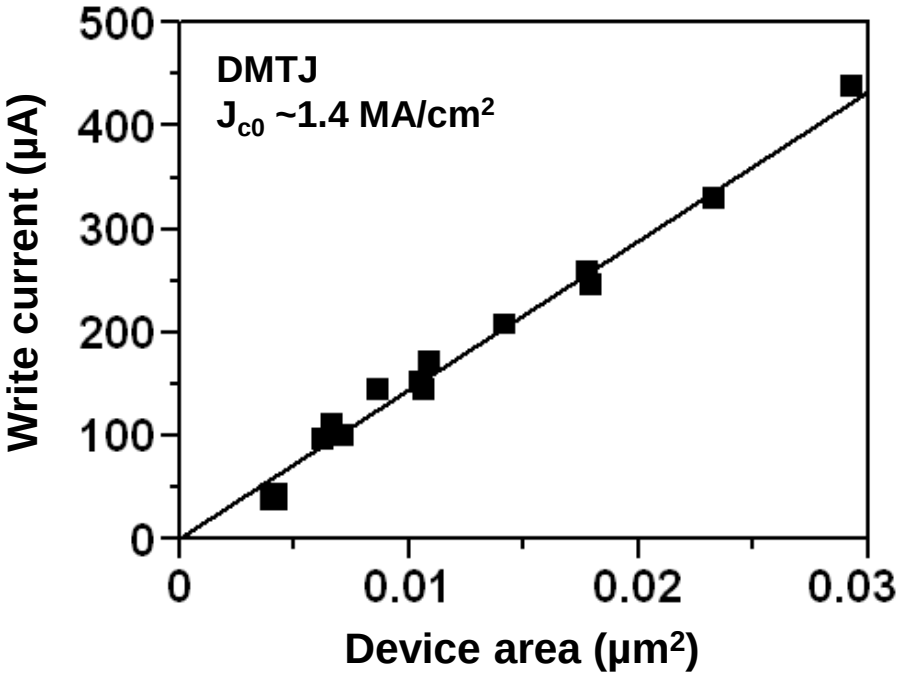
- **STT-RAM write current scales linearly with device area**
- **Confirmed experimentally over a wide range of device sizes**
  - At 90 nm: write current ~150 μA (device area ~0.013 μm^2)
  - At 45 nm: write current ~40 μA (device area ~0.003 μm^2)



STT-RAM Minimum Cell Size

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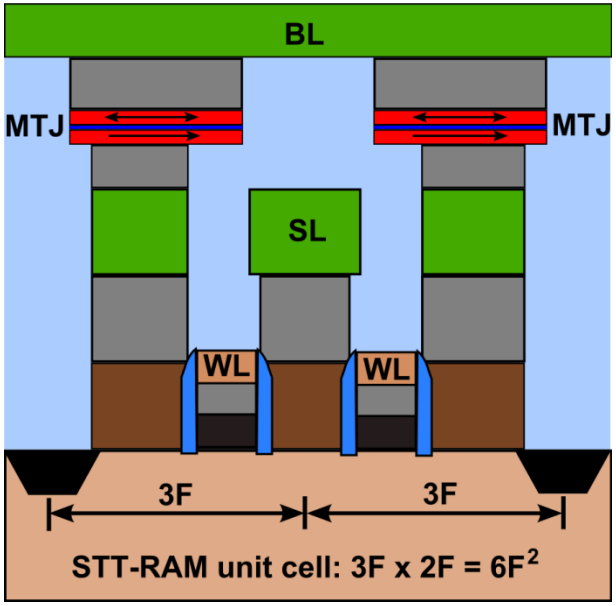
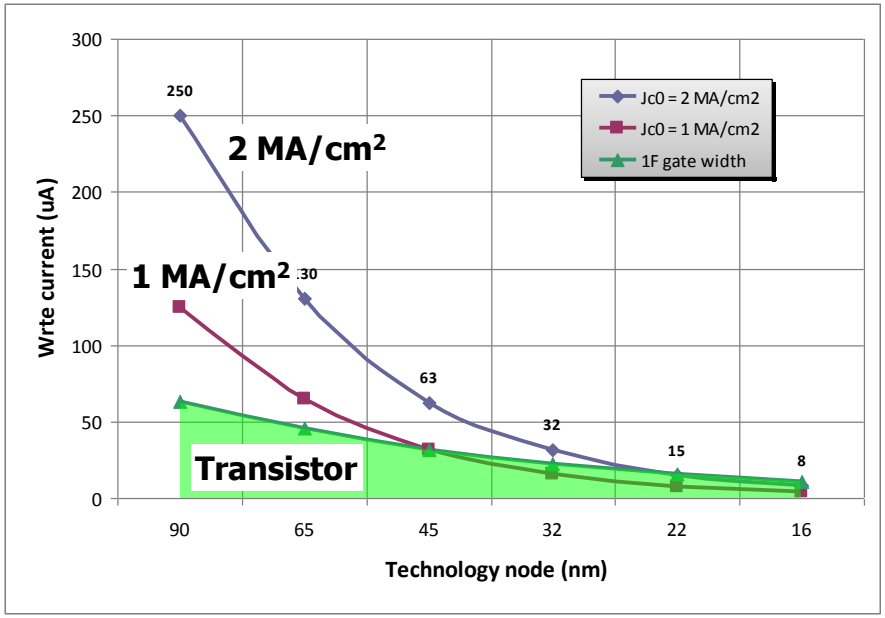
- **6 F^2 is standard minimum cell size with shared source line architecture**
  - Minimum 1 F gate width transistor can drive 6 F^2 cell beyond 45 nm





- **Vertical transistors, multi-level cells and/or cross-point architectures will enable further cell size reduction to 4 F^2 and beyond**

STT-RAM Key Parameters and Challenges

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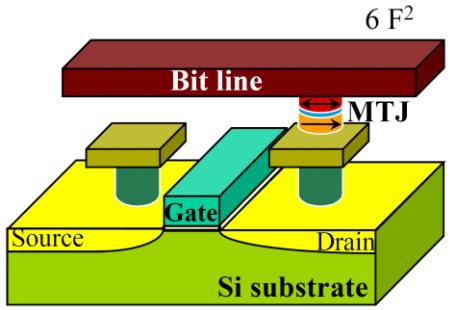
- **J_{c0} (write current density)** => cell size, write speed
- **TMR (read signal)** => sense margin, read speed
- **Δ (thermal stability)** => data retention, read disturb, memory size, etc.
- **V_{BD} (MTJ breakdown voltage)** => lifetime, endurance

Key challenge is achieving low STT write current density and high thermal stability at the same time

STT-RAM Cell



Write current:

$$I_{c0} = \frac{2\alpha A M_S t_F e}{\eta\,\hbar}\left[H_K + \frac{H_d}{2}\right], \qquad H_K = H_{Intrisic} + H_{shape} + \ldots$$

Thermal stability:

$$\Delta = \frac{M_S \mathrm{H_K}\, t_F A}{2k_B T} \propto \frac{M_S^2 t_F^2 A}{k_B T}$$

Assuming intrinsic anisotropy is much smaller than shape anisotropy

STT-RAM Resistance Distribution

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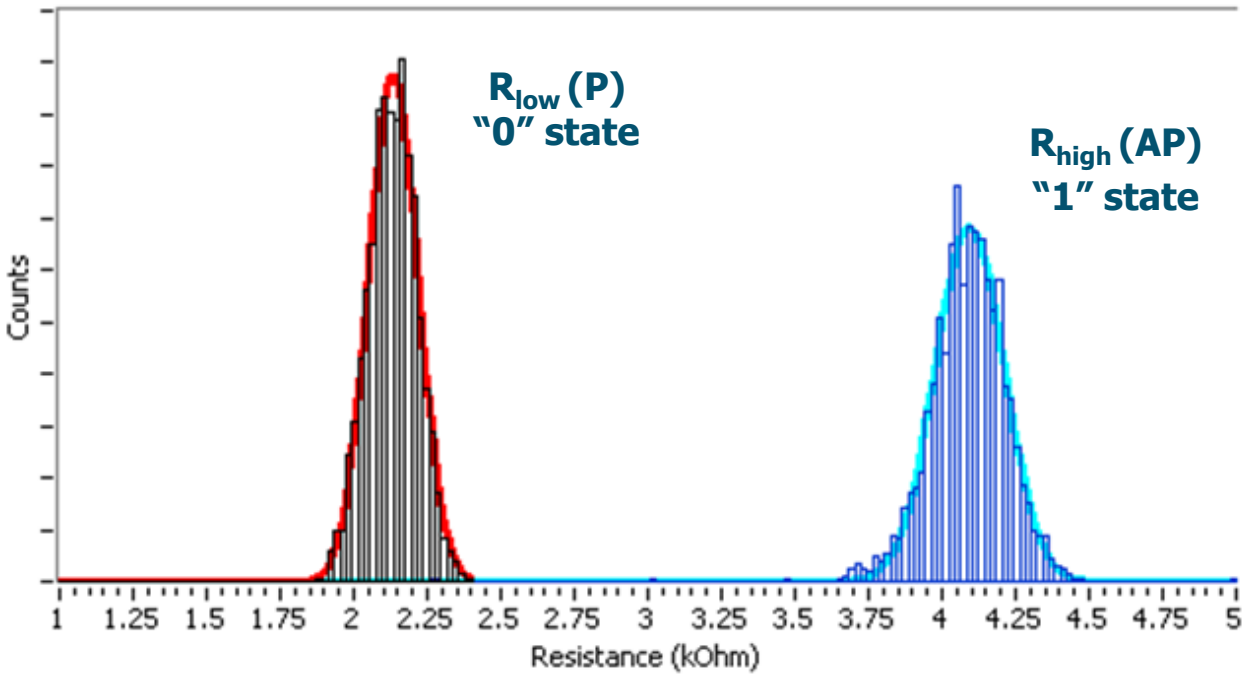
- **Large separation between resistance states and small process distribution provide excellent read characteristics**
  - TMR (Tunneling Magnetoresistive) signal ~100%
  - R_{low} distribution sigma 4% (1σ), R_{high} distribution sigma 3% (1σ)
  - $R_{high} - R_{low}$ separation = 20σ



STT-RAM Write Voltage Distribution

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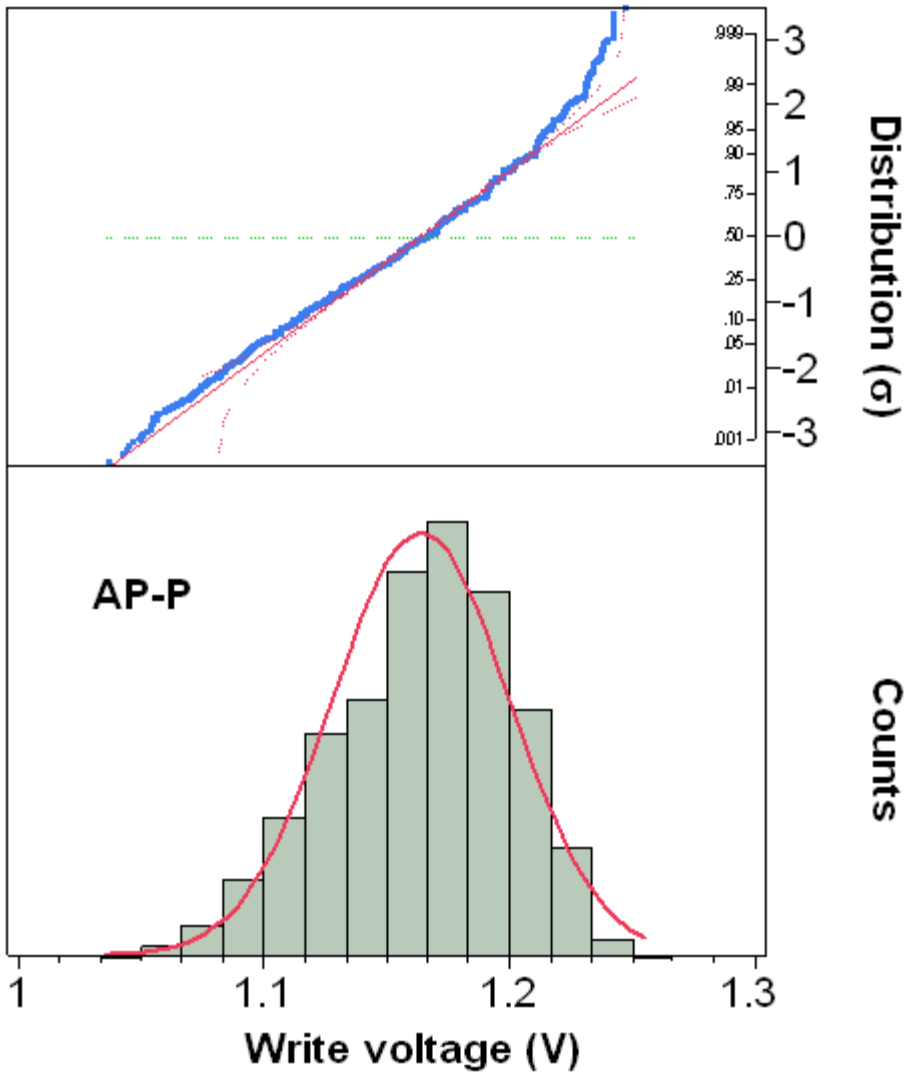
- **Mean write voltage ~1.15 V**
  - Includes voltage across both transistor and MTJ
  - MTJ write voltage ~0.4 V
- **Write voltage distribution ~3% (1σ) or ~9% (3σ)**
  - Pulse width 50 ns
- **Target write voltage distribution for STT-RAM products is <15% (3σ)**



STT-RAM Endurance

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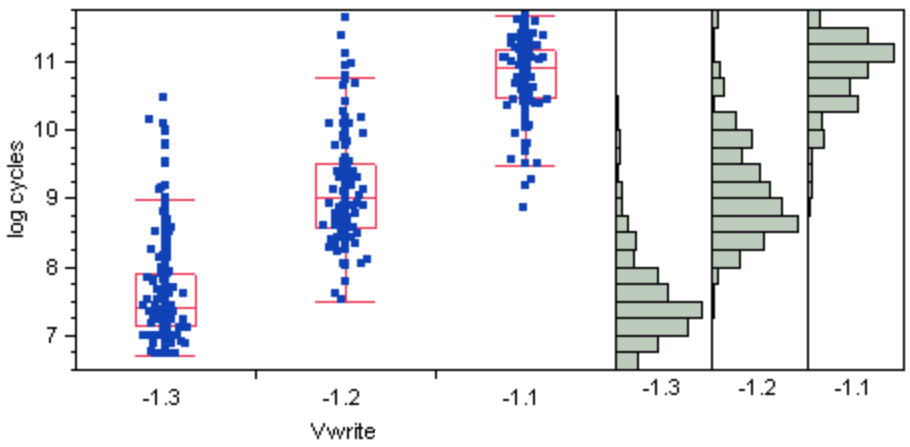
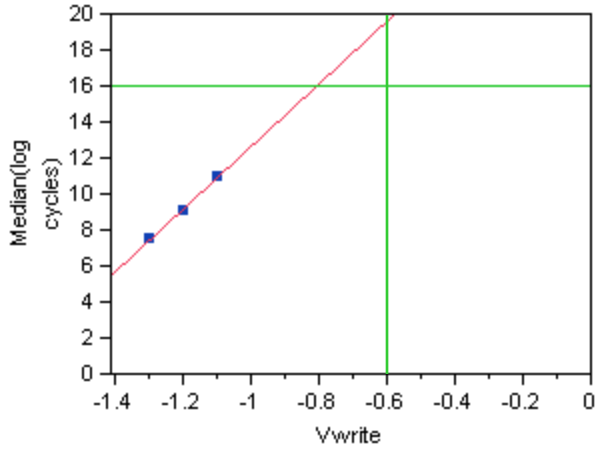
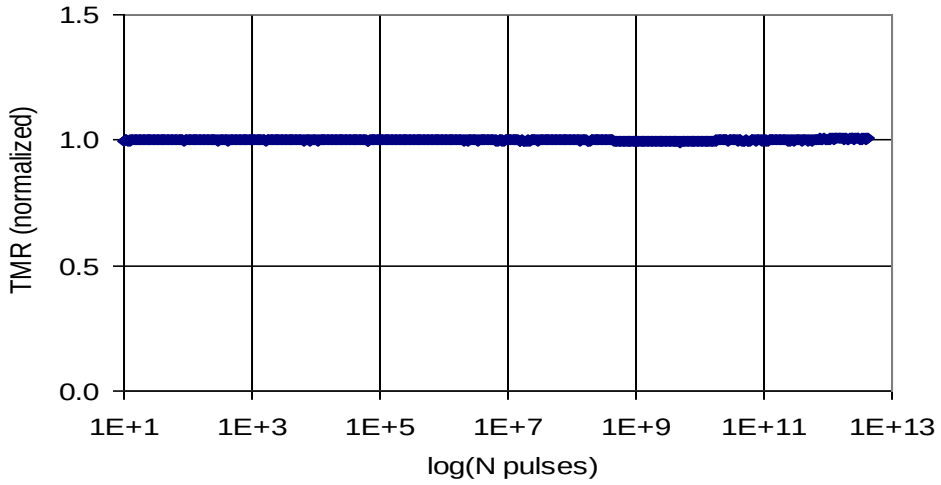
- **Unlimited write endurance (>10^{16} cycles) projected from TDDB tests with stressed voltage and temperature**
  - 10^{13} endurance demonstrated to date under real operating conditions







Latest Developments

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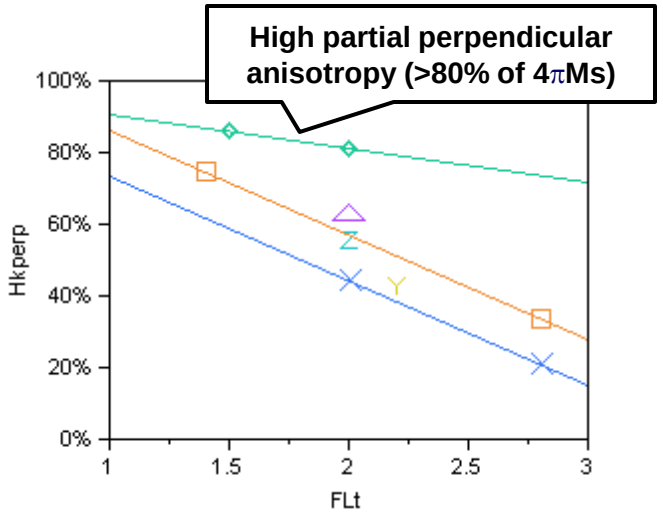
- **New class of in-plane MTJ structures with high partial perpendicular anisotropy excellent for maintaining thermal stability as devices shrink**
  - Perpendicular anisotropy approaching 90% of $4\pi M_s$ achieved
  - Slow drop with increasing free layer thickness excellent for scaling

Standard In-plane MTJ

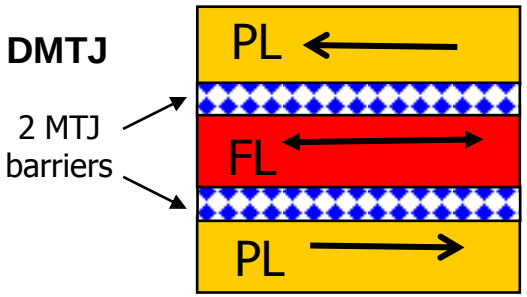
$I_{c0}/\Delta \sim \alpha/\eta\ [1 + H_d/(2H_k)]$

In-plane MTJ with Partial Perpendicular Anisotropy

$I_{c0}/\Delta \sim \alpha/\eta\ [1 + (H_d - H_{k\perp})/(2H_k)]$



- **Dual MTJ structures with two barrier layers significantly increase STT efficiency and reduce J_{c0} while maintaining thermal stability**



MTJ Write Current Density (J_{c0})

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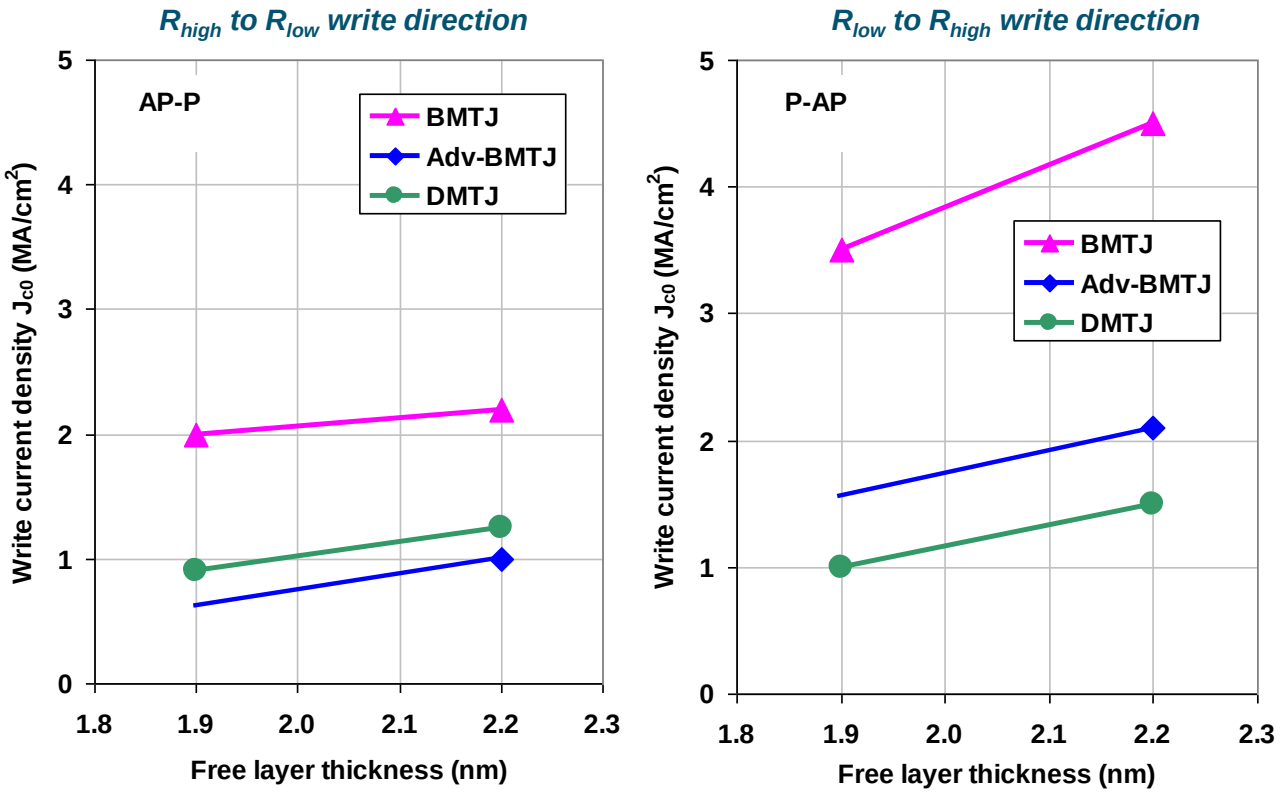
- **Average write current density J_{c0} for advanced MTJs is 1–2 MA/cm²**
  - Advanced MTJ (Adv-BMTJ) devices with partial perpendicular anisotropy ~1–2 MA/cm²
  - Dual barrier MTJ (DMTJ) devices have lower and more symmetrical J_{c0} ~1 MA/cm²



All J_{c0} data quoted by Grandis are obtained statistically by fitting write current vs device area data from thousands of MTJs over a wide range of device sizes

Achieving High TMR with DMTJ

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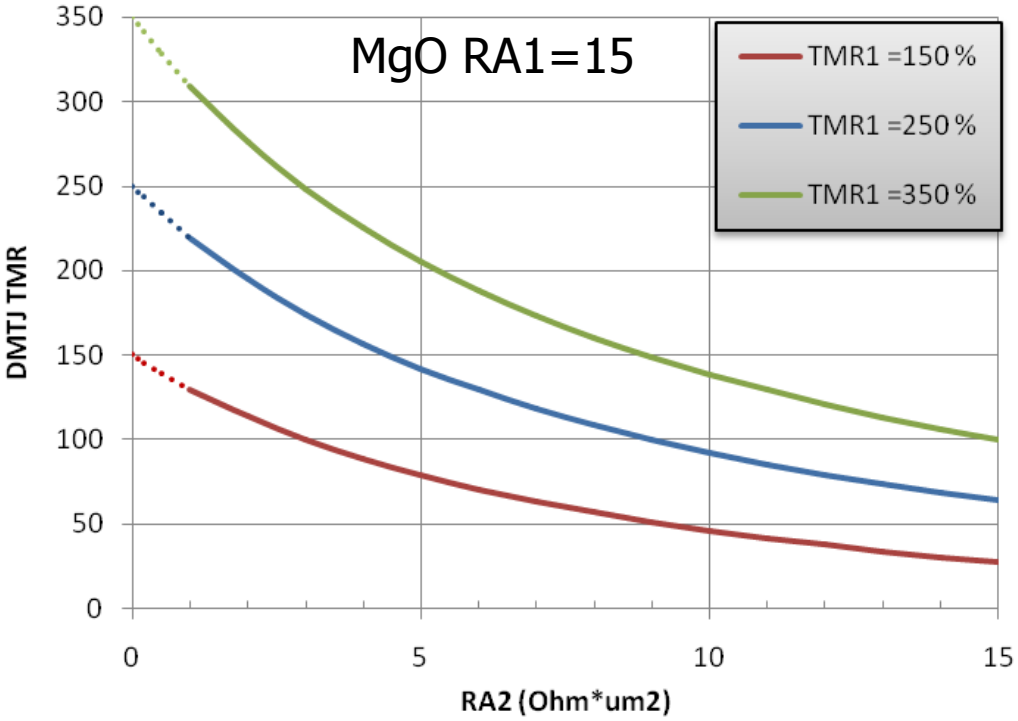

- High TMR can be achieved with DMTJ with reduced 2nd MgO barrier thickness
- High intrinsic TMR and larger MgO barrier asymmetry gives higher TMR

Effect of Partial Perpendicular Anisotropy on Switching Current

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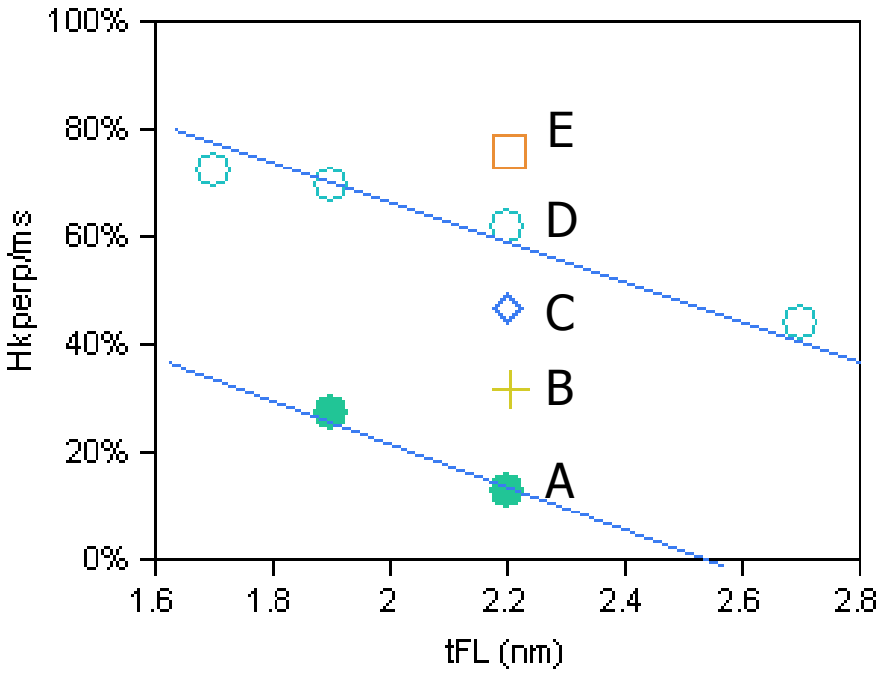
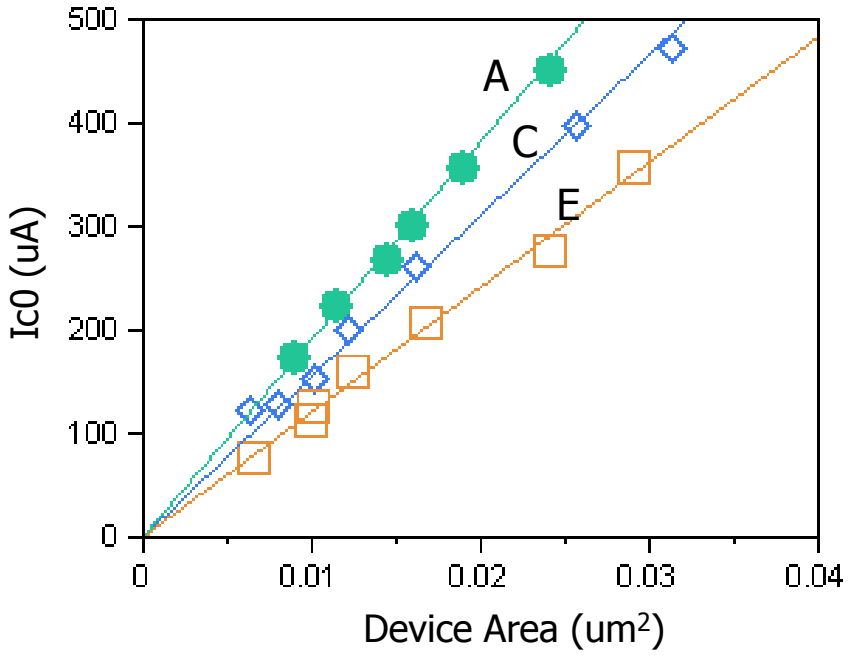
Partial Perpendicular Anisotropy Measured in FMR and VSM



Improved Switching Current Measured in QSW



- Grandis know-how resulted in obtaining films with High Partial Perpendicular Anisotropy (as measured by FMR and VSM)
- Switching measurements confirm expected improvements in switching current

Switching Current Scalability with FL Thickness

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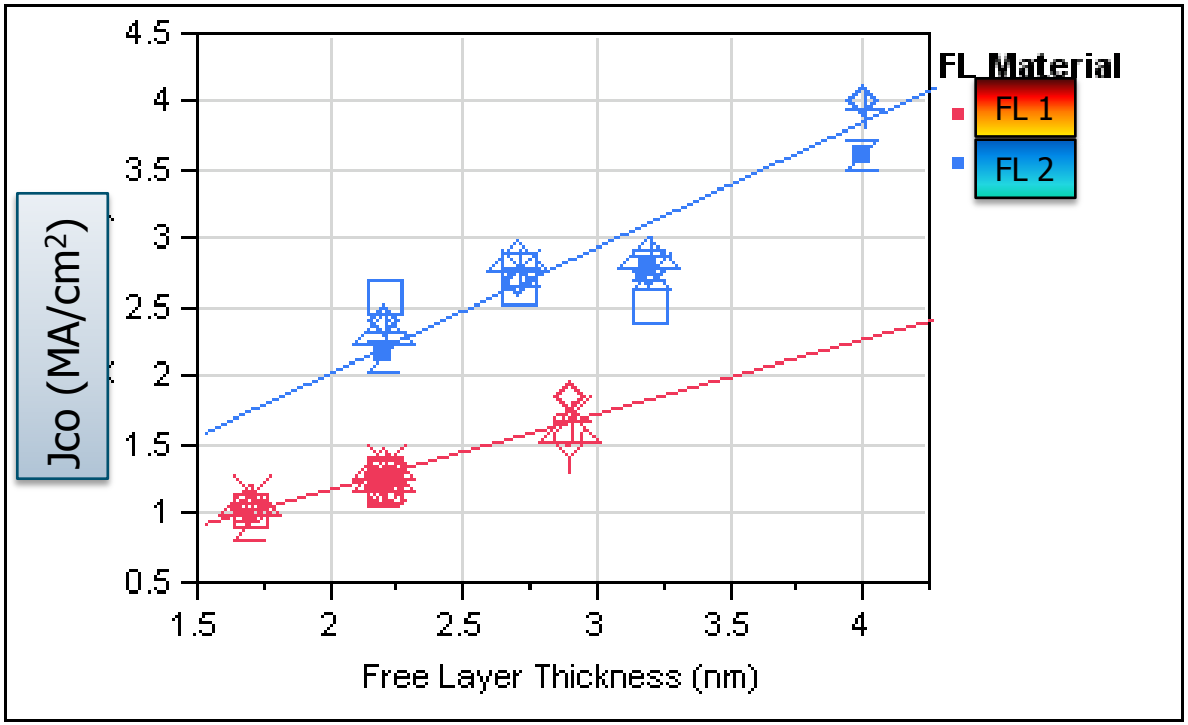
Grandis EXPERIMENTAL DATA confirms Jco scaling with FL thickness



- The graph above shows Jco scaling with free layer thicknesses for 2 different FL materials
- Both FL types show Jco proportional to FL thickness

* Each point on the graph is an average of ~100 MTJ devices

Maintaining Thermal Stability

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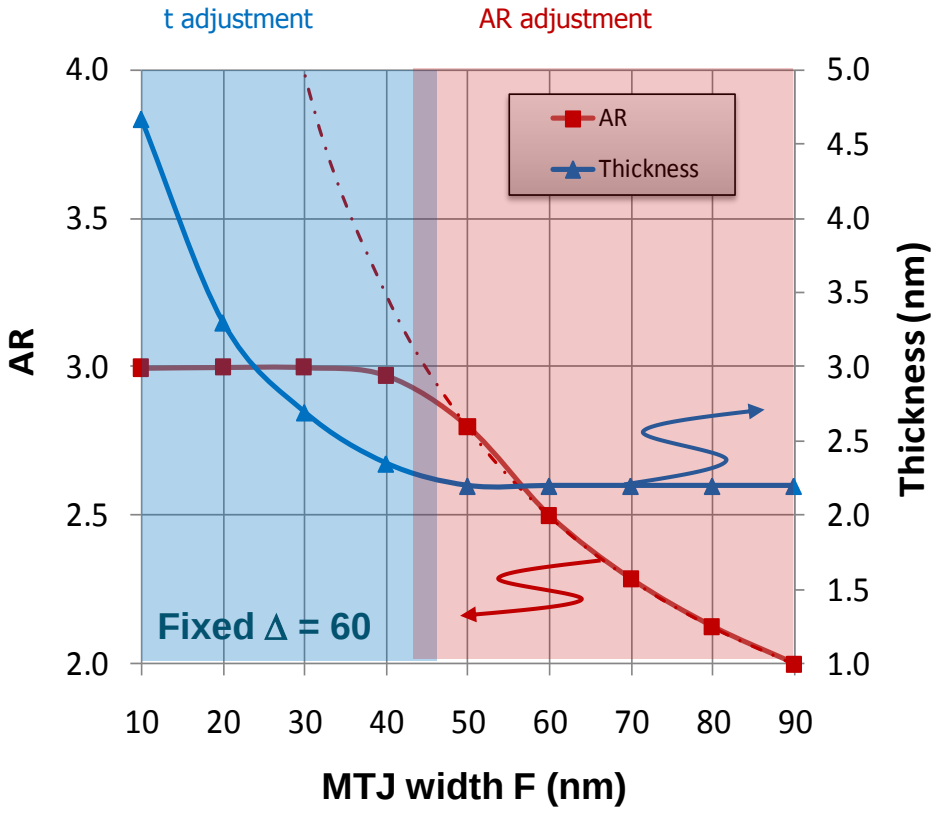
- **Several approaches to maintaining thermal stability of smaller devices:**
  - Increase MTJ aspect ratio (AR) – but not applicable to P-STT-RAM
  - Increase MTJ free layer thickness (t)
  - Use innovative MTJ materials or processes



D. Apalkov, et al., IEEE Trans. Magn. 46, 2241 (2010)

Conclusions

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- **Spintronics (spin electronics) is a rapidly emerging field**
  - STT-RAM and spin logic will have a significant impact on technology in the 21st century, enabling a new era of instant-on, high-speed portable devices with extended battery life
- **STT-RAM has a huge potential market as a universal, scalable memory**
  - It can replace eSRAM & eFlash < 32 nm, DRAM < 28 nm, and ultimately replace NAND Flash as a storage class memory at 22 nm and beyond
- **Worldwide STT-RAM development has increased significantly**
  - Government programs in the US (DARPA), Korea, Japan, France, and Singapor
  - IBM, Qualcomm, Intel, Micron, Everspin, TSMC, Hynix, Samsung, Renesas, Toshiba, Hitachi, Fujitsu, …
- **Grandis is focused on commercializing STT-RAM in 2–4 years**
  - Low MTJ write current density achieved, now the focus is on chip distributions and yield
  - Characterization of thermal stability through read disturb and write error rates is critical
  - In-plane STT-RAM with partial perpendicular anisotropy is scalable beyond 20 nm

Acknowledgement:

Grandis colleagues: D. Apalkov, A. Driskill-Smith, D. Lottis, V. Nikitin, X. Tang, S. Watts, K. Moon and E. Chen

Work partially funded by NIST ATP grant, DARPA contract and NSF grants

Please visit
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for more information

MTJ Junction in Recording Head Technology

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- **MTJ material and stack** <— AFM pining, spin-injection, free layer properties
- **MTJ annealing** <— Time and temp. to form max TMR, low α, and high η
- **MTJ patterning** <— Damage free stack & CD control
- **Capping & post processing** <— Damage free stack

HDD Read Head Experience

- Average 3 MTJ junctions per 1 HDD
- Over 5 billion MgO-MTJ's shipped
- Current density in MTJ exceeds 5 MA/cm^2 (STT writing current ~ 1 MA A/cm^2)
- Manufacturability, reliability and endurance of MgO-MTJ is proven