Leakage Study of 45nm SRAM Devices with Different Layouts Using Advanced e-beam Inspection Systems

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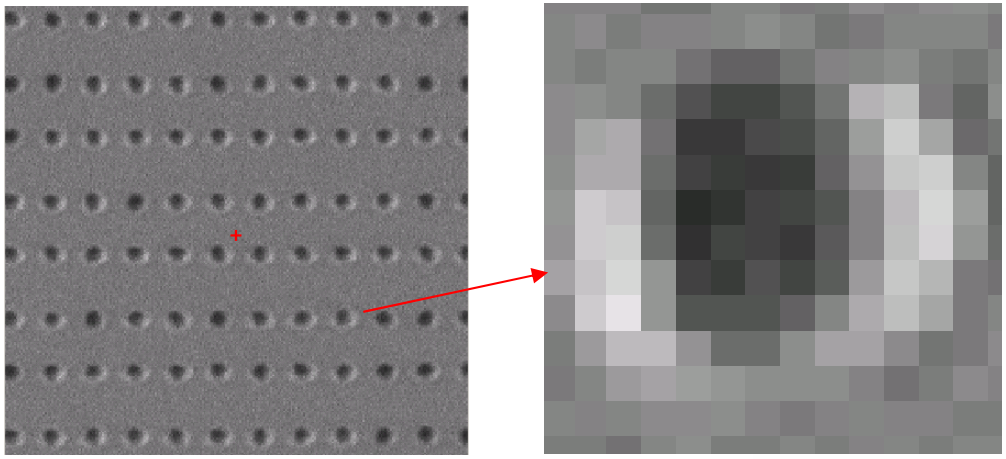
List of Topics

- About HMI
- Introduction
- Experiment Setup
- Experiment Results
- Summary

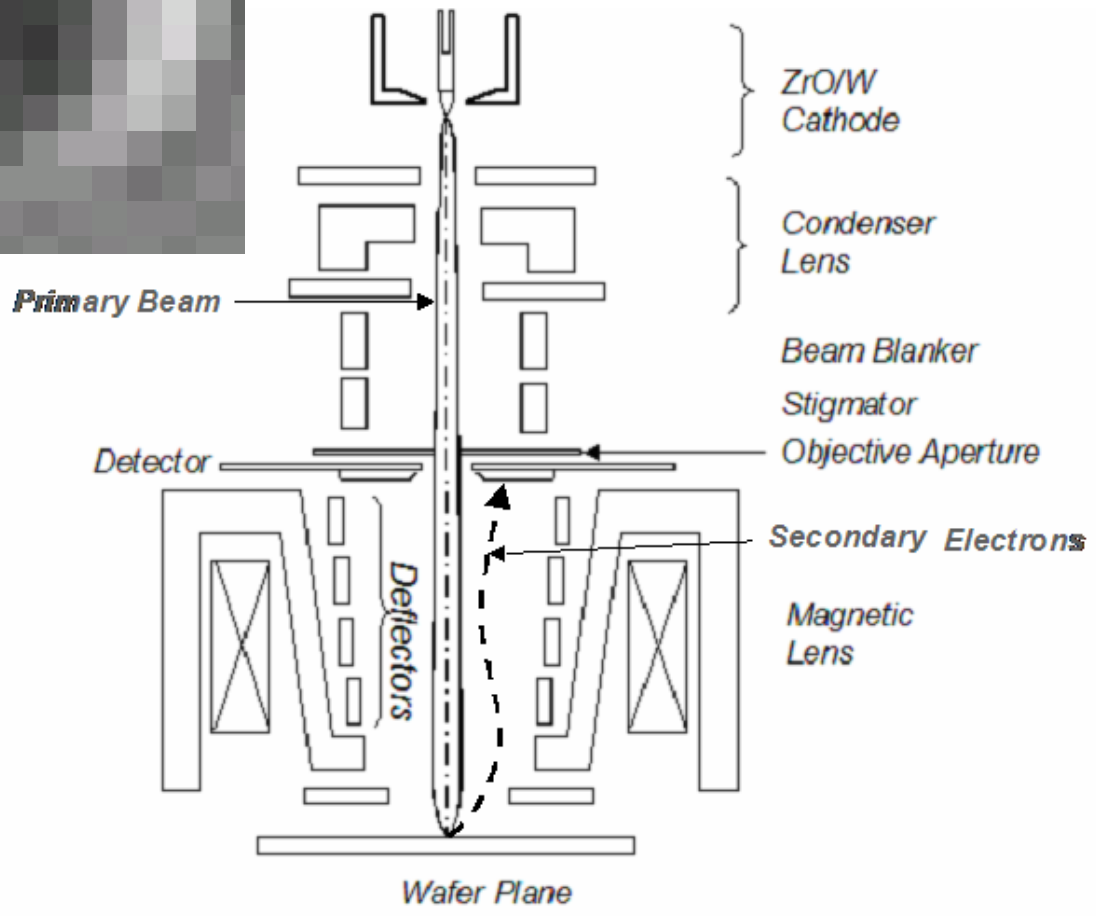
About HMI

- Founded in June 1998 at silicon valley.
- Financed by Hermes-Epitek Co.
- Well established leading EBI system provider for wafer and mask defect solution.
- 38 wafer EBI systems installed worldwide.
  - Multiple systems in leading foundry fabs.
  - Multiple systems in leading memory fabs.
  - Major image sensor manufacturer.
  - Leading automobile chip manufactures.

Introduction: EBI Basics



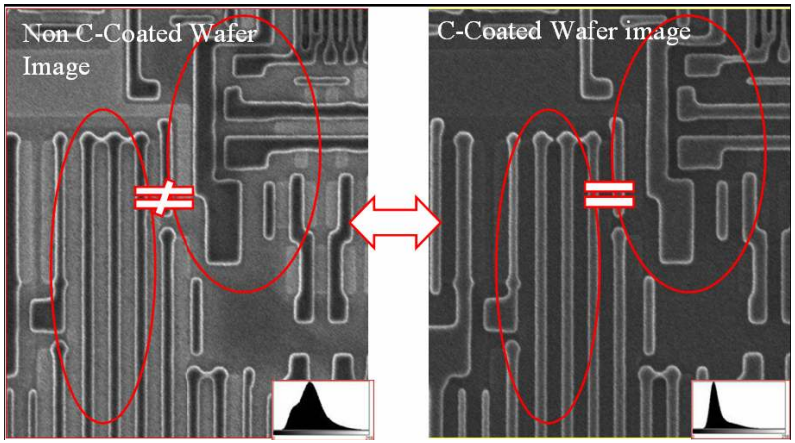
GLV of the pixel is determined by number of SE from that pixel collected by the detector



Introduction: EBI Basics

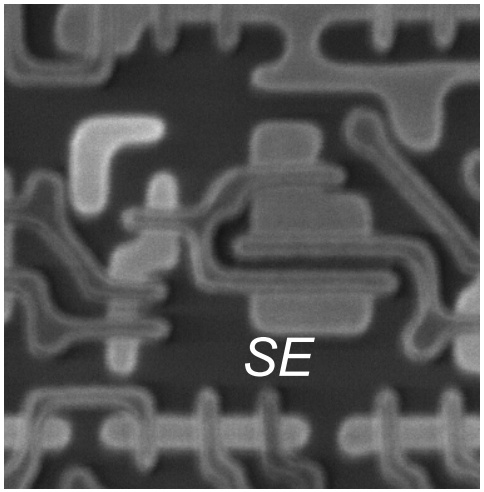
- Topography contrast (TC)
  - Physical defects
- Material contrast (MC)
  - Physical defects
- Voltage contrast (VC)
  - Electrical defects
  - Mid to high I, low or mid LE for positive mode
  - High I, High LE for negative mode

SEM Contrasts

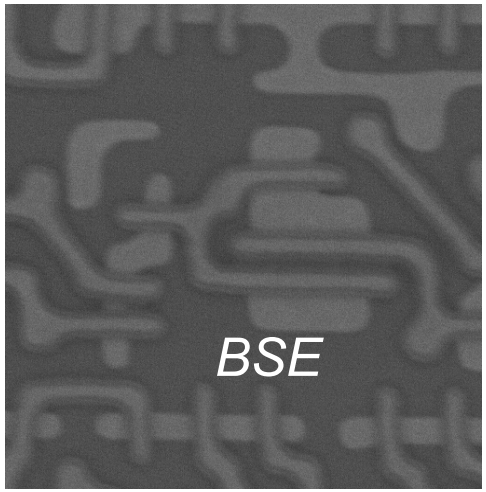


TC, MC and VC TC dominate

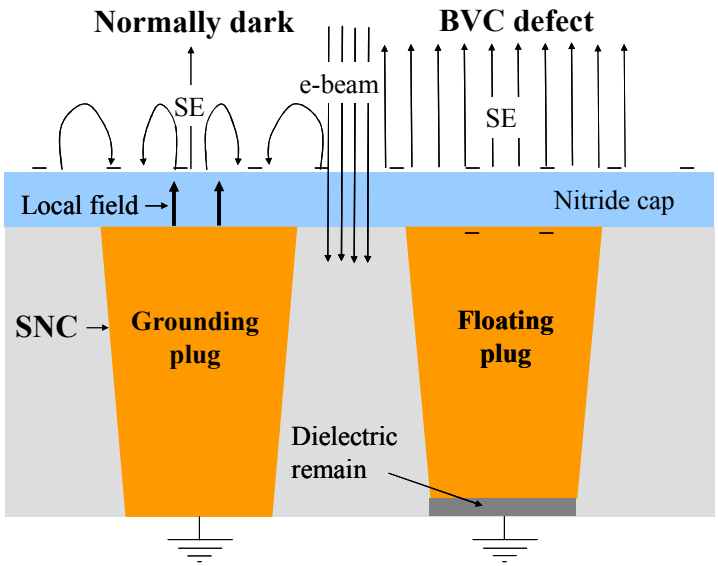
Jeong-Geun Park, et. al., Proc. of SPIE, 6299-83 (2006)

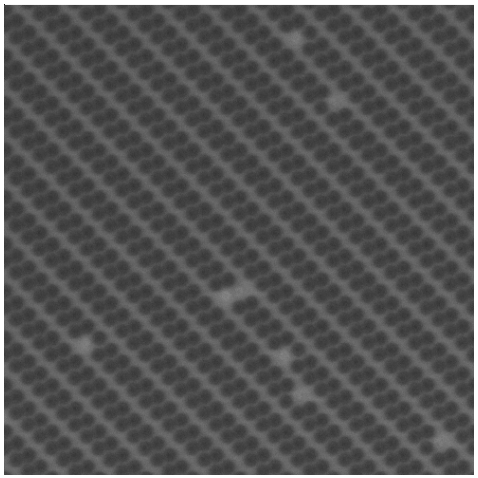


TC, MC and VC



MC dominate



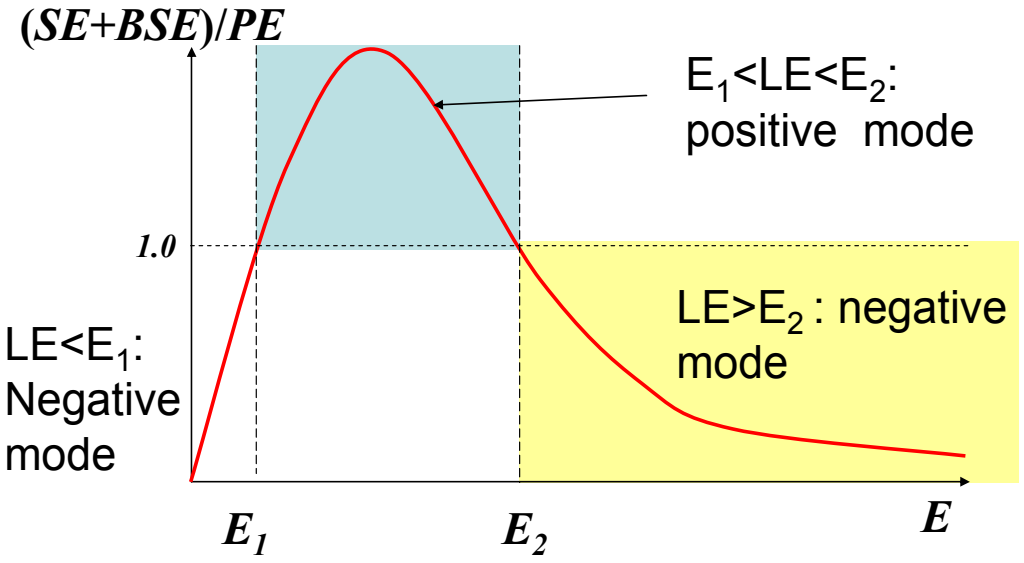


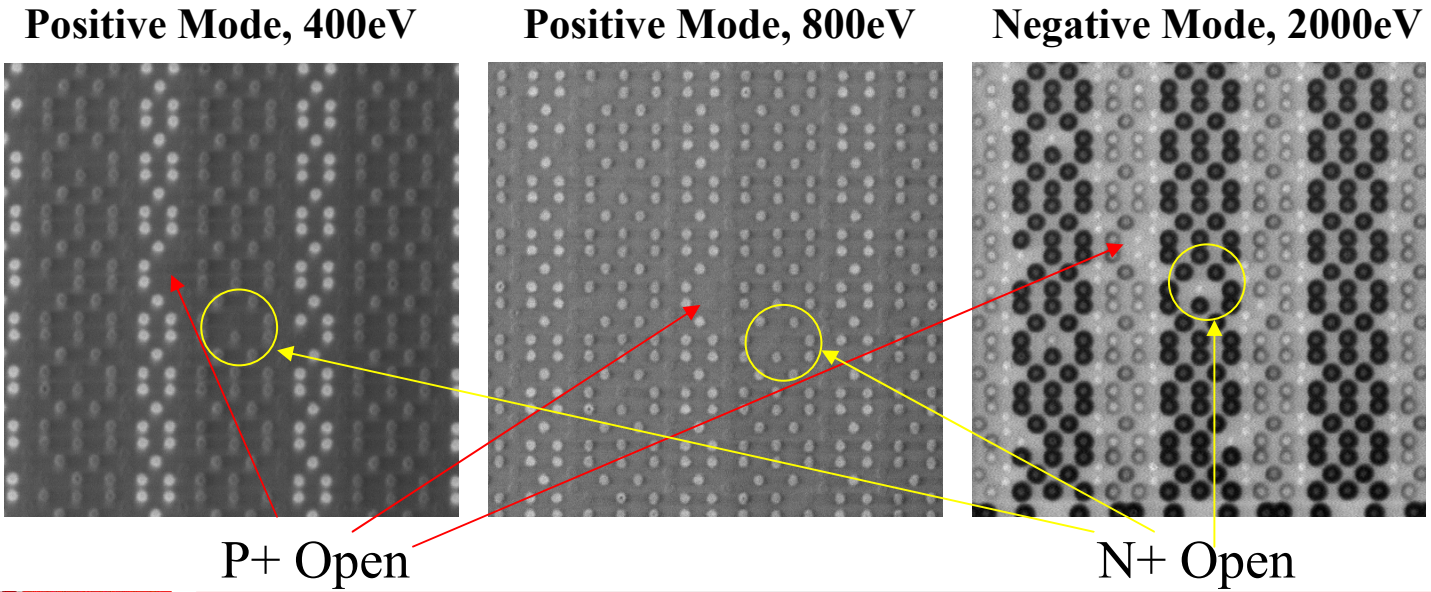
VC dominate

Conducting plugs with thin dielectric cap

Luke Lin (PSC) and Hong Xiao (HMI), Proc. of ISSM, pp.594, 2007

EBI Inspection Modes





Introduction

- EBI Applications
  - VC and physical defects
- Device leakage
  - NMOS
  - PMOS
  - Gate
- Early detections of device leakage issues
  - WCMP
  - NiSi

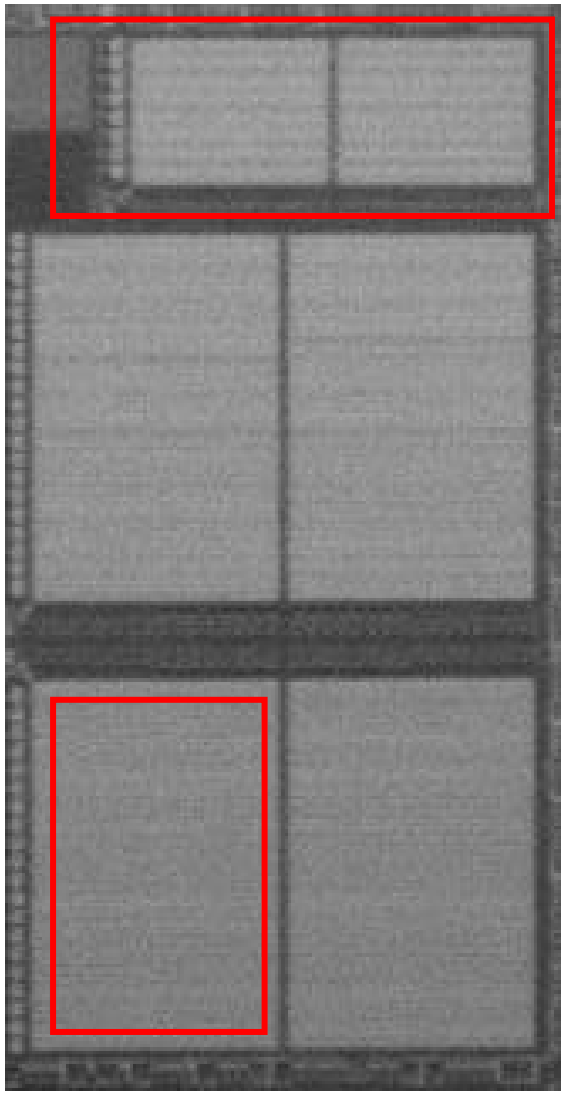
Experiment 2 Setup

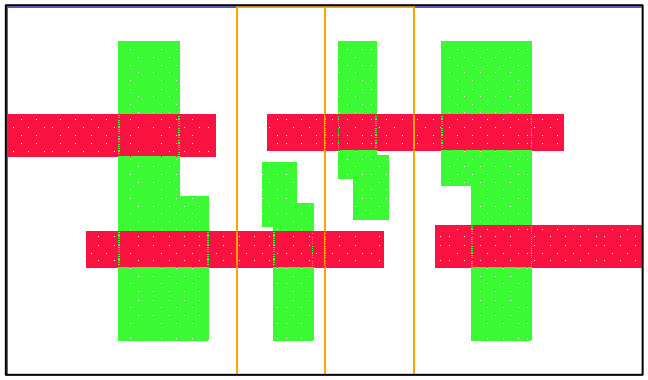
- Experiment equipment
  - eScan®Lite

- Experiment Sample
  - One 45nm NiSi wafer
  - One 45nm WCMP wafer
  - Same mask, same processes until NiSi

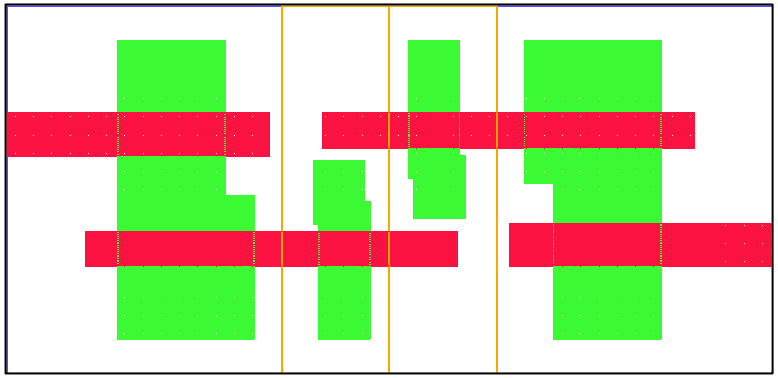
Sample of Experiment 2

SRAM 3





SRAM 1

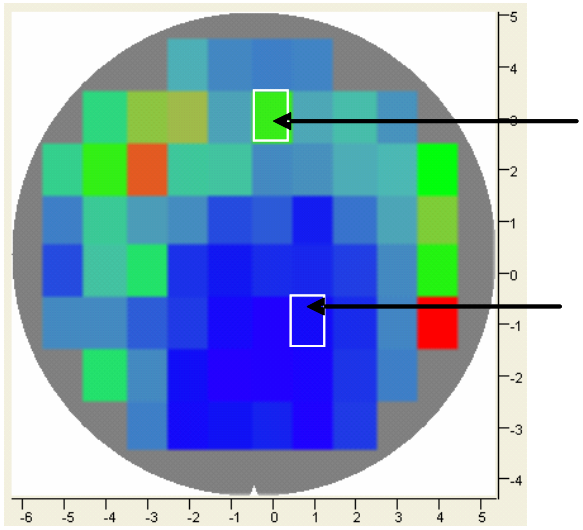


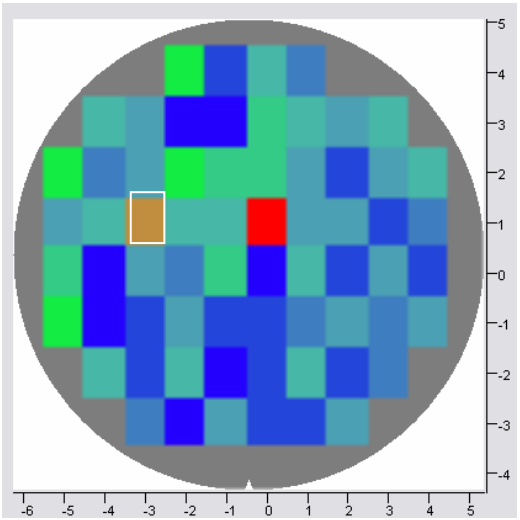
Results of Experiment 2

- PMOS Leakage
  - DVC of WCMP Negative Mode™
  - SRAM 1 & SRAM 3 have different signatures
    - SRAM 1 has “horseshoe” signature
    - SRAM 3 has random signature
  - SRAM 1 has much more PMOS leakage than that of SRAM 3.

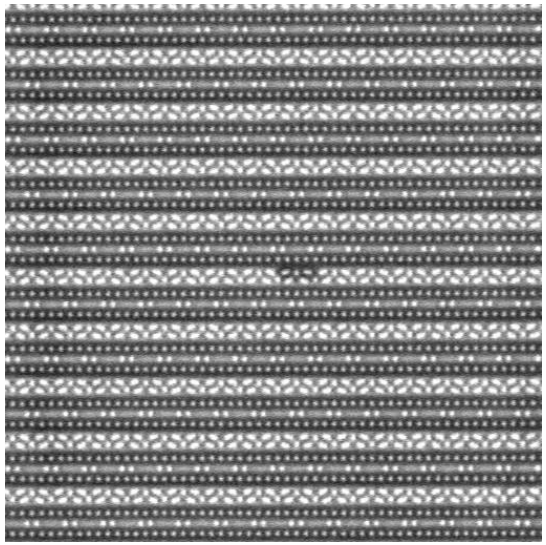
P+/N-well Leakage (WCMP DVC)

SRAM 1
52782

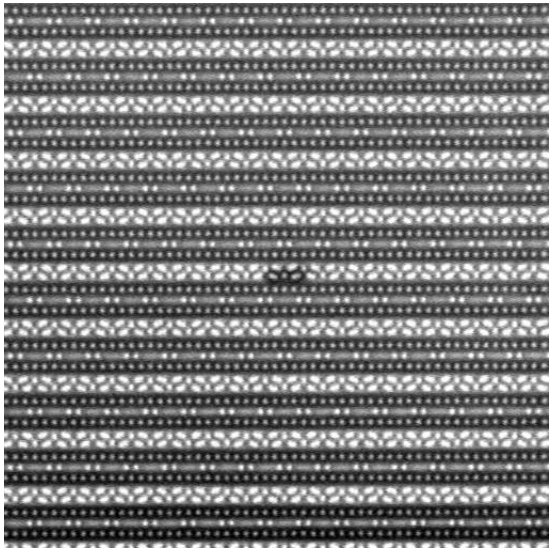




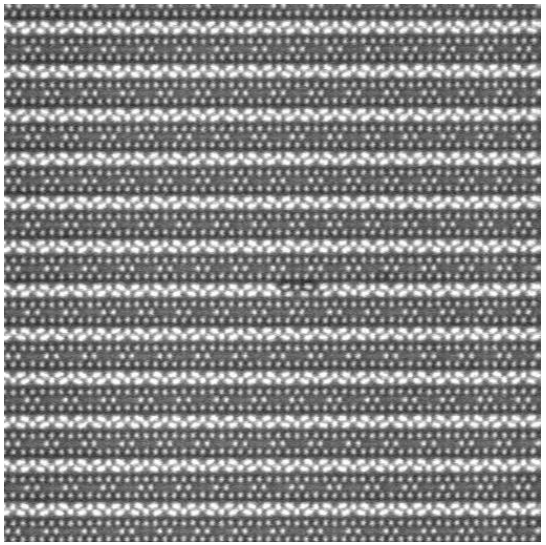
SRAM 3
195



SRAM 1 site 1

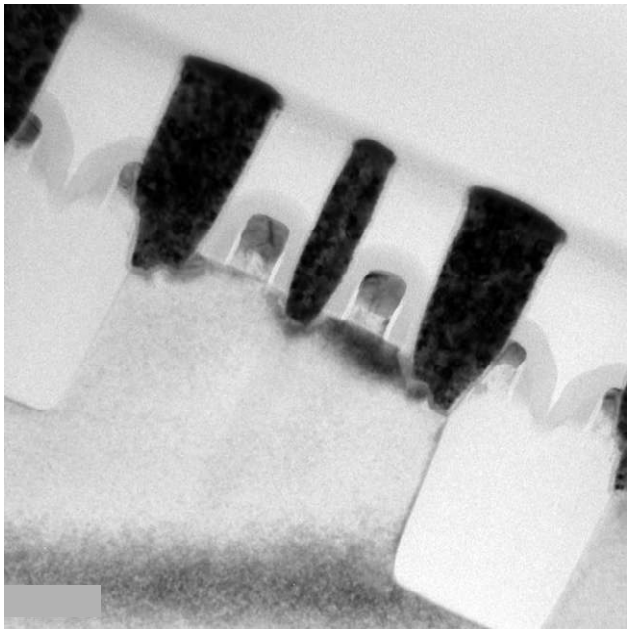


SRAM 1 site 2

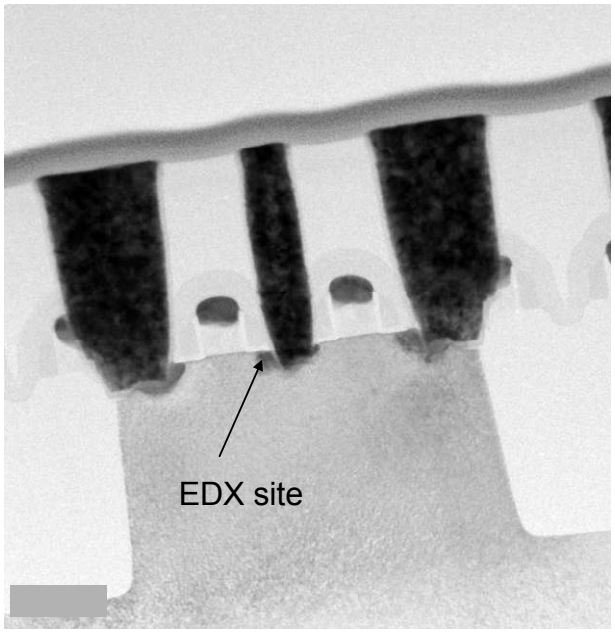


SRAM 3

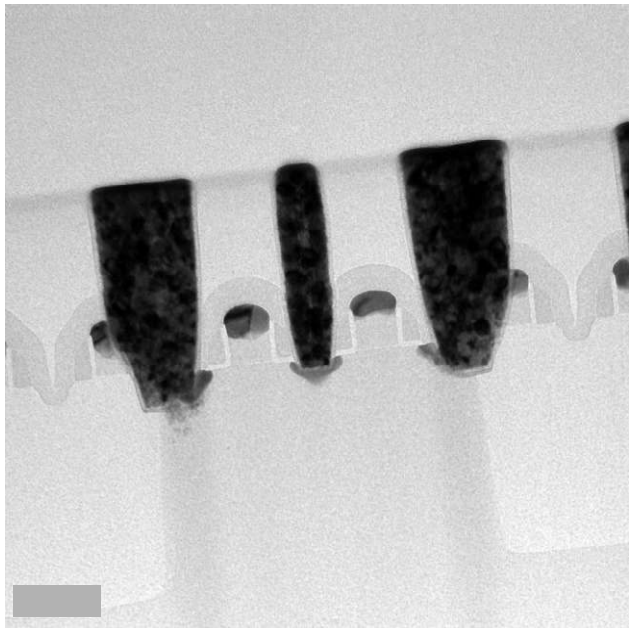
P+/N-well Leakage FA



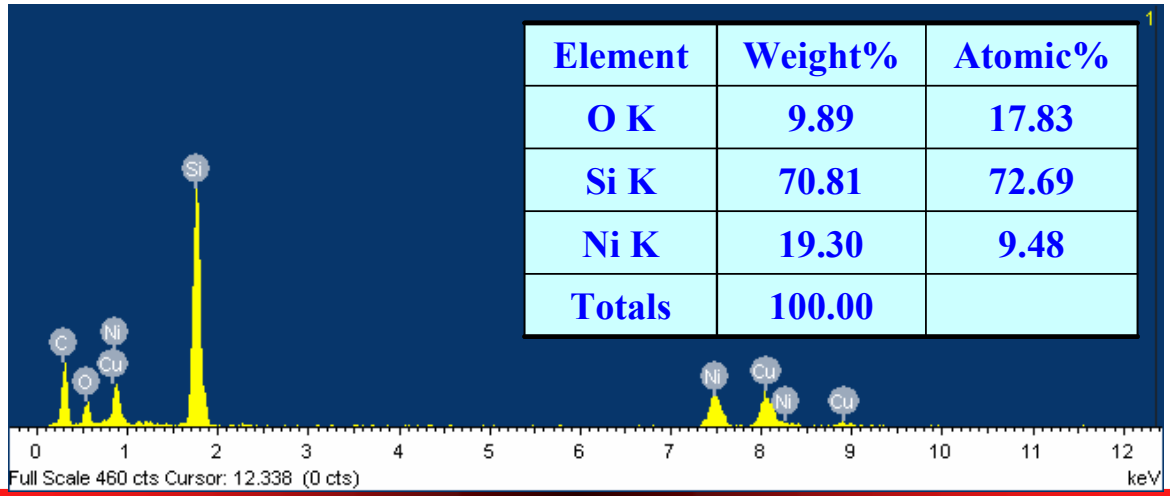
SRAM 1 site 1



SRAM 1 site 2



SRAM 3



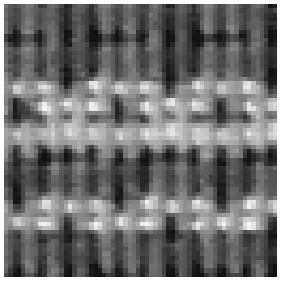
Element	Weight%	Atomic%
O K	9.89	17.83
Si K	70.81	72.69
Ni K	19.30	9.48
Totals	100.00	

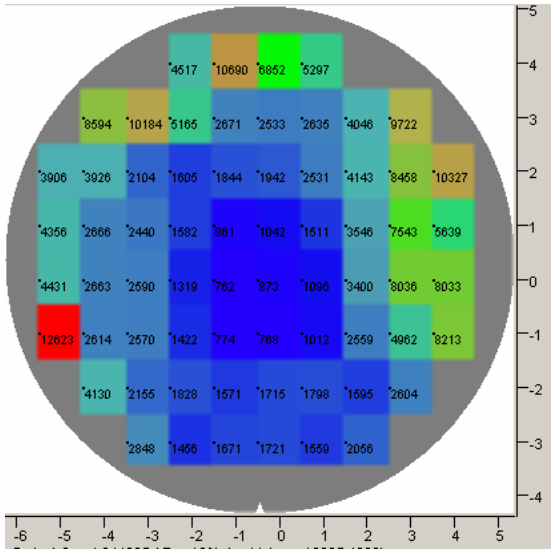
Results of Experiment 2

- NMOS Leakage
  - BVC of WCMP positive mode
  - DVC of WCMP Negative Mode™
  - BVC of NiSi positive mode
- N+/P-well leakage has different signature from P+/N-well leakage signature in SRAM 1
- SRAM 1 and SRAM 3 have different N+/P-well leakage signatures

SRAM 1 Leakage

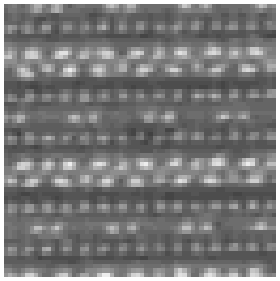
NiSi: N-leak

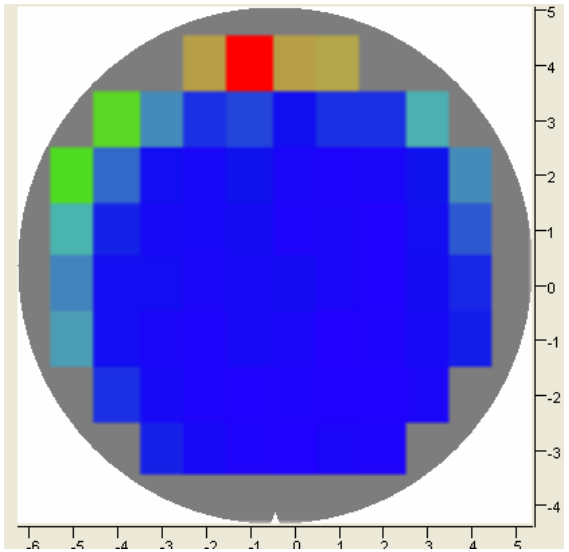




244305

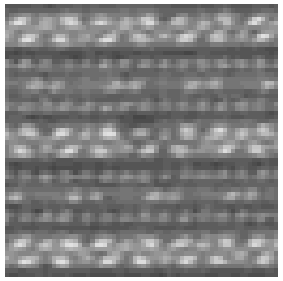
WCMP: N-leak

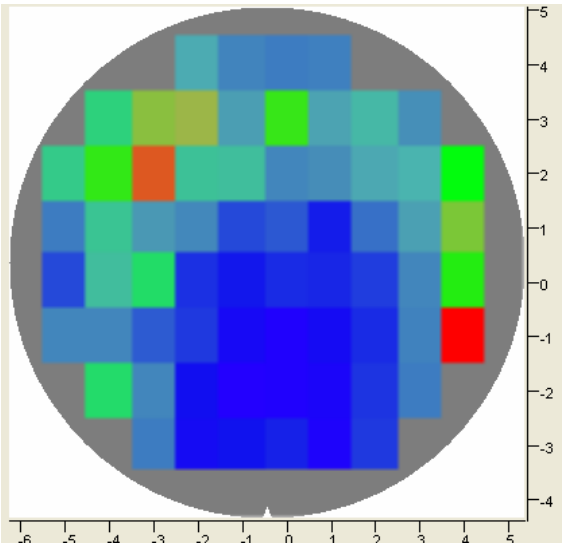




3794

WCMP: P-leak

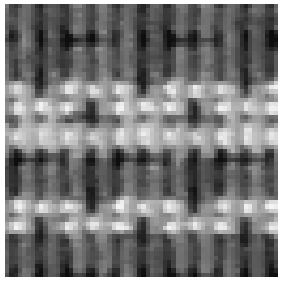


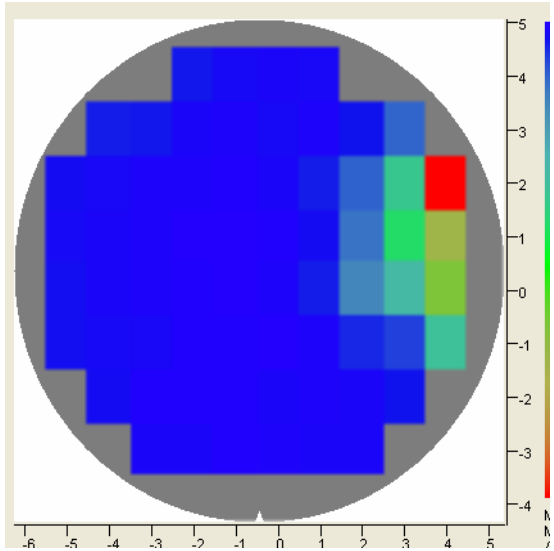


52782

SRAM 3 Leakage

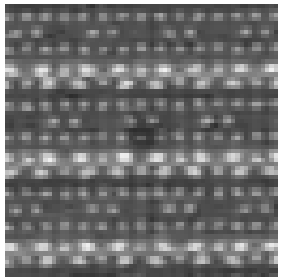
NiSi: N-leak

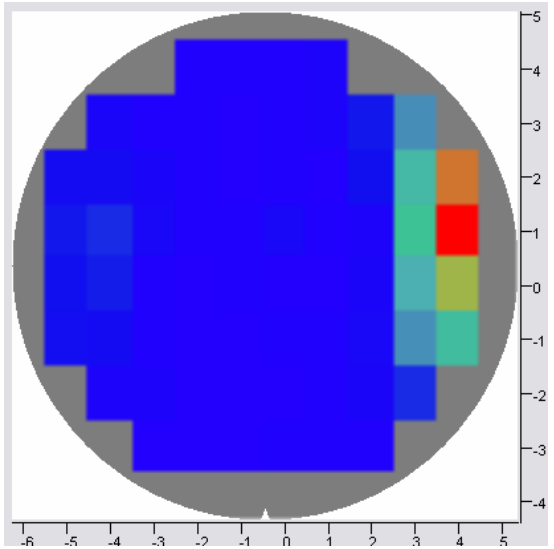




27857

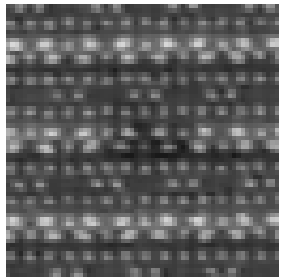
WCMP: N-leak

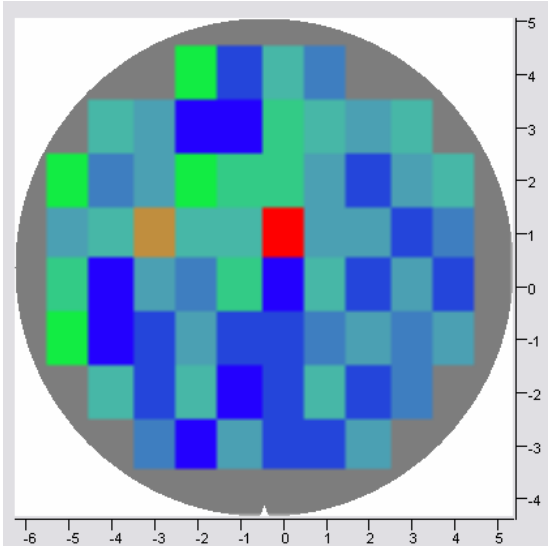




22540

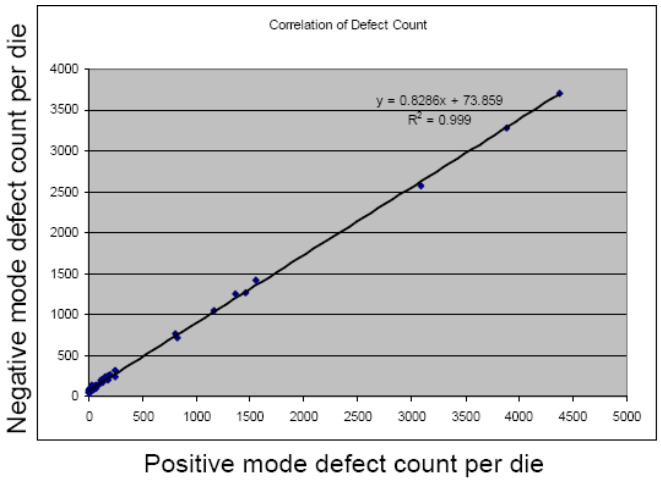
WCMP: P-leak



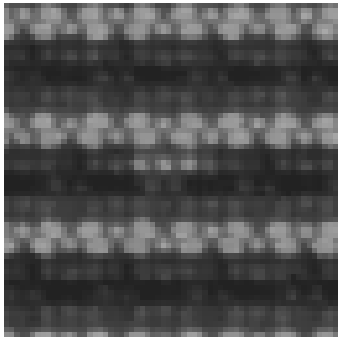


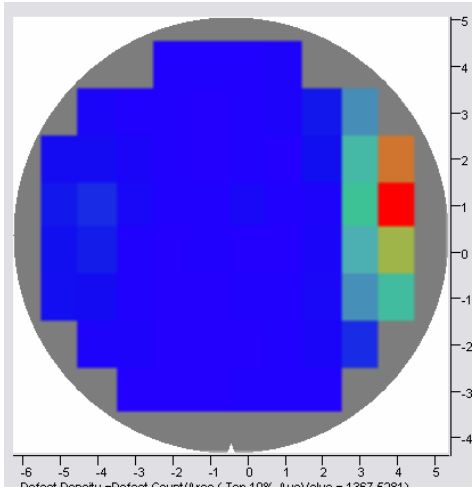
195

N-Leak/short of SRAM 3



WCMP Positive Mode

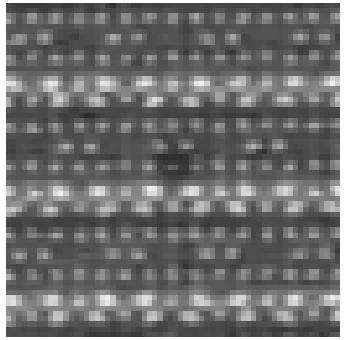


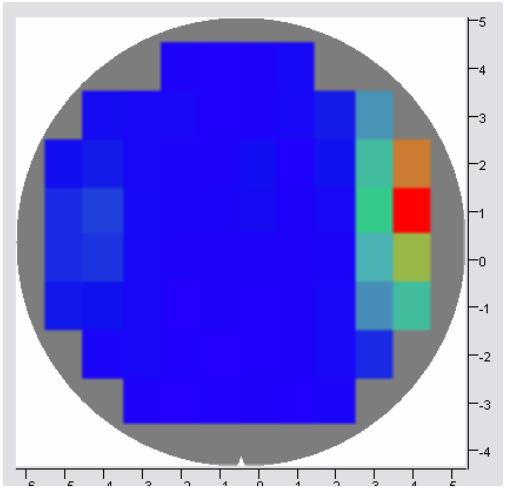


21320

500eV/50nA

WCMP Negative Mode



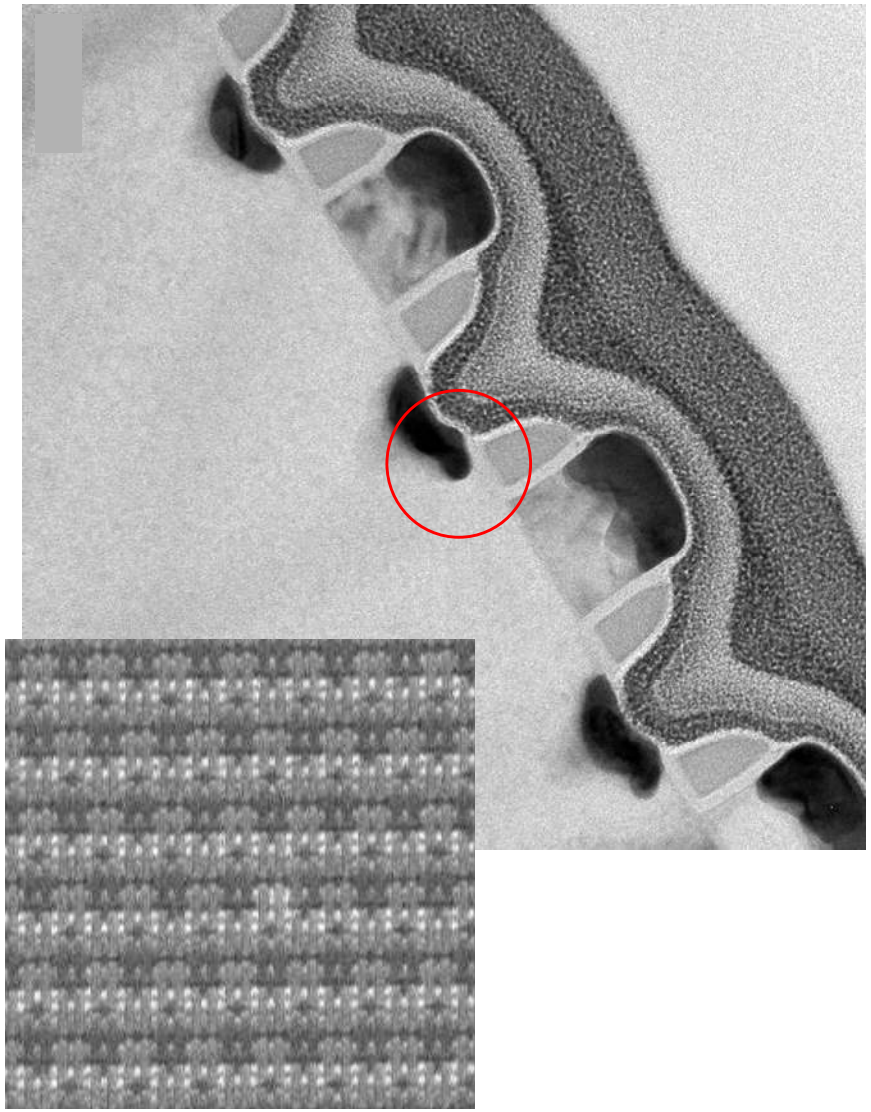


22540

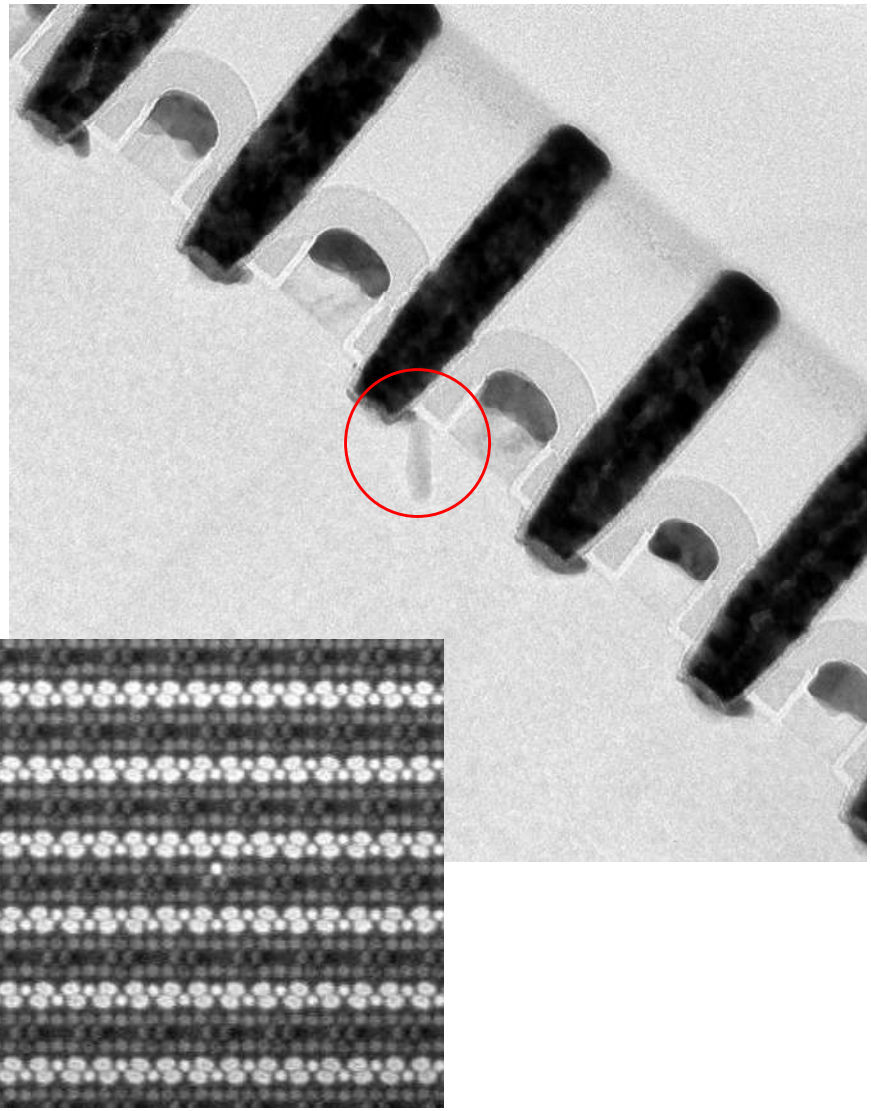
3000eV/100nA

N-Leak/short of SRAM 3

NiSi: NMOS BVC

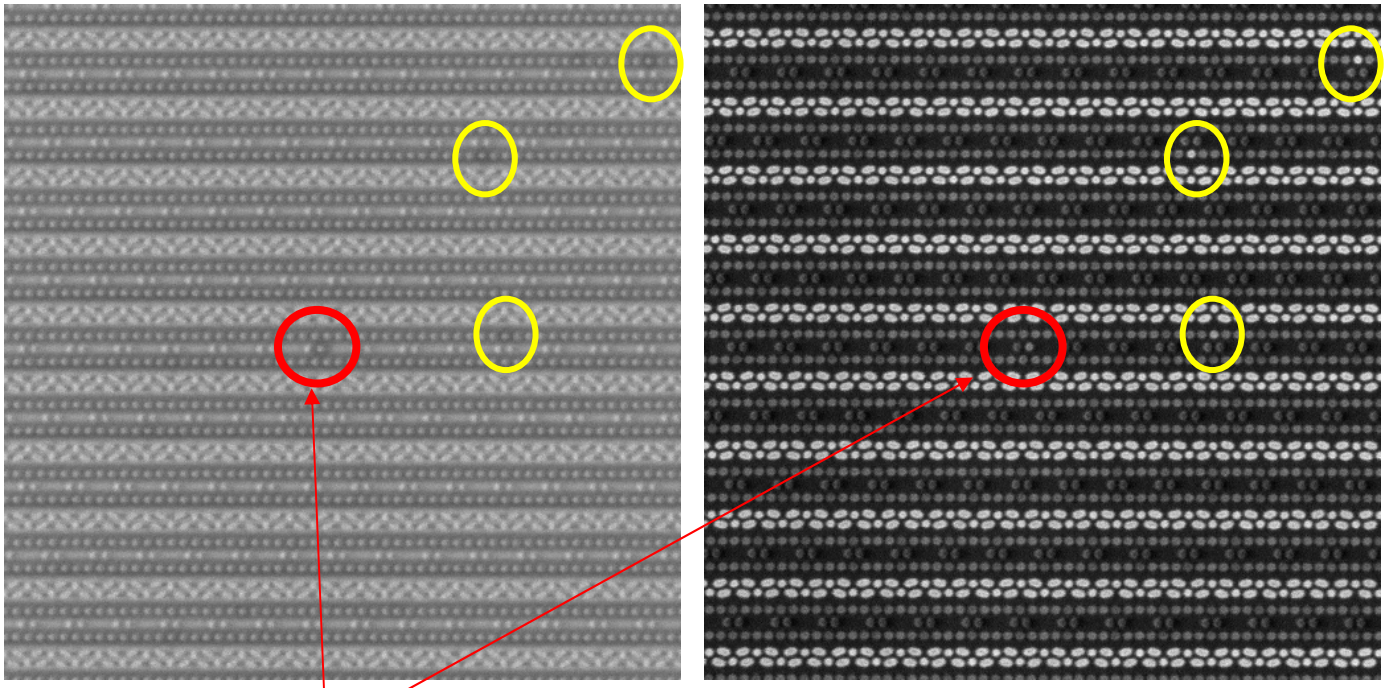


WCMP: NMOS BVC



More Experiment 2 Results

- Possible contact-to-poly short
  - Pass gate: WCMP Negative Mode™ DVC
  - Pass gate: WCMP positive mode Weak BVC

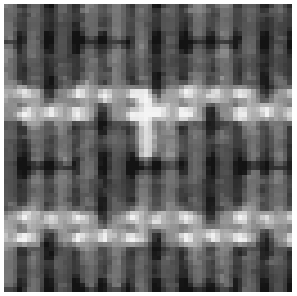


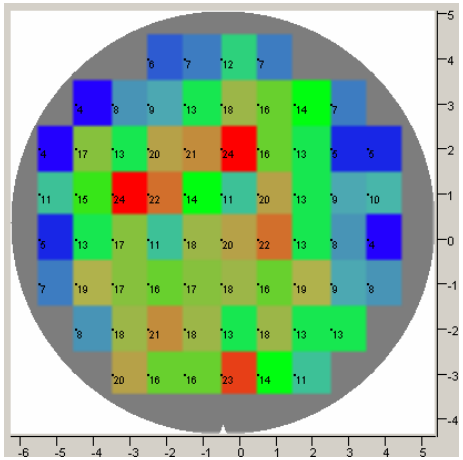
Gate poly short to N+ contact plug

More Experiment 2 Results

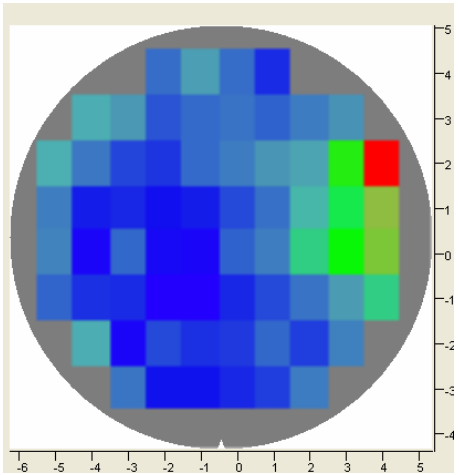
- Gate Leakage: NiSi gate BVC

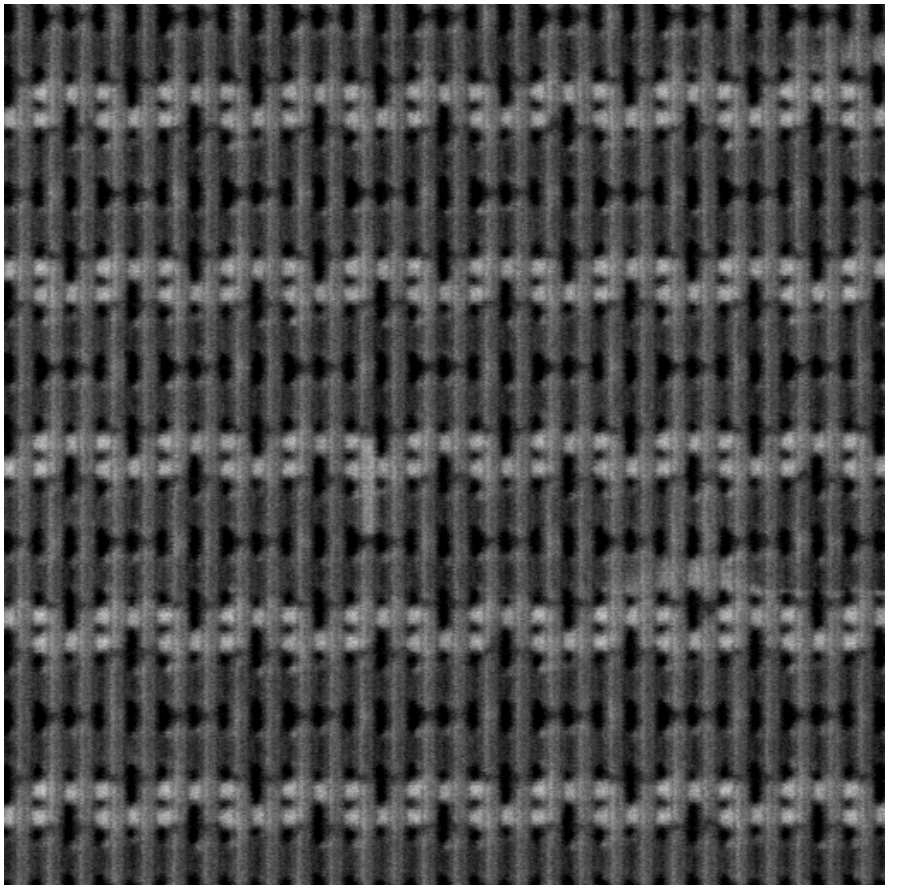
SRAM 1
907





SRAM 3
16066

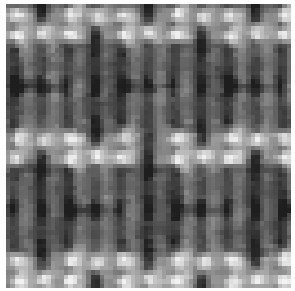


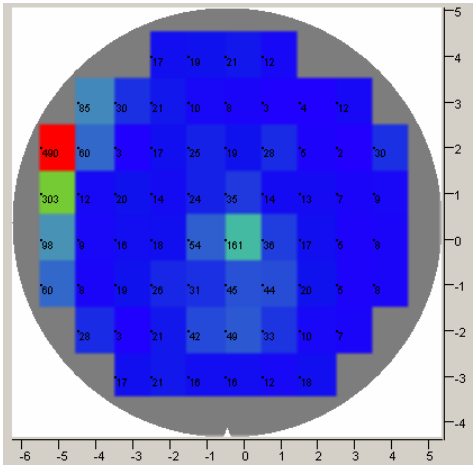


More Experiment 2 Results

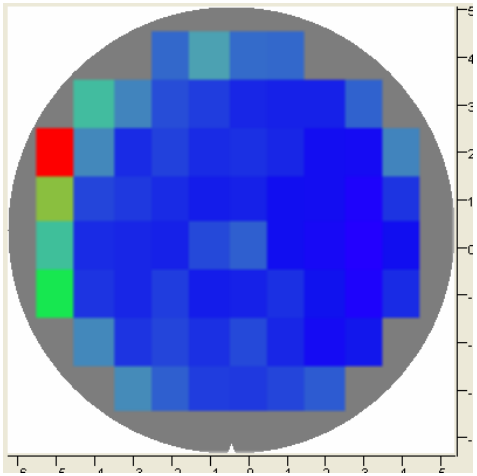
- NiSi dark defect likely caused by NiSi missing

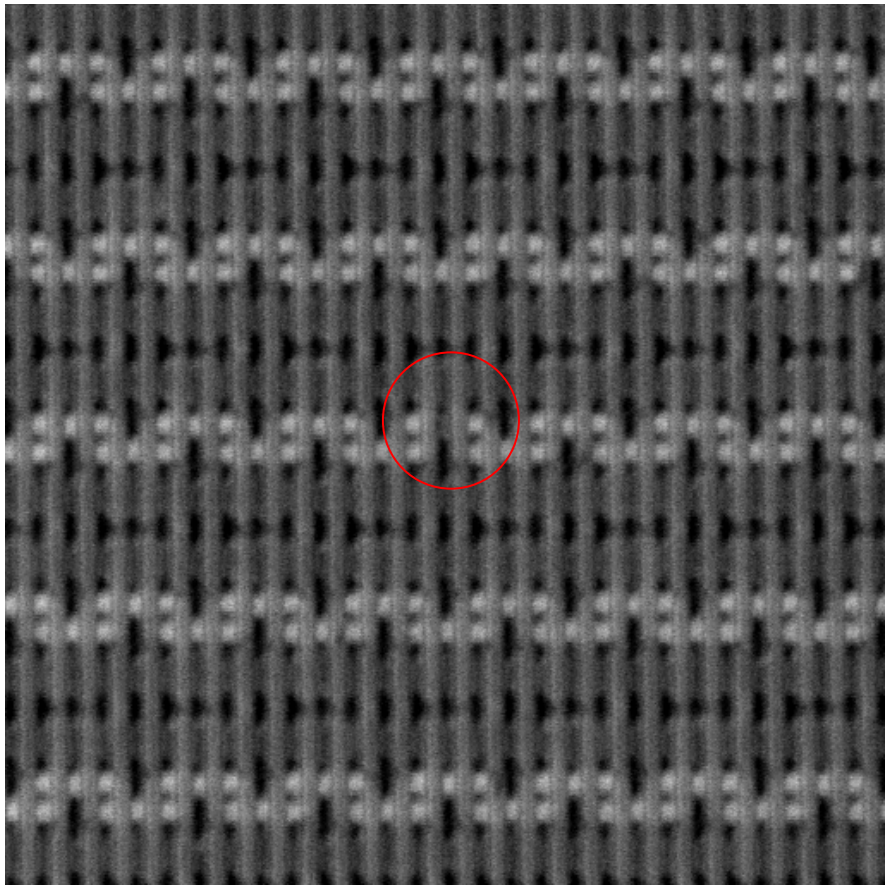
SRAM 1
2353



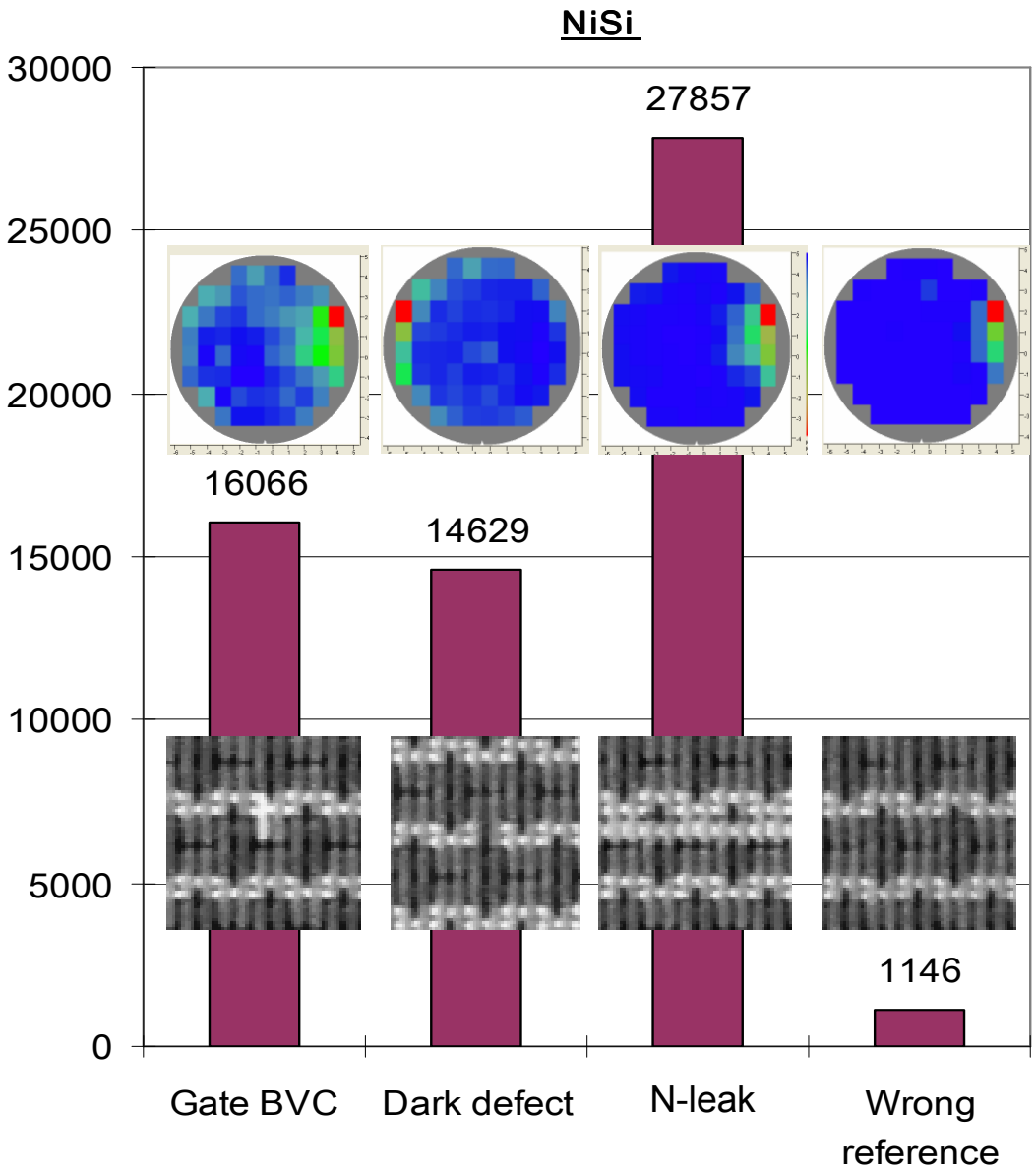


SRAM 3
14629

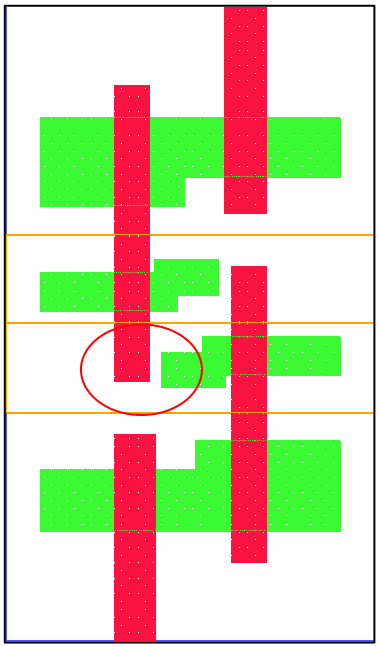


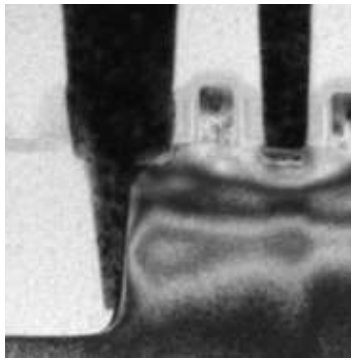


SRAM 3 NiSi Defect Pareto



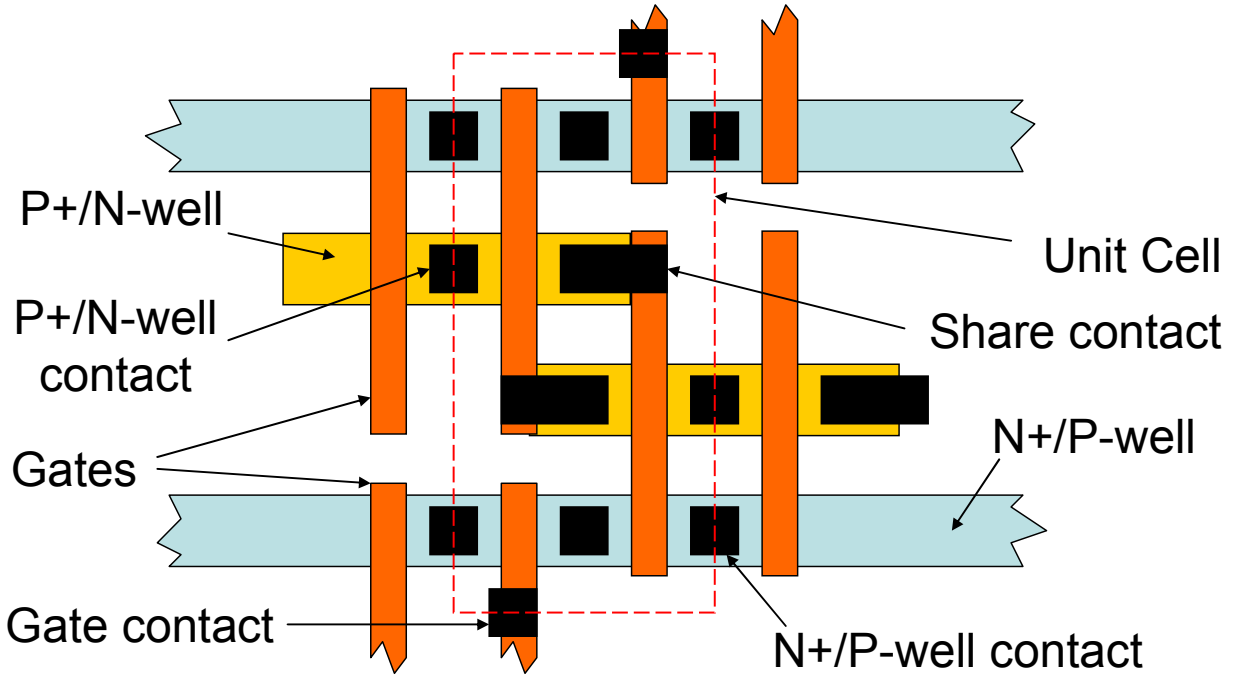
Discussion





Shuen-chen Lei, et al., Proc. of SPIE, Vol. 6518, pp. 65184I, (2007)

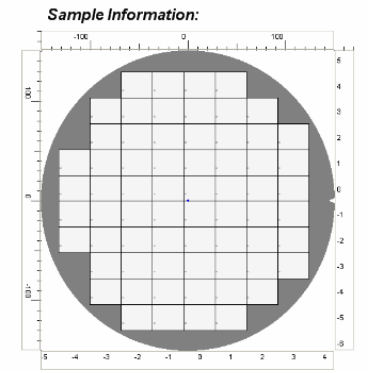
- Overlap inverter gate and N-well AA
- Avoid share contact touching STI
- Over etch can cause PMOS leakage

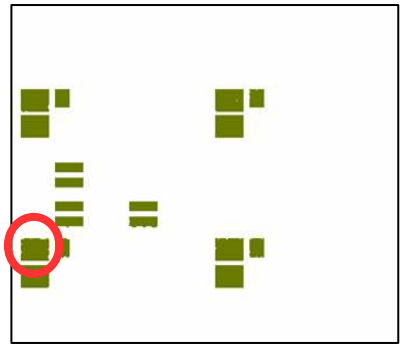


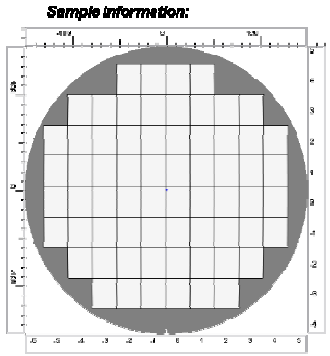
Summary of Experiment 2

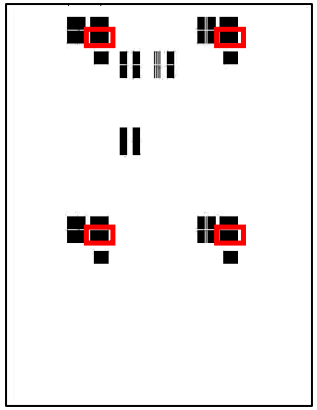
- We focused on leak/short in this study:
  - NiSi EBI captured NMOS and gate leak,
  - WCMP positive mode captured NMOS leak,
  - WCMP Negative Mode™ EBI captured PMOS leak, NMOS leak and contact-to-poly short.
  - Good correlations among positive mode NMOS leak, negative mode NMOS leak and NiSi NMOS leak.
- SRAM arrays with different layouts have different leakage signatures
  - SRAM 1 has higher overetch-induced PMOS leakage which is sensitive to pattern density.
- There are different signatures of NMOS and PMOS leakage in the same SRAM array, due to different leakage mechanisms.

Comparison of Two Experiments









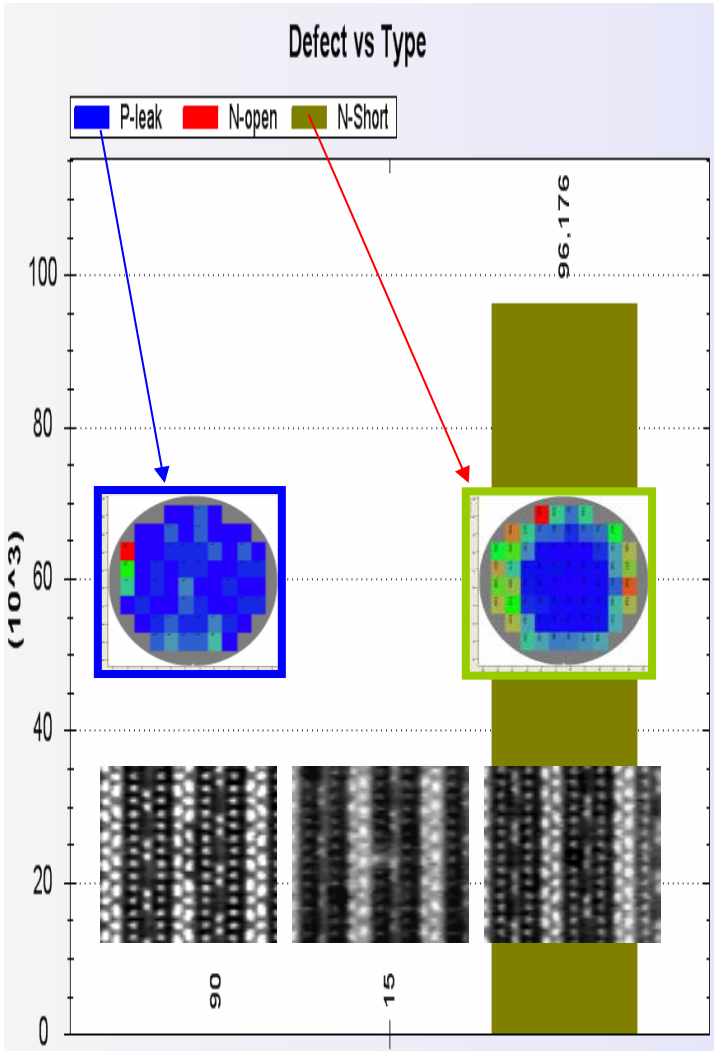
Experiment equipment	eScan®310
Experiment sample	45nm WCMP wafer
Notch	Right
Stage/Scan Direction	LS Mode
Total/Inspected Die	66/66
Landing Energy/B current	3000eV / 94 nA
Scan Average	1D1L1F
Pixel Size	40nm
Inspection Time	1h0m56s
Total Defect	96281

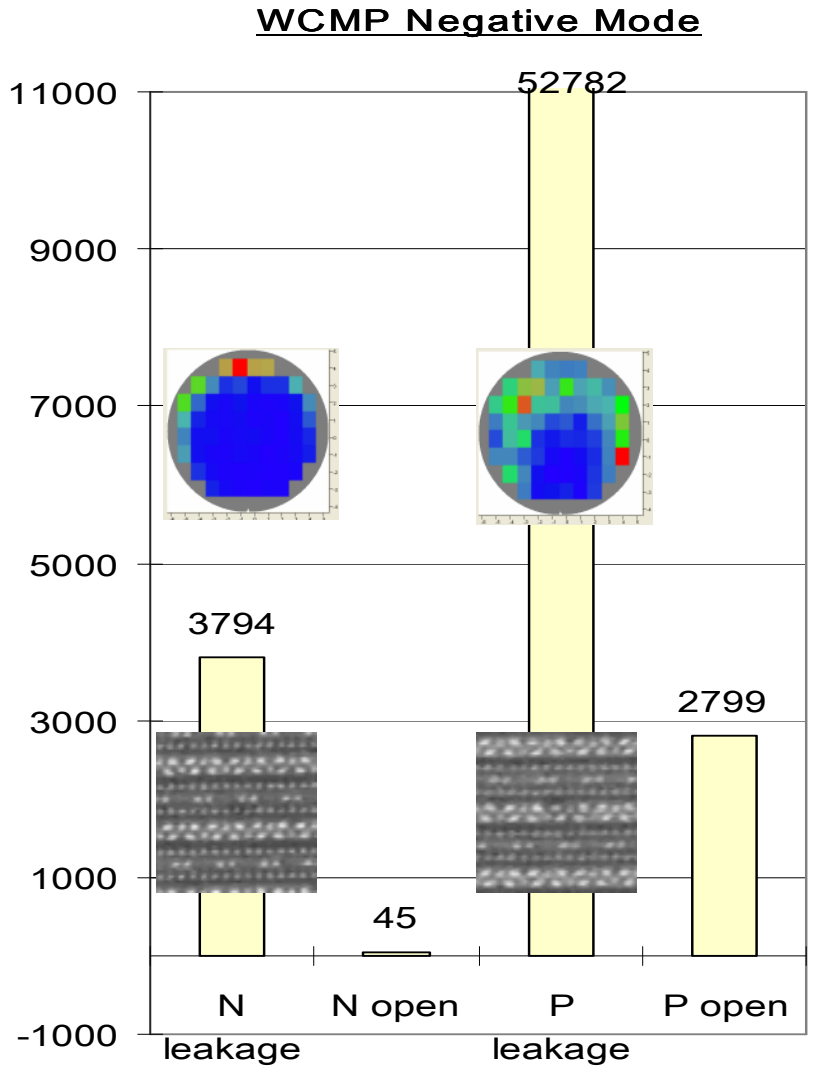
Experiment 1: Sep. 2007

Experiment equipment	eScan®Lite
Experiment sample	45nm WCMP wafer
Notch	Down
Stage/Scan Direction	LS Mode
Total/Inspected Die	66/66
Landing Energy/B current	3000eV / 26.49 nA
Scan Average	1D1L1F
Pixel Size	40nm
Inspection Time	44m29s
Total Defect	59420

Experiment 2: May. 2008

WCMP Negative Mode EBI Results





Experiment 1 total defects: 96281

Experiment 2 total defect: 59420

SRAM1 Leakage Summary

- Experiment 1
  - N-leak: 96176
  - P-leak: 90
- Experiment 2
  - N-leak: 3794
  - P-leak: 52782

Recommendation

- EBI at NiSi to capture N+/P-well and gate leakage at the earliest stage.
- Positive mode EBI at WCMP layer to capture N+/P-well leakage, gate leakage and P+/N-well contact open.
- Negative Mode^{TM} EBI at WCMP layer to capture P+/N-well leakage, N+/P-well contact open and poly-to-contact short.
- For engineering studies, always review WCMP VC defects with both charging modes.

Acknowledgement

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Thank You!