HiK/MG Gate Stack Issues and Landscape

Steven Hung

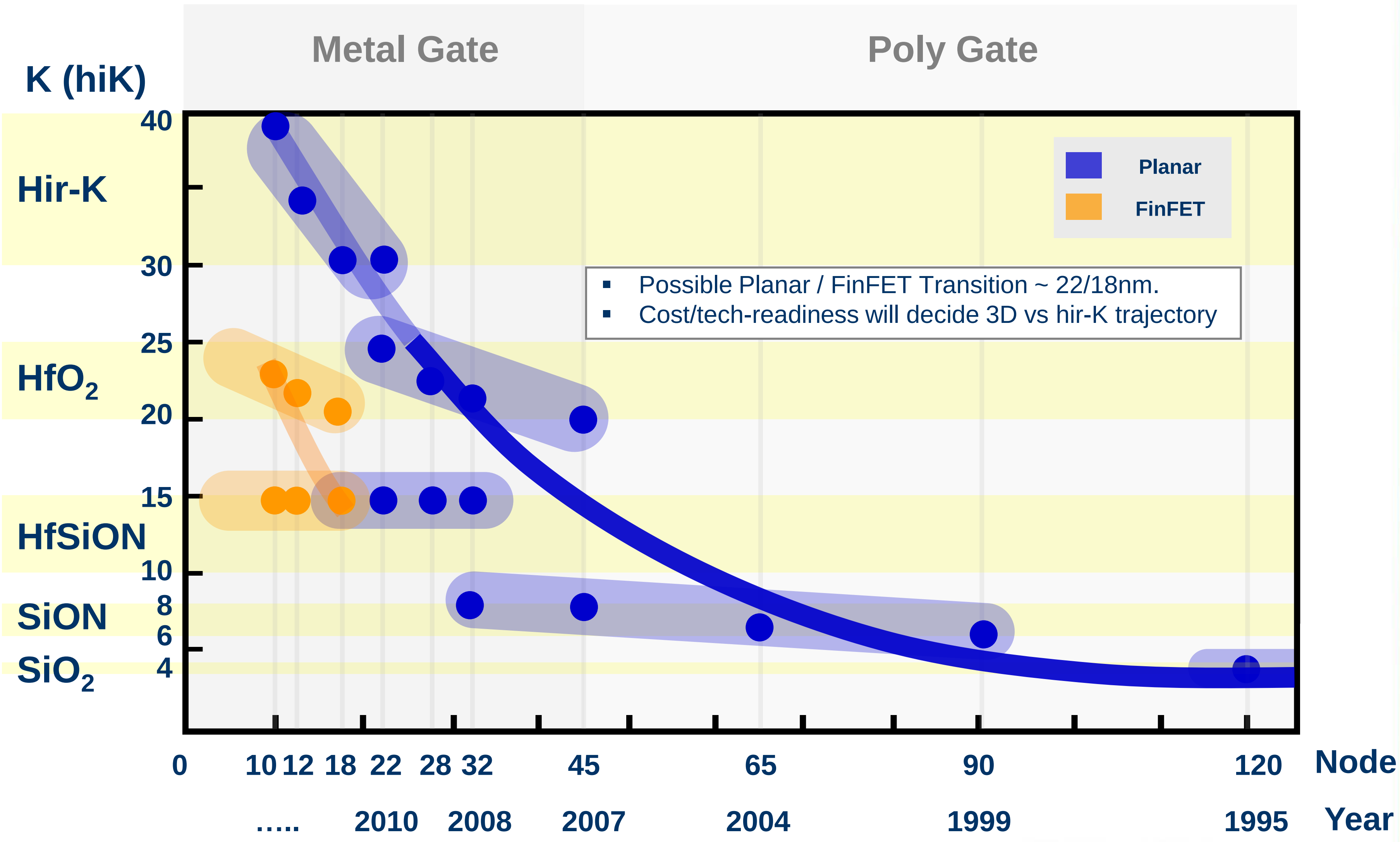
think it. apply it.™

APPLIED MATERIALS.

Outline

- The K-evolution
- Integration Landscape Overview
- Scaling trend and Limitation
- The Fundamental Gate Stack Material Issues

Evolution of K-scaling

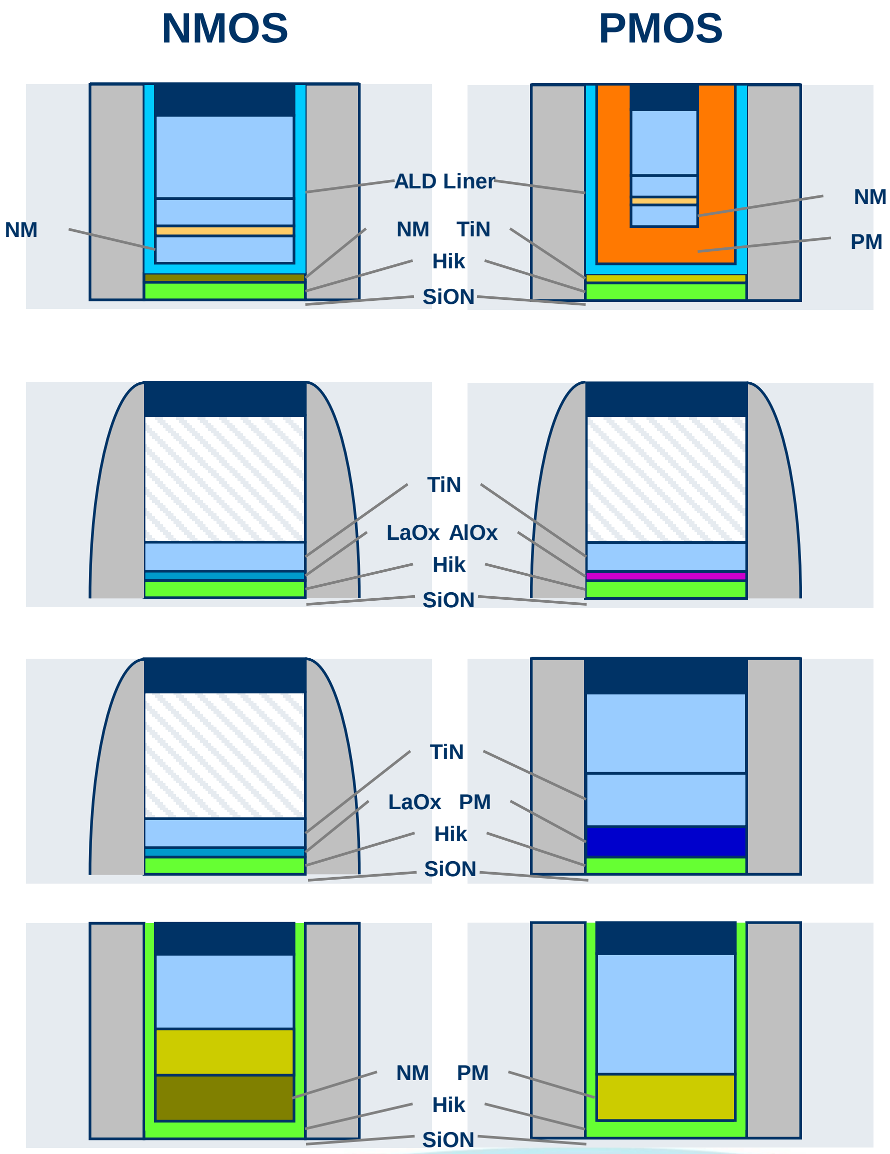


- Possible Planar / FinFET Transition ~ 22/18nm.
- Cost/tech-readiness will decide 3D vs hir-K trajectory

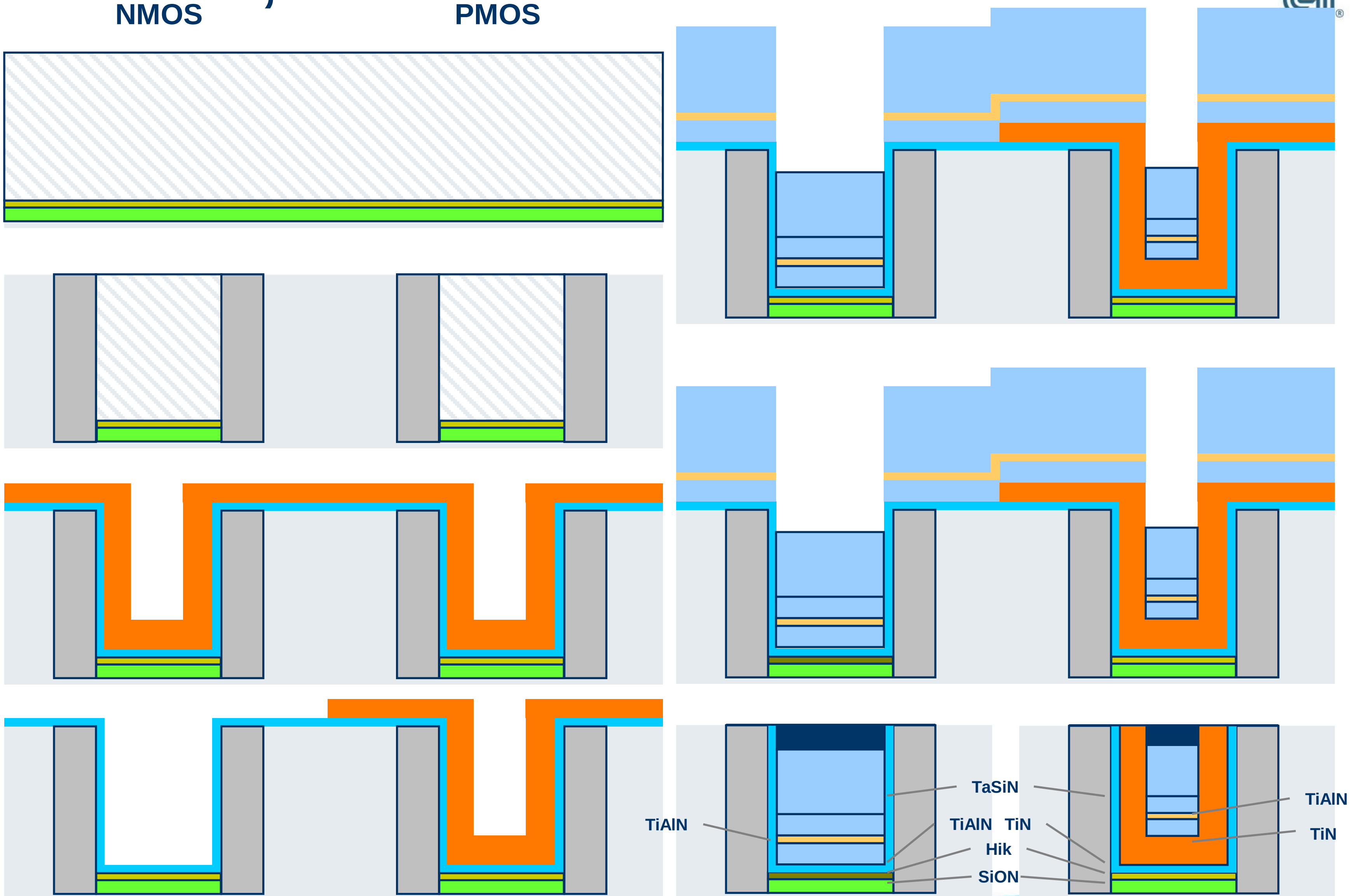
Overall Landscape
on
HiK/MG

General Landscape

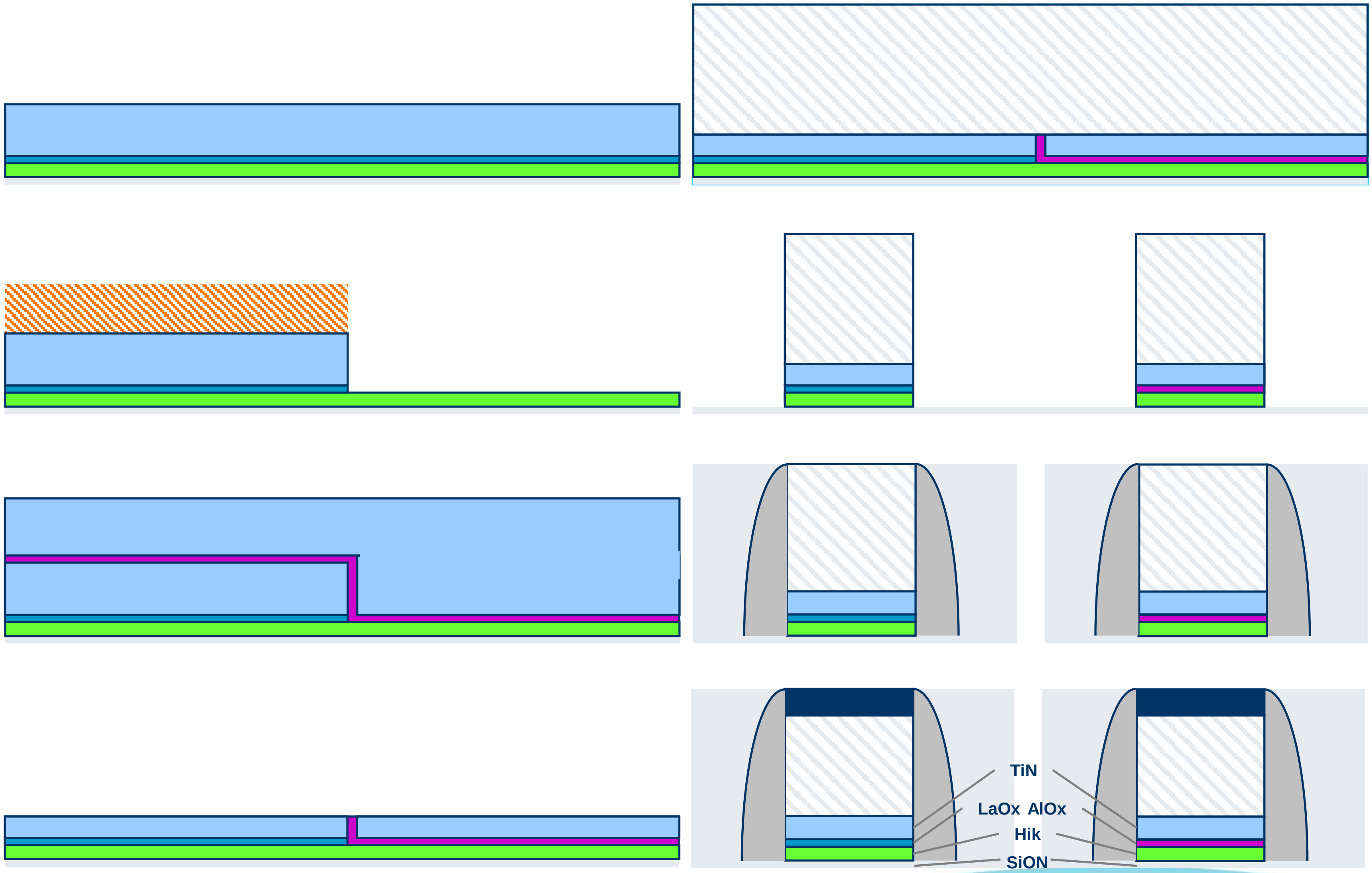
Integration	Process Flow
HiK F + MG L	▪Base Ox + HiK + TiN + Poly + Gate Etch ▪S/D formation + spike ▪CMP + poly strip ▪ALD liner + P-metal ▪NMOS: P-metal wet etch ▪N-metal + Al fill + reflow ▪Al CMP
GF	▪Base Ox + HiK ▪Dep AlOx / Midgap Metal ▪Etch of AlOx / MG on NMOS ▪Dep LaOx / Midgap Metal ▪Etch of LaOx / MG on PMOS ▪Poly + Gate Etch + S/D formation + spike
Hybrid GF (N) GL (P)	▪Base Ox + HiK ▪Dep LaOx / Midgap Metal ▪Etch of LaOx / MG on PMOS ▪Poly + Gate Etch + S/D formation + spike ▪Poly strip on PMOS ▪P-metal dep + Al fill + reflow ▪CMP
Pure GL	▪Dummy dielectric + Poly + Gate Etch ▪S/D formation + spike ▪CMP + poly strip ▪Base Ox + HiK + N-metal dep ▪N-metal etch from PMOS ▪P-metal dep + metal fill ▪CMP



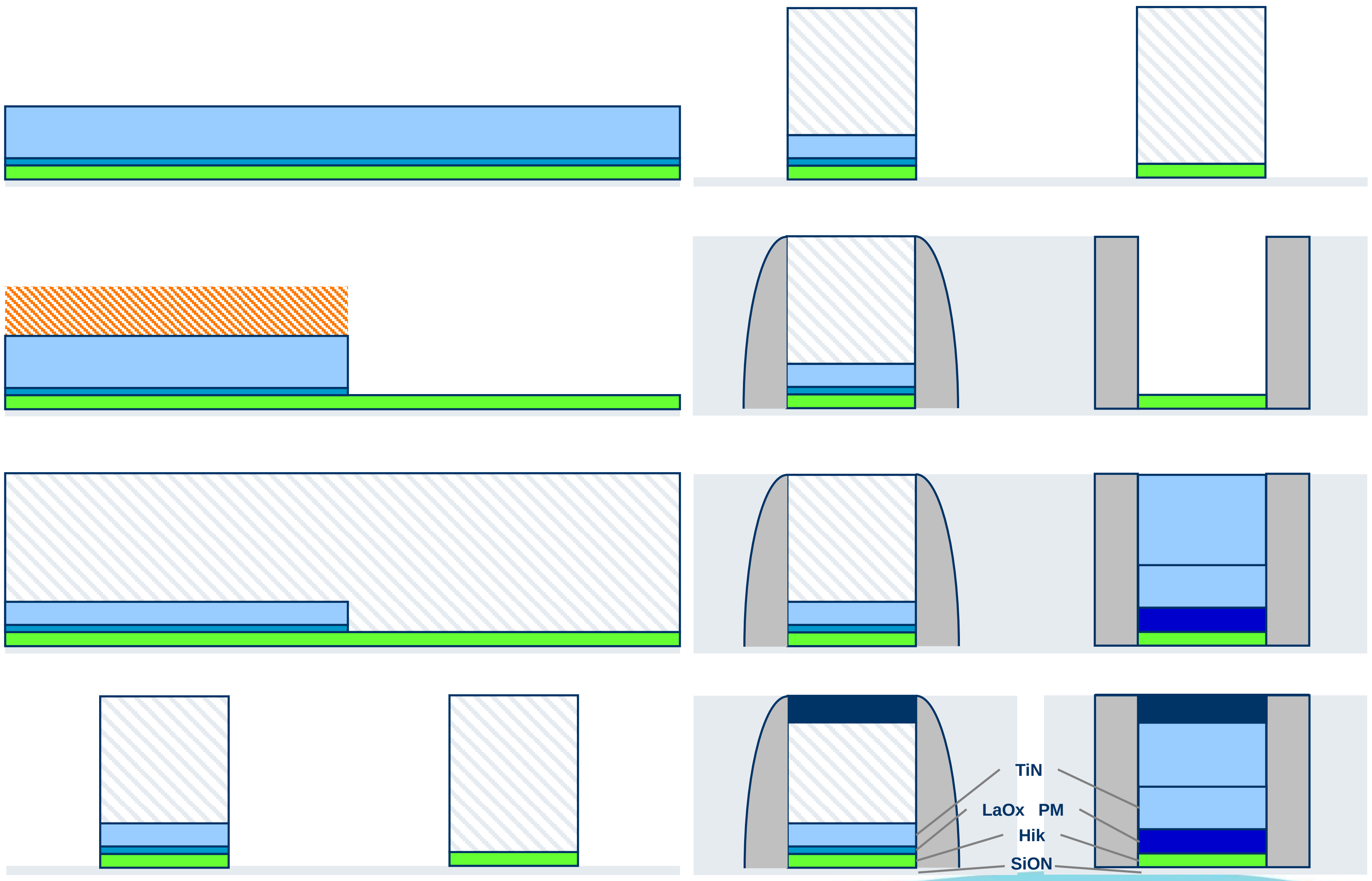
HiK First, MG Last



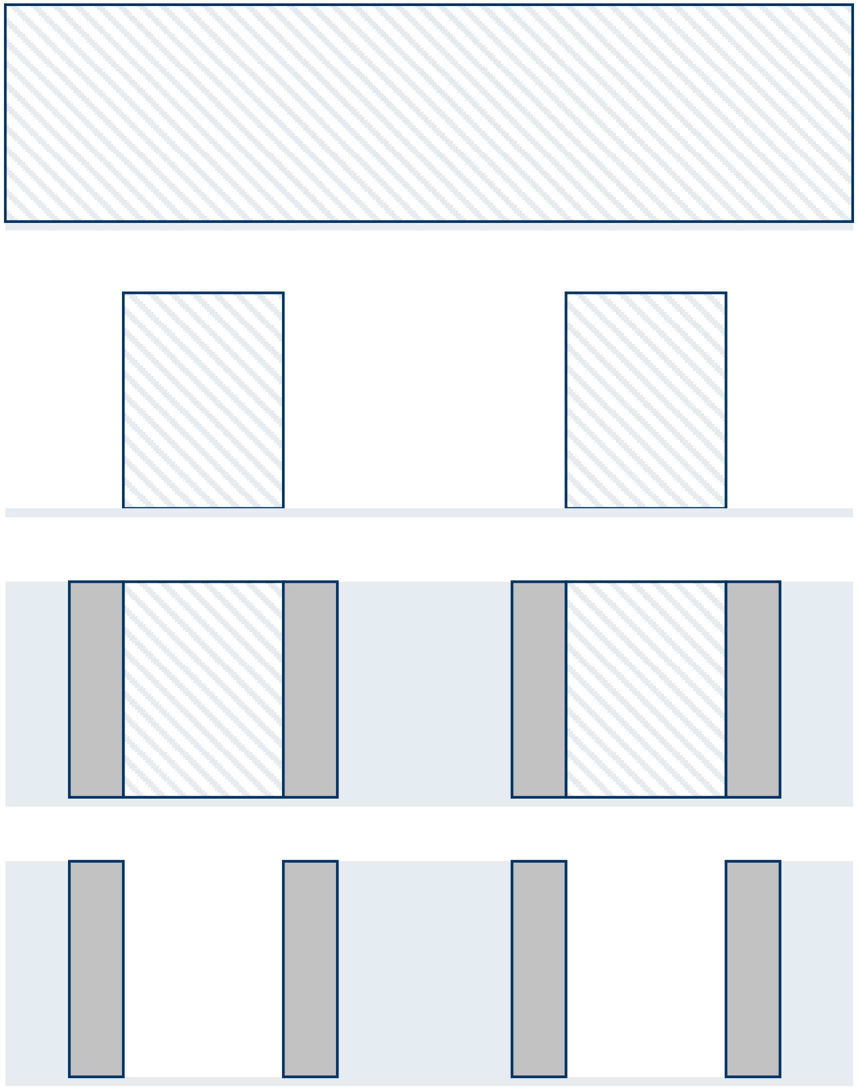
Gate First (GF)

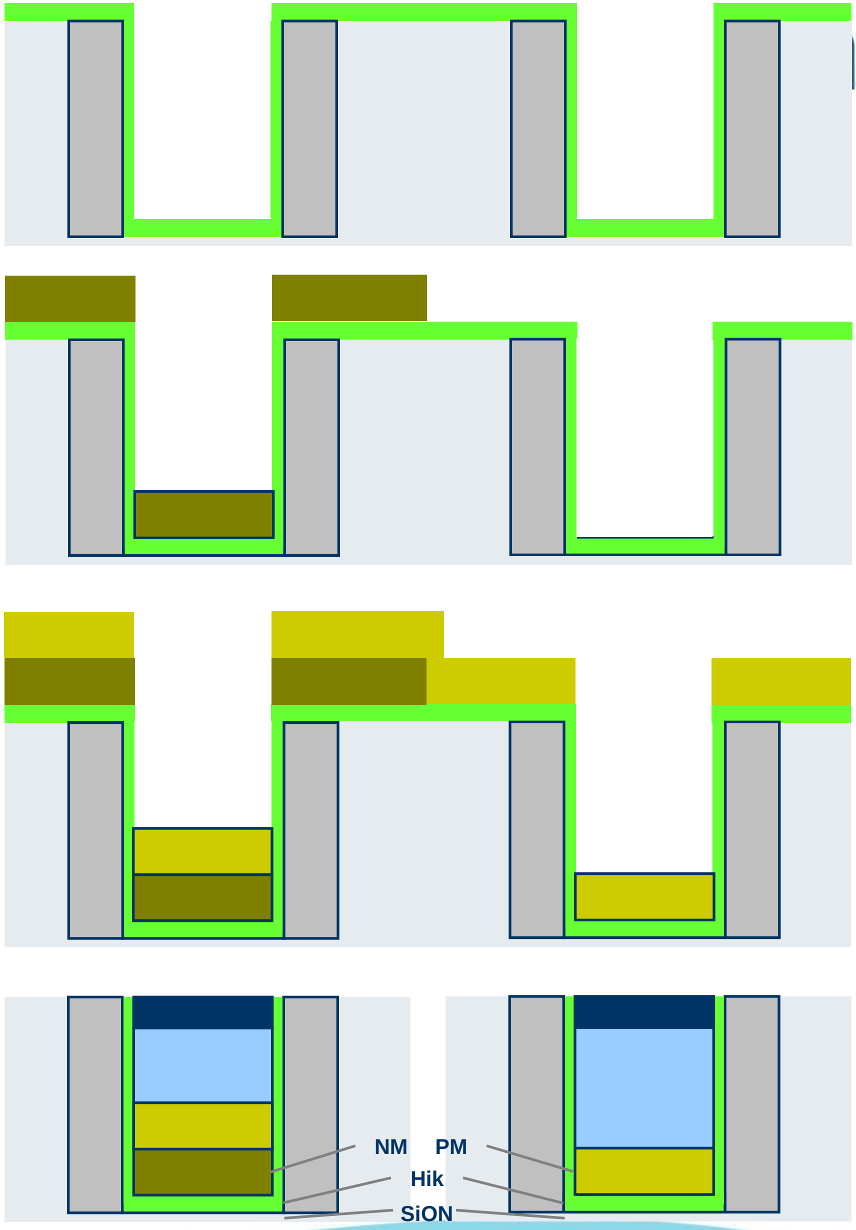


GF (NMOS) / GL (PMOS)



Gate Last (GL)





Issues and Challenges for Hik/MG Stack

- Base Oxide
  - Development of sub-10A higher-K Box for EOT scaling
  - SiON: Proper N-dose and profile to maximize K and minimize EOT

- Hik
  - Morphology stability for GF & GL applications
  - Process control to minimize Oxygen vacancy (Vo)
  - Post deposition passivation for Oxygen vacancy suppression

- Capping layer
  - Deposition sequence and etch selectivity
  - Insufficient Vt adjustment on PMOS with AlOx (requires $\Delta V_t > 300mV$)
  - Mobility degradation due to over diffusion of La and Al species
  - Stringent uniformity requirement for Vt control WIW & WTW

- MG
  - Deposition process control to prevent damage to cap layer & hiK
  - Gap fill and overhang issue for both N and P devices

Trends and Solutions for 32nm and beyond

- Base Oxide
  - Use of SiON for aggressive EOT scaling in HP application
  - Utilize densified Base Ox to prevent trace element penetration into channel

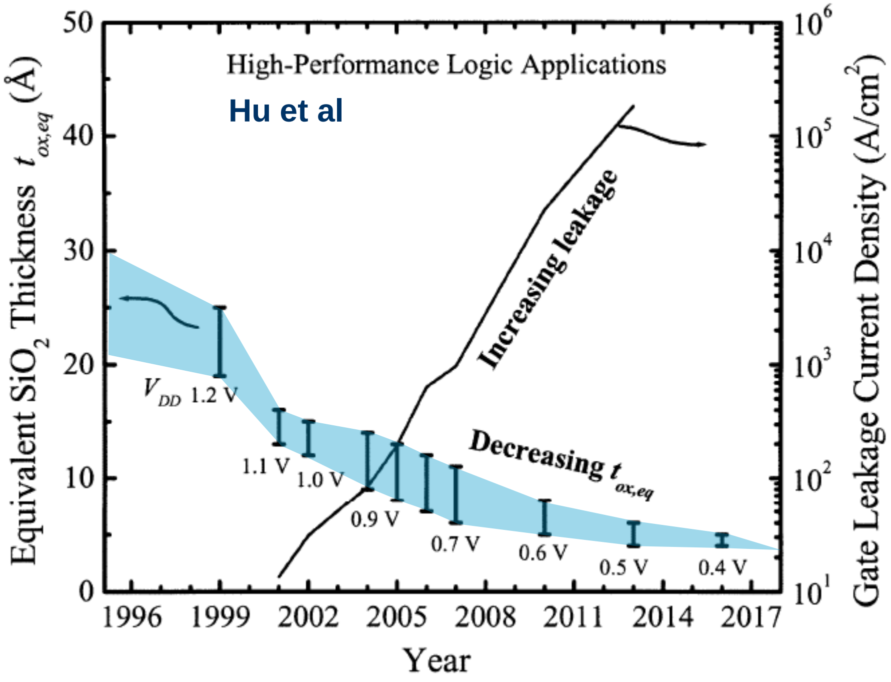
- HiK
  - Use of optimal ALD seq and temp for complete & secure in-film bonding
  - Post deposition anneal to suppress Vo formation (ie; NH3 PDA)
  - Post deposition nitridation for morphology stability and Vo reduction

- Capping layer
  - Possible alternatives for PMOS: MnOx, VOx, TaOx, ZrOx
  - Use of densified Base Ox to prevent La or Al penetration to channel
  - Use of uniform deposition technique / process for Vt control

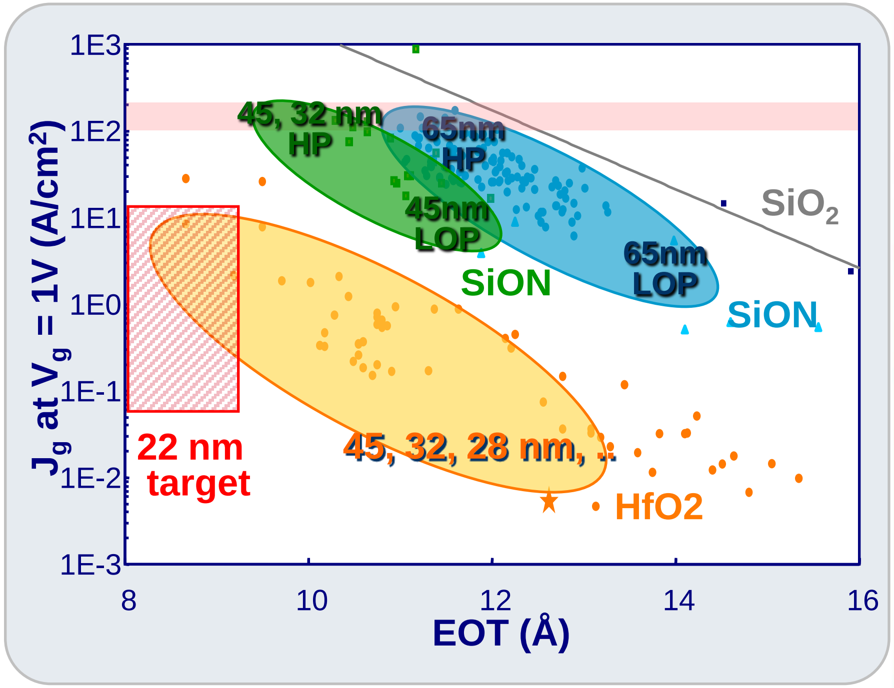
- MG
  - Low damage deposition to prevent Metal or N diffusion into hiK
  - ALD metal dep for GL or 3D applications

Fundamental Challenges
on
HiK/MG Stack

Evolution of Jg/EOT



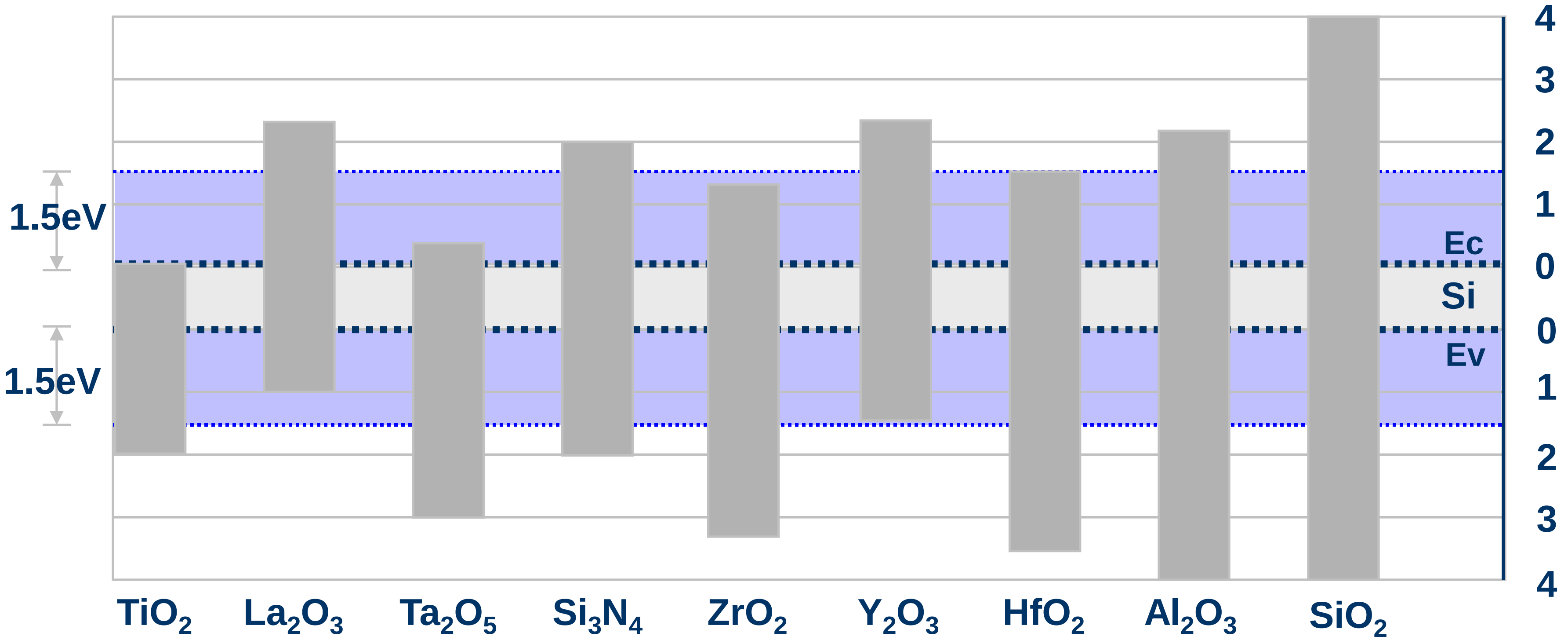
IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 50, NO. 4, APRIL 2003



- Scaling limitation of SiON: Jg ~ 1E2 A/cm2, EOT ~ 10A.
- 100x Jg reduction from SiON requires new dielectric system.
- Poly depletion forces the use of metal gate for EOT control.

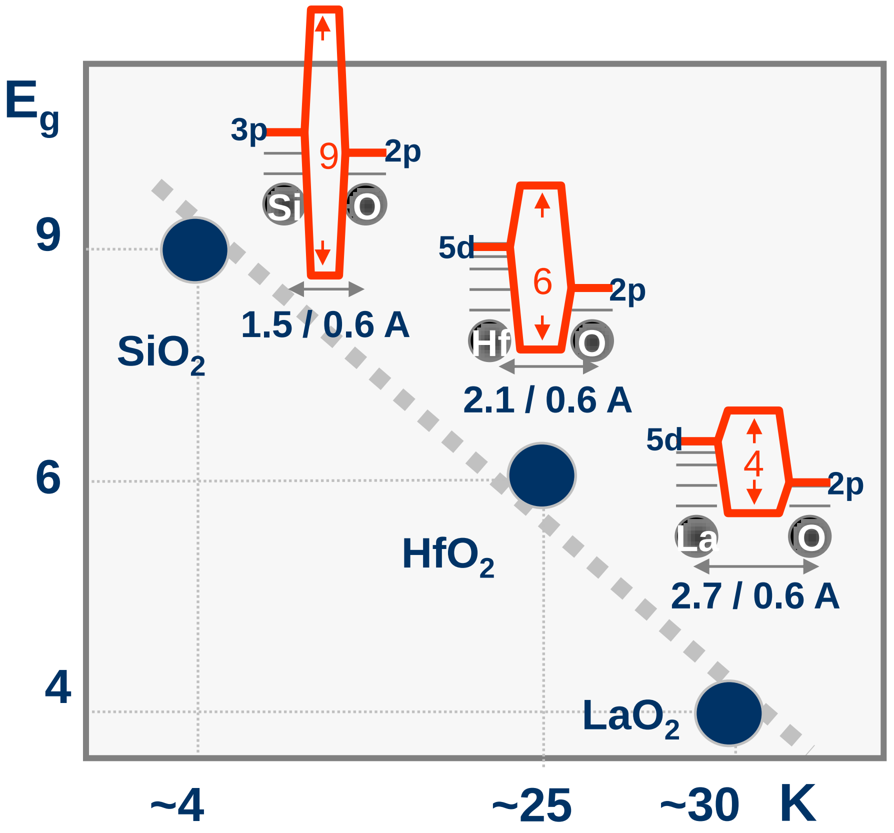
Scaling Comparison of Various Dielectrics

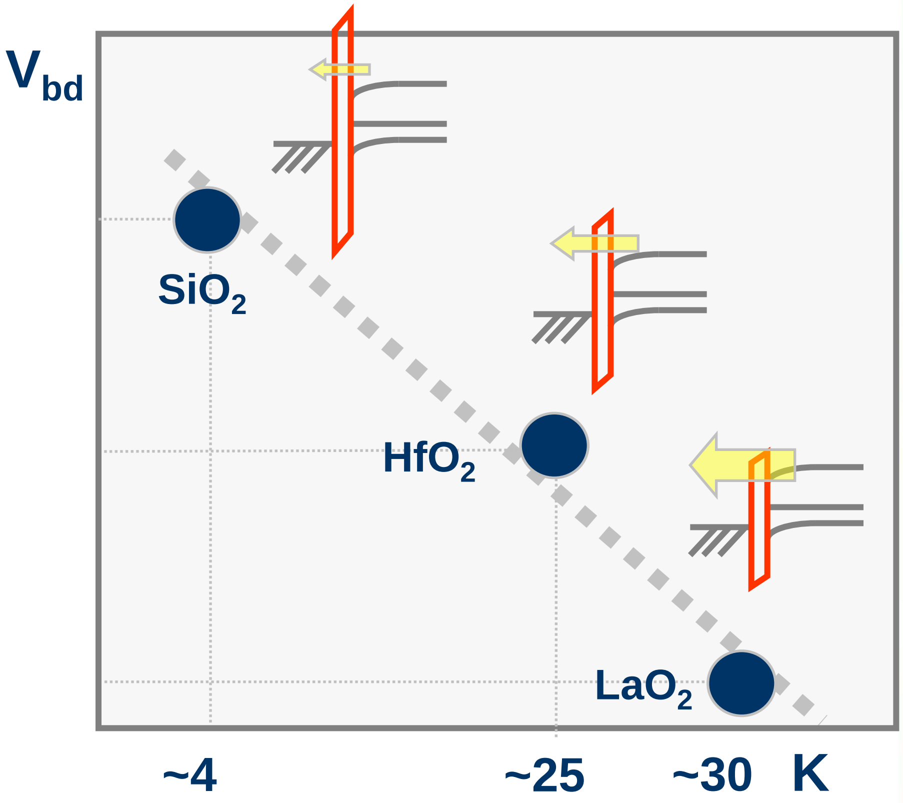
- Barrier height needs at least 1.5 eV for proper leakage suppression.



3	4.3	4.5	5.1	5.4	5.6	6	8.7	9	Eg
0	2.3	0.4	2	1.4	2.3	1.5	2.1	4	$\Delta\Phi c$
2	1	3.1	2.1	3	2.3	3.5	5.6	4	$\Delta\Phi v$
60	30	25	7	30	15	25	9	3.9	k

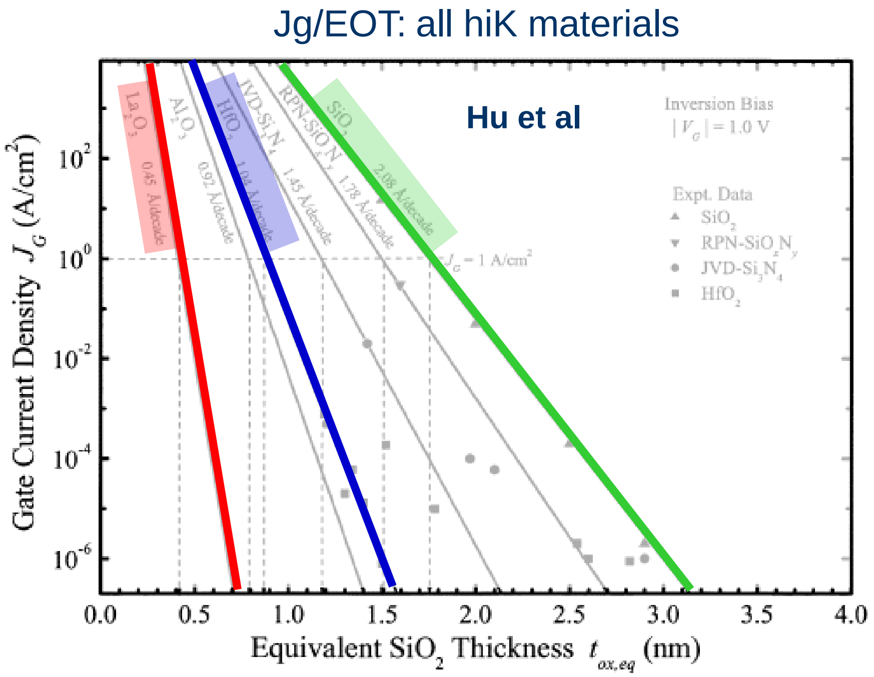
Fundamental Conflicts: E_g vs K vs V_{bd}



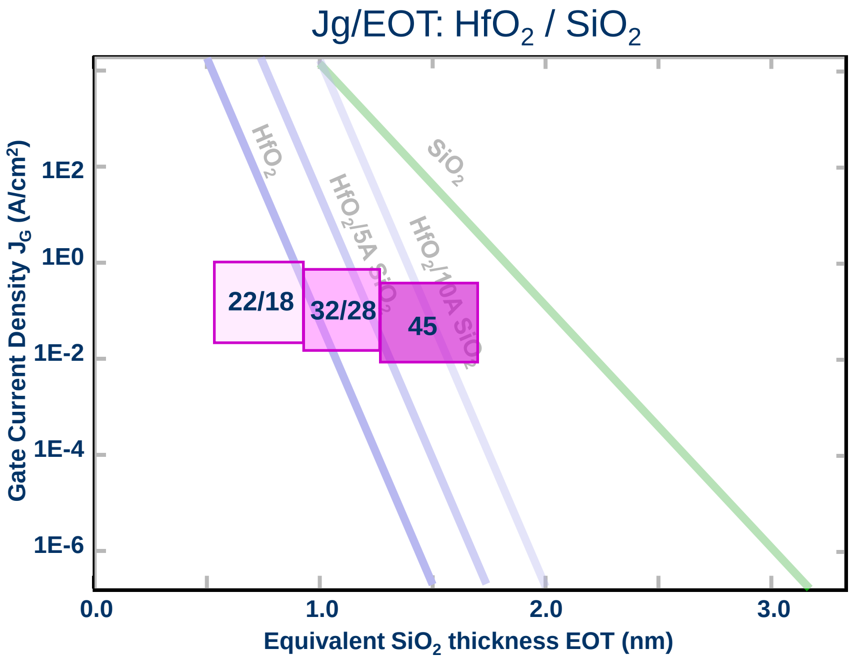


- Small bonding radius (ex SiO2): Larger Eg, smaller K, larger Vbd.
- Large Bonding radius (ex LaO2): Smaller Eg, larger K, smaller Vbd.

Jg/EOT Scaling Trajectory (w/ & w/o SiO_2)

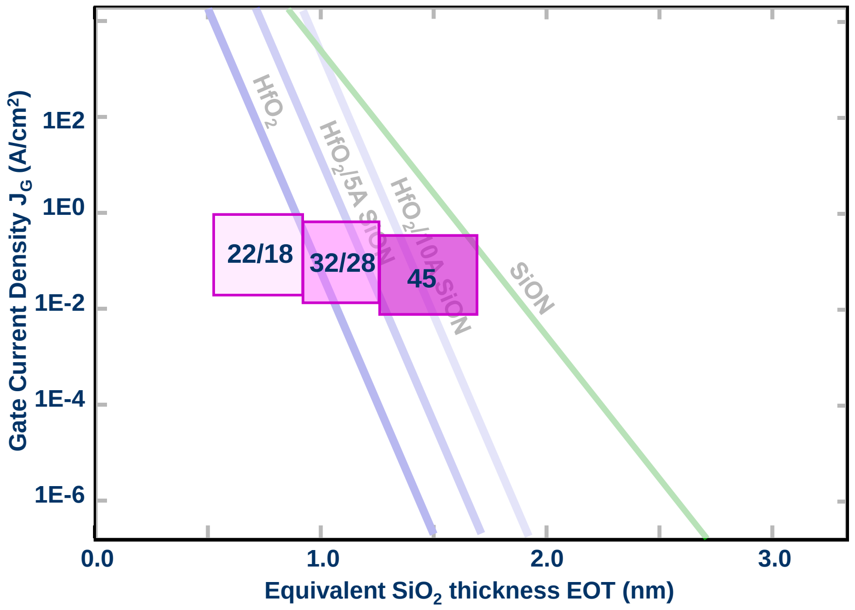

Jg/EOT: all hiK materials

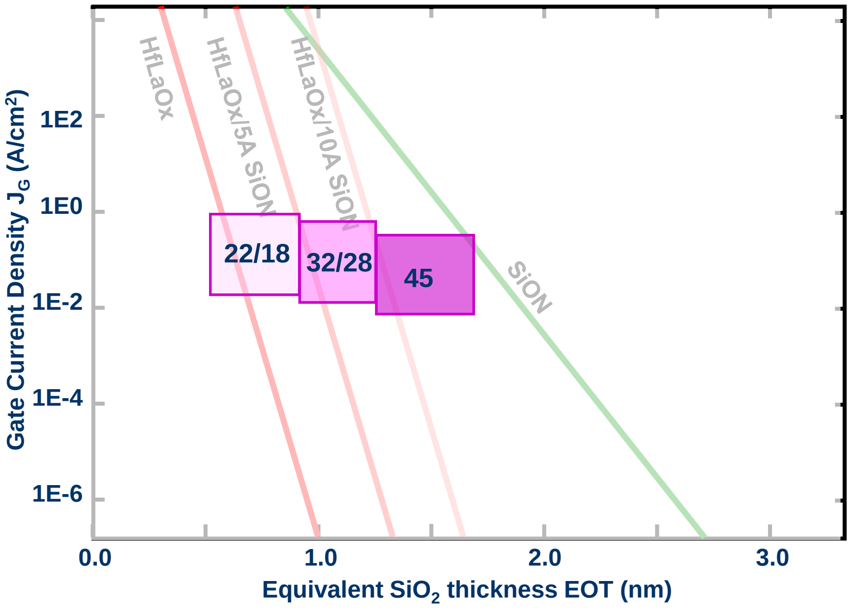
IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 50, NO. 4, APRIL 2003


Jg/EOT: HfO_2 / SiO_2

- Without Box, HfO_2 can reach 1/10 ($1A/cm^2$ J_g & 10A EOT), but with low μ.
- The addition of 5A SiO_2 as Box, HfO_2/SiO_2 stack can not reach 1/10.
- Box has significant effect on the scalibility of HfO_2 for 32nm and beyond.
- Higher-K Box, in combination with HfO_2, will be needed for 22nm (10^{-1}/8).

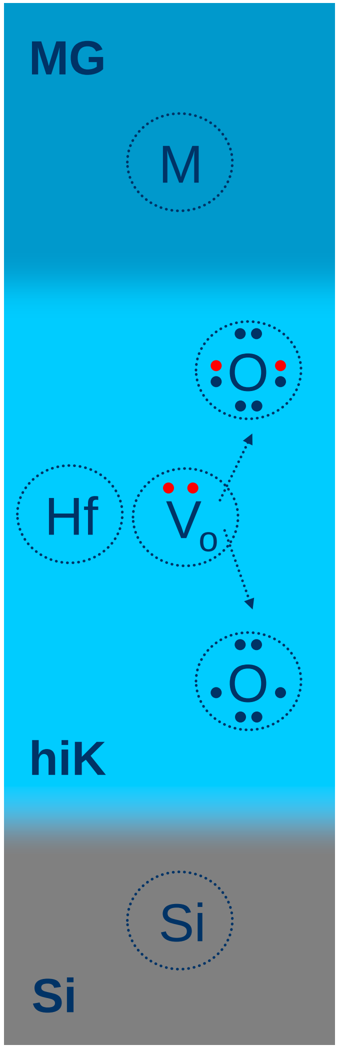
Jg/EOT Scaling Trajectory (HfO_2 vs HfLaOx)


Jg/EOT: HfO2 / SiON


Jg/EOT: HfLaOx / SiON

- The HfO2 + SiON can reach 32nm (1/10), but will be hard for 22nm (10^{-1}/8).
- Higher-K dielectric (ex: HfLaOx with K ~ 27) can provide additional scaling.
- HfLaOx (as ex.), in combination with SiON, can reach both 10^{-1}/8 and 10^{-3}/7.
- Development of higher-K (>25) will be crucial for sub 22nm applications.

Evolution of Material and Device Issues



Thermal instability of Hf-O bonding w/r to Si-sub and MG

Formation of oxygen vacancy (V_o) & Interstitial (I_o) in hiK

Redistribution of Ox and formation of dipole

Fundamental material issue

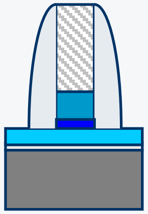
- **Fermi / V_t Pin**
- **V_t roll off**

- **Gate leakage**
- **V_t instability**

- **Low V_{bd}**
- **Low T_{bd}**

Subsequent device issue

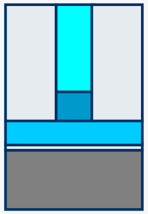
GF



passivation and reduction of V_o

Cap layer for V_t readjustment

Hik 1st, MG last

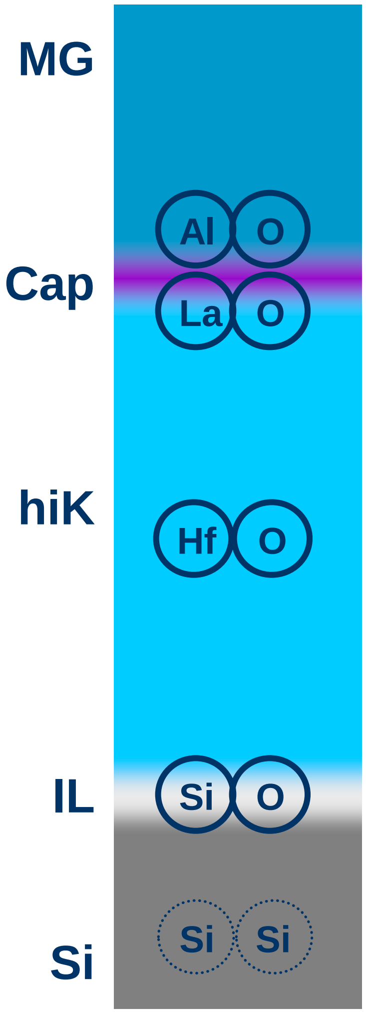


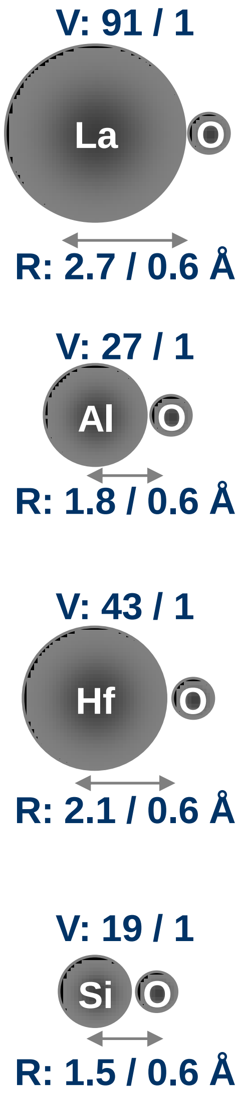
passivation and reduction of V_o

IL layer for V_o reduction

Integration solutions

Stability of the HiK/MG Stack





V: 91 / 1

R: 2.7 / 0.6 Å

V: 27 / 1

R: 1.8 / 0.6 Å

V: 43 / 1

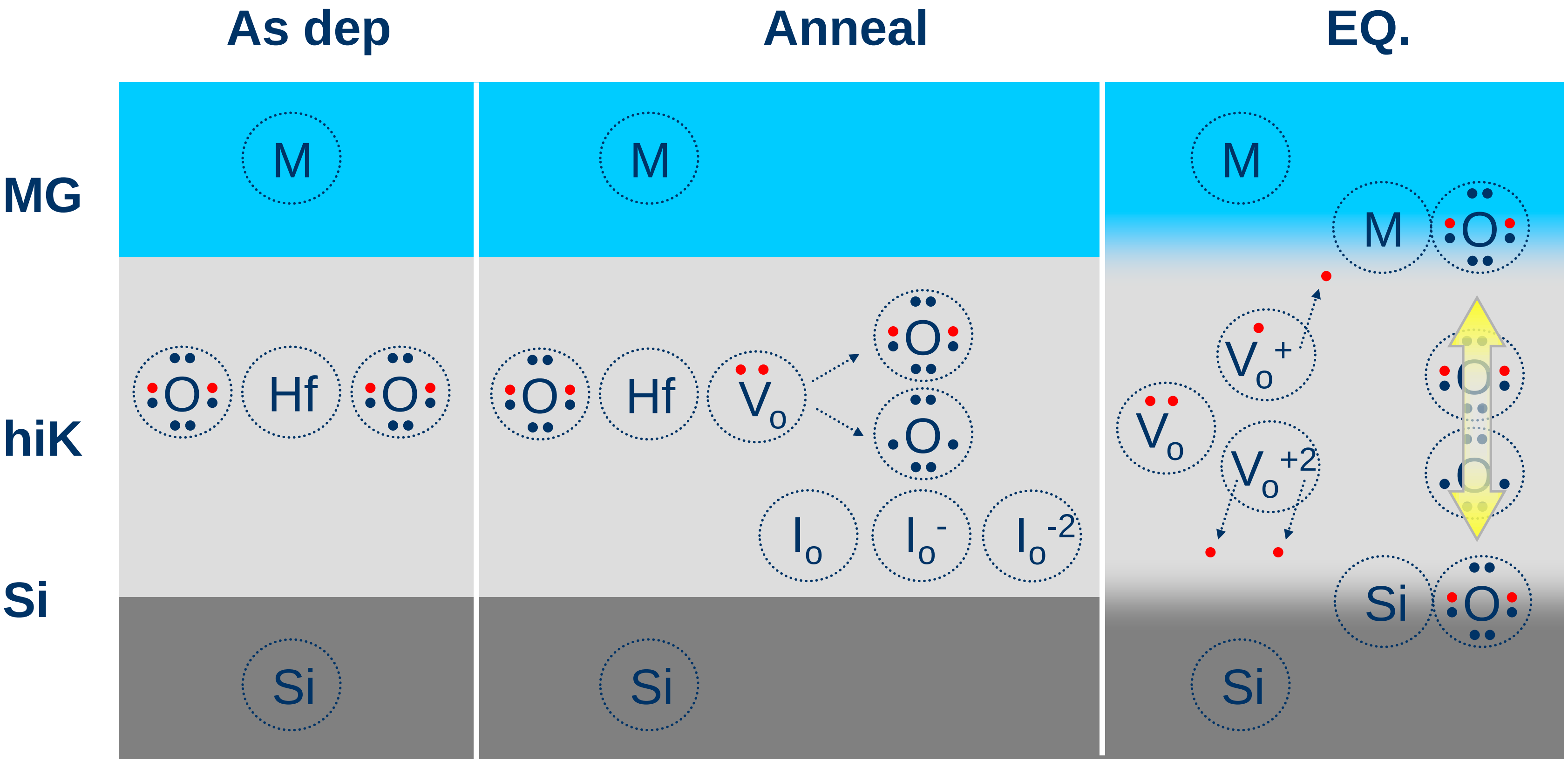
R: 2.1 / 0.6 Å

V: 19 / 1

R: 1.5 / 0.6 Å

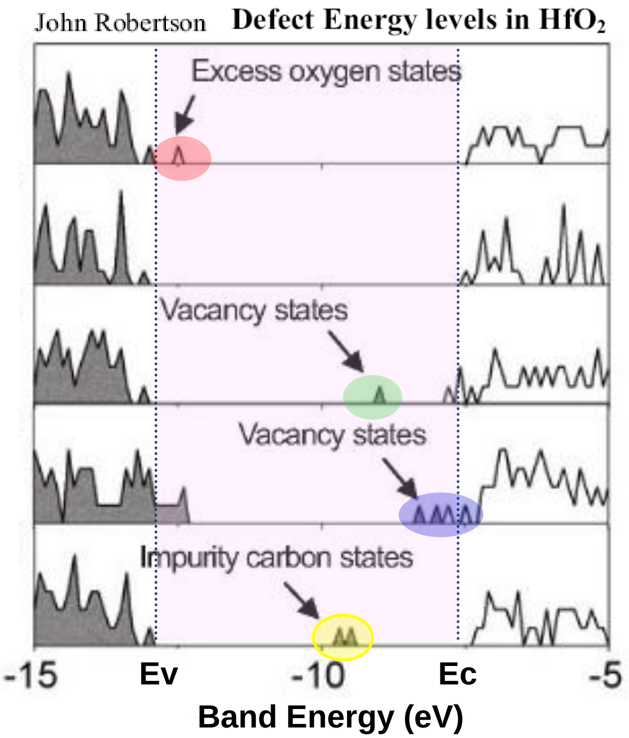
Bonding pair	Bonding Energy (KJ/mole)
W-W	666
Ti-N	476
La-O	798
Al-O	501
Hf-N	535
Hf-O	801
O-N	631
Si-N	437
Si-O	799
Si-Si	310

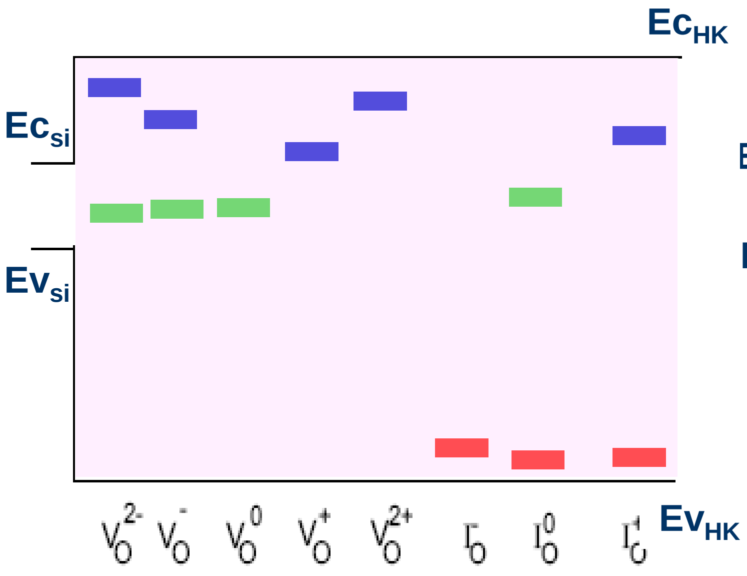
Evolution and Formation of Vo and Io

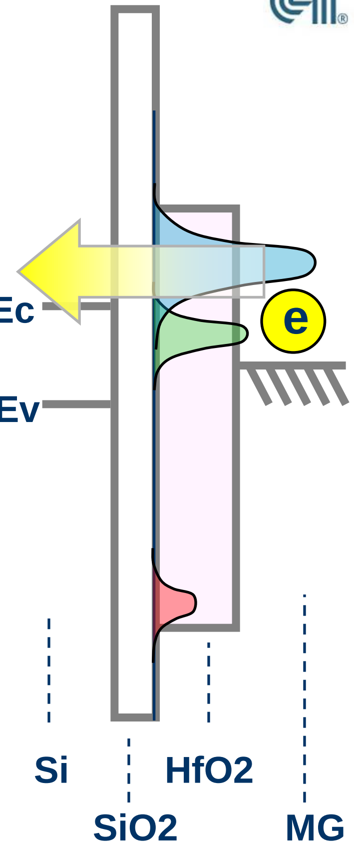


- Oxygen atoms have the tendency to diffuse into Si sub and MG.
- Formation Oxygen vacancy (V_o^+) or Oxygen interstitial (I_o^-) in hiK layer.
- Formation of SiOx IL (below hiK) and MOx IL layer (above hiK).
- Electron redistribution across IL's results in uncontrollable dipoles.

Gap States Induced by Vo and Io

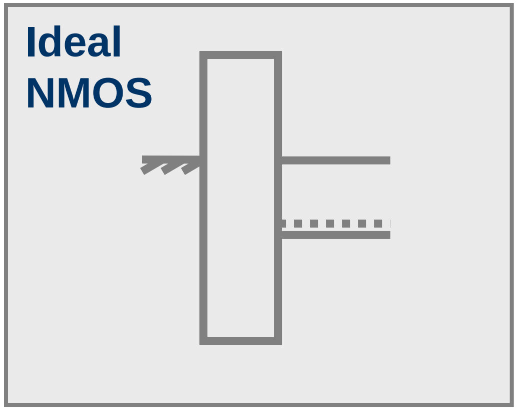


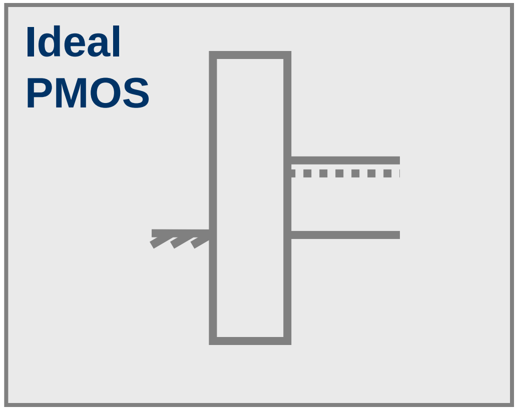


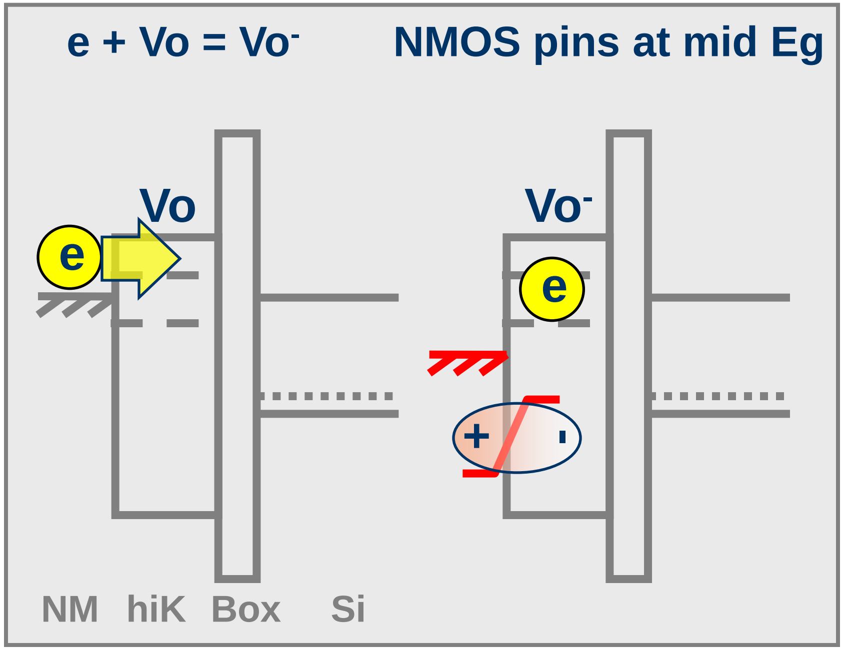


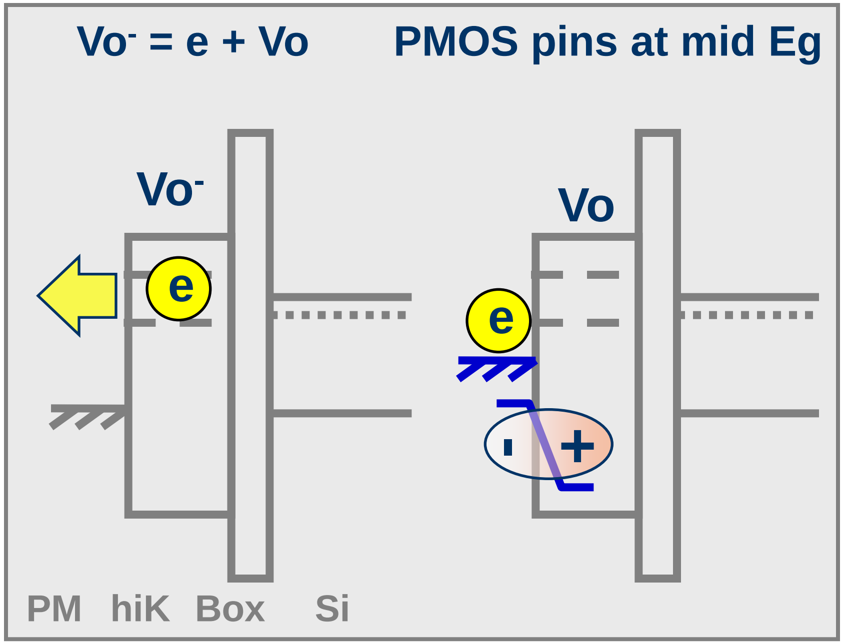
- Vo causes defect states near Ec edge, leads to electron leakage.
- Both Vo and Io reduce effective Bandgap of HfO_2.
- Carbon atoms induce midgap states in HfO_2, increase Jg.

Fermi & Vt Pinning by Vo in HfO_2

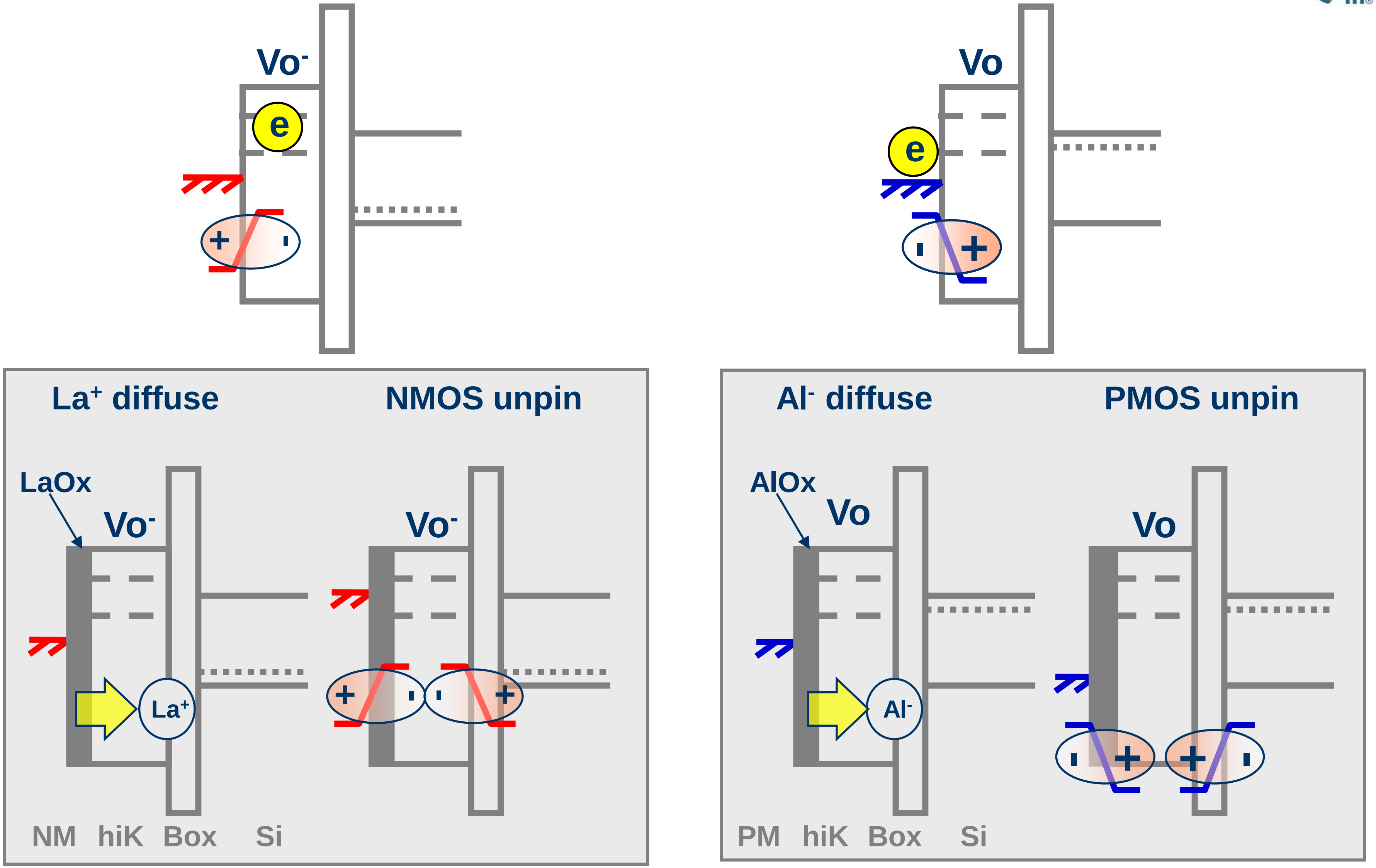








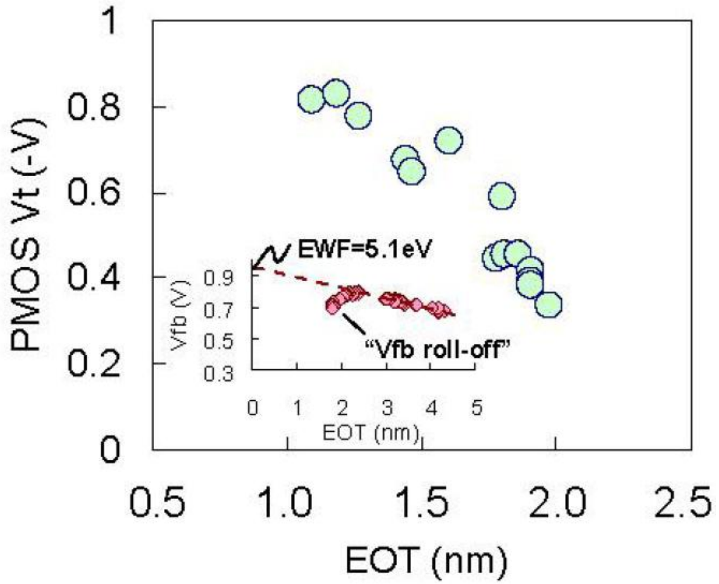
Resolving Fermi Pinning with Cap Layer

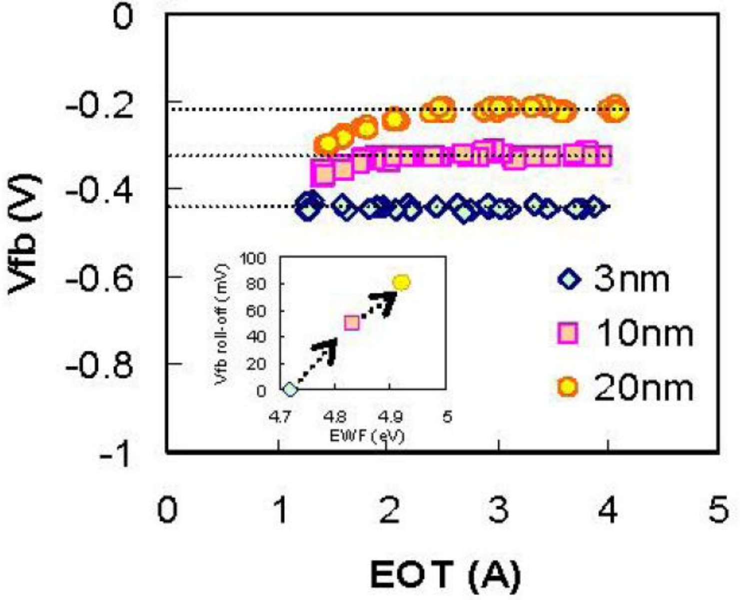


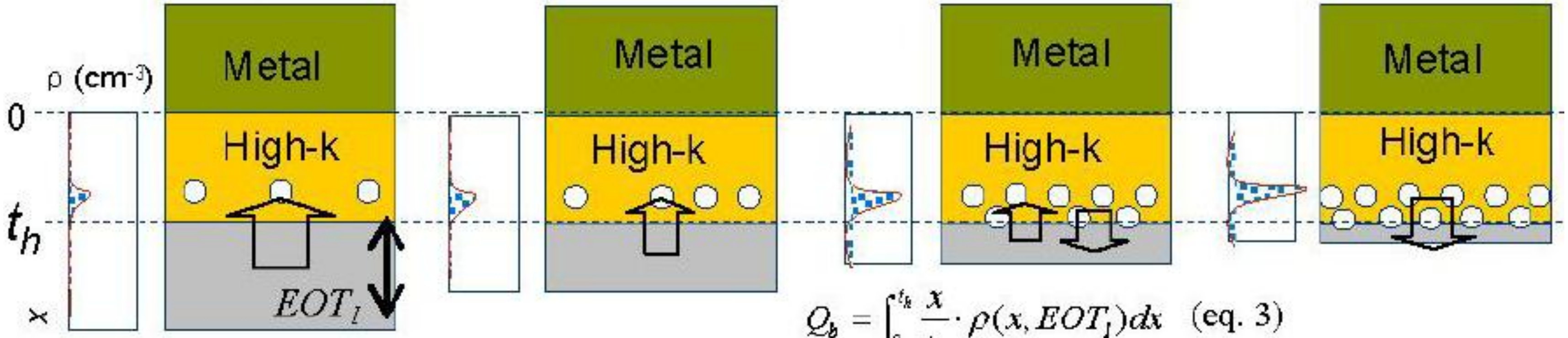
Vo Induced Vt roll-off (Sematech)

Mechanism of V_{fb} roll-off with High Work function Metal Gate and Low Temperature Oxygen Incorporation to Achieve PMOS Band Edge Work function

S. C. Song et al







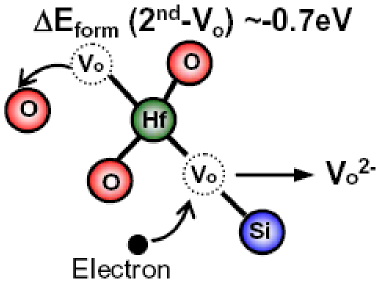
$$Q_b = \int_0^{t_h} \frac{x}{t_h} \cdot \rho(x, EOT_1)dx \quad \text{(eq. 3)}$$

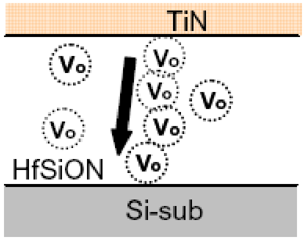
Vo Induced Gate Leakage (Selete)

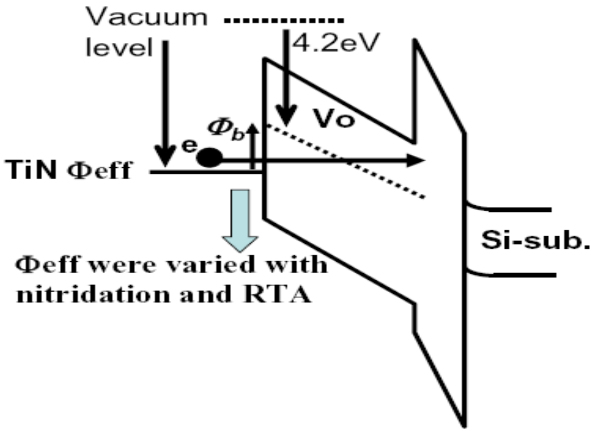
CATHODE ELECTRON INJECTION BREAKDOWN MODEL AND WORK FUNCTION DEPENDENT TDDB LIFETIME FOR HIGH-K / METAL GATE STACK PMOSFETS

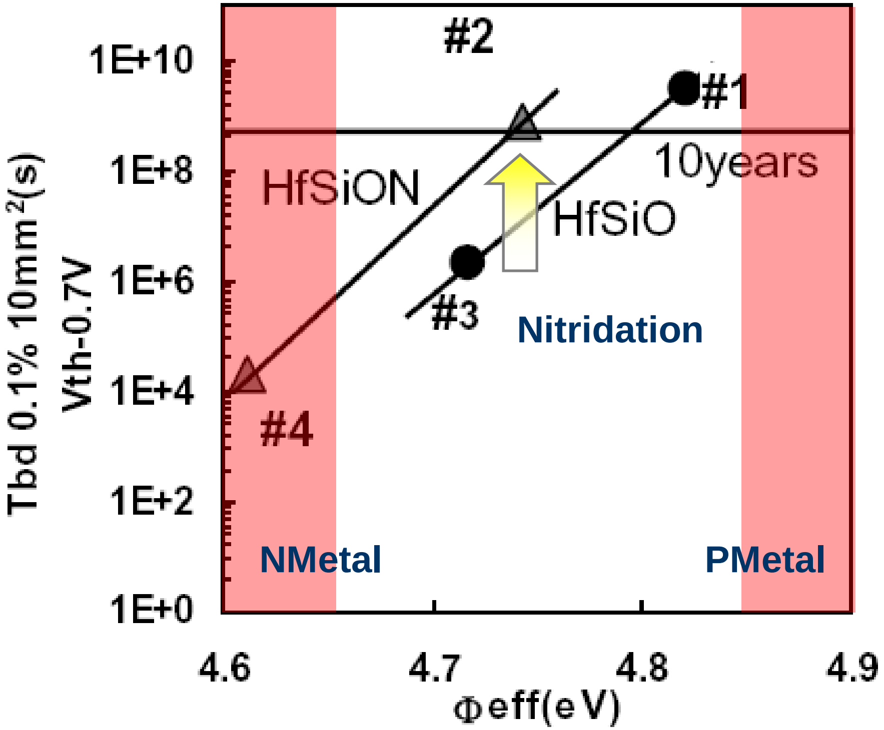
Motoyuki Sato et al

IEEE CFP08RPS-CDR 46th Annual International Reliability Physics Symposium, Phoenix, 2008









- Vo chain reaction can be initiated by electron leakage current (Jg_e).
- Jg_h result in less Vo trap state generation than Jg_e
- Nitridation passivates Vo and therefore improves Tbd.
- Low EWF metal will suffer more Vo generation within hiK, and thus lower Tbd.