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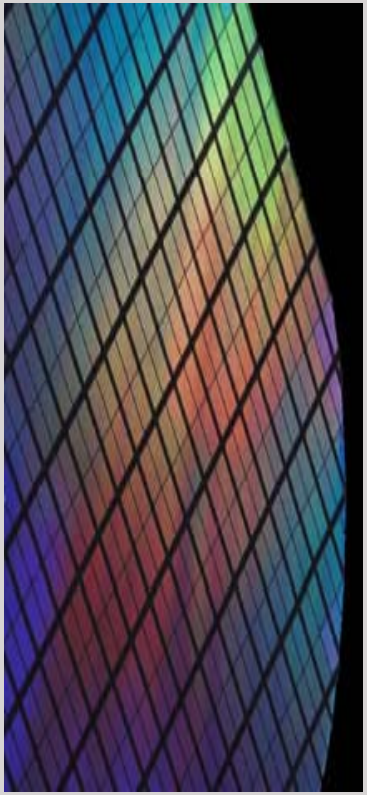
Phase Change Memory:

Status and Challenges to Navigate an Increasingly Competitive Memory Landscape

Chuck Dennison
Ovonyx, Inc.
14-Oct-2009

Outline

- Phase Change Memory (PCM) Overview
- PCM Scaling
- Comparative Memory Technology Roadmap
- Product Roadmap
- Summary



PCM Attributes

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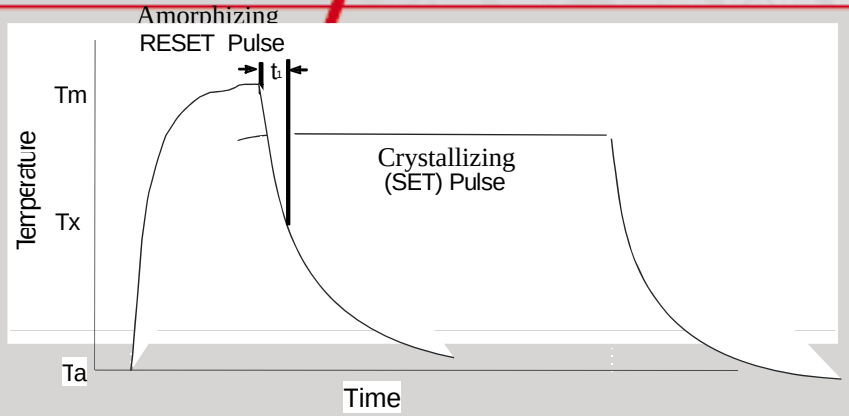
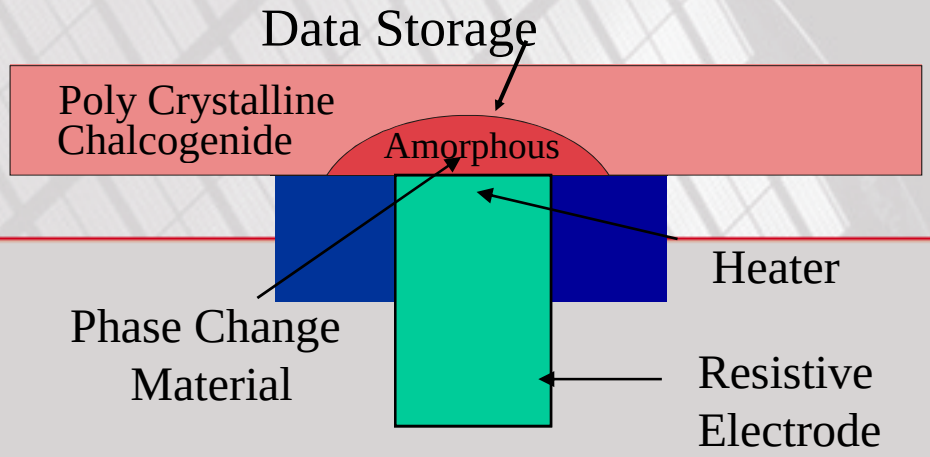
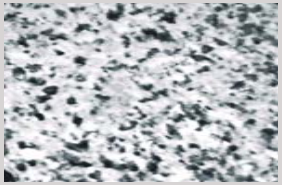




Amorphous Phase

TEM Images

Crystalline Phase



Electron Diffraction Patterns

- Short-range atomic order
- Low free electron density
- High activation energy
- High resistivity

- Long-range atomic order
- High free electron density
- Low activation energy
- Low resistivity

- **Operation**
  - Chalcogenide material alloys used in re-writable CDs and DVDs
  - Energy (heat) converts the material between crystalline (conductive) and amorphous (resistive) phases
    - CD's: Laser energy / reflectivity
    - PCM: Electrical energy for programming and read by measuring resistance
- **Attributes**
  - \+ Non-volatile
  - \+ Potentially fast write
  - \+ High density
  - \+ Non-destructive fast read
  - \+ Low voltage
  - \+ ~ 10^8 - 10^{12} write/erase cycles
  - \+ Integrate-able w/ CMOS logic
  - \+ Bit alterable (no block erase)

PCM Programming

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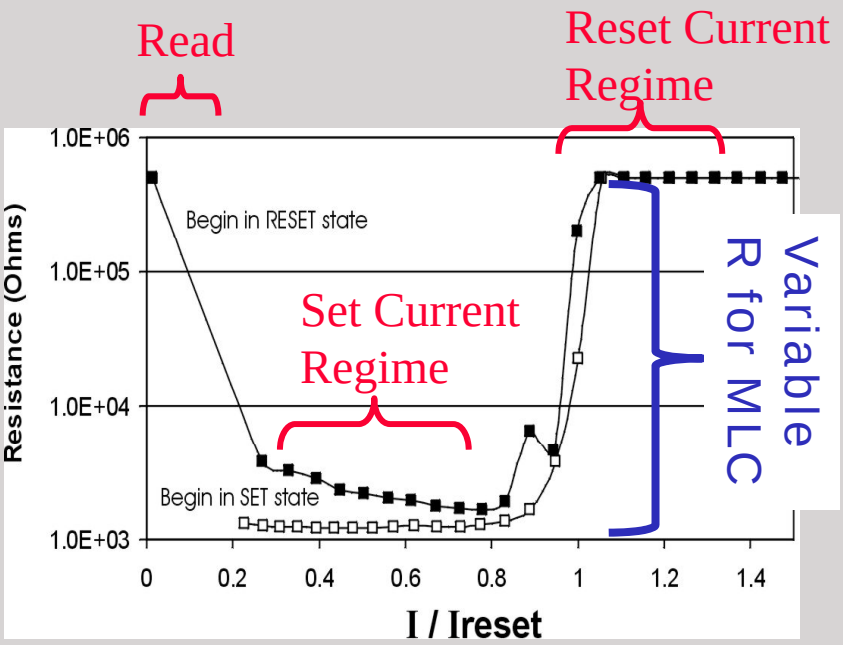
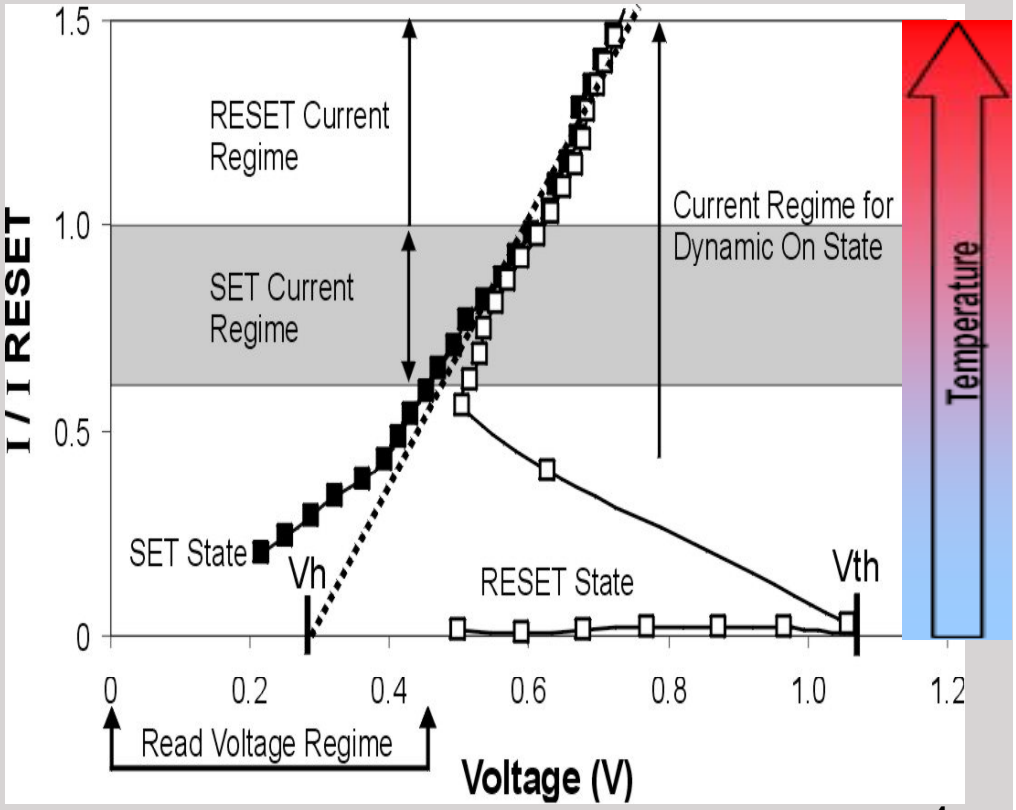
R_{set} and R_{reset} as Function of Cell Current



IV Curve of Chalcogenide Element



Reset Amorphous Phase

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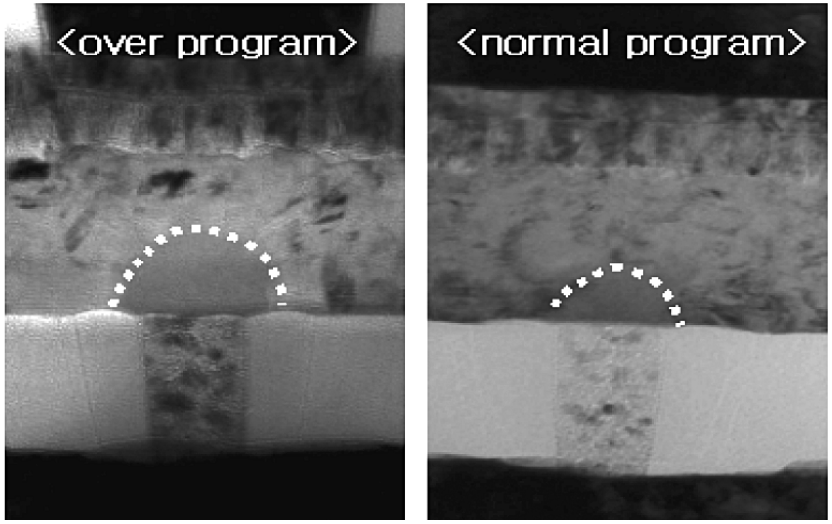

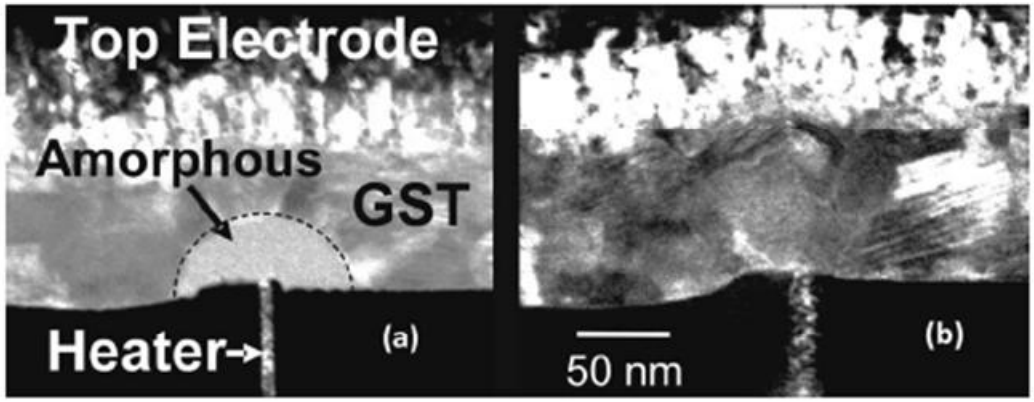

FIG. 1. Cross-sectional transmission electron micrograph of active region of a PCM cell in (a) reset and (b) set states.

K. Kim and S.J. Ahn, Samsung Electronics Proc. IEEE 43rd IRPS157 (2005).

J. Sarkara, *Flash Memory Group, Intel Corporation* APPLIED PHYSICS LETTERS **91, 233506 2007** (now Numonyx)

Data Retention

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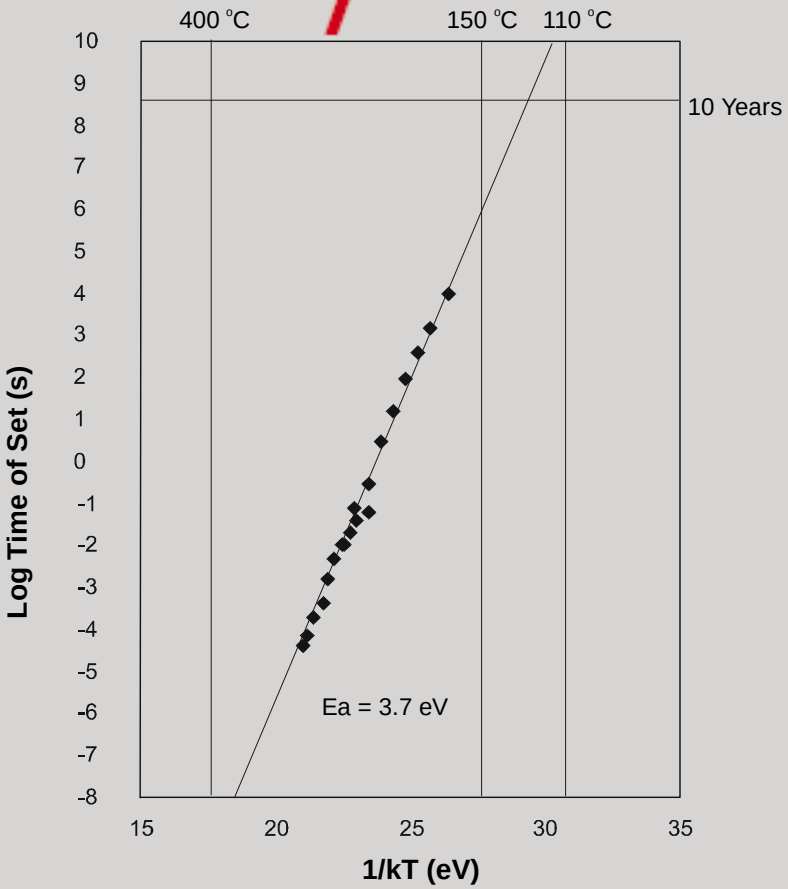


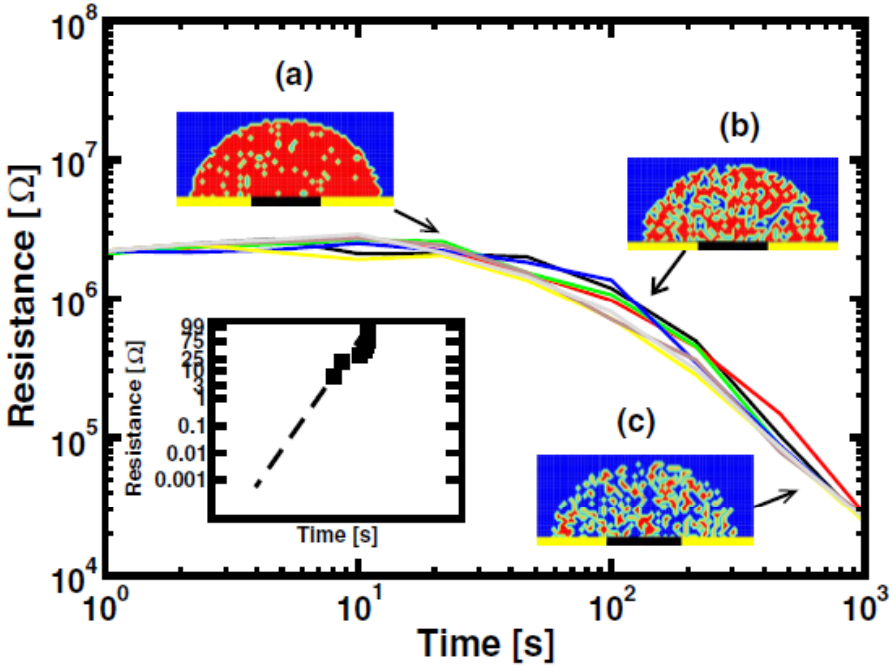


Fig. 3. Calculated R as a function of time, according to the Monte Carlo model for crystallization. The phase distribution for three points in the $R-t$ curve are shown. Crystal grains are in blue, amorphous phase in red.

"Impact of Crystallization Statistics on Data Retention for Phase Change Memories" A. Redaelli, et.al. Dipartimento di Elettronica e Informazione, Politecnico di Milano, and ST 2005 IEDM

Data Retention: Is the stochastic nature of percolation an issue for Mbit arrays?

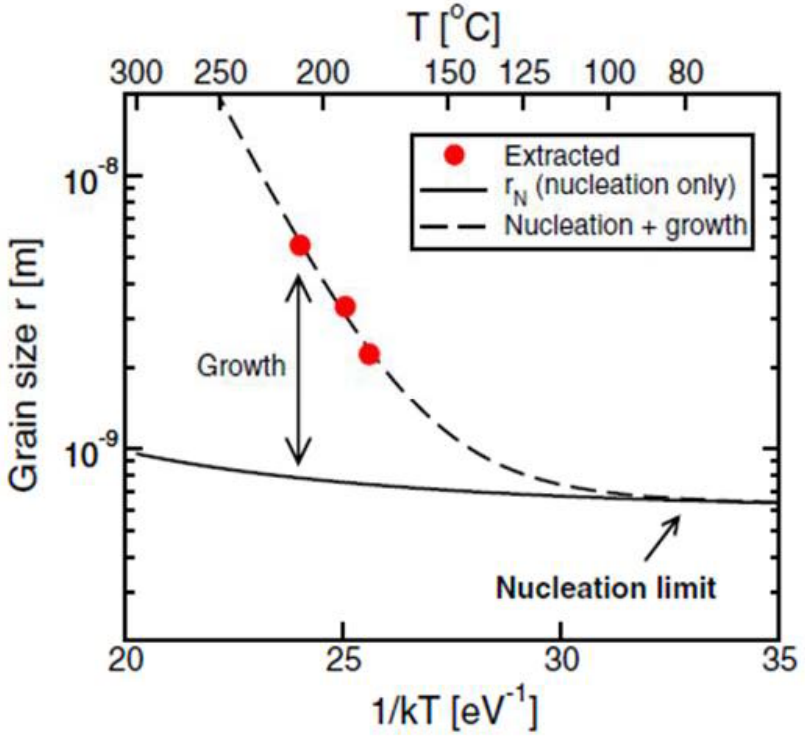


Fig. 8. Effective grain size r as a function of $(kT)^{-1}$ (Arrhenius plot). Data extracted from Fig. 7 are compared with theoretical nucleus size r_N, allowing to evaluate the contribution of the growth kinetics (dashed line).

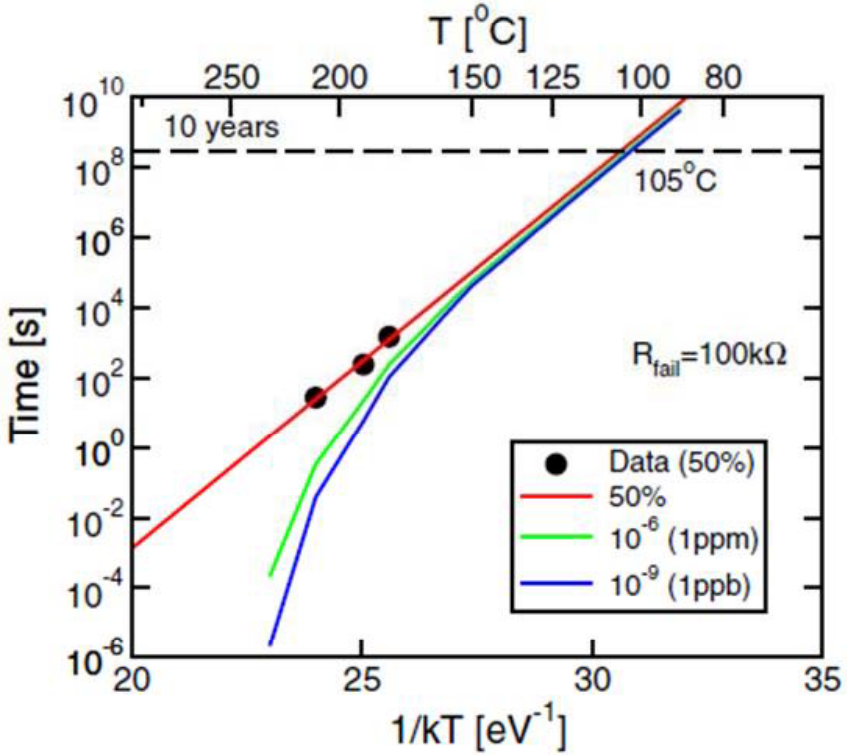
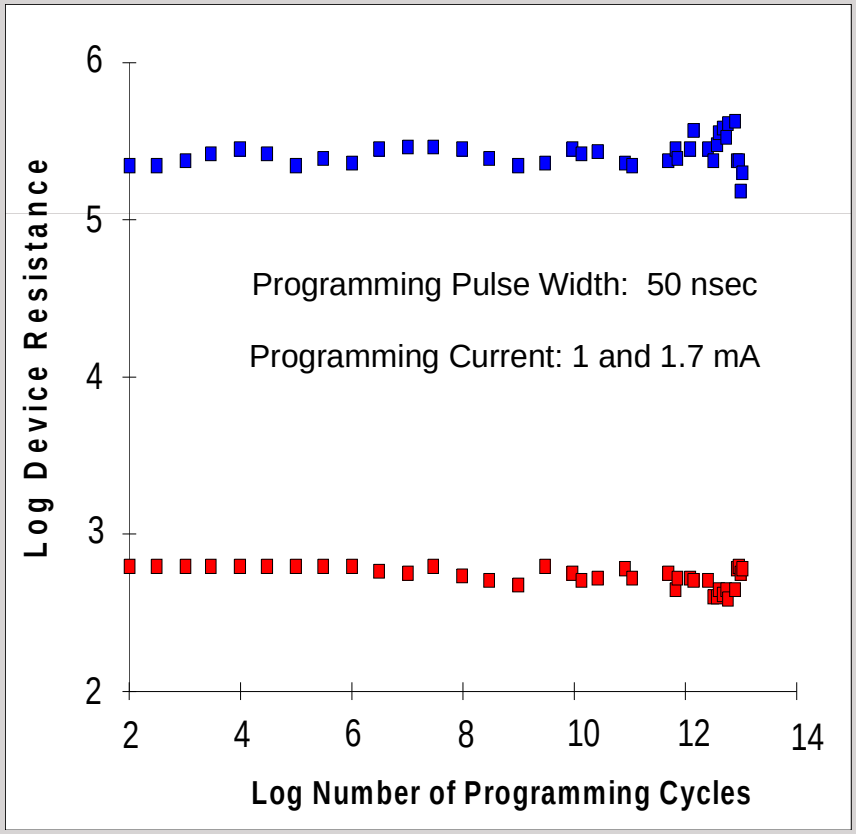


Fig. 11. Calculated retention times at $R_{fail} = 100$ kΩ, assuming failure probabilities 50%, 10^{-6} and 10^{-9}. Data for the 50% percentile at $T = 180$, 190 and 210°C are also shown. The projected maximum temperature for 10-years data retention negligibly depend on the failure percentile, as a result of growth de-activation and β enhancement at small T.

"Impact of crystallization statistics on data retention for phase change memories" A. Redaelli, et.al. Politecnico di Milano, and ST 2005 IEDM

Cycling Endurance

Intrinsic cycle life > 10^{13} write/erase cycles, Demonstrated Mbit Array cycling > 10^{8}



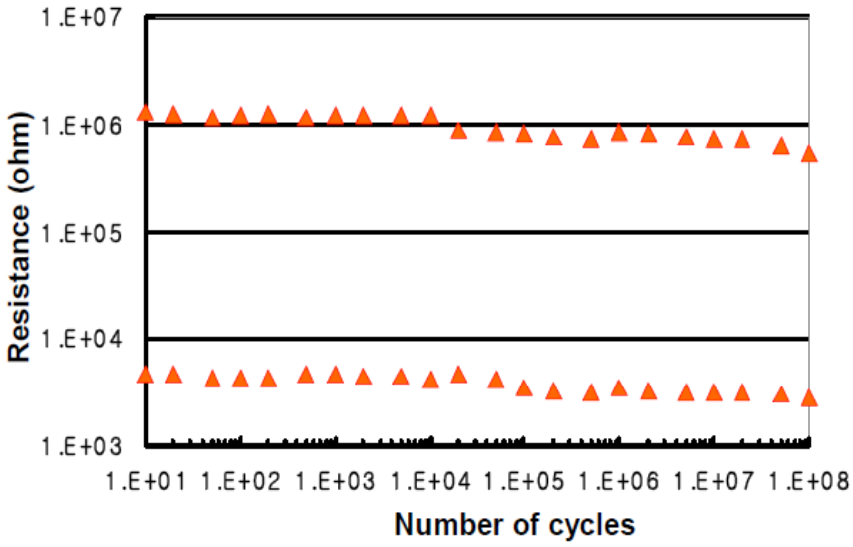


Fig. 12 Endurance properties of GST cells in full integrated 256Mb PRAM.

Y.J. Song, et. al 2006 Symp. on VLSI Technology Digest of Papers.

Cycling Endurance

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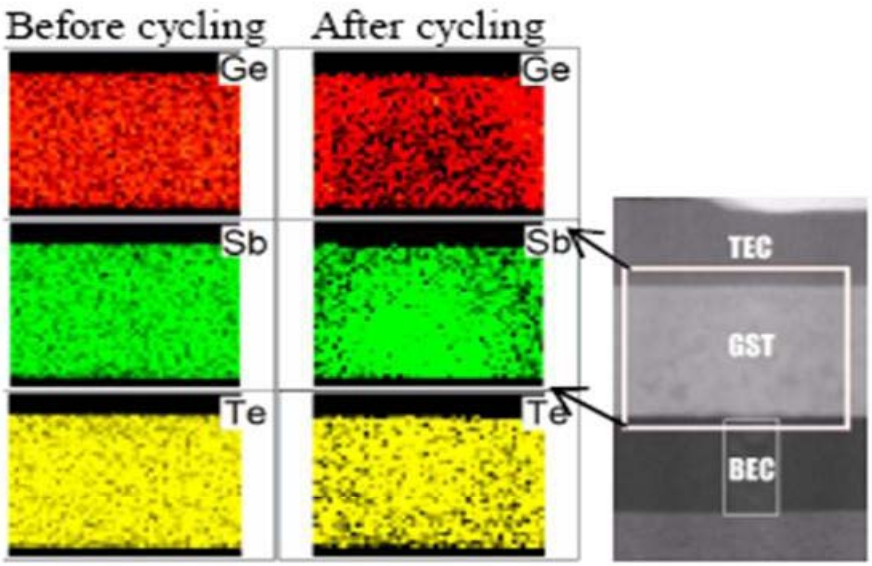

Fig. 12: Results of EDX elemental analysis showing an agglomeration of Sb atoms at the GST/BEC interface after cycling.

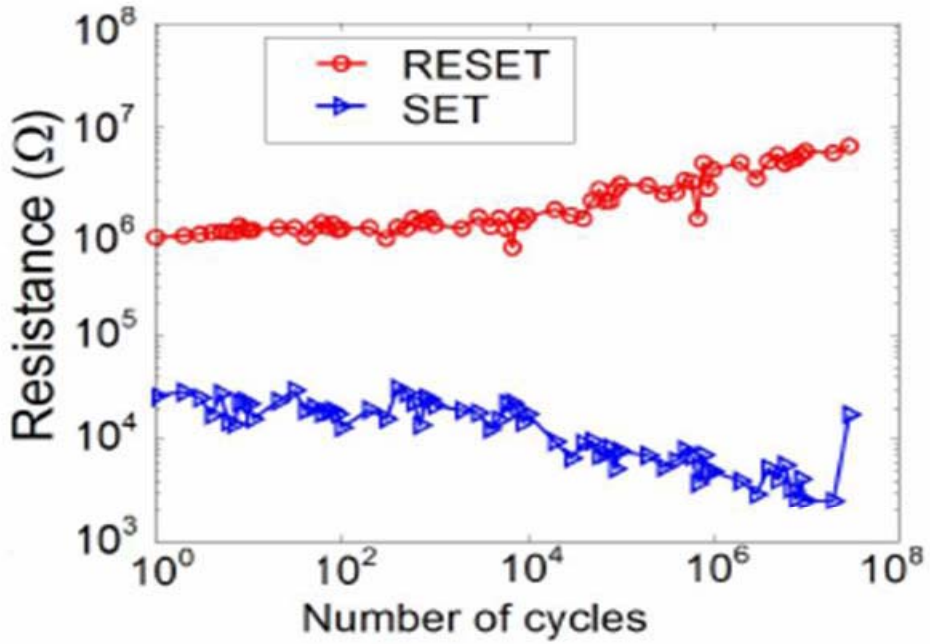

Fig. 9: Shift in resistance levels with cycling.

Energy Dispersive X-ray analysis of the active volume of memory cells indicates that Sb atoms begin to agglomerate near the BEC/GST interface with cycling (Fig. 12), resulting in a dome-like metallic region at the interface. This effectively increases the area of contact between the BEC and GST (as if the BEC were 'protruding' into the GST), explaining the steady decrease in SET resistance with cycling

"On the Dynamic Resistance and Reliability of Phase Change Memory"
B. Rajendran, et. al. IBM Macronix PCRAM Joint Project

2008 Symposium on VLSI Technology Digest of Technical Papers p96

Cycling Endurance

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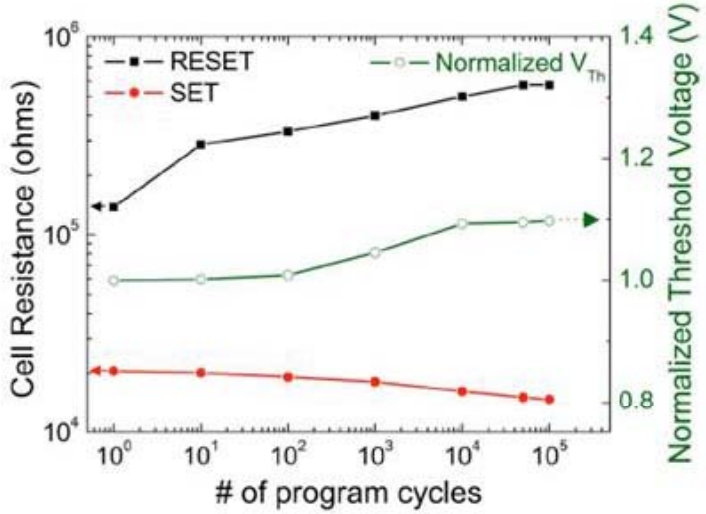
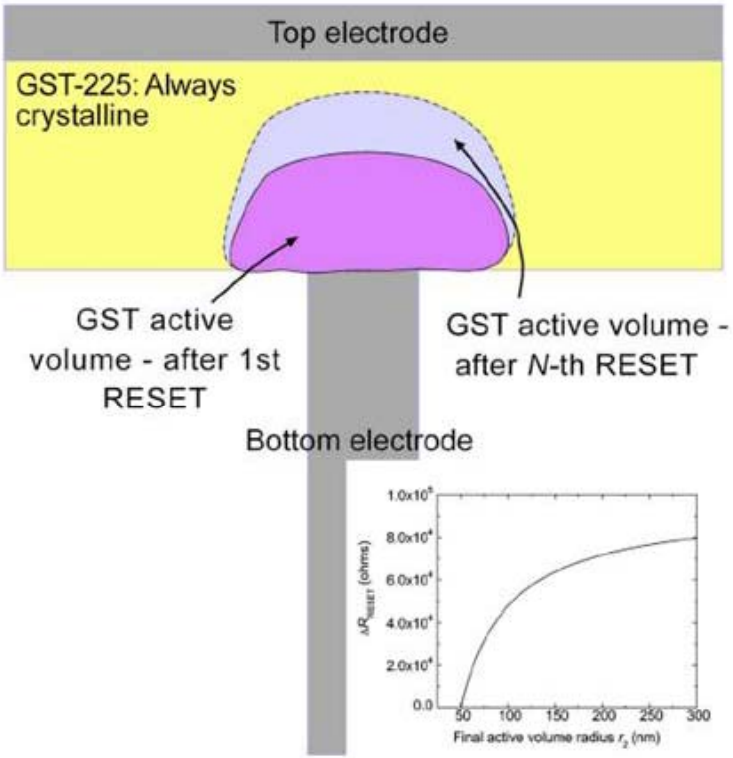


FIG. 2. (Color online) Improvement in reset- and set-state resistances (solid symbols, left axis) and the normalized threshold voltage (hollow symbols, right axis) with operational/programming cycles of a representative PCM cell. The points on this curve correspond to the median of a distribution of 25 kbits of a multimegabit array.

the temperature gradient during programming.[7] Ryu *et al.*[8]



Cycling Endurance

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Significantly longer cycle life (>10^{10} seen for scaled devices with confined cell

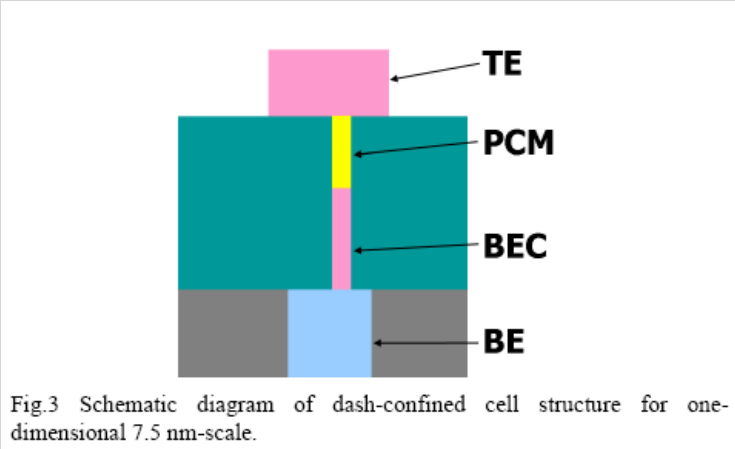
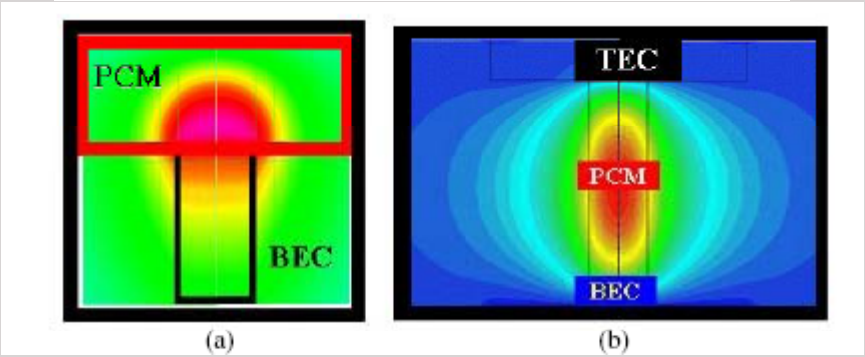


Fig.3 Schematic diagram of dash-confined cell structure for one-dimensional 7.5 nm-scale.



A Unified 7.5nm Dash-Type Confined Cell for High Performance PRAM Device D.H. Im, Samsung

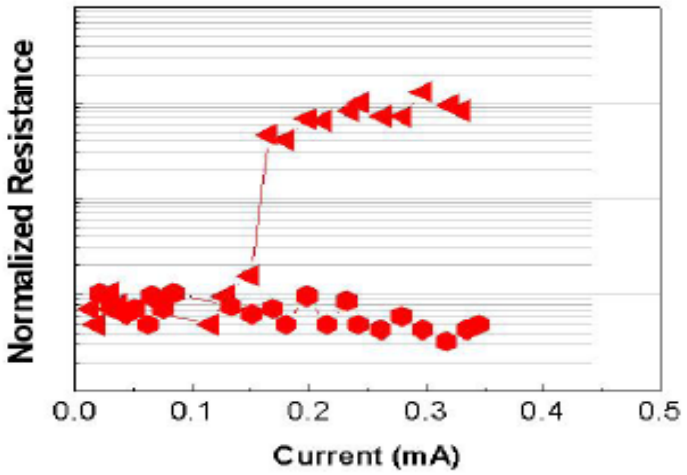


Fig.6 R-I curve of dash-confined cell.

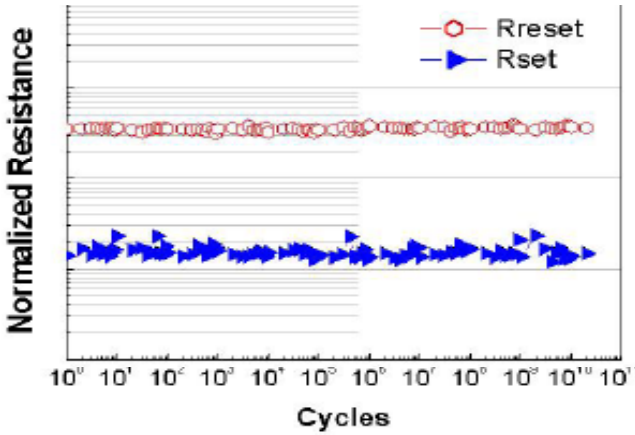
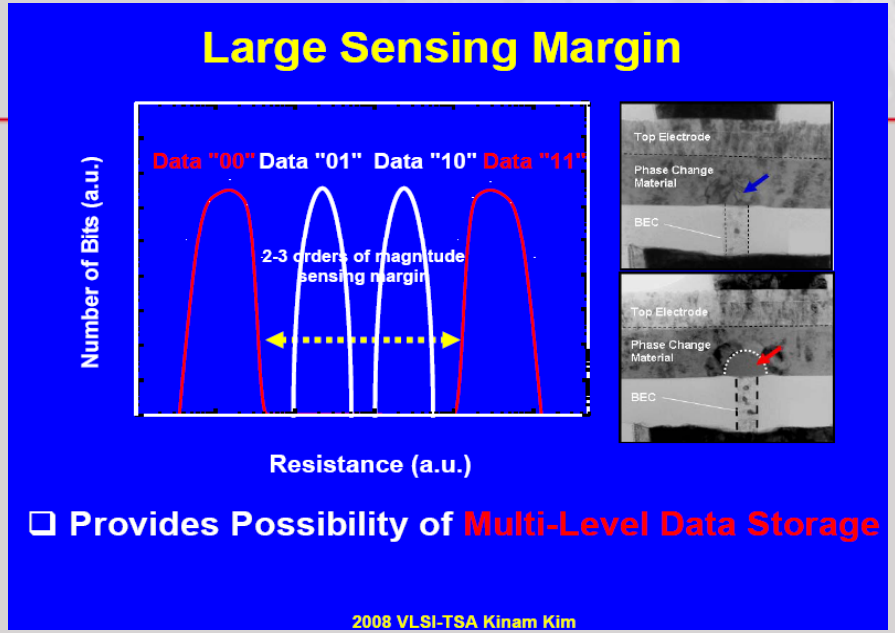
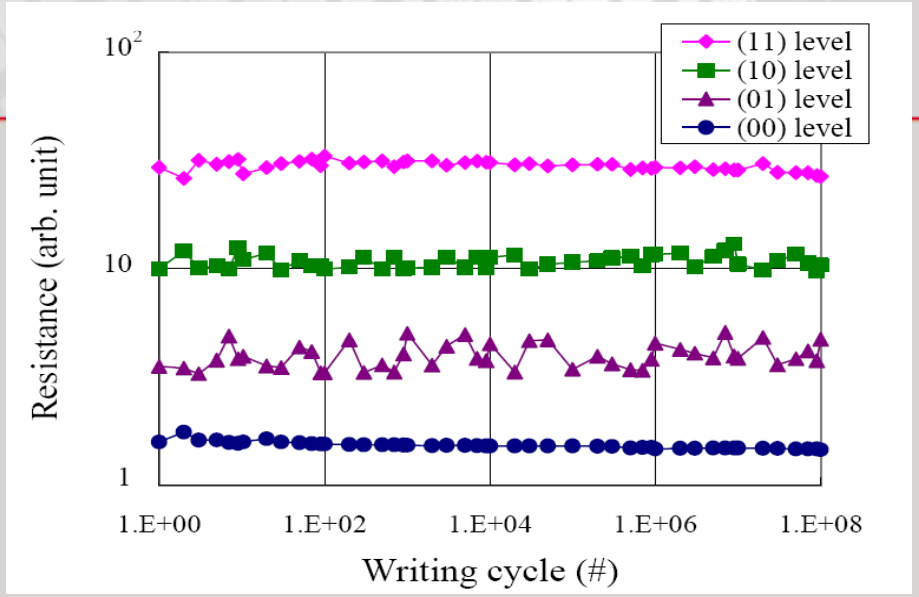


Fig.10 Endurance characteristic of a dash-confined cell.

MLC Opportunity / challenges in Phase Change Memory





Two-bit Cell Operation in Diode-Switch Phase Change Memory Cells with 90nm Technology" Symposium on VLSI Techn., 98 (2008)

Phase Change memory has a wide dynamic resistance range thus providing Multi-Level Cell, but has is not without challenges:

1.) Accurate Placement: requires Write/read Verify with some iteration
2.) Resistance change with Temperature (Ea) dependent on resistance (amount crystalline vs. amorphous) : requires temp tracking
3.) "Resistance Drift" Increase in resistance over time (minimal for low R crystalline GST, increases with programmed R (amount of amorphous material)

MLC challenge: "Resistance Drift"

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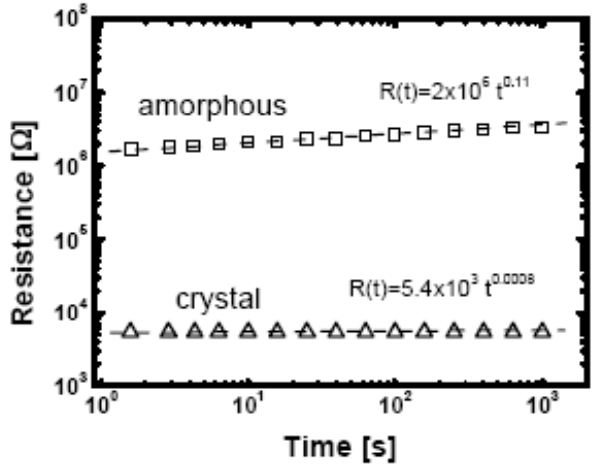
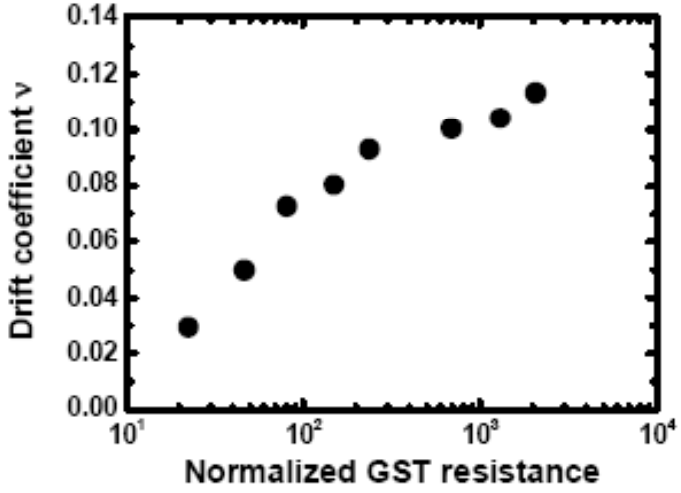


Figure 1: Time-instability of low filed resistance of a PCM device. It is worth noting that amorphous phase increases its resistance towards higher values with a power law dependence.



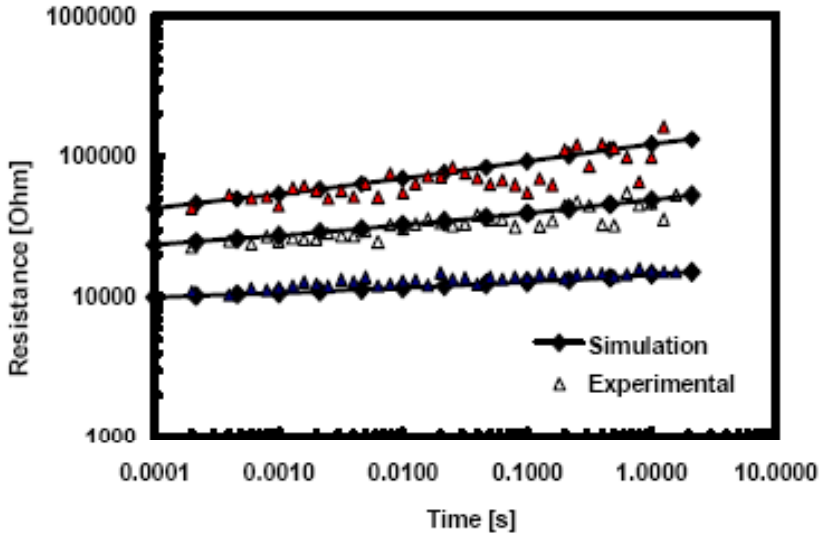
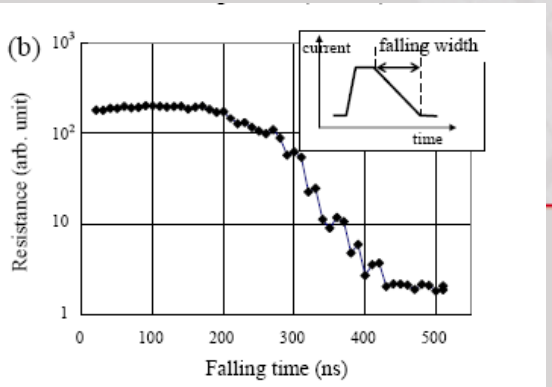


Figure 6: Measured resistance versus time for different starting amorphous levels. A good agreement between data and simulations has been achieved both for the initial value and for the low field resistance slope.

"Resistance drift" increase in R over time (dependent on R, low R crystalline GST – low drift, higher R increased drift).
Significant research effort on modeling and understanding

"Numerical Implementation of Low Field Resistance Drift for Phase Change Memory Simulations" ," Proc. NVSMW-ICMTD (2008). A. Redaelli, A. Pirovano, A. Locatelli and F. Pellizzer

MLC Opportunity / challenges in Phase Change Memory



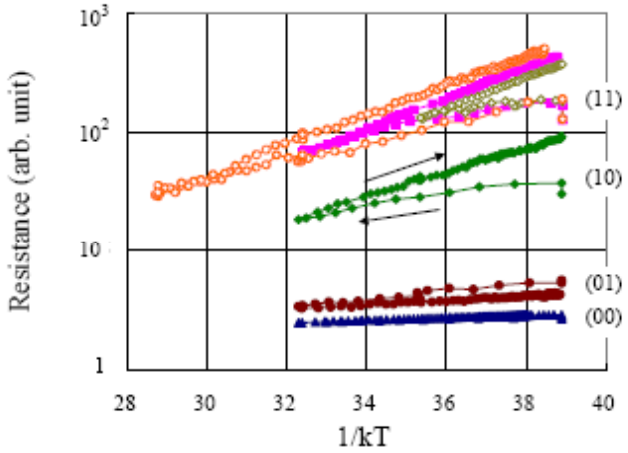


Figure 7. Resistance change of four levels level according to thermal history (i.e., the temperature is increased from room temperature to 55°C, 85°C, or 130°C and then is decreased to room temperature).

D.H. Kang, et al., "Two-bit Cell Operation in Diode-Switch Phase Change Memory Cells with 90 nm Technology," 2008 Symposium on VLSI Techn., 98 (2008).

Samsung MLC operation at the 90 nm using "moderate-quench" writing technique to place resistance

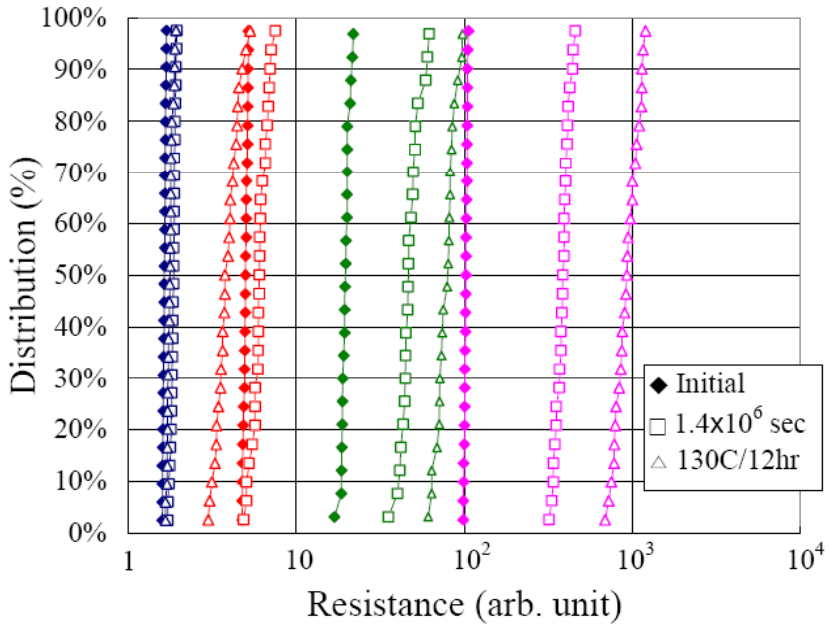


Figure 6. Resistance distributions four resistance levels of (00), (01), (10), and (11) after an elapse of 400 hr (1.4×10^6 sec) and an additional thermal annealing at 130°C for 12 hr bake.

Outline

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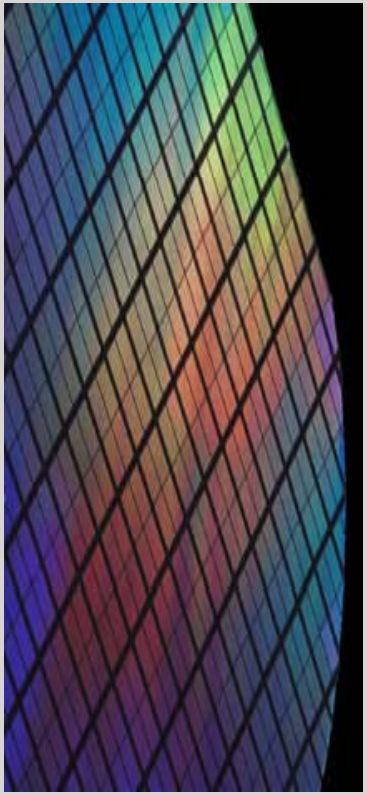
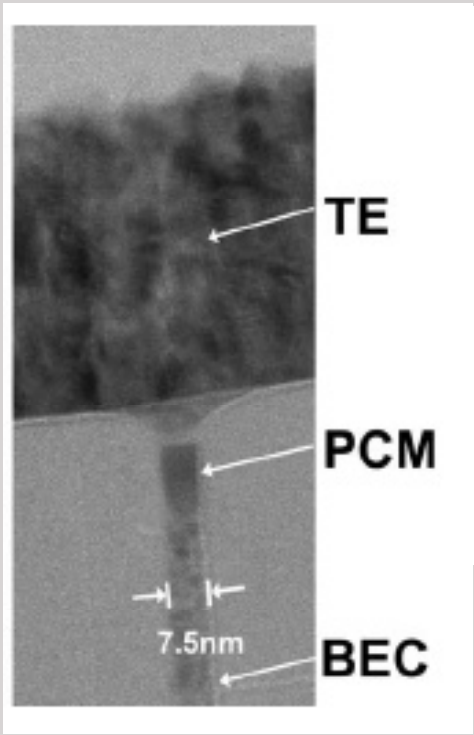


Reset Current Scales with Contact Area

- **Reset programming current continues to reduce with scaling !!!!**
  - **-> One of the key factors why so much activity in PCM!**
  - **-> Constantly ignored in many technology comparison…**

- Ireset of only 50 uA demonstrated



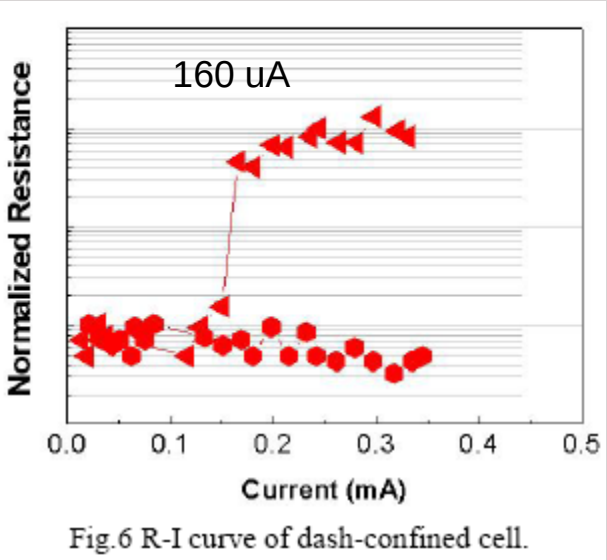
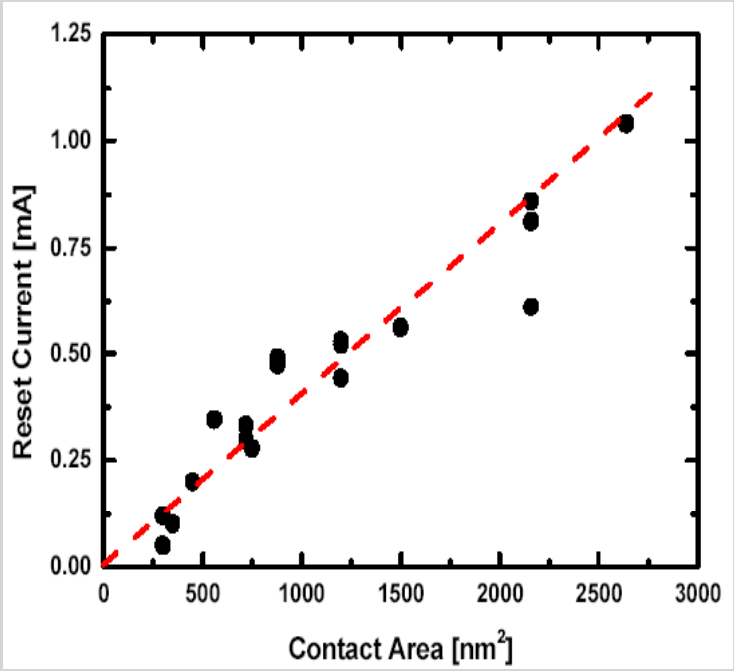


Fig.6 R-I curve of dash-confined cell.

"A Unified 7.5nm Dash-Type Confined Cell for High Performance PRAM Device" D.H. Im, Samsung IEDM 2008



"Scaling Analysis of Phase-Change Memory Technology.", A. Pirovano, A.L. Lacaita, A. Benvenuti, F. Pellizzer, S. Hudgens, and R. Bez, IEDM Technical Digest 2003.

Data Retention vs. Scaling

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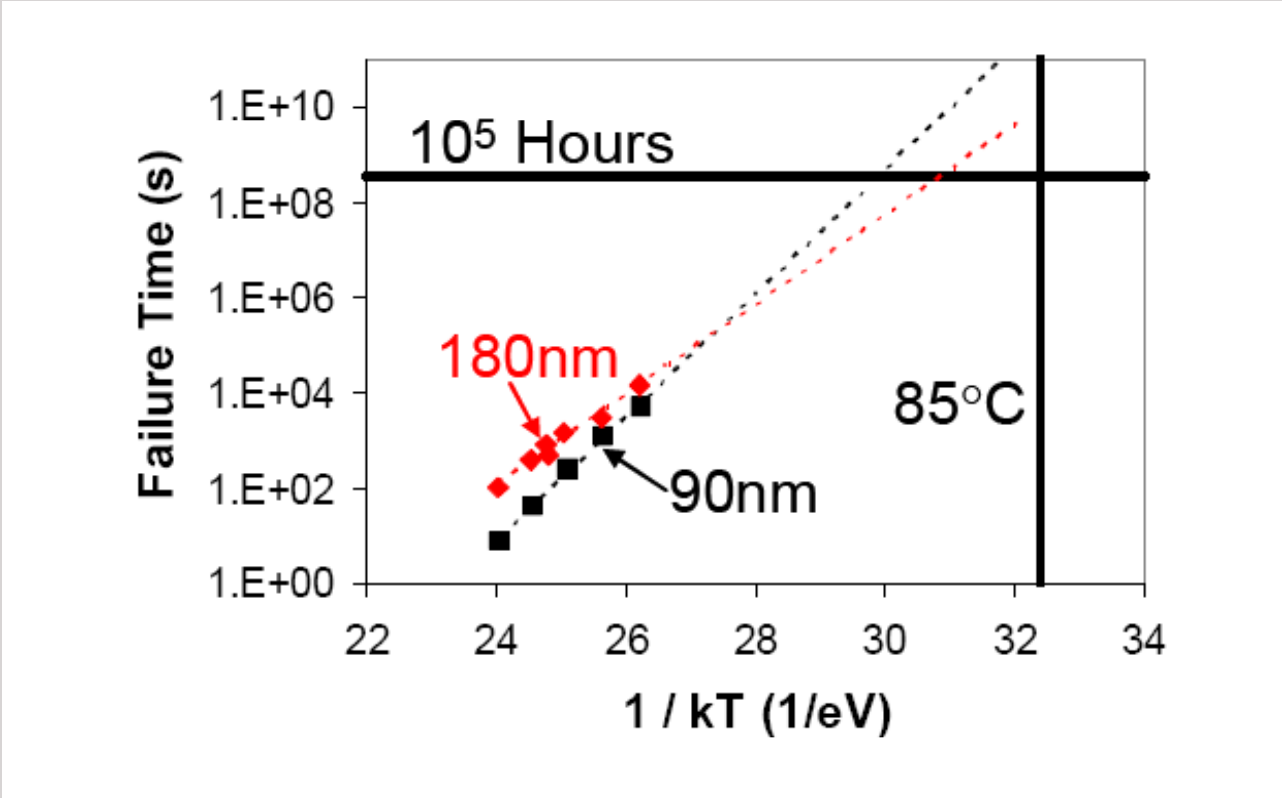
Data retention is not intrinsically degraded with process scaling. Failure rate < 1 PPB at 85C, 10^5 hours in large arrays.



B. Gleixner, et al.,Intel / Numonyx Proc. Intl. Rel. Phys. Symp. 542 (2007).

Thermal Disturb Scaling

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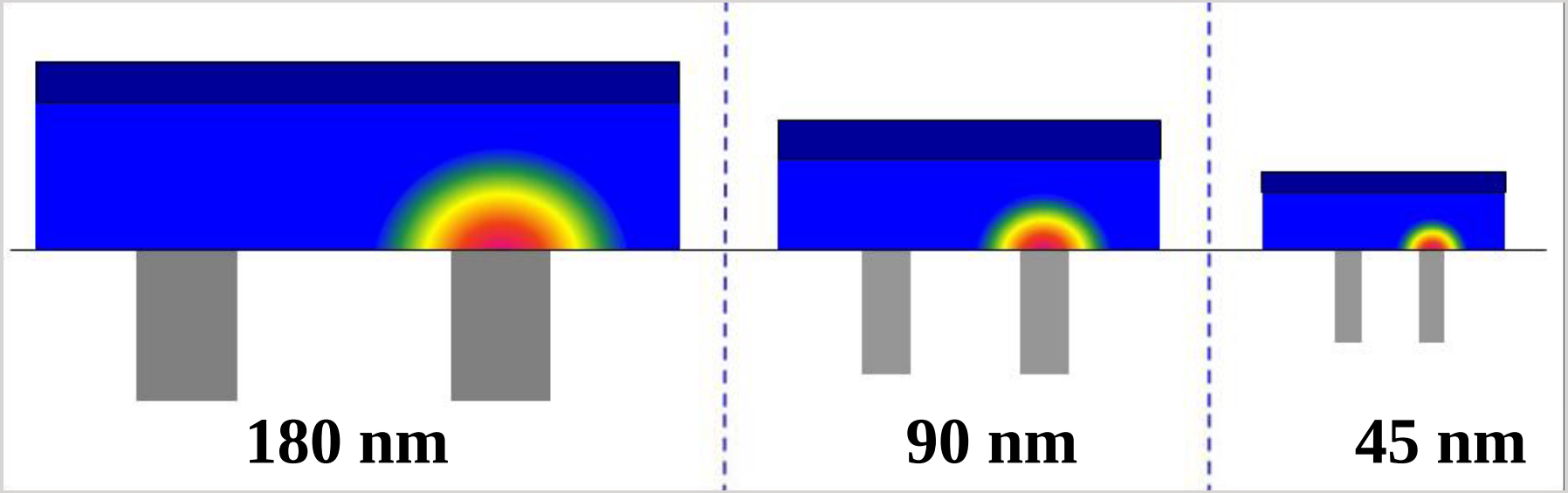
- Key aspect of scaling OUM cell is to scale contact area of heater to phase change material with technology node -> reducing volume of programmable material with each technology node.
- Contact area of heater to phase change material scales with technology node.
- Ireset/Iset reduces with scaling.
- Margin for thermal proximity disturb is **approximately** constant through scaling.



From **2002** Symposium on VLSI Technology rump session (presented by **C. Dennison**)

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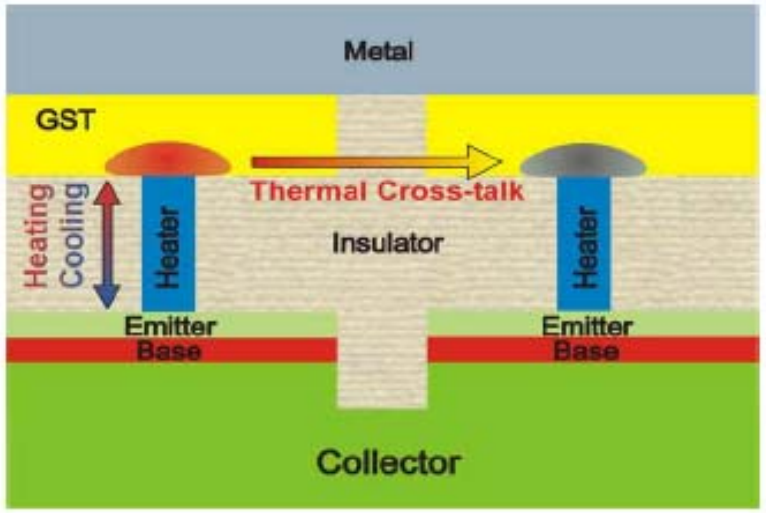
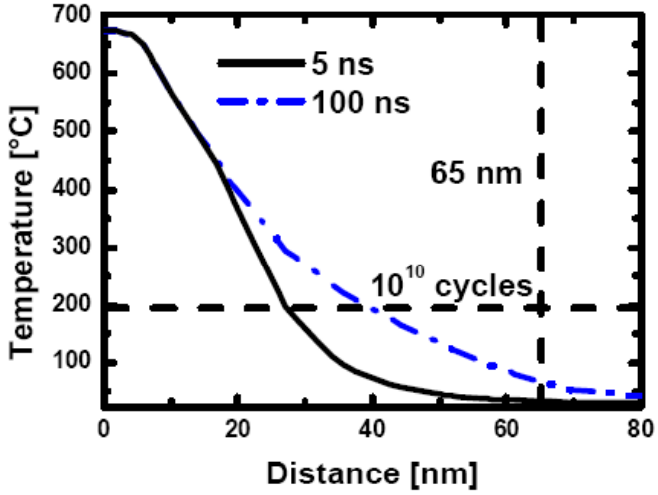
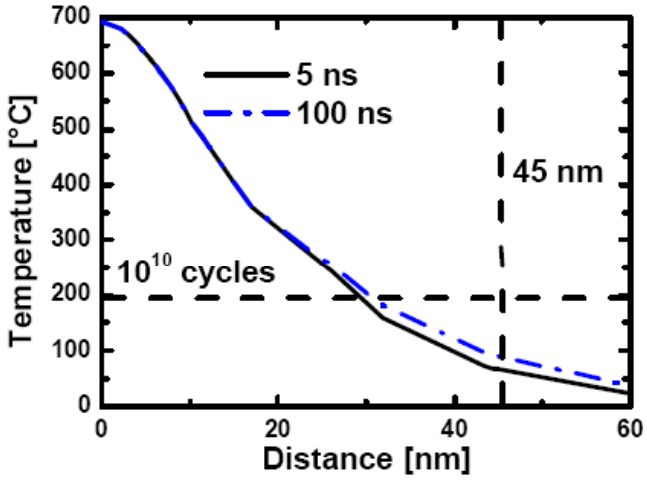
No Measured Thermal disturb at 90 nm node and various simulation data shows no thermal disturb to 65 or 45 nm technology node



Simulated Cross-talk for 65/45 nm Cells





PCM scaling is not limited by intrinsic disturb

A. Pirovano *et al.*, IEDM Tech. Dig. 2003

A. Pirovano, "Reliability Study of Phase-Change Non-Volatile Memories", (IEEE Transactions on Device and Materials Reliability Vol4 No3 September 2004

Thermal Disturb Scaling

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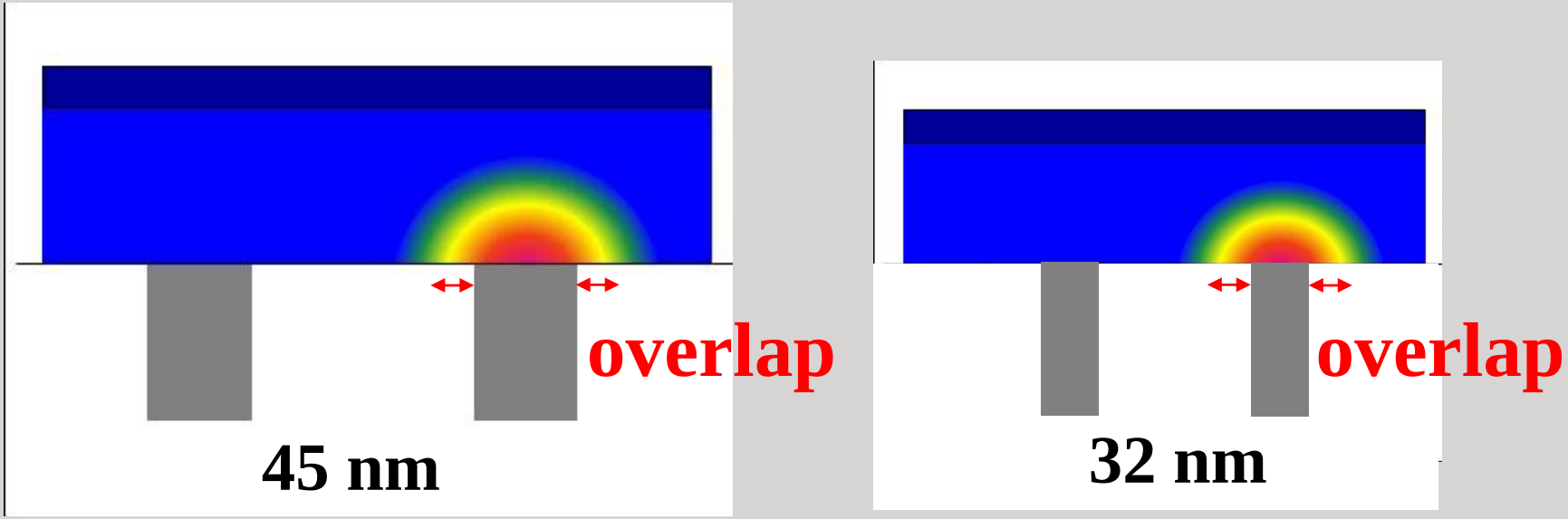
- In a planar PCM cell, eventually thermal proximity disturb will become an issue because a minimum (fixed) melt / amorphous region is required to ***overlap*** past the bottom electrode to insure both adequate high resistance and Vth

- Many simulations show good thermal isolation at 45-65 nm, so it is believed that at ~ 32 nm an alternative cell will be required



Solution: Move to a confined cell structure, dependent on the scaling (isotropic / aggressive)

Thermal Disturb Scaling

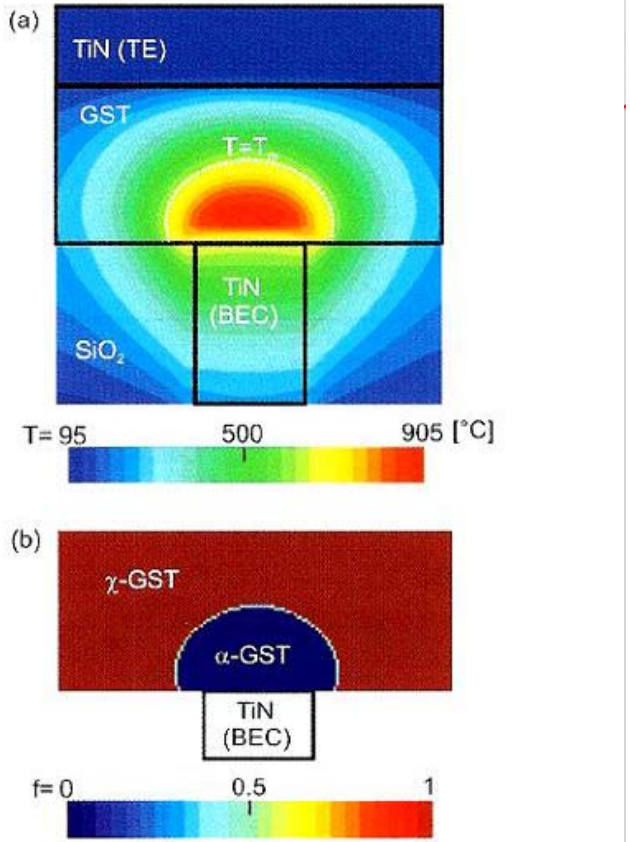


Fig. 5. (a) Temperature distribution $T(x = 0, y, z)$ at the end of the pulse ($t = 20$ ns) and (b) phase distribution $f(x = 0, y, z)$ after RESET operation ($t = 40$ ns) for the vertical PCRAM cell.

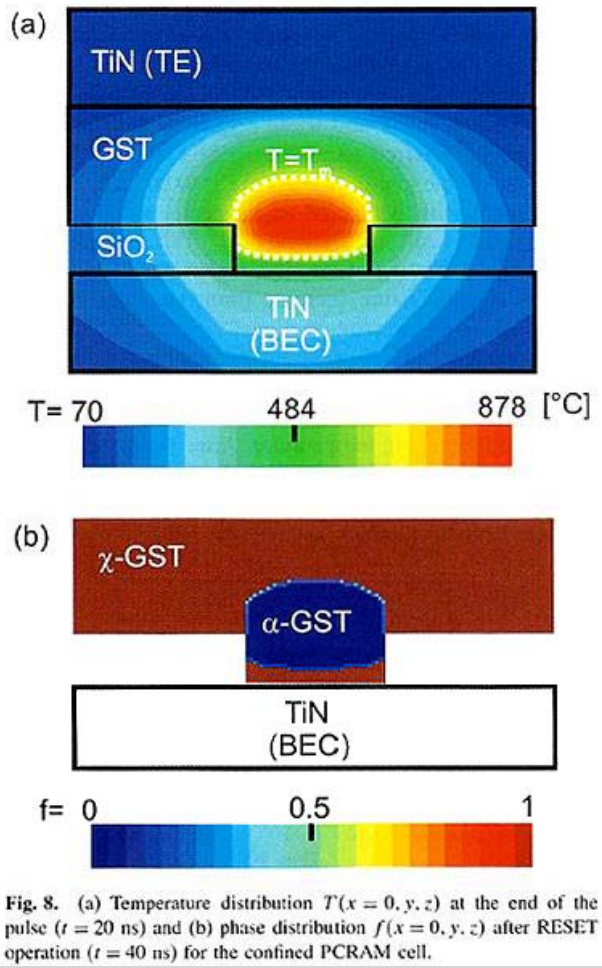


Fig. 8. (a) Temperature distribution $T(x = 0, y, z)$ at the end of the pulse ($t = 20$ ns) and (b) phase distribution $f(x = 0, y, z)$ after RESET operation ($t = 40$ ns) for the confined PCRAM cell.

In confined cell there is no overlap of programmed amorphous region past the area of the bottom electrode

–> thus thermal disturb scales

D.H. Kim, et. al., "Simulation-Based Comparison of Cell Design Concepts for Phase-Change Random Access Memory," J. Nanoscience and Nanotechnology, v. 7, 298 (2007).

Material Scaling Limit

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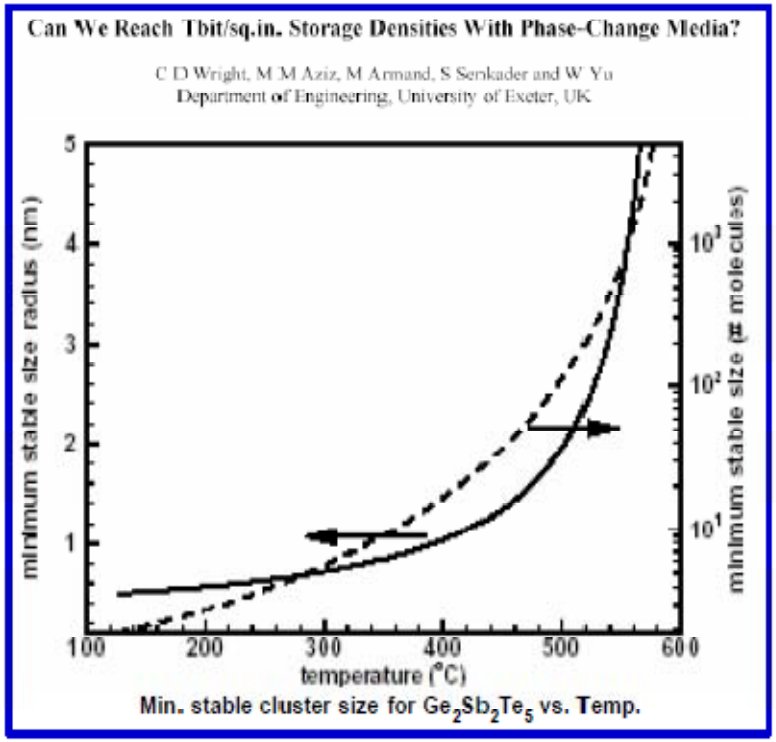
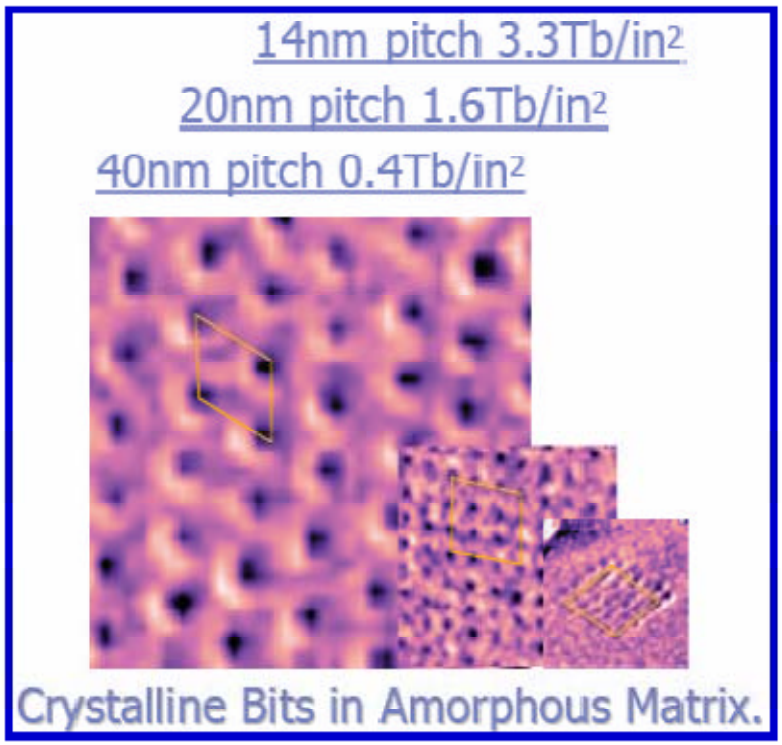
Phase Change Mechanism Appears Scalable to at Least ~5nm

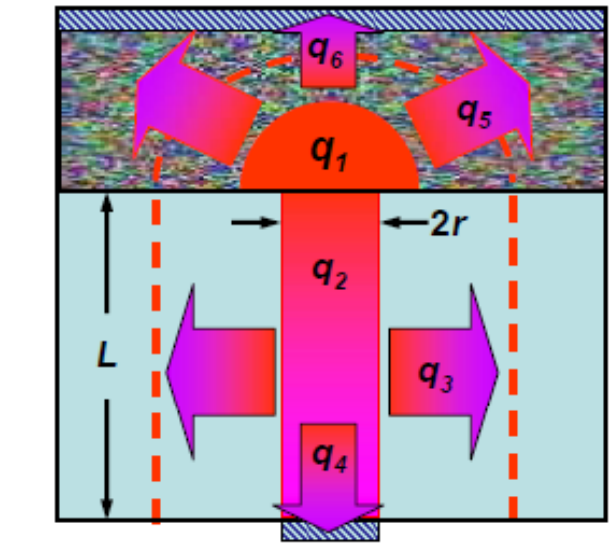


Source: C.D Wright et al., EPCOS 2004

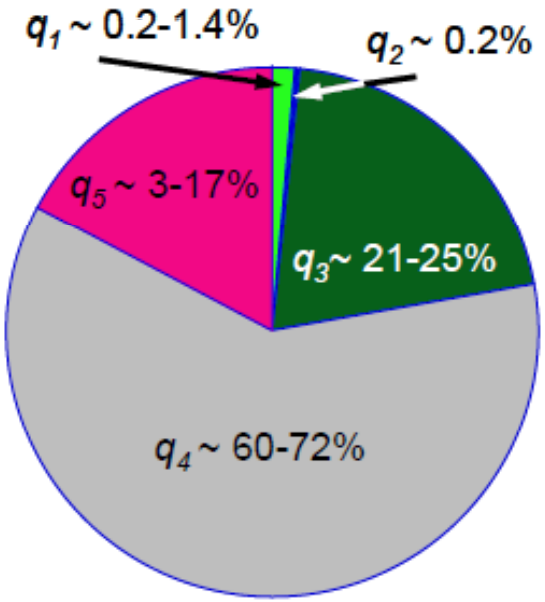


Source: C. Lam, SRC NVM Forum 2004

Review of Planar PCM cell



(a)



- In planar cell the Contact heat loss is the dominant thermal inefficiency in all cell geometries other than line cell and confined cell. 60-72% heat loss through bottom electrode (q_4)
- In Planer cell 'fire ball' / highest temperature region is adjacent to bottom electrode

S.M. Sadeghipour, L. Pileggi, and M. Ashegi, "Phase Change Random Access Memory Thermal Analysis," Proc. ITHERM06 (2006) 660

Structural Scaling: Confined Cell

OVONYX

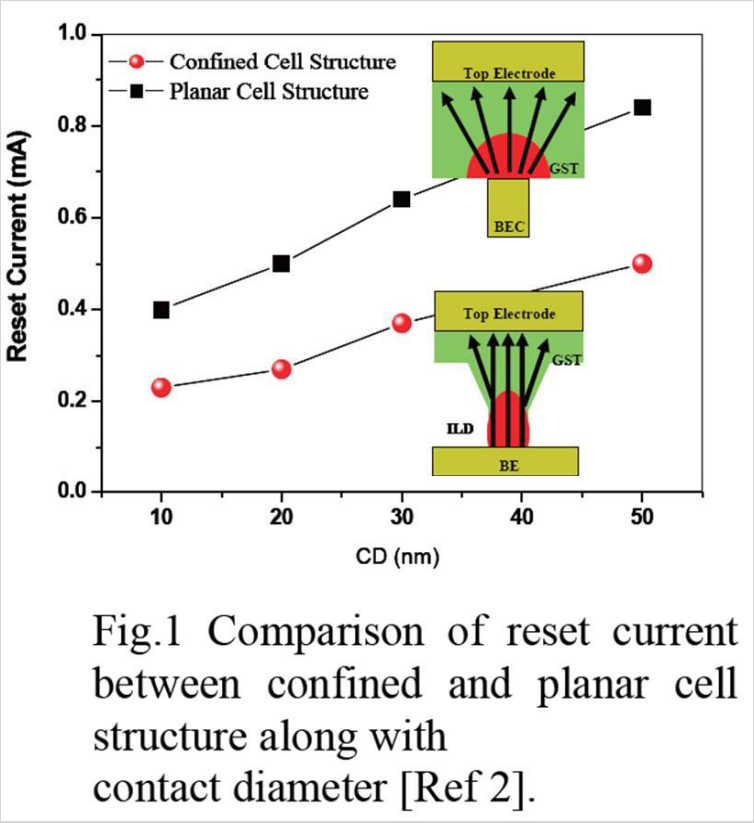


Fig.1 Comparison of reset current between confined and planar cell structure along with contact diameter [Ref 2].

J. Lee et al., "Highly Scalable Phase Change Memory with CVD GeSbTe for Sub 50 nm Generation", 2007 Symp on VLSI Tech, pp 102.

- Confining the GST into the pore, the reset current is reduced by ~50%
- It also reduces the horizontal spread of the heated region, further facilitating scaling
- Integrated with a diode, the cell structure is highly scalable
- "Fireball moved away from bottom electrode => Improved cycle endurance
- Reduced lithography and process steps: Cost Reduction

Structural Scaling: Confined Cell

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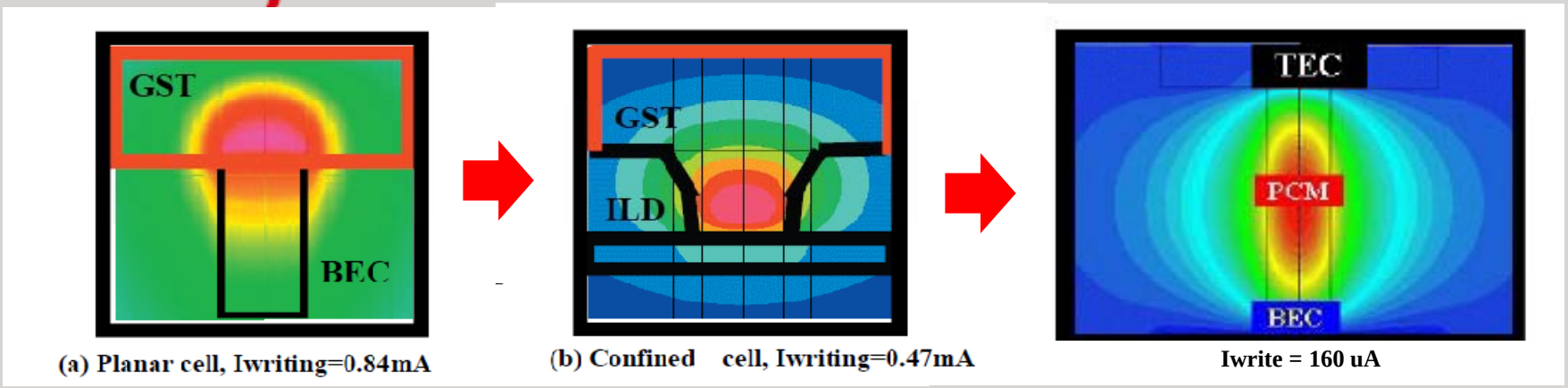


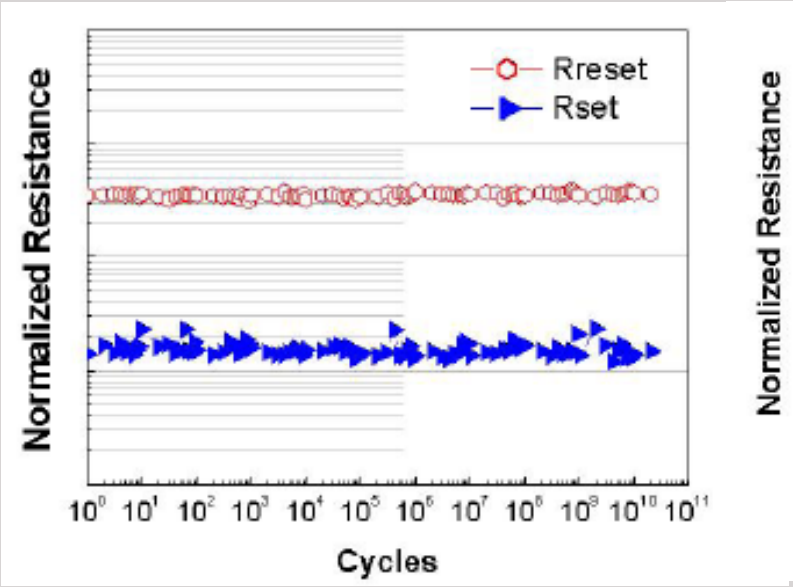
(a) Planar cell, Iwriting=0.84mA

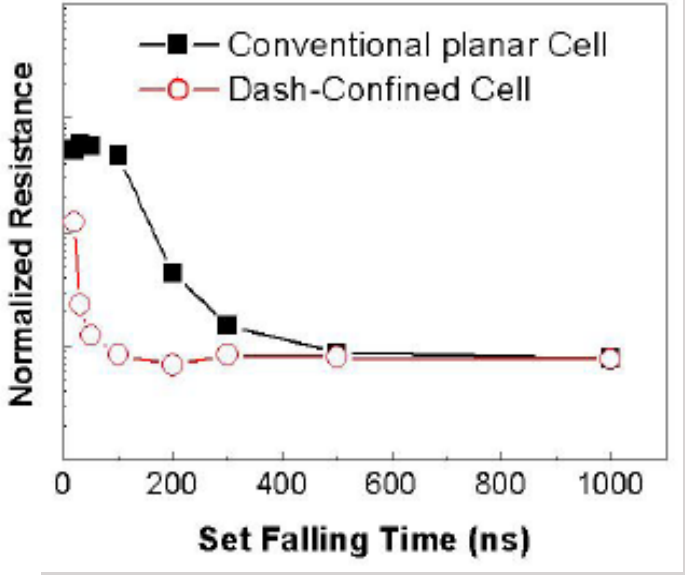
(b) Confined cell, Iwriting=0.47mA

Iwrite = 160 uA

S.L. Cho, et. al. , Samsung Electronics Co.,2005 Symposium on VLSI Technology Digest of Technical

D.H. Im, Samsung Electronics , IEDM 2008

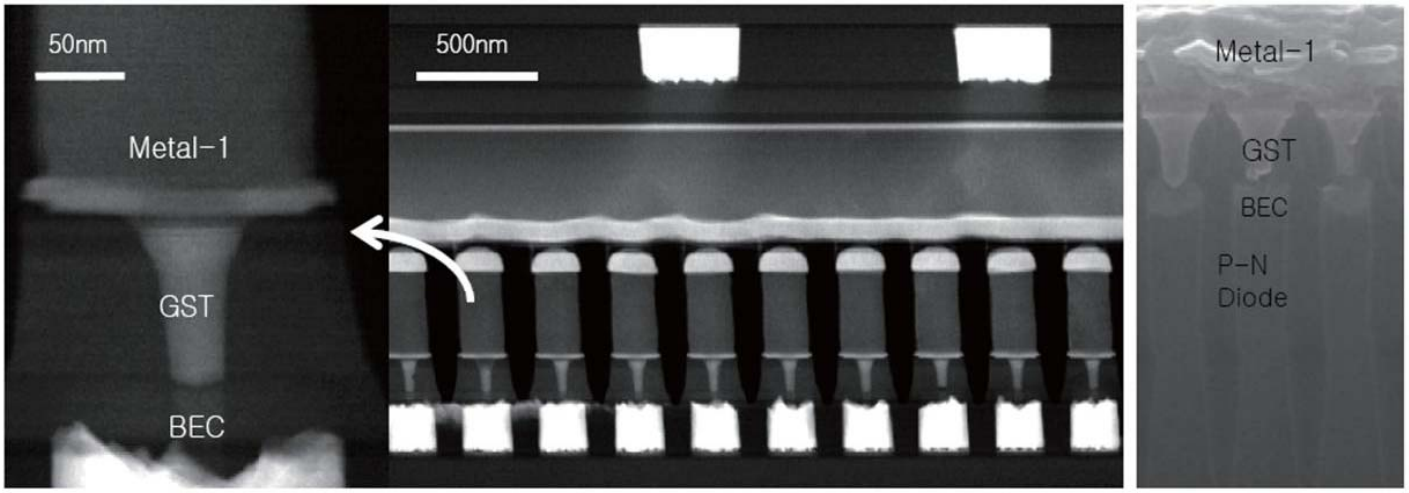




"the programming time of dash confined cell much improved to **50ns** due to smaller amorphous volume as shown in Fig. 8"

TEMs of Confined Cell

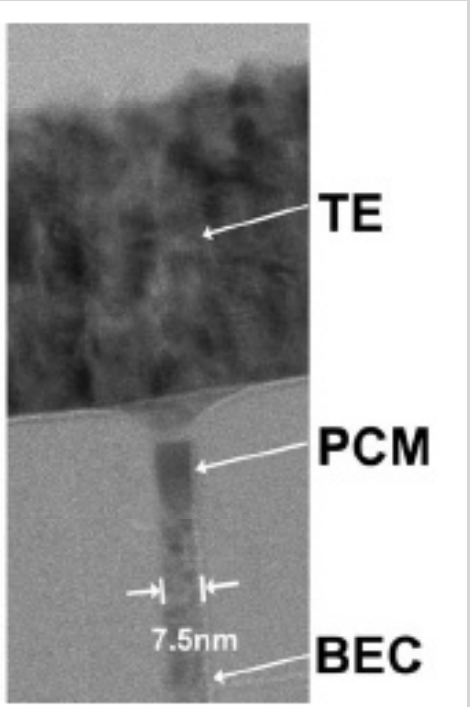
OVONYX



(a) (b)

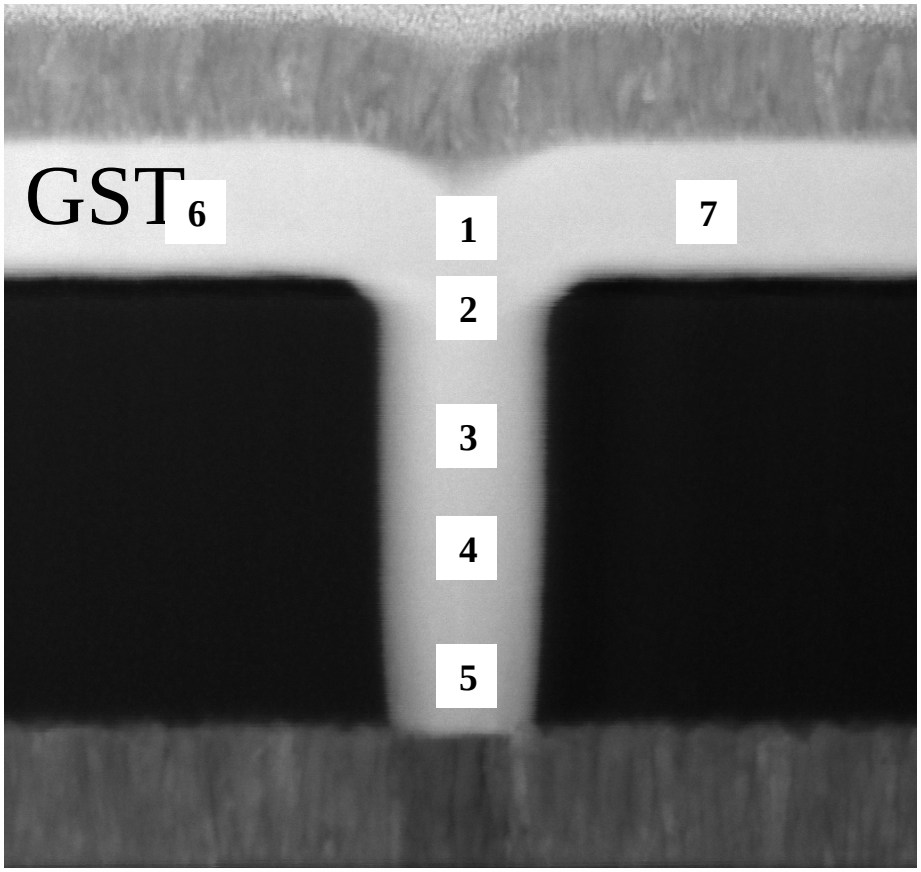
Fig.11 (a) Magnified TEM images of GST on 50nm contact device, (b) SEM image of fully integrated confined cell structure on diode.

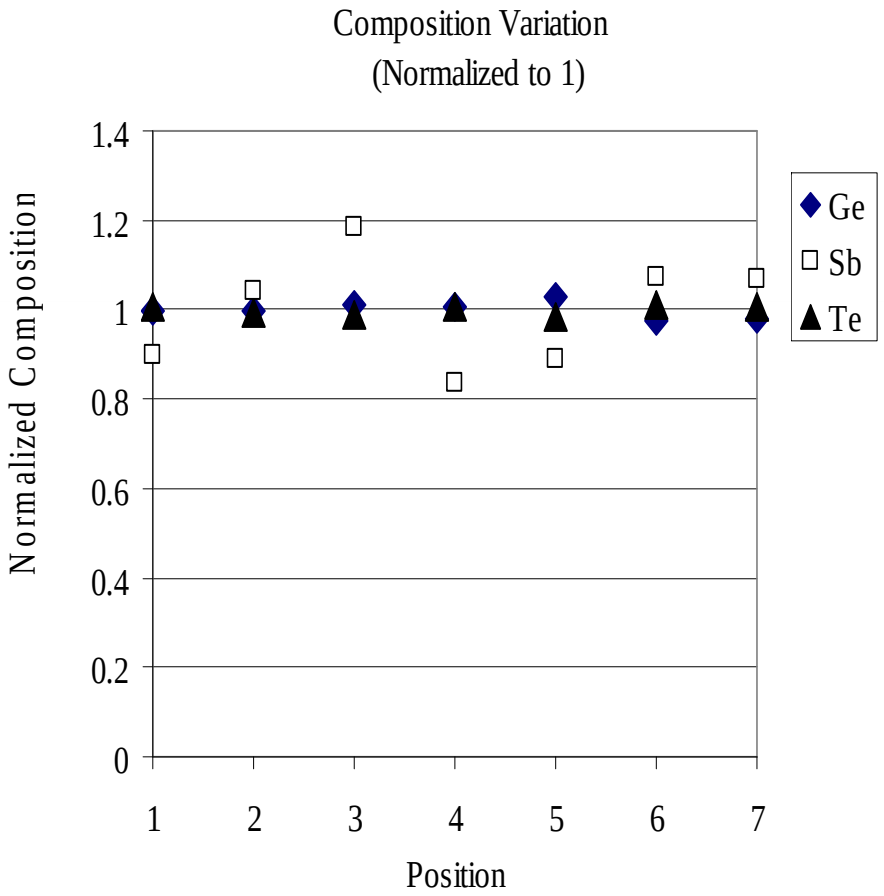
D.H. Kang,, **"Two-bit Cell Operation in Diode-Switch Phase Change Memory Cells with 90nm Technology"** 2008 Symposium on VLSI Techn., 98 (2008).



A Unified 7.5nm Dash-Type Confined Cell for High Performance PRAM Device
D.H. Im, Samsung Electronics IEDM 2008

GST fill of High Aspect Ratio Hole Structure and Composition Uniformity





Conformal MOCVD Deposition of GeSbTe in High Aspect Ratio Via Structure for Phase Change Memory Applications
Journal: 2009 MRS Spring Meeting

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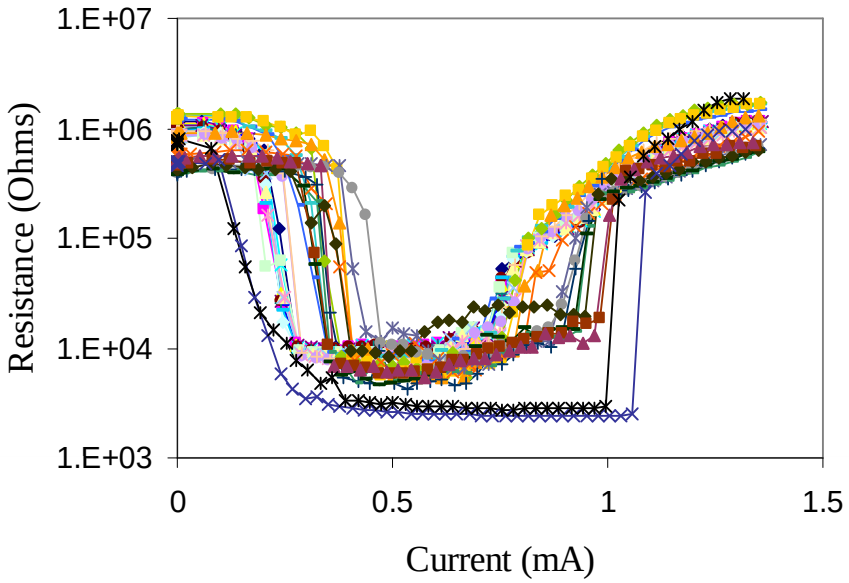
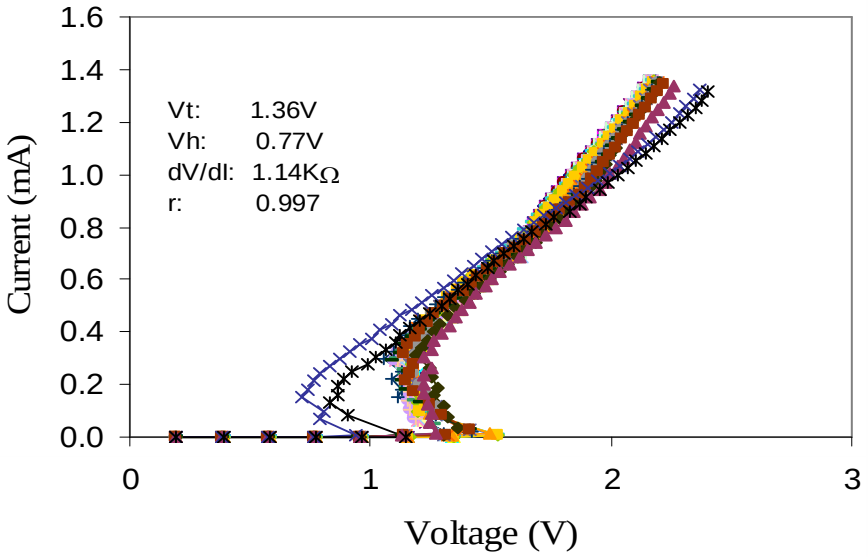
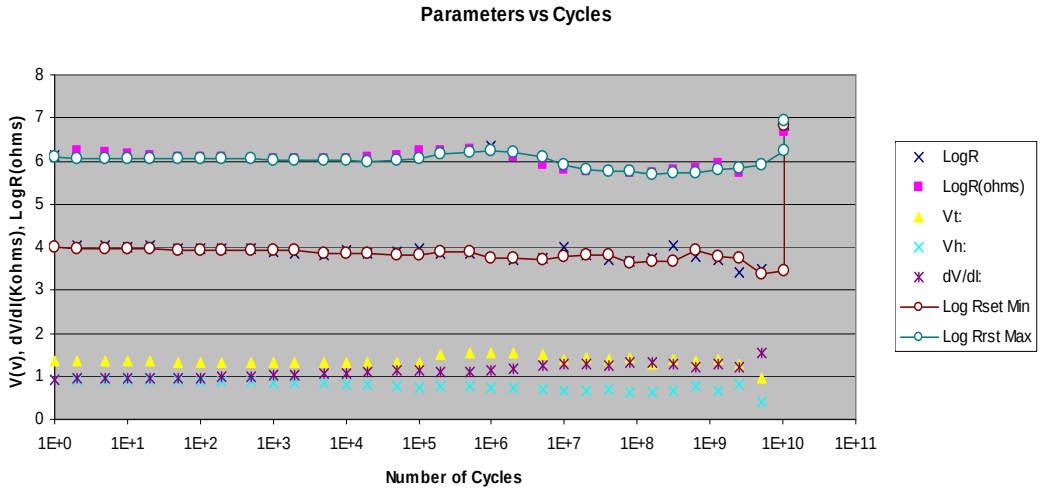
Best MOCVD Based Device with $1x10^{10}$ Cycles







- **I reset ~ 1mA, cycled between set and reset at 1MHz**
- **Failed open circuit after 10^{10} cycles**

Conformal MOCVD Deposition of GeSbTe in High Aspect Ratio Via Structure for Phase Change Memory Applications
Journal: 2009 MRS Spring Meeting

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Advantages of Confined Phase Change Cell

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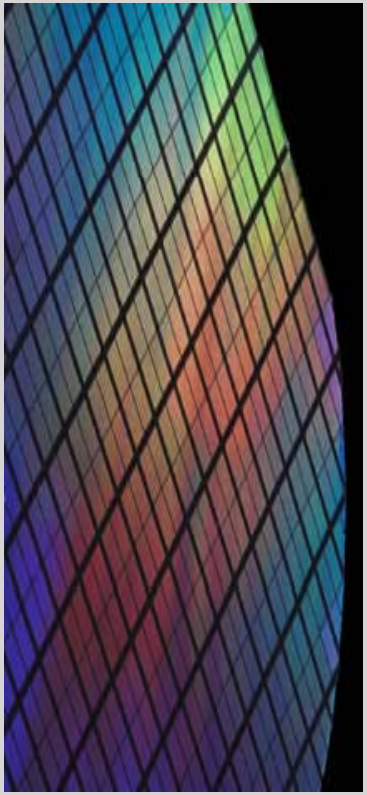
1. Compared to plug cell significantly reduced programming current for given lithography node
   - **Smaller cell size for embedded MOS select device**
2. Improved scaling:
   - Reduced Thermal disturb (greater spacing between melt regions)
   - Eliminates needed lateral overlap of ‘plug’ bottom electrode – leads to smaller cell size
3. Potential improved cycle endurance due to melt programming volume displaced from electrode – minimizing electro/thermal chemistry and migration with electrode. Also more uniform and reduced peak current density in both electrode and phase change layer
4. Reduced lithography and process steps –> enables process flow with only 1-2 added litho step (compare to 3 litho steps for plug flow and 3-4 for uTrench)
5. No need to etch phase change material (no etch sidewall contamination)

Outline

- Phase Change Memory (PCM) Overview
- PCM Scaling
- Comparative Memory Technology Roadmap
- Product Roadmap
- Summary



Flash eventually runs out of electrons leading to degraded performance at lower cost MLC scaled solutions

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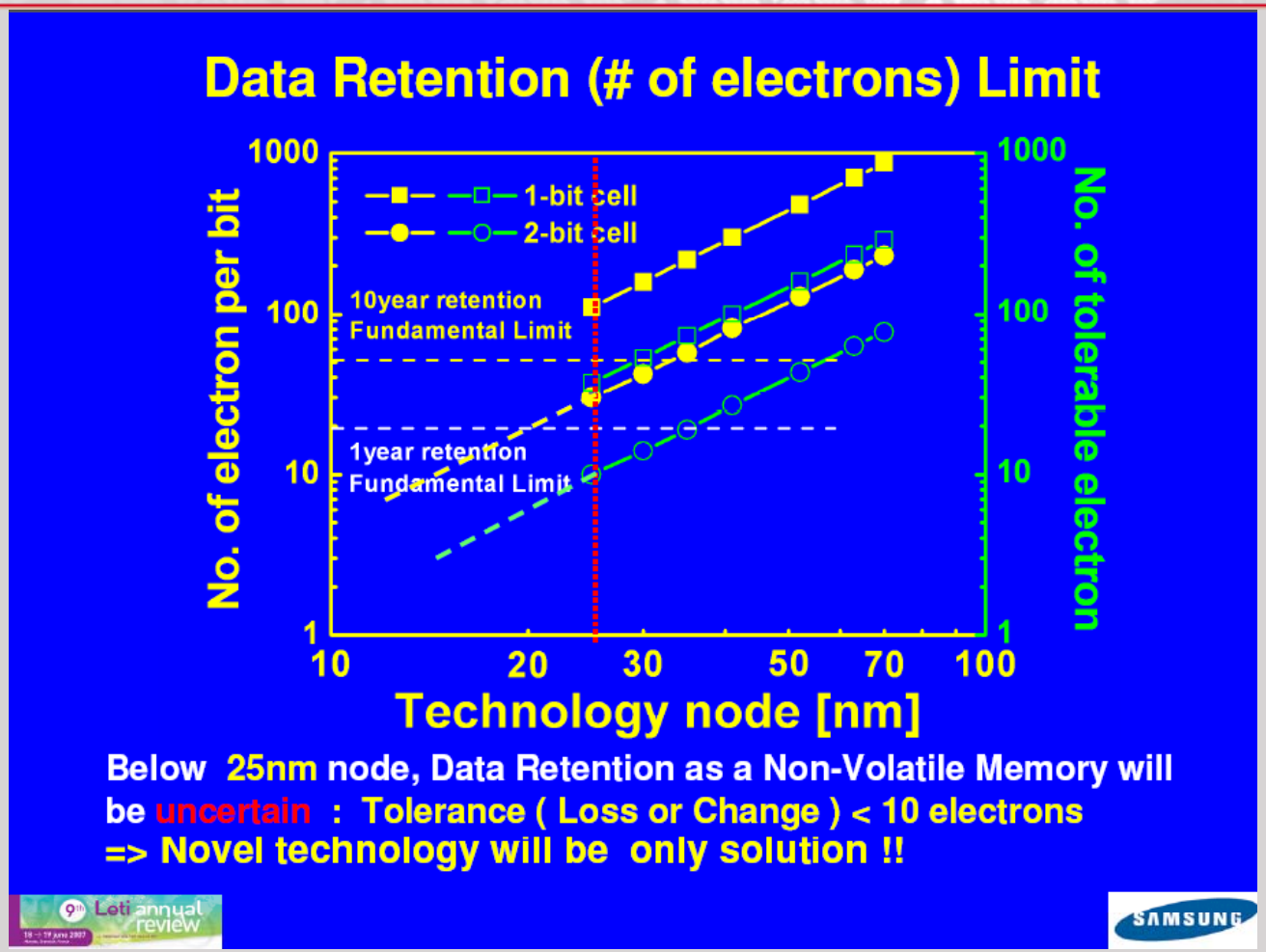
As NAND flash scales it will indeed continues to lower the cost per bit, but at a price of reduced reliability (data retention, cycle endurance) and large page sizes reducing the random R/W performance.

This reverse scaling of speed and reliability increases the need for a high a performance *supplemental* memory to bridge the gap and between the lowest cost MLC NAND and system requirements.

Lower the cost for NAND -> greater the need for PCM as NV 'buffer' memory



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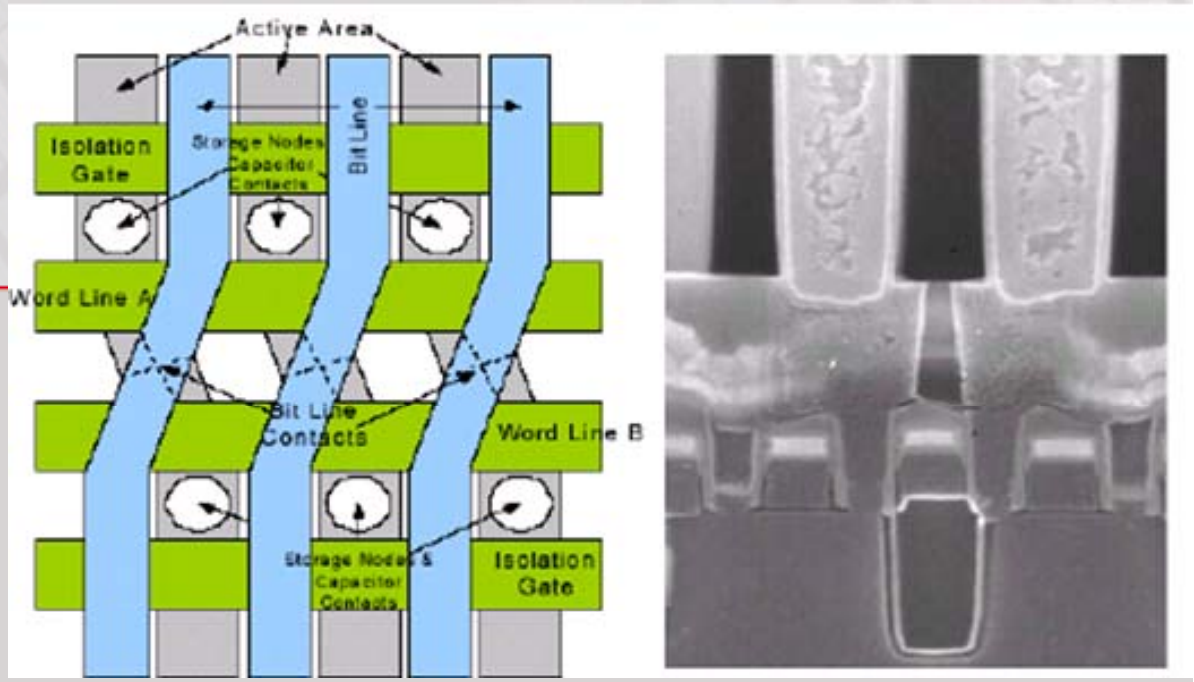
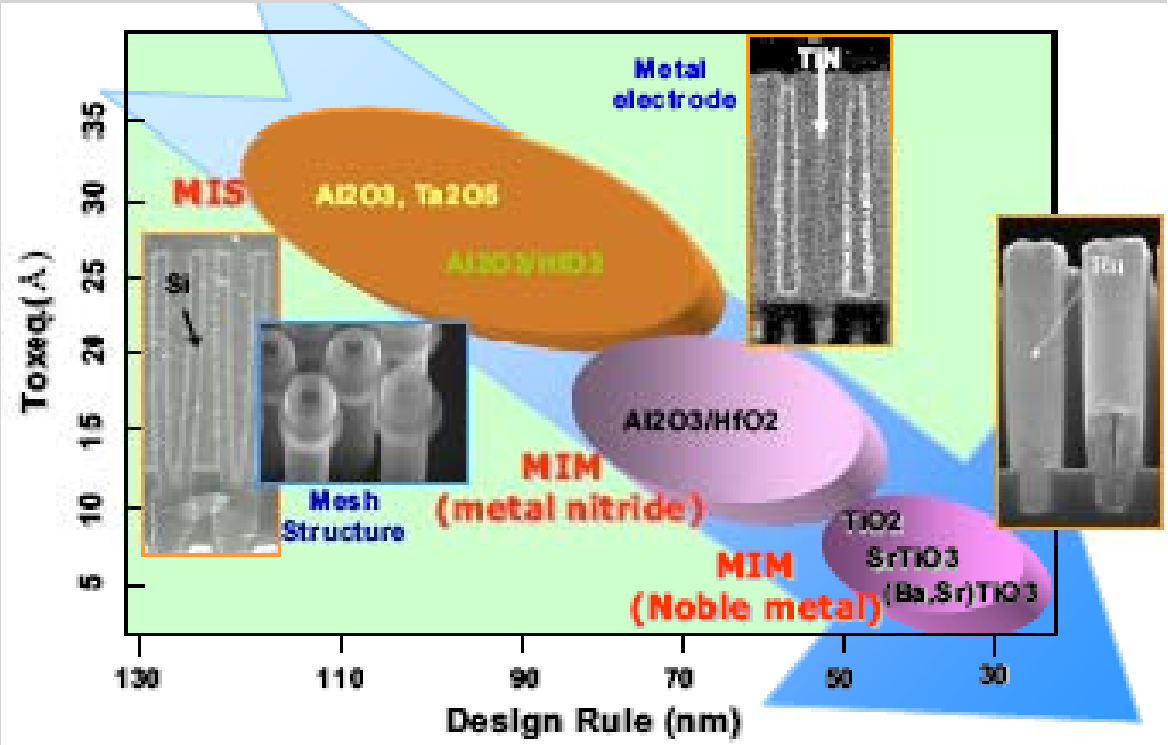
DRAM Scaling:
Non litho friendly

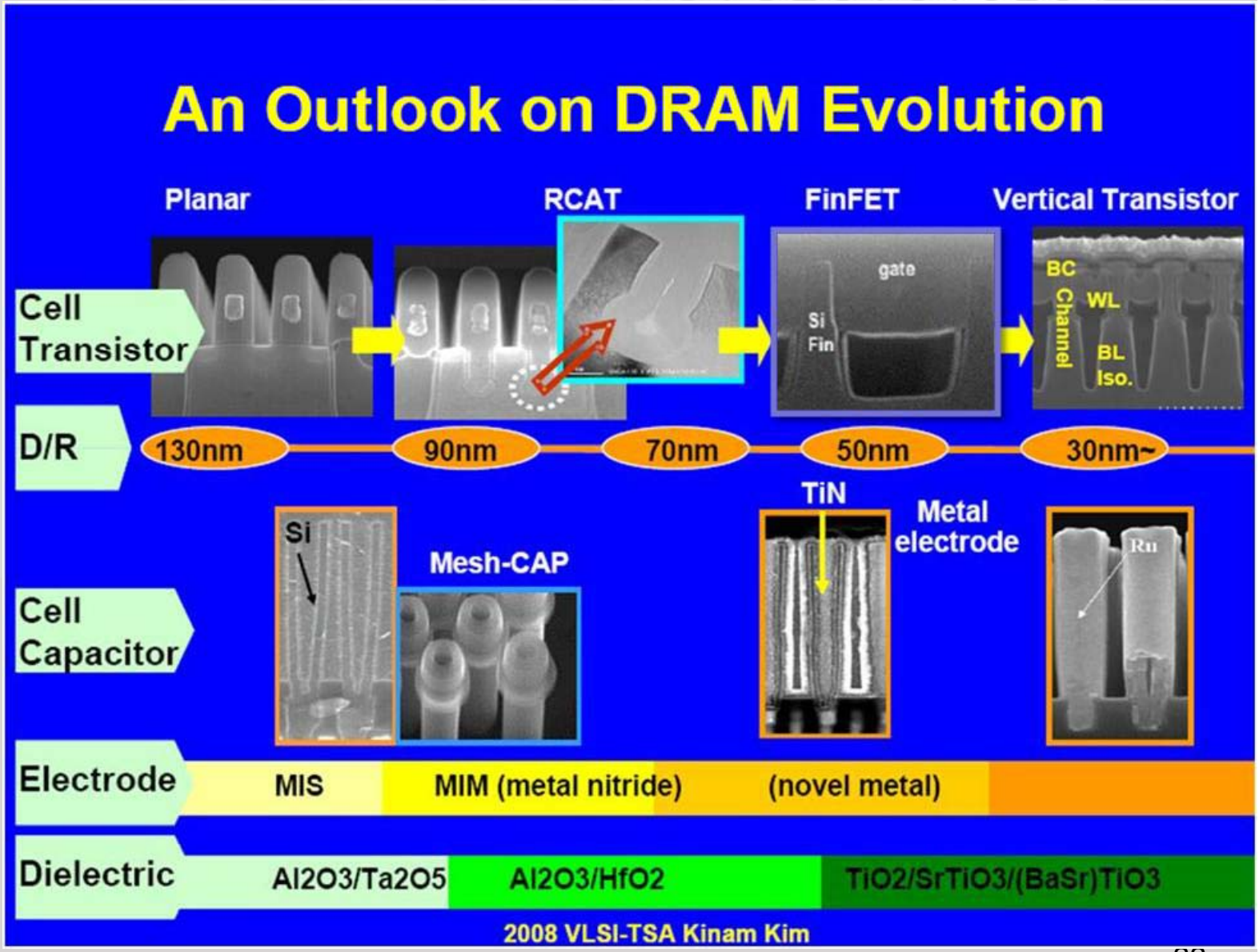


DRAM Scaling:
Stacked DRAM storage capacitor needs new materials deposited to in increasing high aspect ratio requiring ALD for both electrodes and new dielectrics



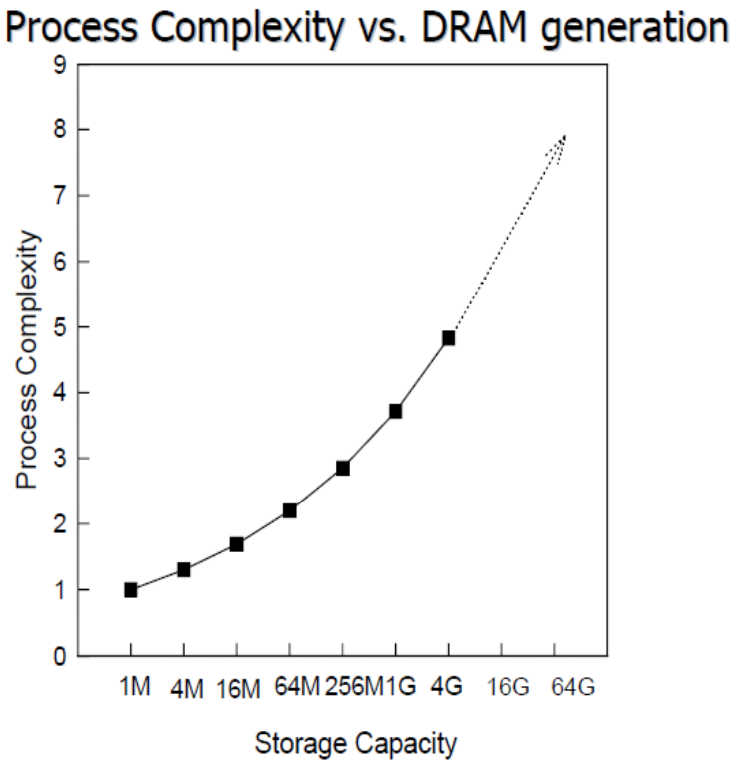
DRAM: New structures, new materials, more steps: Process Complexity = $$

DRAM has no MLC capability and is already lagging behind NAND by at least a full litho node



Process Complexity = $$

OVONYX



Kinam Kim

DRAM Technology

: Fundamentals, Challenges in DRAM, Future technology direction

As the Process Complexity continues to increase the historical cost reduction rate of 32% is becoming more and more difficult to achieve.

DRAM does not have MLC capability and is already lagging behind NAND Flash by at least a full litho node

2007 ITRS Roadmap DRAM vs. PCRAM

Table PIDS4a DRAM Technology Requirements—Near-term Years

Year in Production	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*	*2014*	*2015*
DRAM ½ Pitch (nm) [1]	*68*	*58*	*50*	*45*	*40*	*36*	*32*	*30*	*25*
DRAM cell size (μm^2) [2]	0.0277	0.0202	0.0150	0.0122	0.0096	0.0078	0.0061	0.0054	0.0038
DRAM storage node cell capacitor dielectric: equivalent oxide thickness EOT (nm) [3]	1.2	0.90	0.80	0.60	0.50	0.40	0.30	0.30	0.30
DRAM storage node cell capacitor voltage (V) [4]	0.65	0.65	0.60	0.60	0.55	0.55	0.5	0.50	0.45
Equivalent Electric field of capacitor dielectric, (MV/cm) [5]	5.7	7.2	7.5	10.0	11.0	13.8	16.7	16.7	15.0
DRAM cell FET structure [6]	RCAT	RCAT	RCAT	FinFET	FinFET	FinFET	FinFET	FinFET	FinFET
Cell Size Factor: a [11]	6	6	6	6	6	6	6	6	6
C. PCRAM (Phase-Change RAM)									
PCRAM technology F (nm) [58]	72	58	46	40	35	32	28	25	22
PCRAM cell size area factor a in multiples of F^2 (BJT access device) [59]	4.8	4.0	4.0	4.0	4.0	4.0	4.0	4.0	4.0
PCRAM cell size area factor a in multiples of F^2 (nMOSFET access device) [60]	15.0	14.0	12.0	11.0	10.0	8.9	8.8	8.4	7.4
PCRAM typical cell size (nm^2) (BJT access device) [61]	24883	13456	8464	6400	4900	4096	3136	2500	1936
PCRAM typical cell size (nm^2) (nMOSFET access device) [62]	77760	47096	25392	17600	12250	9114	6899	5250	3582
PCRAM number of bits per cell (MLC) [63]	1	1	2	2	2	4	4	4	4
PCRAM typical cell area per bit size (μm^2) (BJT access device) [64]	24883	13456	4232	3200	2450	1024	784	625	484
PCRAM typical cell area per bit size (μm^2) (nMOSFET access device) [65]	77760	47096	12696	8800	6125	2278	1725	1313	895
PCRAM storage element CD (nm) [66]	45	36	30	25	22	20	18	16	14
PCRAM phase change volume (nm^3) [67]	373,000	195,000	112,000	64,000	43,000	33,000	25,000	18,000	12,000

As time goes on the cost benefit of PCRAM over DRAM is <u>increasing</u>:

2010 cell size comparison

DRAM: 12,200 nm^2

PCRAM: MLC: 3,200 nm^2
SLC: 6,400 nm^2

¼ - ½ DRAM Cell Size

PCRAM will have significantly lower cost (smaller cell / less complex process) compared to DRAM, but can it meet required performance to displace a significant percentage of DRAM?

What is required cycle endurance for PCRAM to replace DRAM in typical applications?

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PCRAM cycle endurance status and potential will be reviewed later, but to first order PCRAM has cycle endurance limitation compared to unlimited (>10^{15}) DRAM cycle life

Wear Leveling extends the lifetime by ensuring that even if an application writes to the same virtual blocks over and over again, the program cycles will be distributed evenly over the entire memory. Required speed and cost overhead must be accounted for as done on all Flash applications.

Required Endurance (E) = TL * BW / (WLeff * Msize)

where *E* is endurance, *TL* is life expectancy of the system, *BW* is memory BandWidth, *WLeff* is wear-leveling efficiency and *Msize* is the system memory size.

Assuming a typical server with a **ten year life (24 hour, 7 day operation)**, **1GB/sec. BandWidth**, **0.1 wear-leveling** efficiency and **16GB Memory size**, the endurance requirement is only **2×10^8**

In other 'mostly read' DRAM applications including 'search engine servers' and mobile applications less demanding cycle endurance offers opportunity for early adaption. The **lower cost** along with **lower power consumption** will drive creative solutions.

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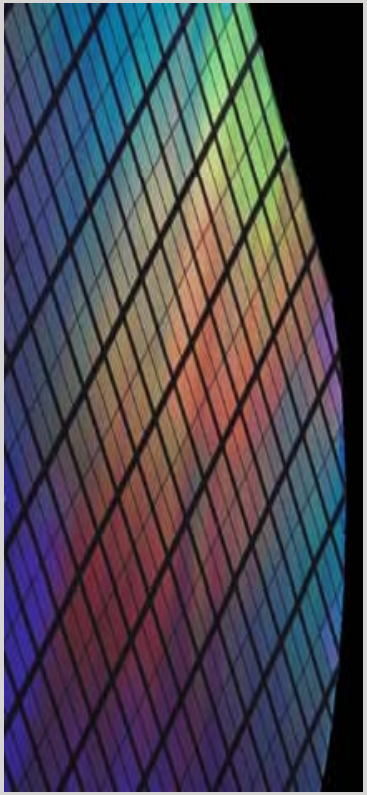

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How do you make a small fortune in the semiconductor memory business?”

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How do you make a small fortune in the semiconductor memory business?”

Answer:

Start with a large fortune!

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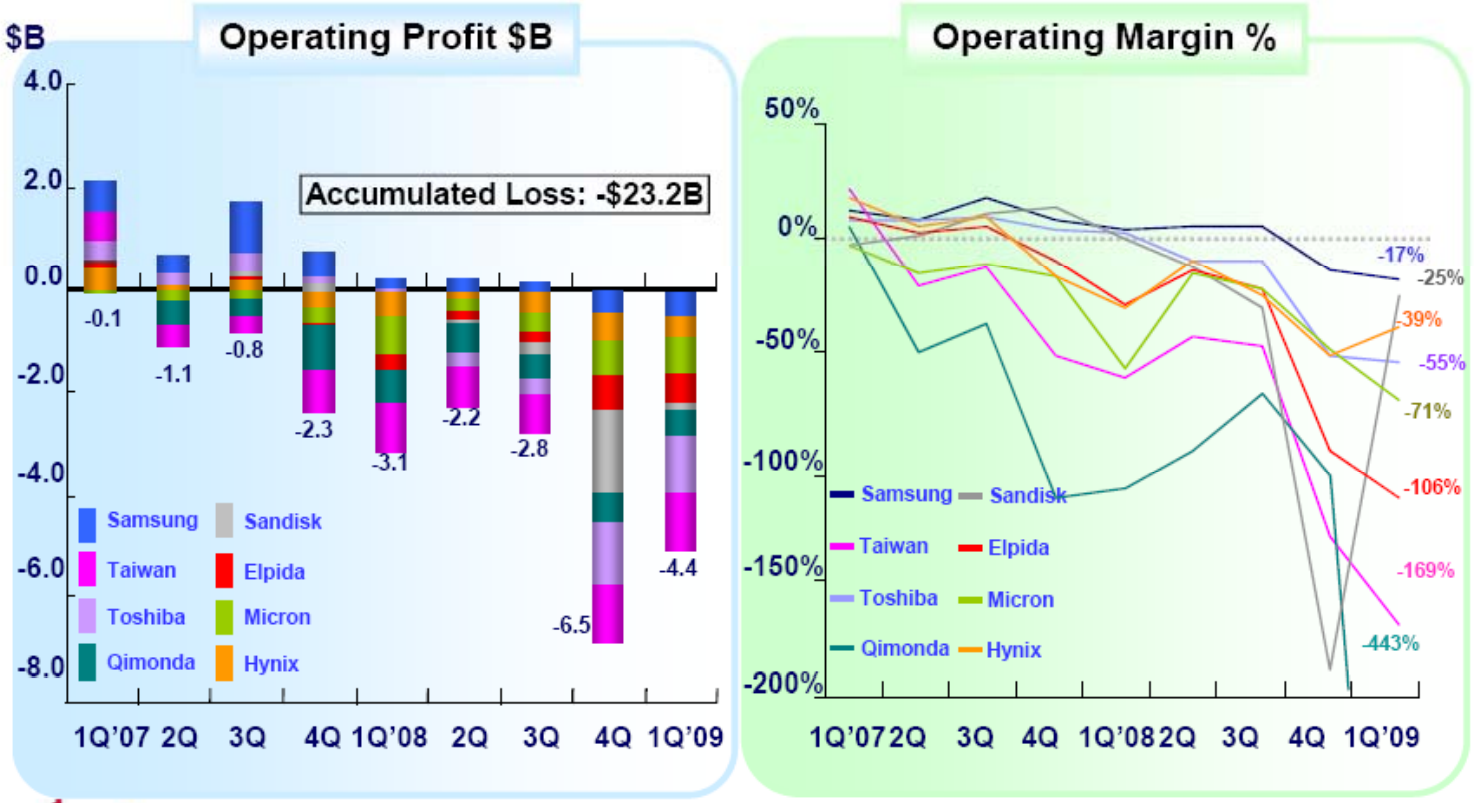
Brutal business environment in semiconductor memory segment: chapter 11 / consolidation, reduced R&D

Memory Vendor Profit History

- $23B Aggregate Losses Since Q2 '07 → **Not Sustainable**



denali MEMCON09

(Source : Company Reports, PSC & Qimonda: BNP Paribas Apr.2009) • OP Figures including Toshiba non-memory & excluding Samsung

SAMSUNG

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New Memory Technology is Rare

SRAM, DRAM, EProm All ~ 30yr Old

- Evolutionary Changes for NVM
  - EProm -> E^2Prom ->Flash
- Even Less Innovation for Volatile Ram
  - Storage Margin Treadmill is Hard to Maintain
  - Going Backward for SRAM 6T →4T → 6T

Year of 1st Shipment	Memory Technology
1969	SRAM
1970	DRAM
1971	EPROM
1989	ETox Flash
1995	NAND Flash
1997	MLC ETox

Memory Scaling is Increasingly Challenged

- Critically Dependent on Fine Line/Space Pattering
- Storage/Stability Hindering Dielectric/Voltage Scaling

"Explosion" of "New" Memory Concepts

- New Storage Materials, New Storage Concepts
- Many Ideas, Varying Functionality/Cost, All Unproven

Are We Nearing a New Memory Inflection ?

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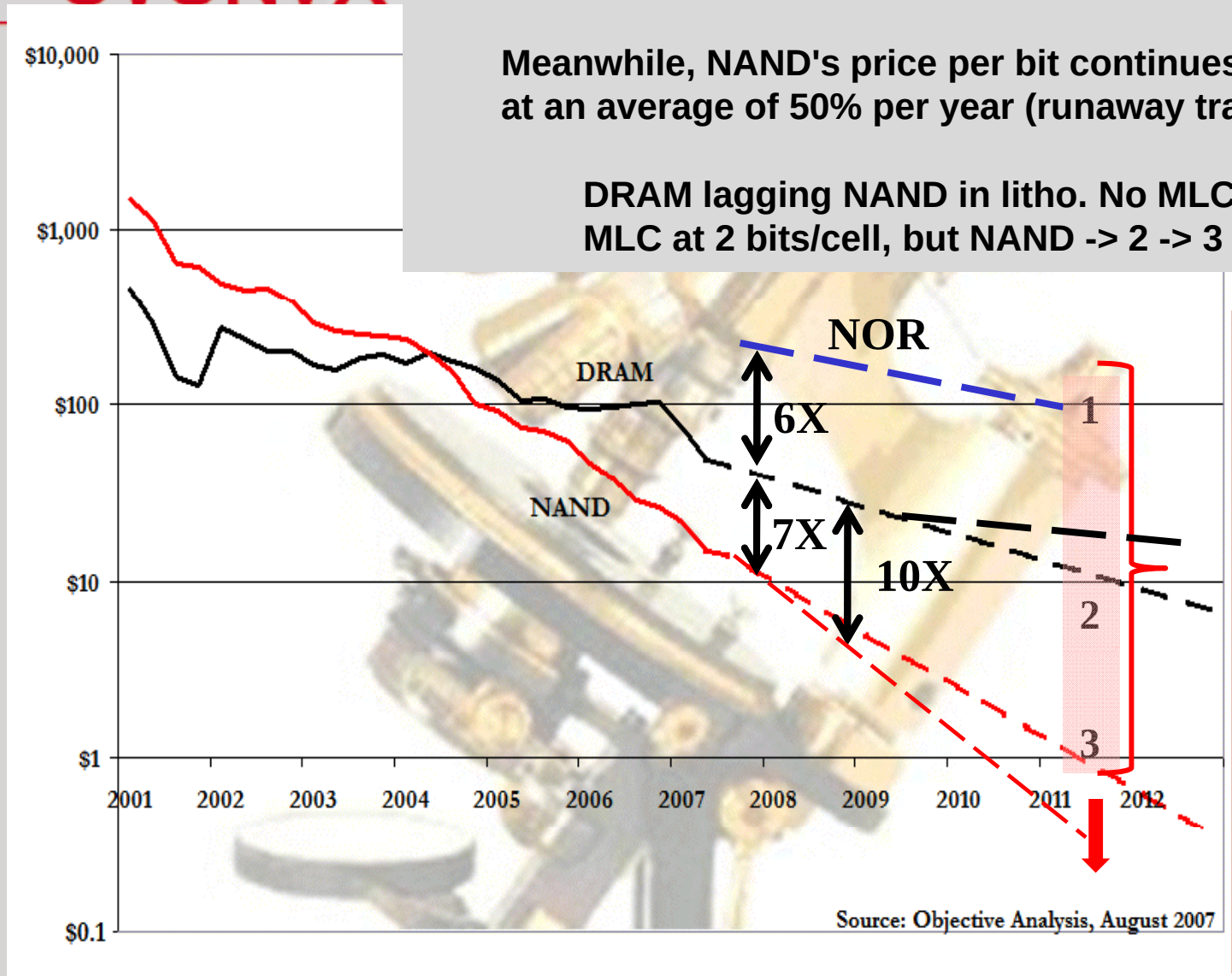
NAND :7X lower $ per/bit than DRAM in 2007, 10X lower 3Q2008

DRAM has declined 32% per year, but there are underlying technical reasons why the historic DRAM price decline will eventually slow down (once supply/demand come in balance)

Meanwhile, NAND's price per bit continues to decline faster, at an average of 50% per year (runaway train!)

DRAM lagging NAND in litho. No MLC for DRAM, NOR MLC at 2 bits/cell, but NAND -> 2 -> 3 -> 4 bits/cell



Existing memory PCM 'replacement'/ displacement priority + target new 'supplemental memory' to better exploit NAND lowering cost at reduced performance

Near term: NOR 'displacement' with higher system level power/speed performance

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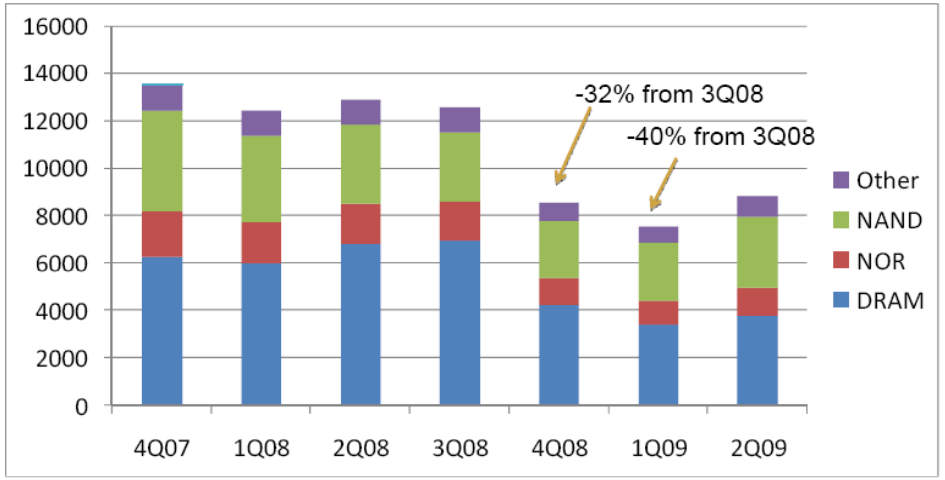
PCM is first addressing the highest value NOR market with 512Mb and 1Gb solutions. Less incentive of cell phone vendors to replace low density NOR with PCM in existing products. Focus on new systems with compelling differentiating system level performance advantages.

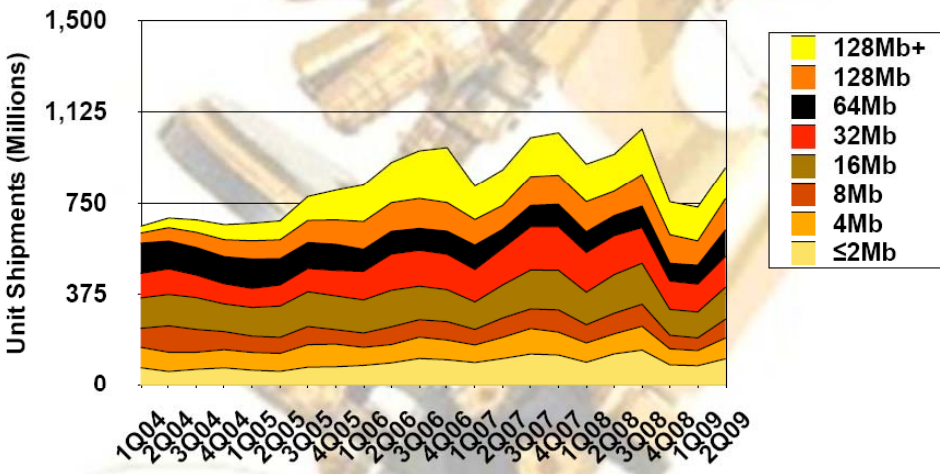
Memory Market Make-up ($M)



Sources: Denali and Industry sources

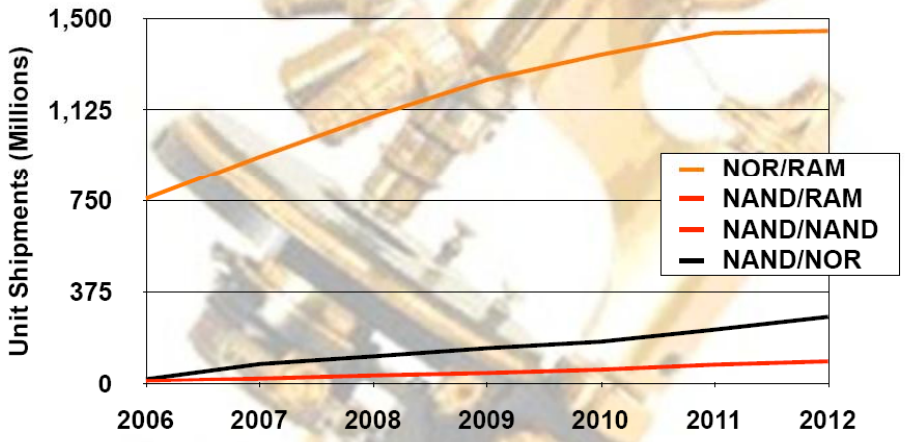
denali MEMCON09

NOR Ships in Many Densities



OBJECTIVE ANALYSIS – www.OBJECTIVE-ANALYSIS.com

NOR Still Big in Cell Phone MCPs



From: ***Flash Packaging: What Phone Makers Want & Why***

OBJECTIVE ANALYSIS – www.OBJECTIVE-ANALYSIS.com

Saturday, August 8, 2009

Numonyx is First to Ship Phase Change Memory for Revenue

"Numonyx achieved a significant milestone in December 2008 – both for the company and the industry. In Q4'08, Numonyx began commercial shipments of the industry's first Phase Change Memory (PCM) products. The 128 Mb Numonyx PCM device, code-named Alverstone, is a non-volatile memory implemented on 90nm lithography.

More than 20 customers received samples of Alverstone in 2008, and many are evaluating Numonyx PCM as the next leading-edge memory technology. Numonyx will expand its roadmap for Phase Change Memory to include not only the embedded and wireless market segments, but storage and computing applications as well."

Samsung Electronics and Numonyx join forces on Phase Change Memory

SEOUL and GENEVA, June 23, 2009 – Samsung Electronics Co., Ltd. and Numonyx B.V. today announced they are jointly developing market specifications for Phase Change Memory (PCM) products, a next generation memory technology that will help enable makers of feature-rich handsets and mobile applications, embedded systems* and high-end computing devices to meet the increasing performance and power demands for platforms loaded with content and data. **Creating common hardware and software compatibility for PCM products** should help simplify designs and shorten development time, enabling manufacturers to quickly transition to high-performance, low-power PCM products from both companies. ……..

Samsung and Numonyx are developing common specifications – or “pin for pin” hardware and software compatibility – for mobile, embedded and other potential computing applications supporting the JEDEC LPDDR2 Low Power Memory Device Standard. The LPDDR2 standard offers advanced power management features, a shared interface for nonvolatile memory (NVM) and volatile memory (SDRAM), and a range of densities and speeds.

Phase change memory has many of the advantages of NAND and NOR flash memory as well as other RAM memories – allowing data to be read at RAM speeds while lowering the cost and power consumption levels by reducing the large amounts of RAM often used in today’s digital applications.

Samsung Announces Production Start of 512 Mbit 60-nm PRAM with 7-10 X faster write than NOR and 20% extended battery life for handset!

OVONYX

September 21, 2009: **Samsung Announces Production Start-up of Its Next-generation Nonvolatile Memory — PRAM**
TAIPEI, Taiwan--(BUSINESS WIRE)--Samsung Electronics Co., Ltd., the world leader in advanced semiconductor technology solutions, today announced at the sixth annual Samsung Mobile Solutions Forum held at the Westin Taipei Hotel that is has begun producing 512-Megabit (Mb) PRAM memory. A new non-volatile memory technology that features high-performance and low power consumption, PRAM (phase change random access memory) is expected to usher in the next generation of non-volatile memory technology for mobile devices.

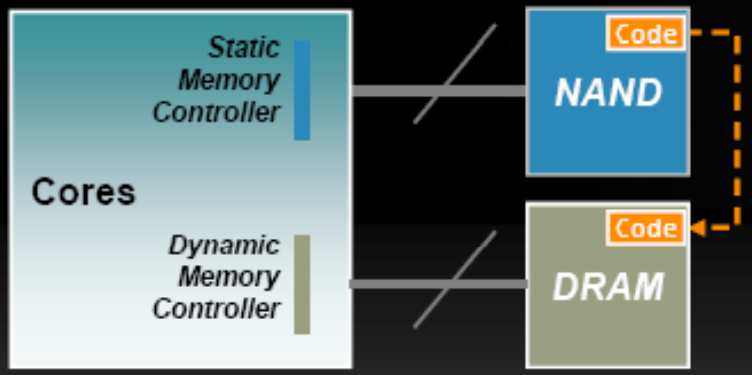
High-density and high-performance are the key technology requirements for smartphones, however these attributes can increase power consumption significantly. Because PRAM's greatly simplified data access logic requires less support from DRAM, its power usage is very efficient. By using PRAM, **the battery life of a handset can be extended over 20 percent.**
"We believe PRAM will make a highly significant contribution to the efficiency of mobile phone designs, particularly for multimedia handsets and smartphones," said Sei-Jin Kim, vice president, mobile memory planning and enabling group, Memory Division, Samsung Electronics. "We expect it to become one of our core memory products in the future."
The 512Mb PRAM can erase 64 Kilowords (KWs) in 80 milliseconds (ms), which is over **10 times faster than NOR flash** memory. In data segments of 5 Megabytes (MBs), PRAM can erase and rewrite data approximately **seven times faster than NOR flash.**

More scalable than other memory architectures now under research, PRAM combines the speed of RAM for processing functions with the non-volatile characteristics of flash memory for storage. Samsung's first PRAM is produced using 60-nanometer class technology, the same process technology used in NOR flash production today. Finer technology nodes will be applied in future generations of PRAM to expedite further commercial adoption.

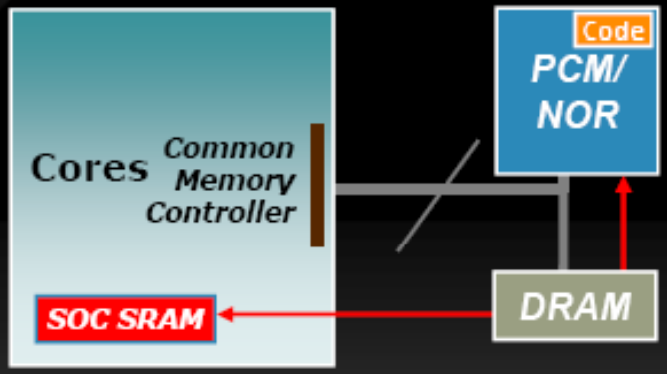
Gartner "If Samsung can show such power savings and other benefits in final products...the company will find itself in a commanding position in the memory segment for the entire mobile handset industry."

Architecture Evolution: Comparison

Paged SnD Solution



PCM/NOR XiP Solution



Key Comparisons:*

Cost:	$X	< $X
Power:	1100uA/stby	650uA/stby
Boot Time:	100s	10s
Performance:	Worse	Better
Reliability:	More RAM	Save RAM

*estimate based on currently available data

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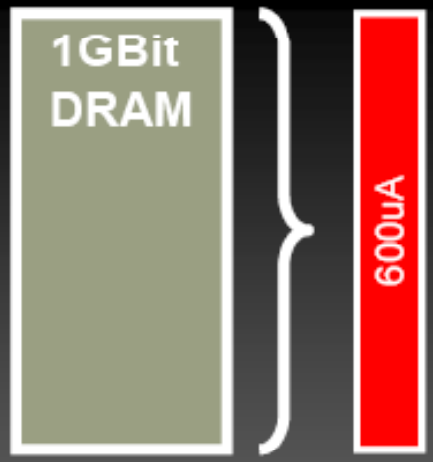
Technology Cost Comparison – Power

Power consumption to "hold"
1Gbit (128MByte) code (IDD6)

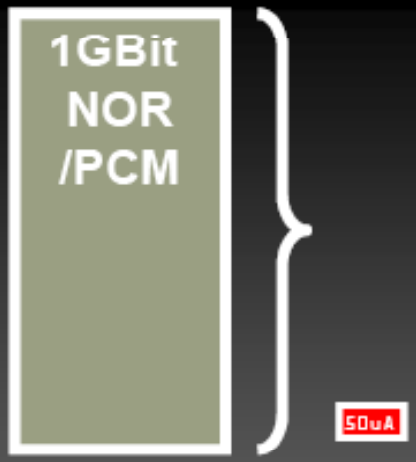
Option #1 – DRAM



Up to 600uA

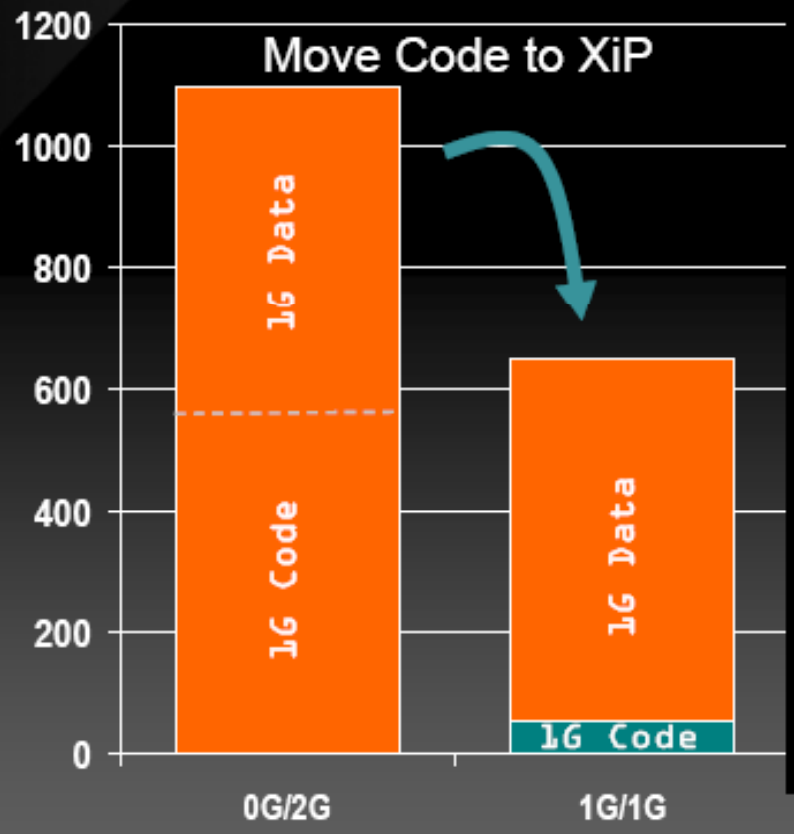
600uA

Option #2 – NOR/PCM



50uA

Up to 50uA



Design Goal: Reduce impact of RAM on power by reducing RAM

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Design Goals for Mobile System

Wireless Customer Values	PCM/NOR XiP	Paged SnD
RAM Savings – Code (XiP) Up to 60% of code is sensitive to paging delays. Must add RAM for performance	+	-
Performance – Boot Time XiP improves boot time – eliminates copying code to RAM	+	-
Performance – Application Switch Time Smooth application performance less application stalls	+	-
Performance – Application Concurrency Using XiP removes code from RAM and allows more code to run concurrently	+	-
Power Savings Smaller RAM improves power in standby & provides more battery for active	+	-
Reliability NAND read disturb & NAND bad blocks – only solution is to use more RAM	+	-

Concept for PCM as "Storage Class Memory and in PC for true instant-on PC. In addition to both speed and power performance advantages -> lower cost solution once PCM price drops below DRAM

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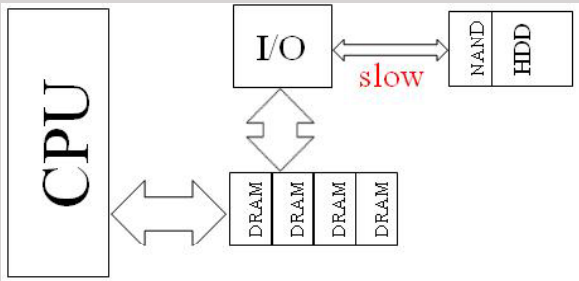
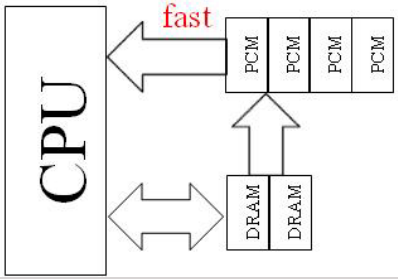


Current



Future

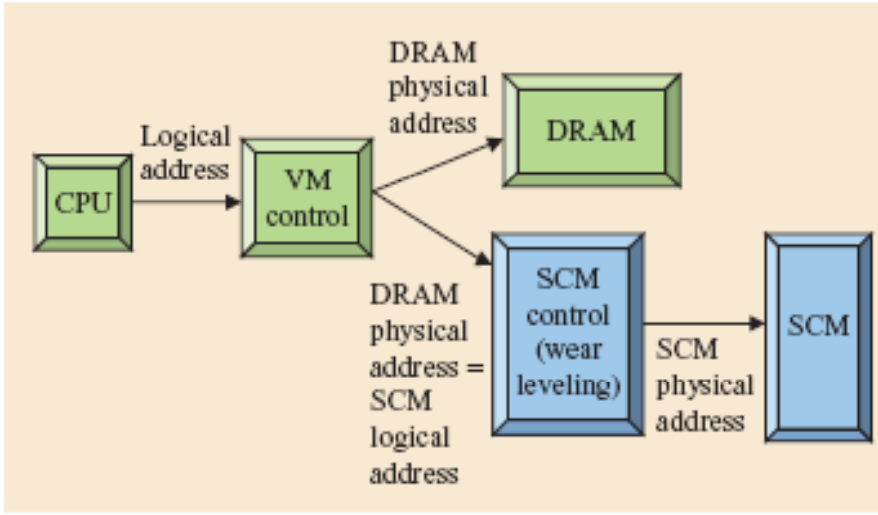


Figure 3

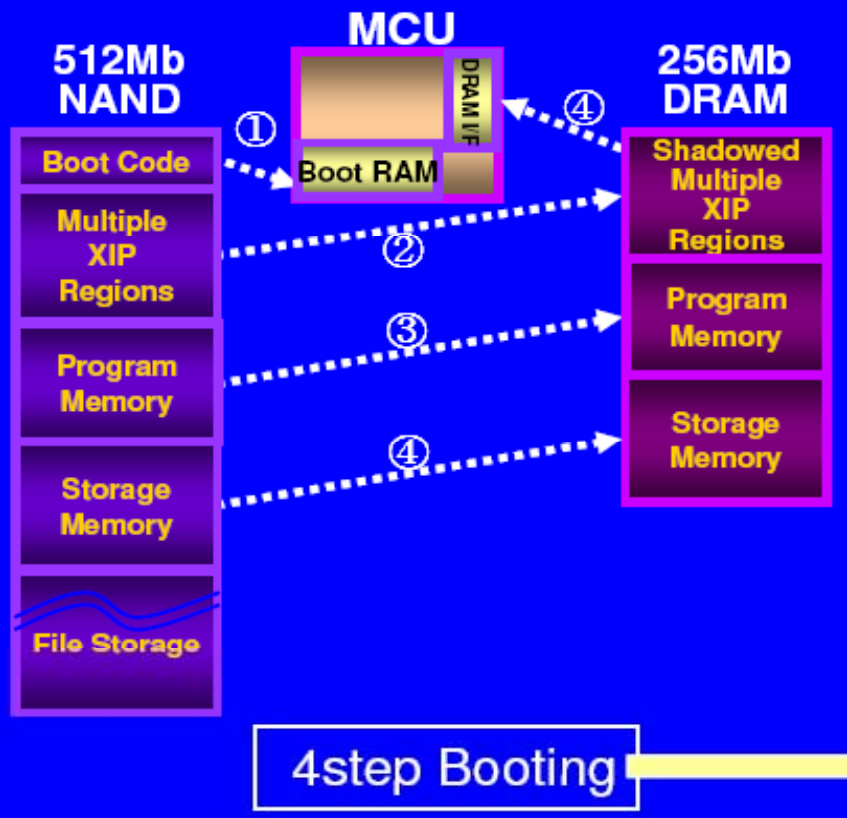
Translation of addresses in a virtual memory system that utilizes both DRAM (dynamic RAM) and storage-class memory (SCM). The virtual memory manager translates some of the CPU logical address space into physical addresses for the DRAM. Addresses destined for SCM undergo a second translation, which takes wear leveling into account. (VM: virtual memory.)

IBM J. Res. & Dev. Vol 2 No. 4/5 July/Sept. 2008

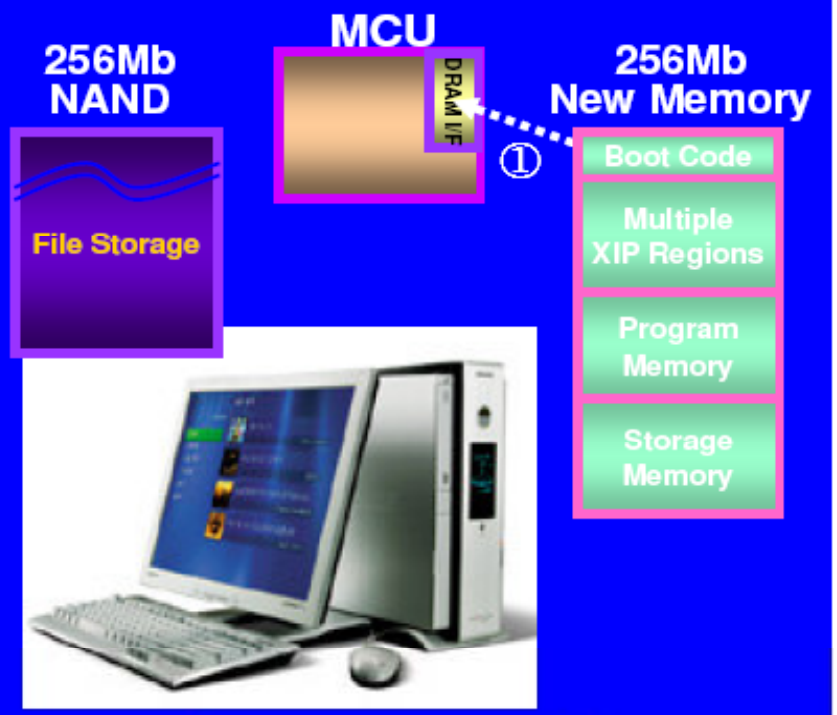
Instant on Application

Faster Booting System

- Current System(PDA, PC,…)



- New Memory Solution



4step Booting → 1step Booting

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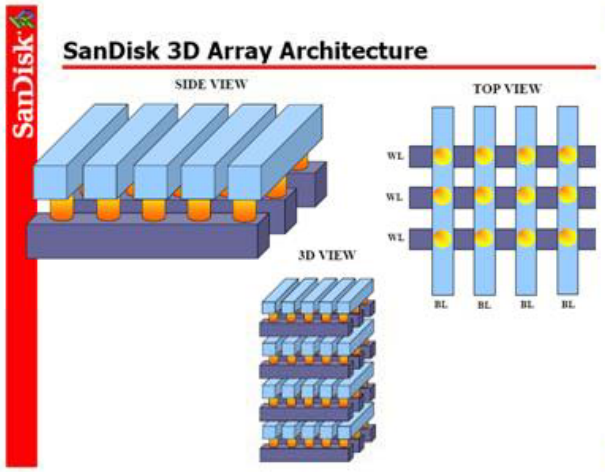
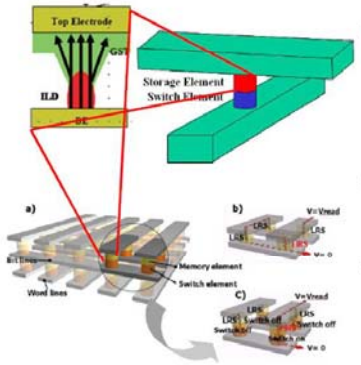
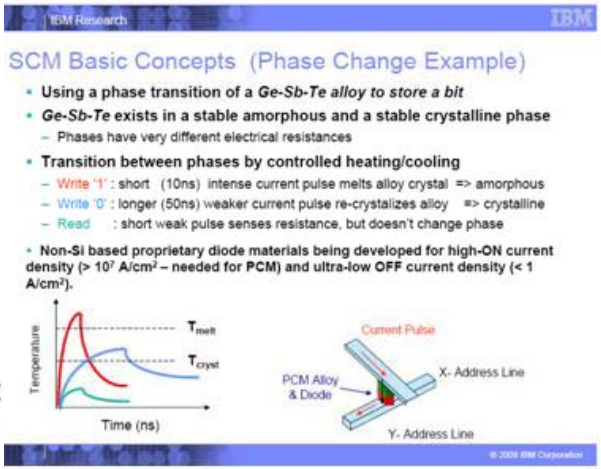
Many Groups exploring multi-layer cross point memory cell as ultimate low cost solution utilizing a Resistive element (such as a phase change or RRAM element in series with a thin film switching element such as a diode).

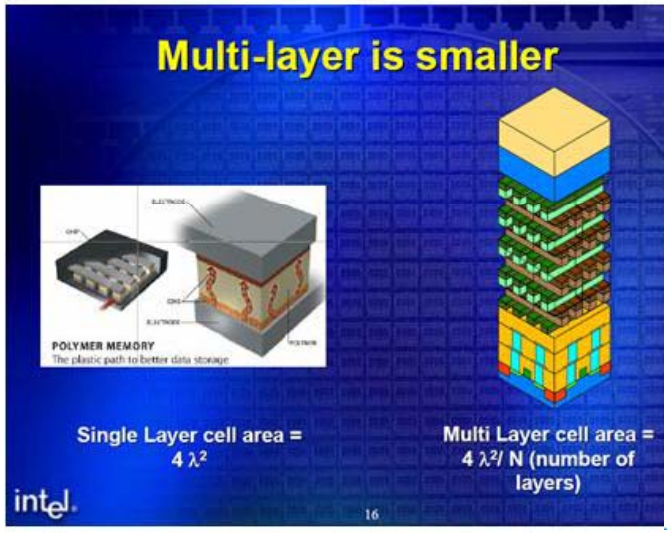


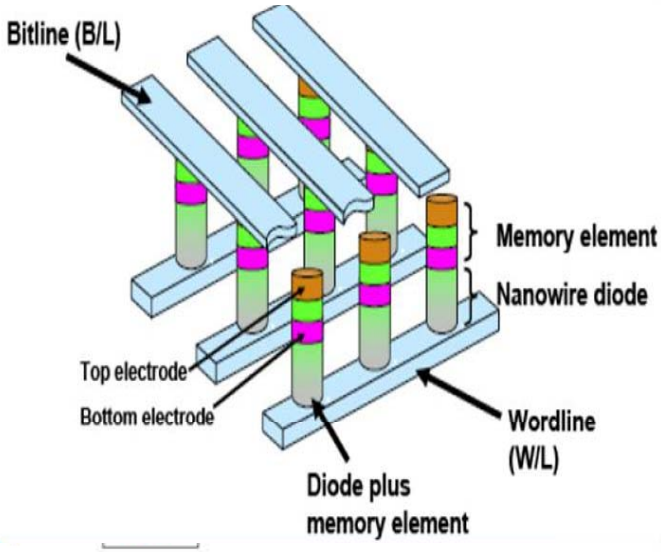
Multi-Layer Memory

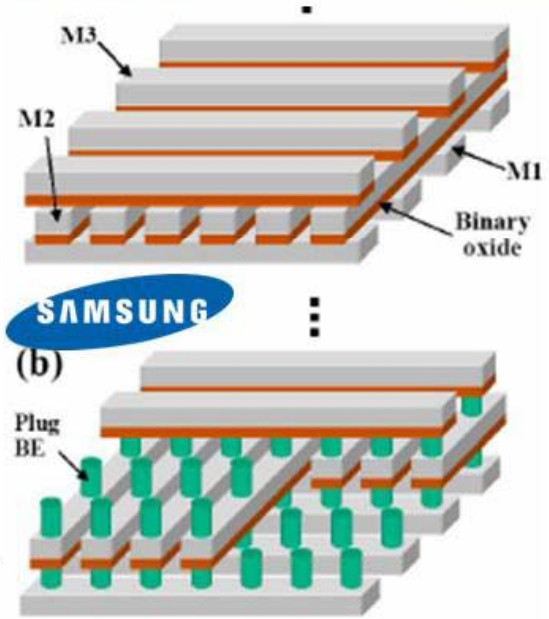


- Thin film PN diode or selector allows stacking of memory layers
- Cell size 4 λ^2/ N layer
- Together with multi-level capabilities: lowest cost memory rivals NAND









Potential Floor Plan with CMOS under Cross-Point Thin Film Memory Array for improved array efficiency

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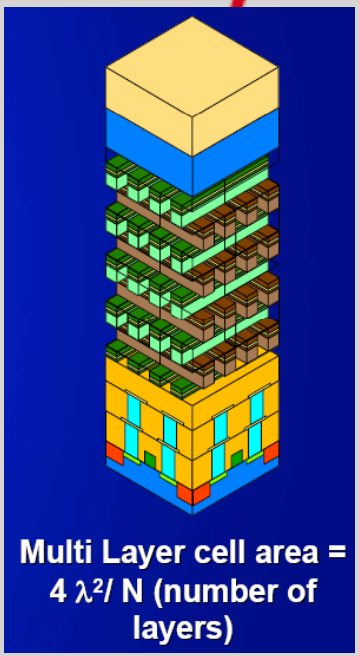

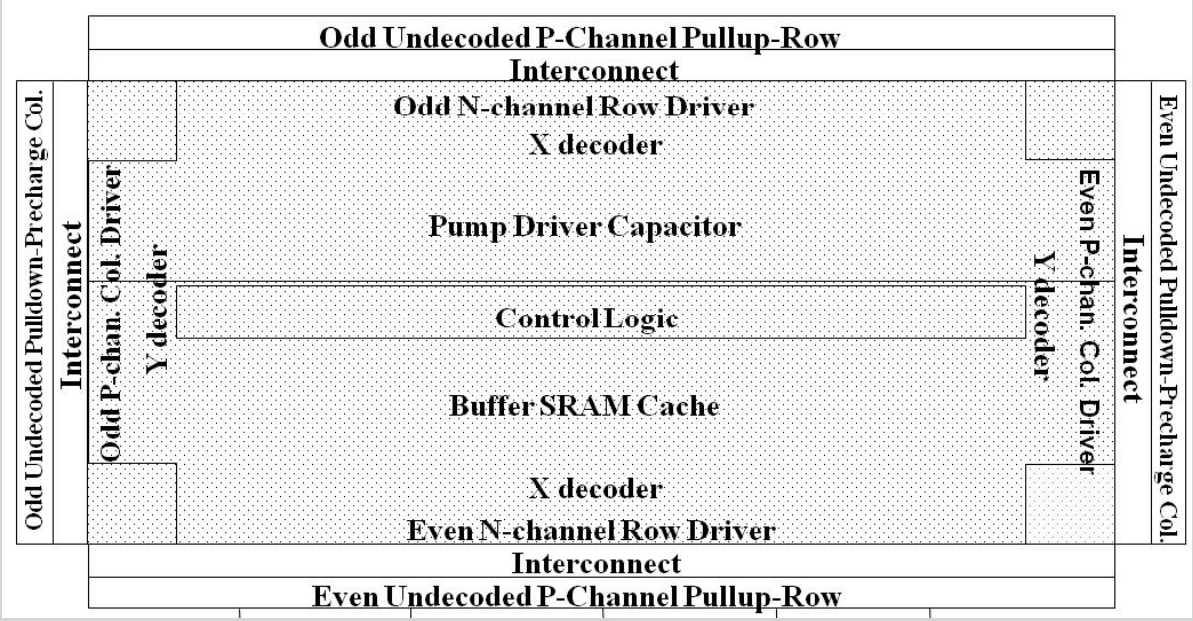

Stacking 3D memory directly over CMOS allows for high array efficiency -> smaller die size

Each memory layer is repeated for lowest cost: cell size: $4F^2$ / layers

CMOS node can lag memory node (hybrid scaling) example 65-90 nm CMOS with 45 nm generation memory scaling

Cross-point cell for lithography driven scaling

Long Term Potential Lowest Cost Memory: Multi-layer Cross Point Cell -> Phase change memory is a leading candidate (especially for high performance storage class memory)

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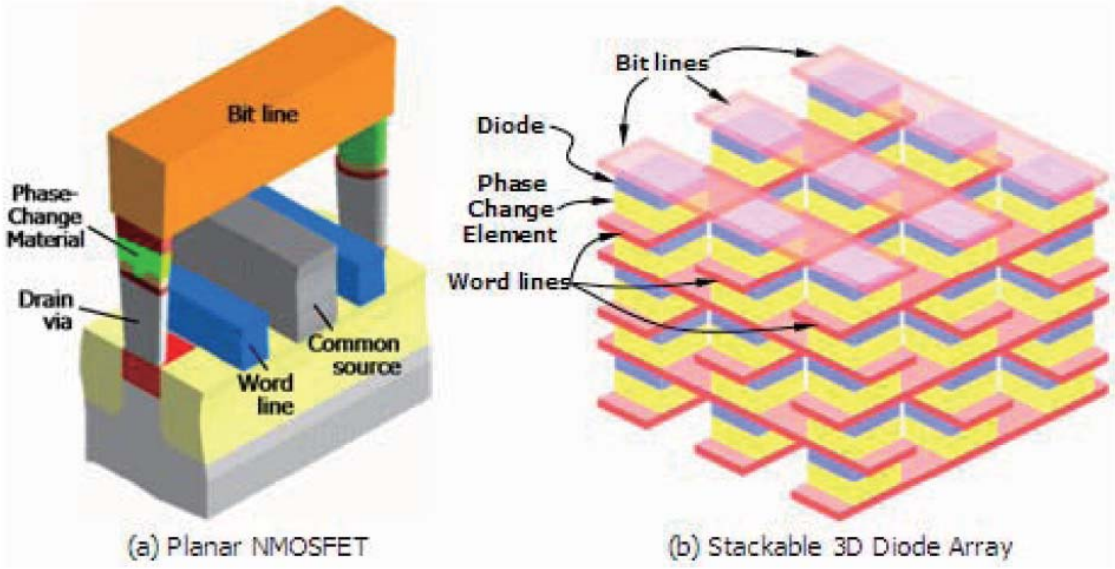

Fig. 10 Configurations of PCM with select

Device Technology Innovation for Exascale Computing , 2009 Symposium on VLSI Technology Tze-chiang (T.C.) Chen IBM T.J. Watson Research Center

Upcoming December 2009 IEDM: Paper 27.1 "A Stackable Cross Point Phase Change Memory", D.C. Kau, et. al, Intel Corp., *Numonyx B.V. **A phase change memory cell is built by coupling PCM with OTS (PCMS) and integrated in a true cross point array**. Multiple layers of PCMS arrays can be stacked over CMOS circuits. This **fast,** durable, and dense memory for random access and storage applications provides a promising, scalable NVM technology.

Alternative stacked NAND and vertical NAND for future lowest cost memory compared to multi-layer Xpoint

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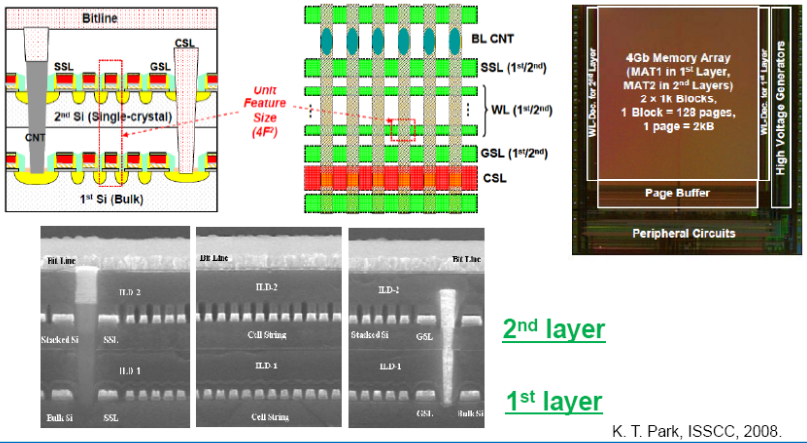
3D-NAND

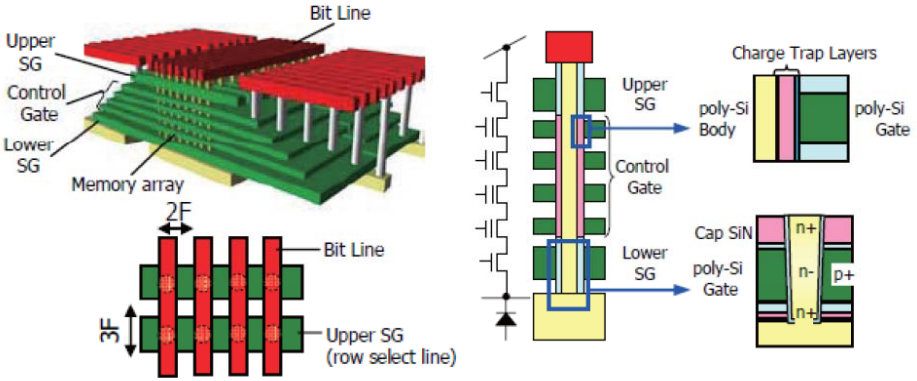
- **Multi-layer NAND (Samsung)**
  - Bit-line and source-line are shared.
  - Cost is still an issue.



K. T. Park, ISSCC, 2008.

3D-NAND (Cont')

- **Vertical NAND (Bit Cost Scalable Cell: Toshiba)**
  - Lower cost expected w. relaxed design rule.
  - Device issues such as a-Si channel.



H. Tanaka, Symposium on VLSI Technology, 2007.

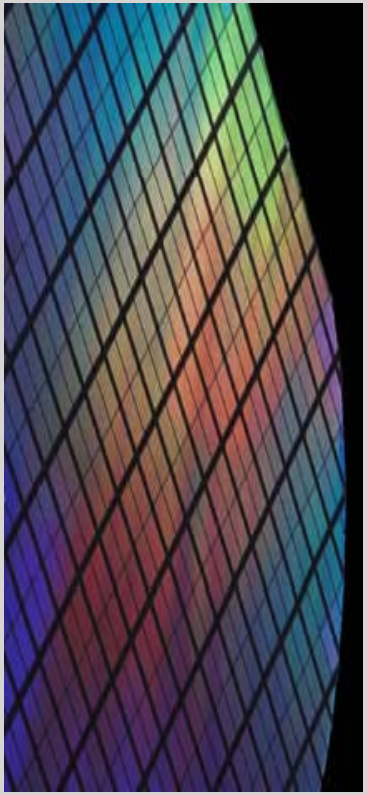
Stacked NAND has many litho layers per each stacked level thus minimizing the cost benefit of stacking.

Vertical NAND is relatively new with no array statistics and many process challenges.

Both stacked and vertical NAND require the use of a poly silicon channel thus reducing the R/W speed performance further negating it use for either XiP or 'storage class memory'

Outline

- Phase Change Memory (PCM) Overview
- PCM Scaling
- Comparative Memory Technology Roadmap
- Product Roadmap
- Summary



Summary

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- Today PCM has been demonstrated by multiple suppliers as viable NVM at 128 - 512 Mbit (greater than two orders of magnitude higher density than competing non Flash based NVM) with forthcoming products at 65/45 nm to substantially lower cost.
- Clear scaling path with 'confined cell' architecture demonstrated. Ireset scales with geometry!
- Near term, market opportunities (focus on added performance (speed / power)
  - "Fusion / Unified" Memory replacing NOR flash in "XIP" cellular market and reducing DRAM for lower power / instant-on / lower cost with low power mobile DRAM reduction -> Multi-billion $ NVM market that doesn't compete on cost with the run-away NAND train!!
- Medium term: DRAM faces significant scaling and cost challenges at and below the 45 nm node
  - Initial opportunity to use of PCM for power sensitive DRAM applications including cellular DRAM exploiting PCM's added benefit of non-volatility
  - Embedded NVM applications
  - Replace DRAM buffer in SSD's with PCM large buffer / 'scratch pad' memory
  - Develop PCM market for low power instant-on computing architecture
- Longer term: develop innovative 3D multi level cross-point architecture resulting in lower cost PCM 'storage class' memory compared to NAND

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Thank you !

Q & A