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Predictable Success

Stress Engineering and its Interactions with High-k/Metal Gate and USJs

Victor Moroz

August 20th, 2008

NCCAVS THIN FILM USER GROUP

Outline

- Stress-Induced Performance Gain
- Evolving Stress Engineering
- Stress in Millisecond Annealing
- Si:C
- Stress and Implant Damage
- Reliability
- Stress Proximity Effects

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- **Stress-Induced Performance Gain**
- Evolving Stress Engineering
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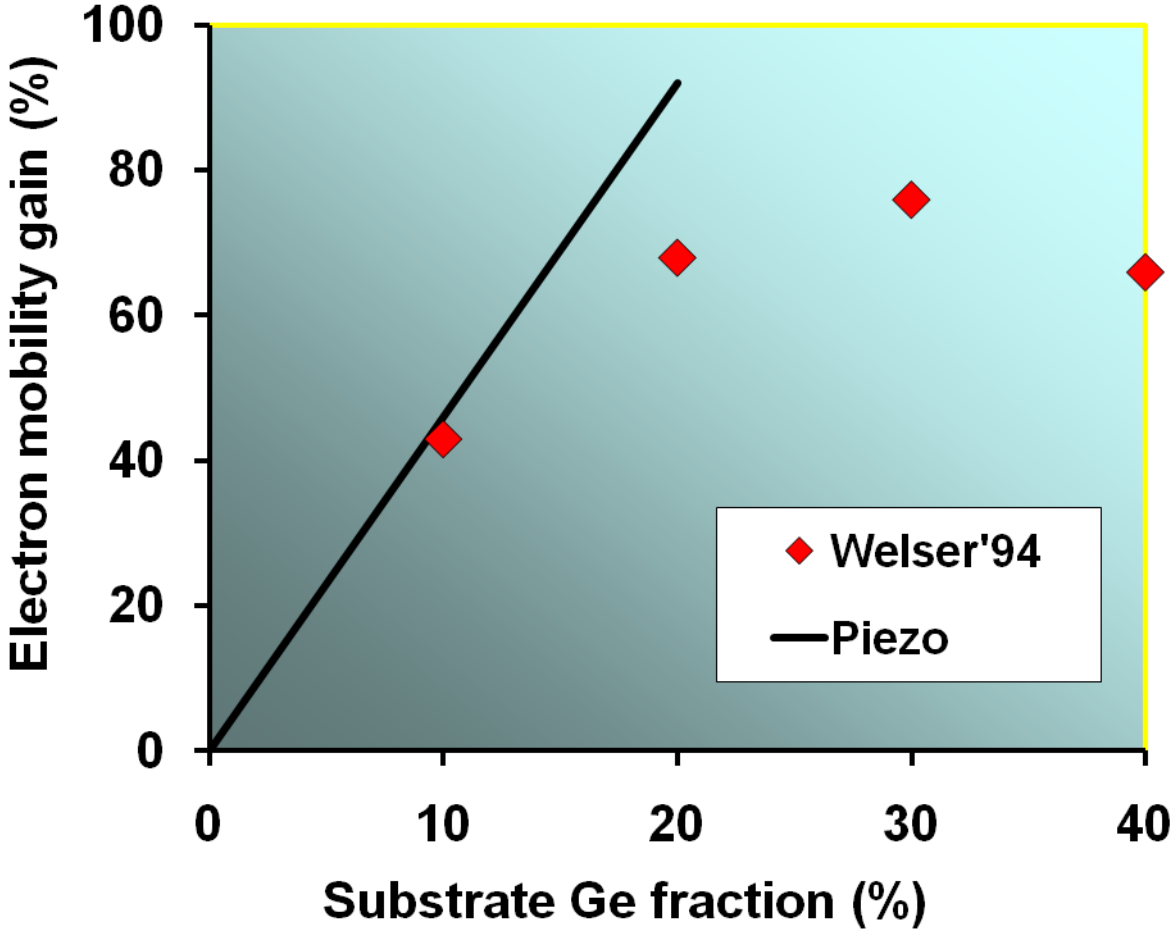
Electron Mobility at High Stress Levels

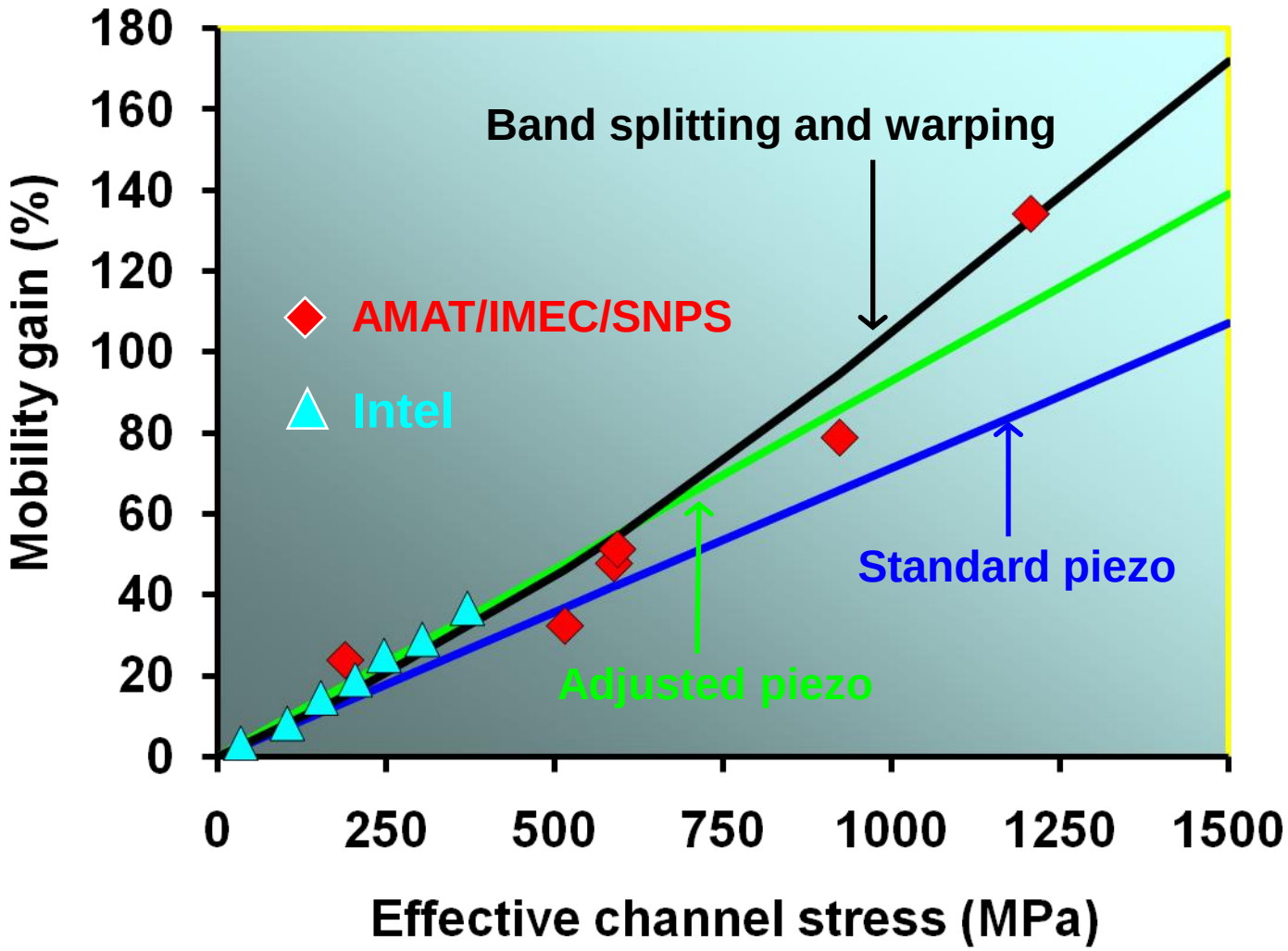


Enhancement saturates at ~70%

Therefore, Idsat gain in nMOSFETs is limited to ~35%

Biaxial global stress generated by SiGe layer

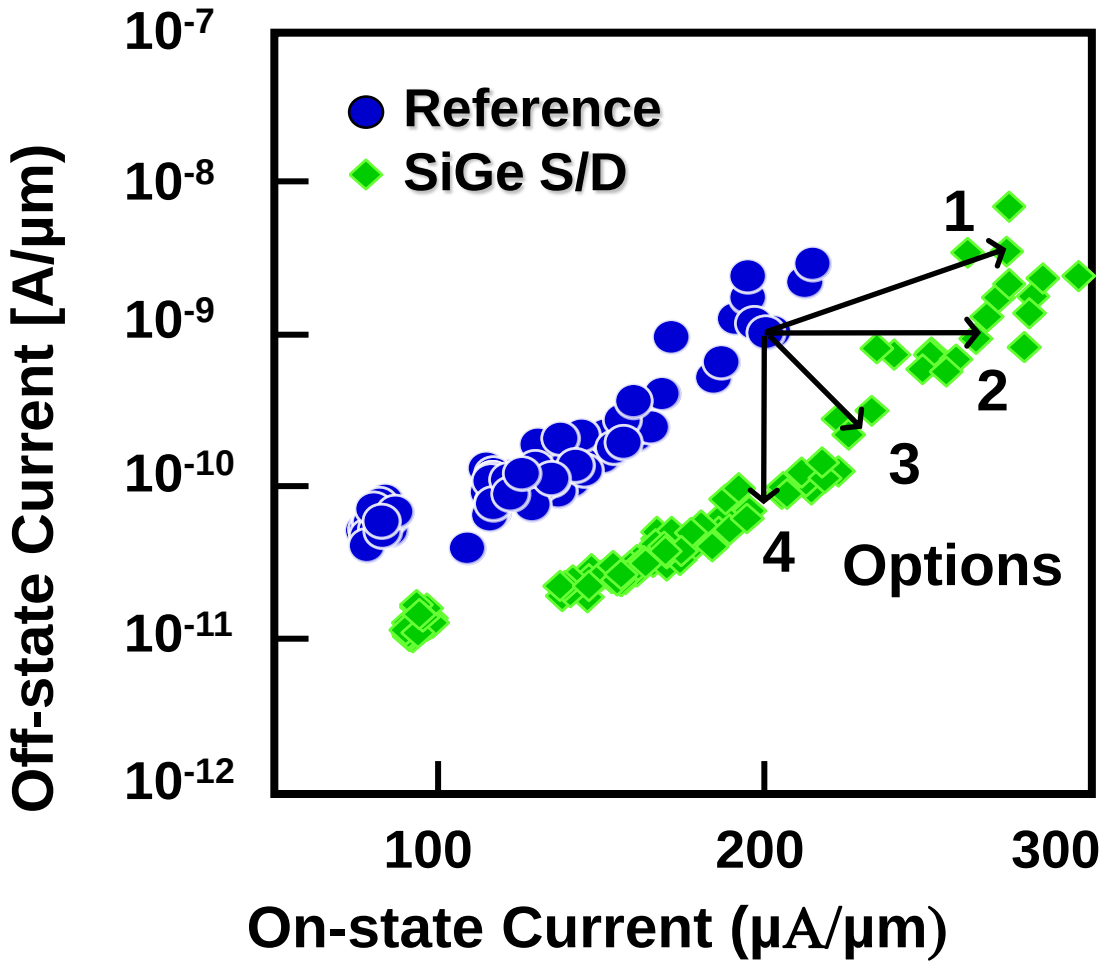
Hole Mobility at High Stress Levels



No saturation in sight, so let's keep pushing it!

Uniaxial stress generated by SiGe source/drain

Different Stress Engineering Options



1. Boost I_{on}, Degrade I_{off}
2. Boost I_{on}, Keep I_{off}
3. Improve both I_{on} & I_{off}
4. Keep I_{on}, Improve I_{off}

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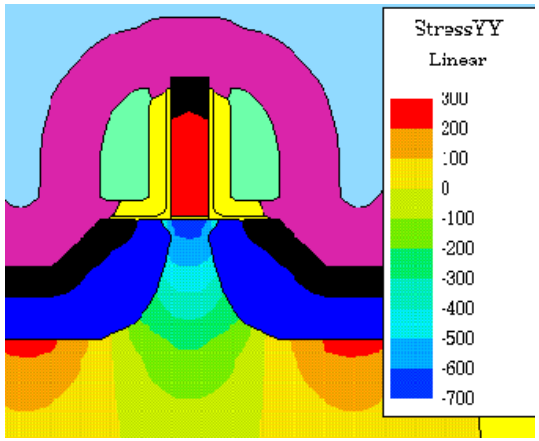
State-of-the-Art Stress Engineering

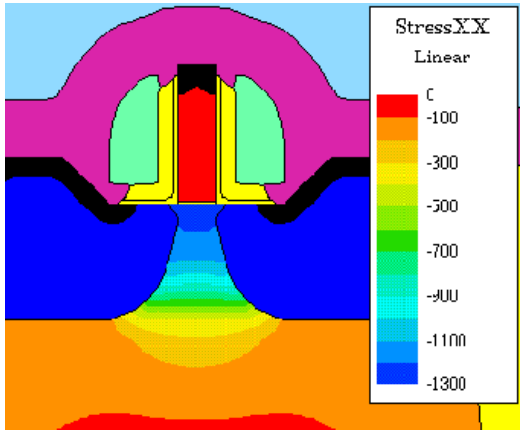
- For the poly gate, the following stress sources are being widely used:
- PMOS
  - Elevated SiGe S/D
  - Compressive CESL
  - Tensile STI
- NMOS
  - Stress memorization technique (SMT)
  - Tensile CESL
  - Tensile NiSi
  - Tensile STI

Evolving Stress Engineering

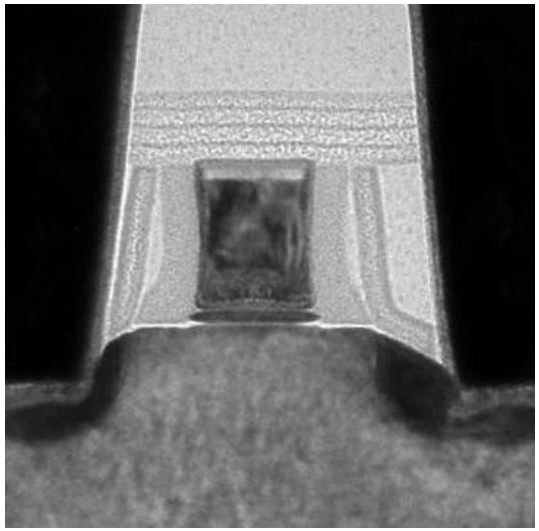
nMOS **pMOS**

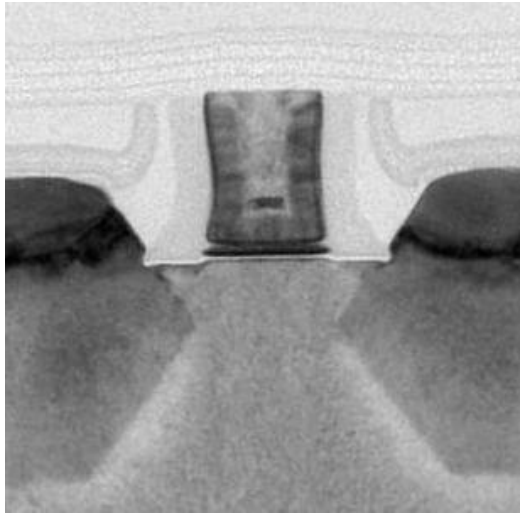
SNPS @ECS'05





Intel @45nm

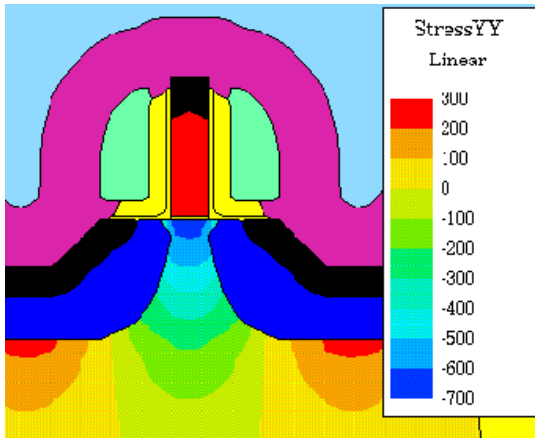




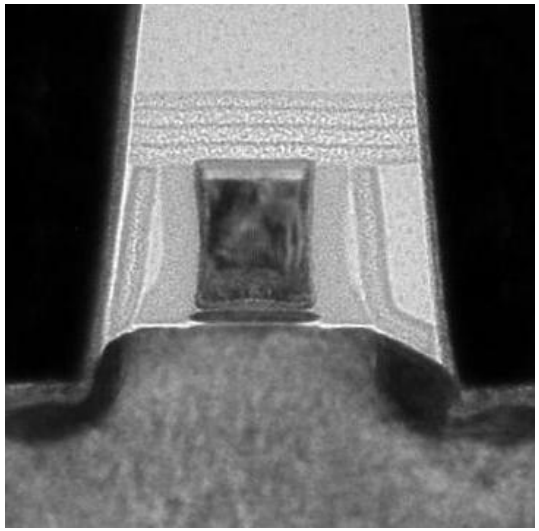
Stress Engineering with HK/MG

nMOS

SNPS @ECS'05



Intel @45nm



- Abandoned strained DSL
- Introduced recessed S/D
- Introduced tensile contacts
- Point contacts -> slot contacts
- SMT in the poly gate is gone
- SMT in the S/D remains
- Compressive metal in the gate
- But no Si:C S/D yet

Stress Engineering with HK/MG

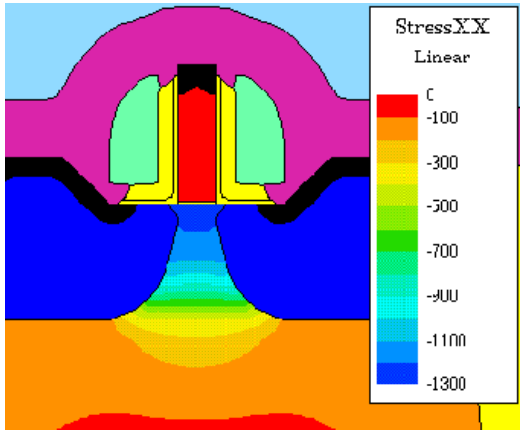
SNPS @ECS'05

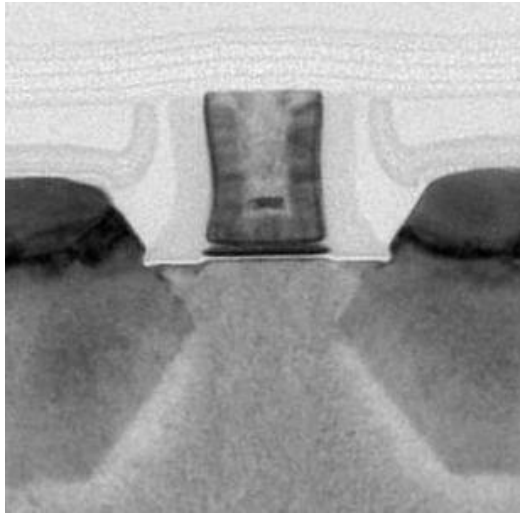
- Abandoned strained DSL
- Keep elevated SiGe S/D
- M.G. increases SiGe stress 1.5x
- Tensile contacts are above Si

Intel @45nm

- Increased Ge to 30%
- Stress triples hole mobility
- Stress doubles drive current
- SiGe facets @(111) planes

pMOS





Removing Poly Increases Channel Stress

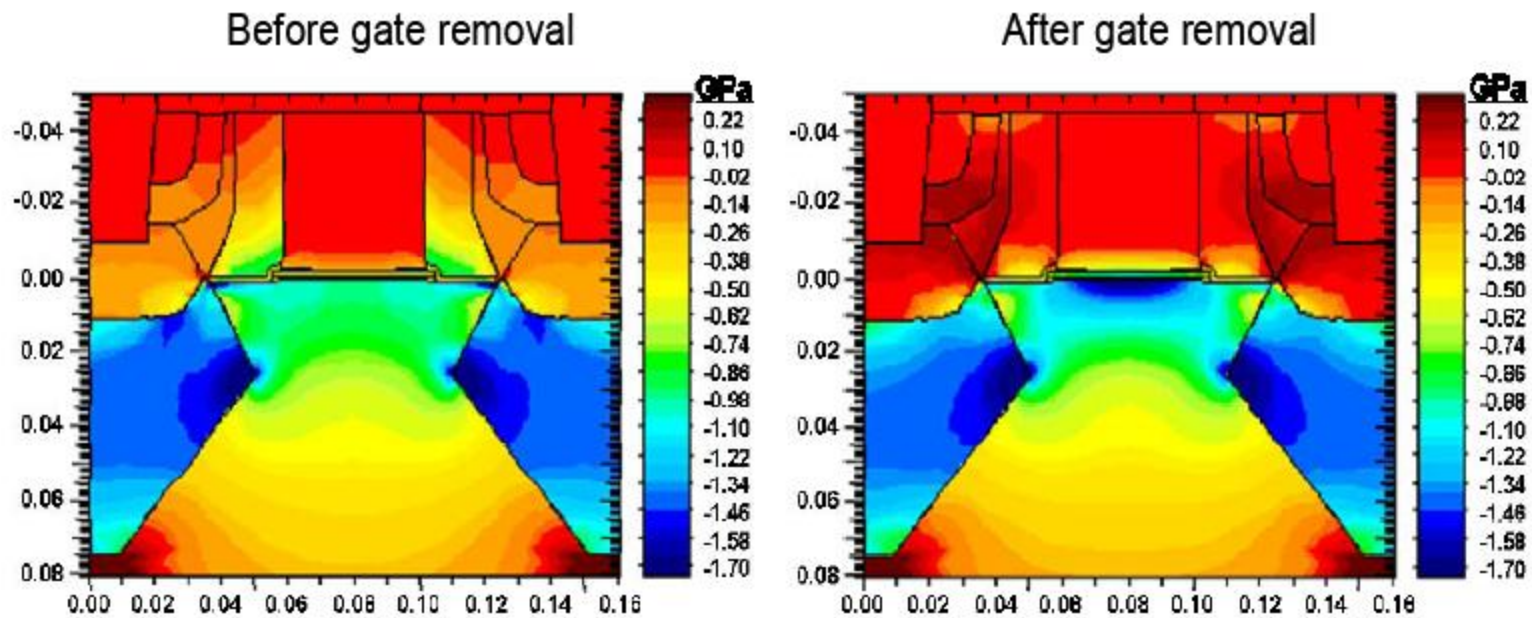


Fig.3 Stress contours in the PMOS transistor before and after the removal of the polysilicon dummy gate. Stress in the channel is shown to increase 50% from ~0.8GPa to >1.2 GPa.

C. Auth et al., VLSI 2008

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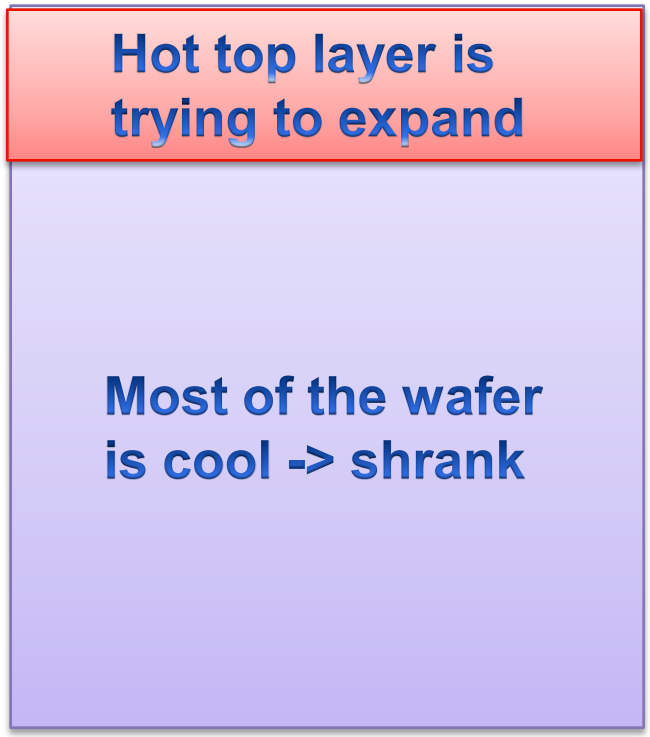
- Reliability
- Stress Proximity Effects

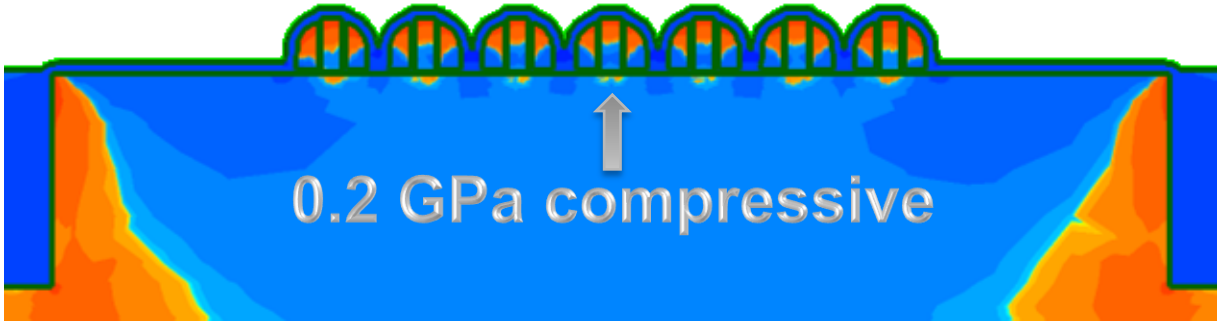
Stress Induced by Temperature Gradient



Compressive stress is expected at the top of Si wafer

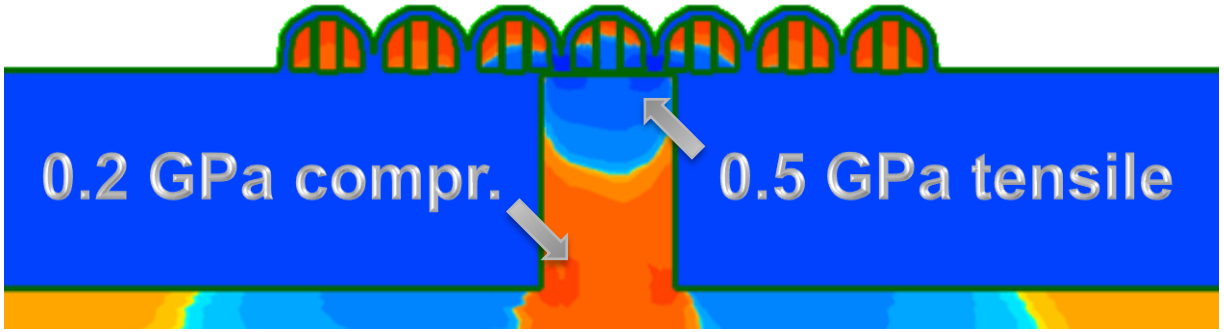
Stress Induced by T Gradient + Pattern

Si-dominant pattern



Depending on local layout, thermal expansion stress changes sign!

STI-dominant pattern



Main concern here is defect formation

V. Moroz et al., MRS 2008

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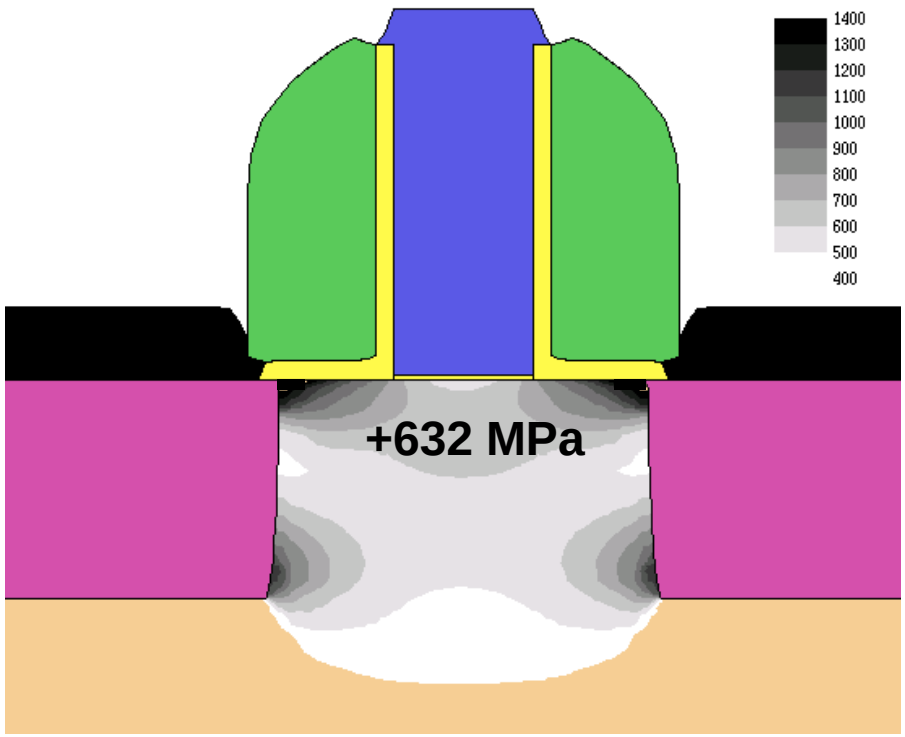
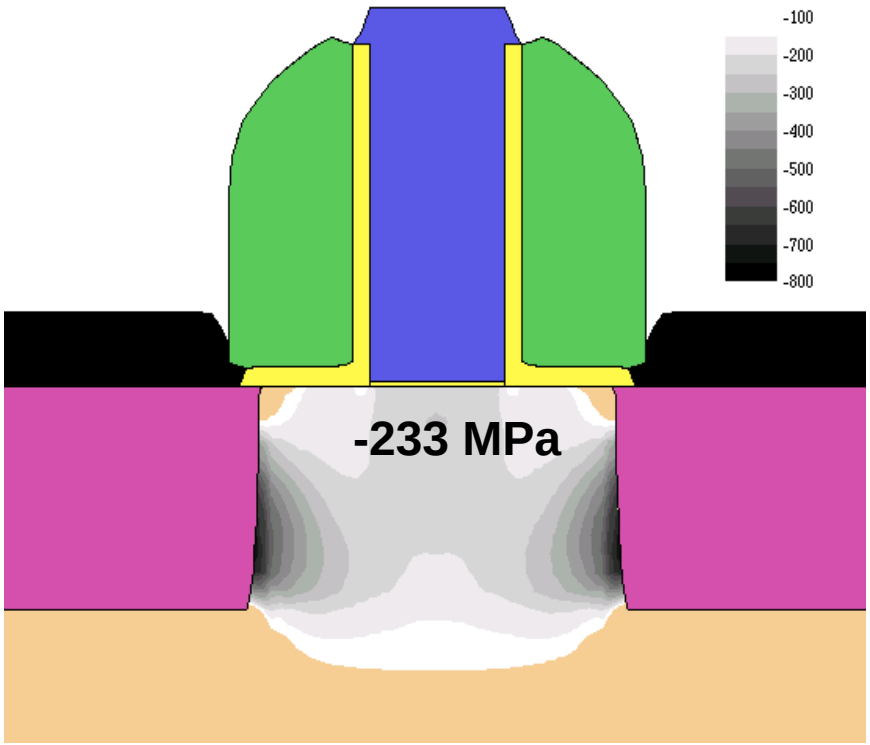
Stress in NFET with 1.8% Si:C S/D



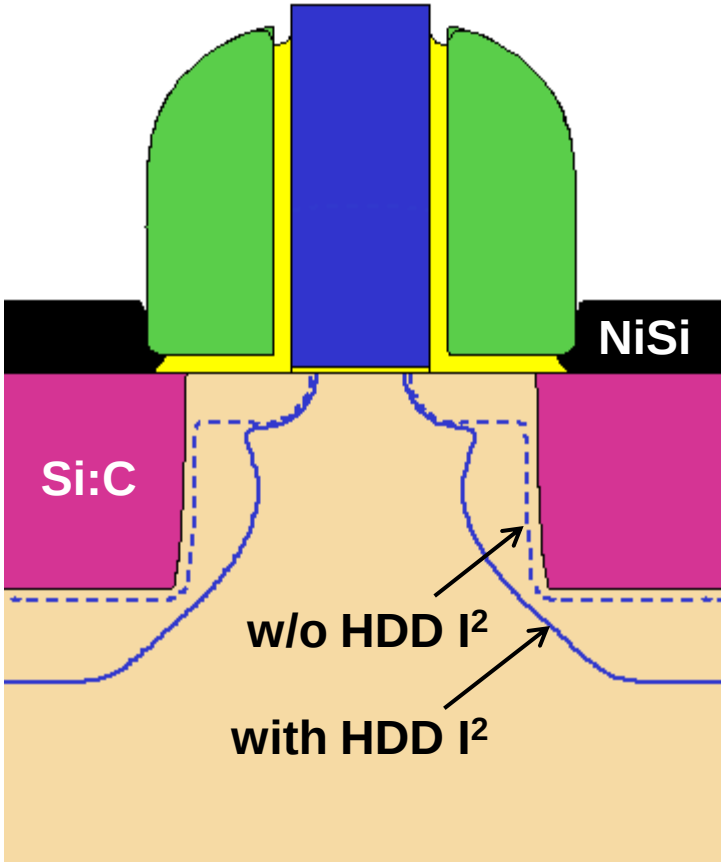
Longitudinal stress

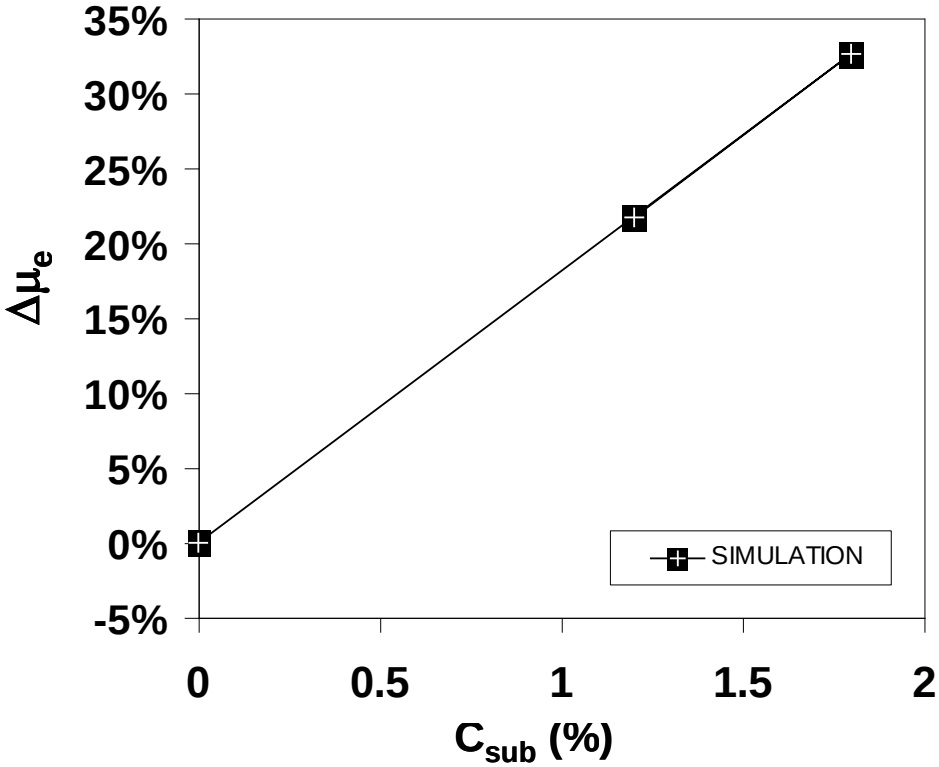


Vertical stress

Y. Cho et al., IEDM 2007

Performance Gain for Si:C





Physical Modeling Approach

Basic C Clustering Reactions

Clusters	*Respective Reaction Rates*
$C_S + CI \Leftrightarrow C_2I$	$R1 = 4\pi\, aD_{CI}\,(C_S\, C_{CI} - K_{r1}\, C_{C2I})$
$C_2I + CI \Leftrightarrow C_3I_2$	$R2 = 4\pi\, aD_{CI}\,(C_{C2I}\, C_{CI} - K_{r2}\, C_{C3I2})$
$C_3I_2 \Leftrightarrow C_3I_3 + V$	$R3 = 4\pi\, aD_v\,(C_{C3I3}\, C_V - K_{r3}\,(C_V^*/\, C_{Vi}^*)C_{C3I2})$

Source: C. Zechner *et al*., *Mat. Res. Soc. Symp. Proc*., v. 994, p. F11 (2007)

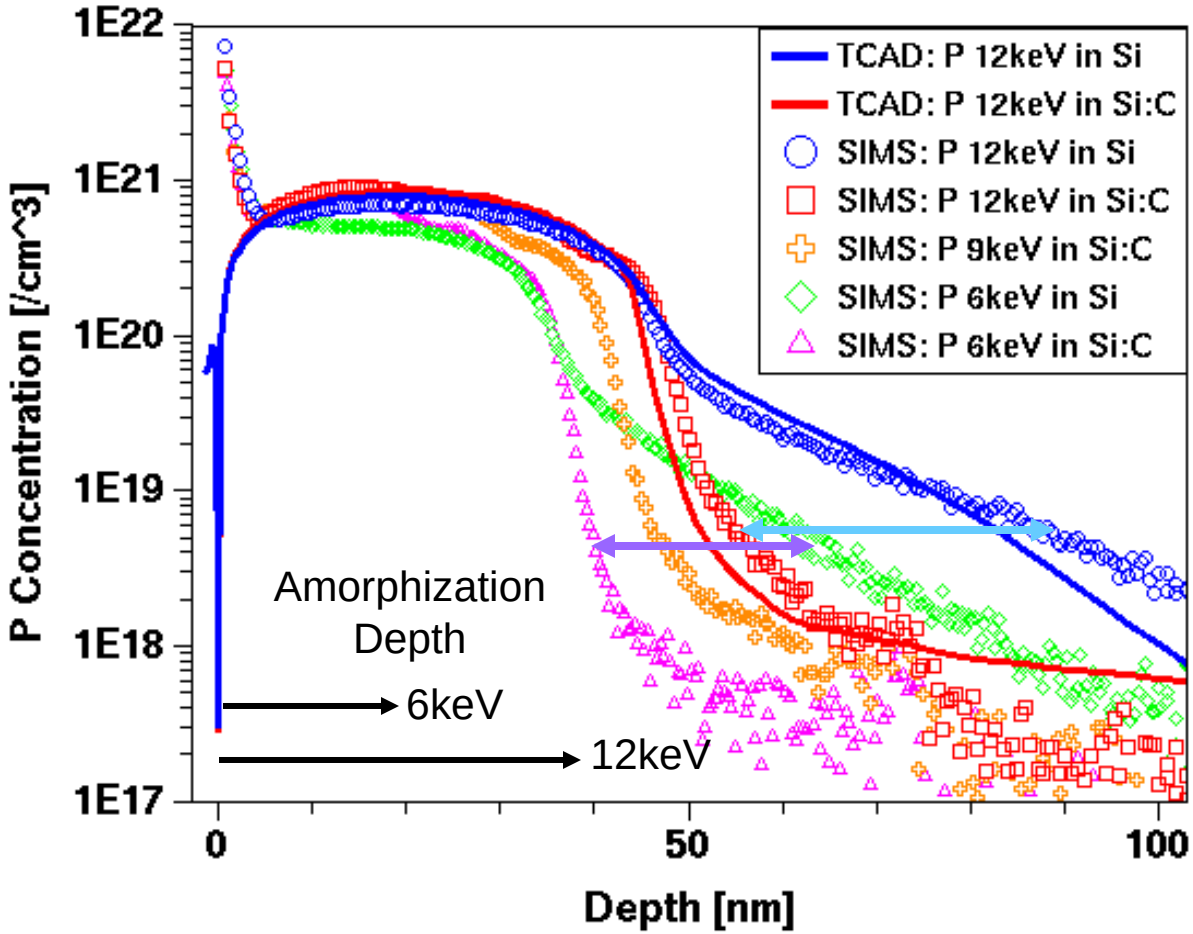
Previously physical model was developed & calibrated for B and Sb diffusion in pre-amorphized, C co-implanted Si

Physical Modeling Approach

Additional Assumptions for Si:C with C >1%

1. C_2 clusters that form at high [C]
2. Full cascade Monte Carlo implant model instead of plus factor
3. Active [As] adjustment in Si:C due to the As and C stress collaboration
4. Impact of C-induced stress on E_g, I*, V*, and pair diffusion
5. Mobile C-I pair formation in Si:C whenever as-implanted I is lower than C
6. Unusual vacancy super-saturation effect that strongly affects As, but only marginally P as a consequence of effect #5

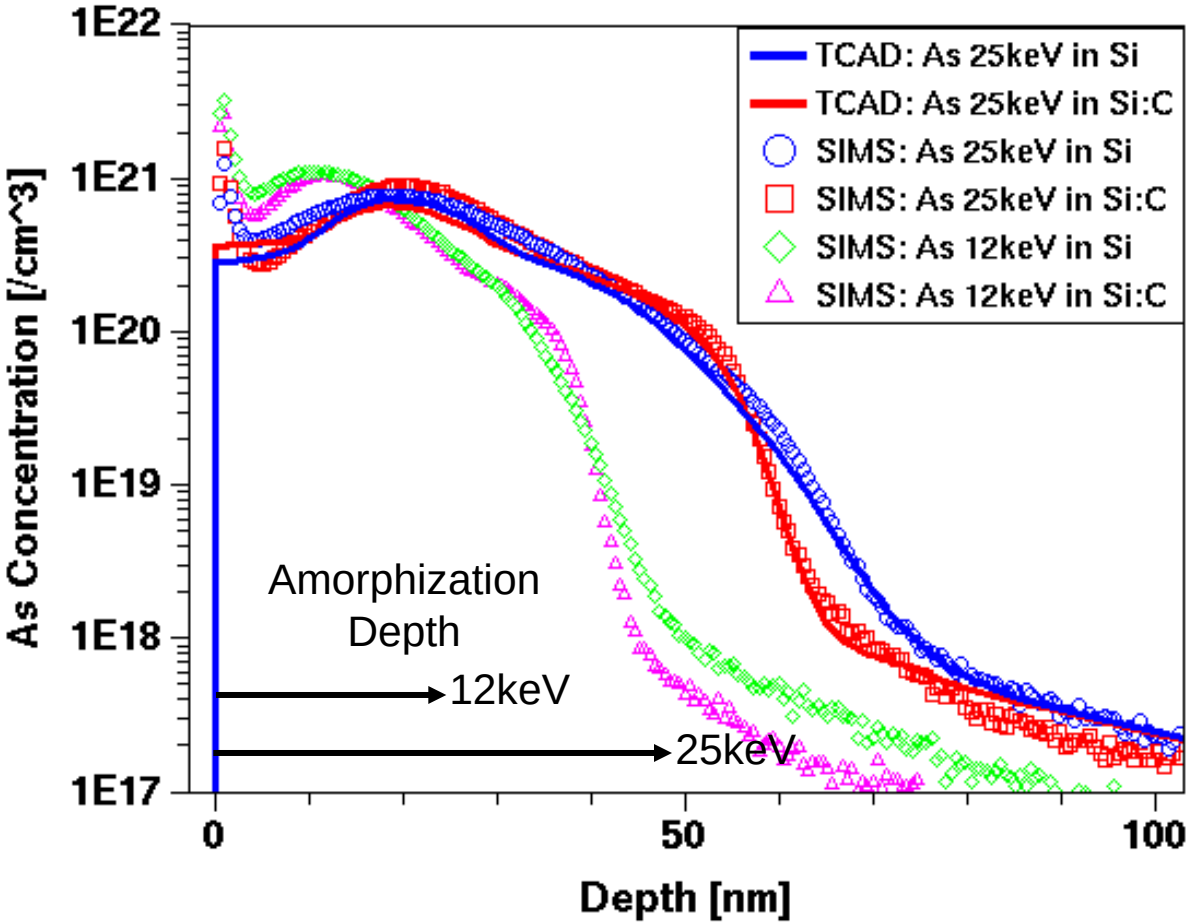
P Diffusion in Si:C



Δx_j (12keV)

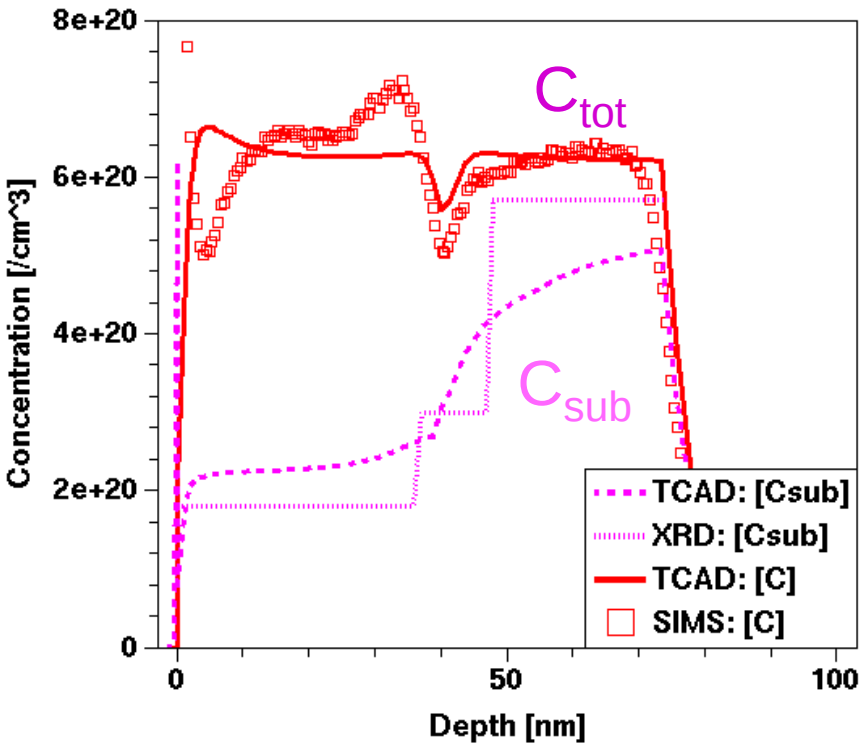
Δx_j (6keV)

As Diffusion in Si:C

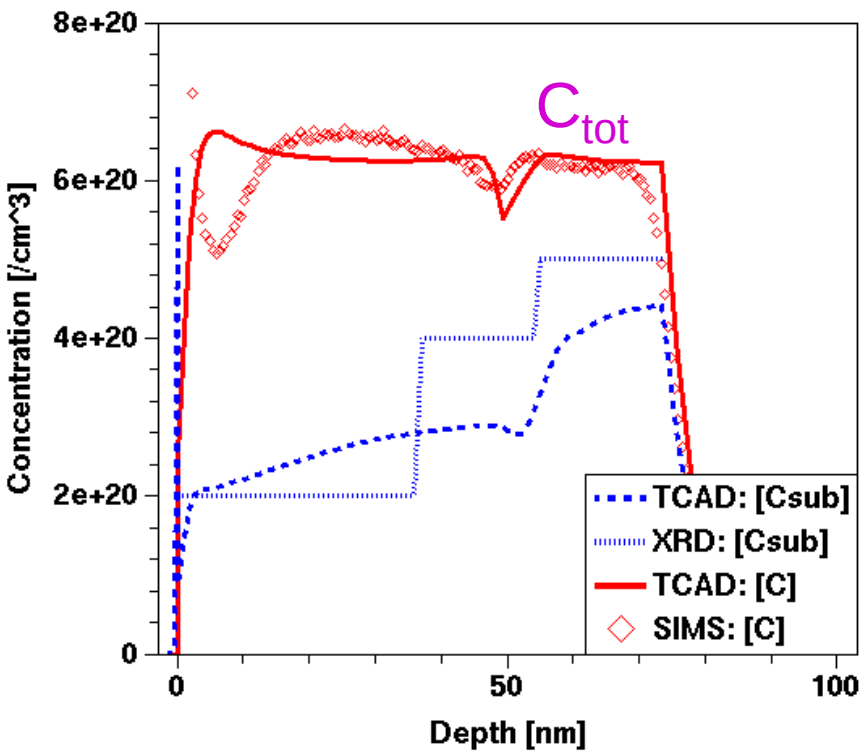


C_{tot} and C_{sub} Profile

P 12keV + 1050°C spike

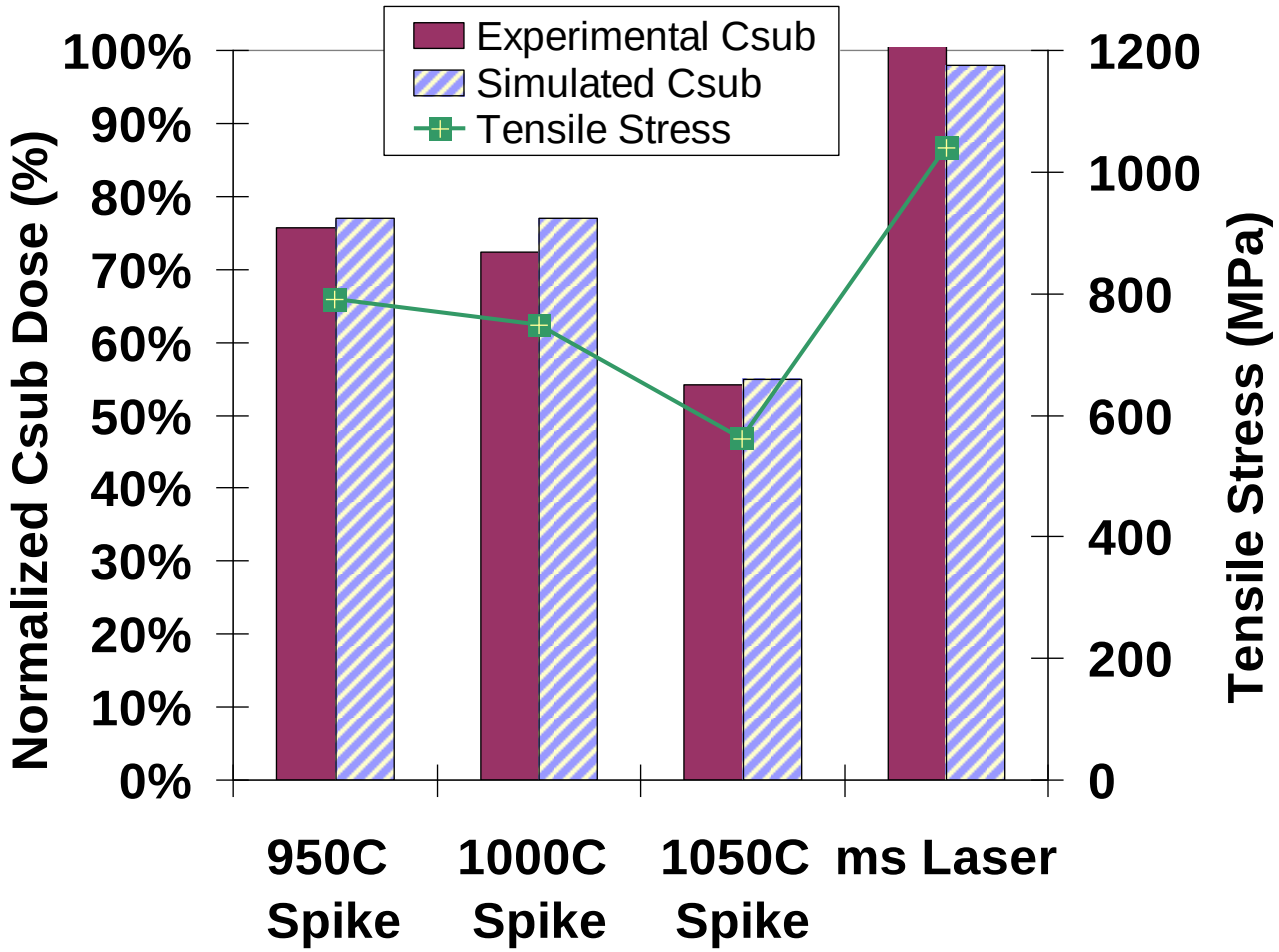


As 25keV + 1050°C spike



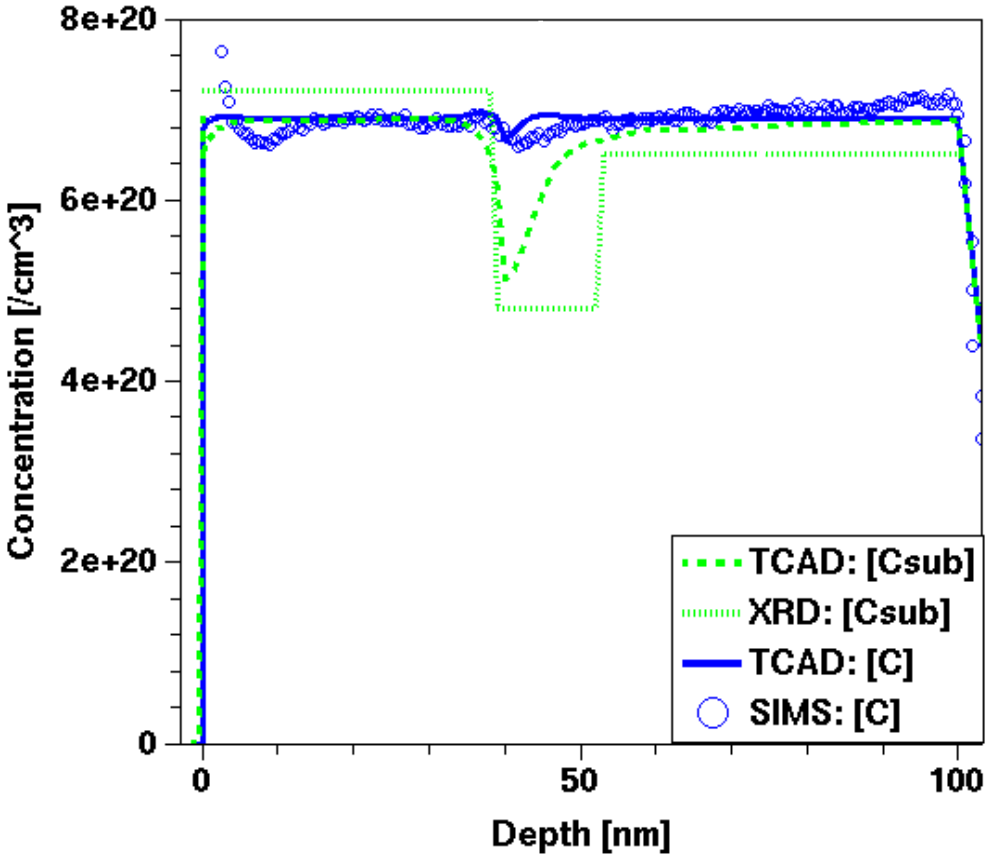
- C profile is predicted by model
- C_{sub} loss is evident in implanted layer

How To Keep the Fragile Si:C Stress?



Higher thermal budget anneal induces higher C_{sub} loss

C_{sub} Profile After ms Laser Anneal



Nearly 100% of Initial C_{sub} is recovered after ms anneal

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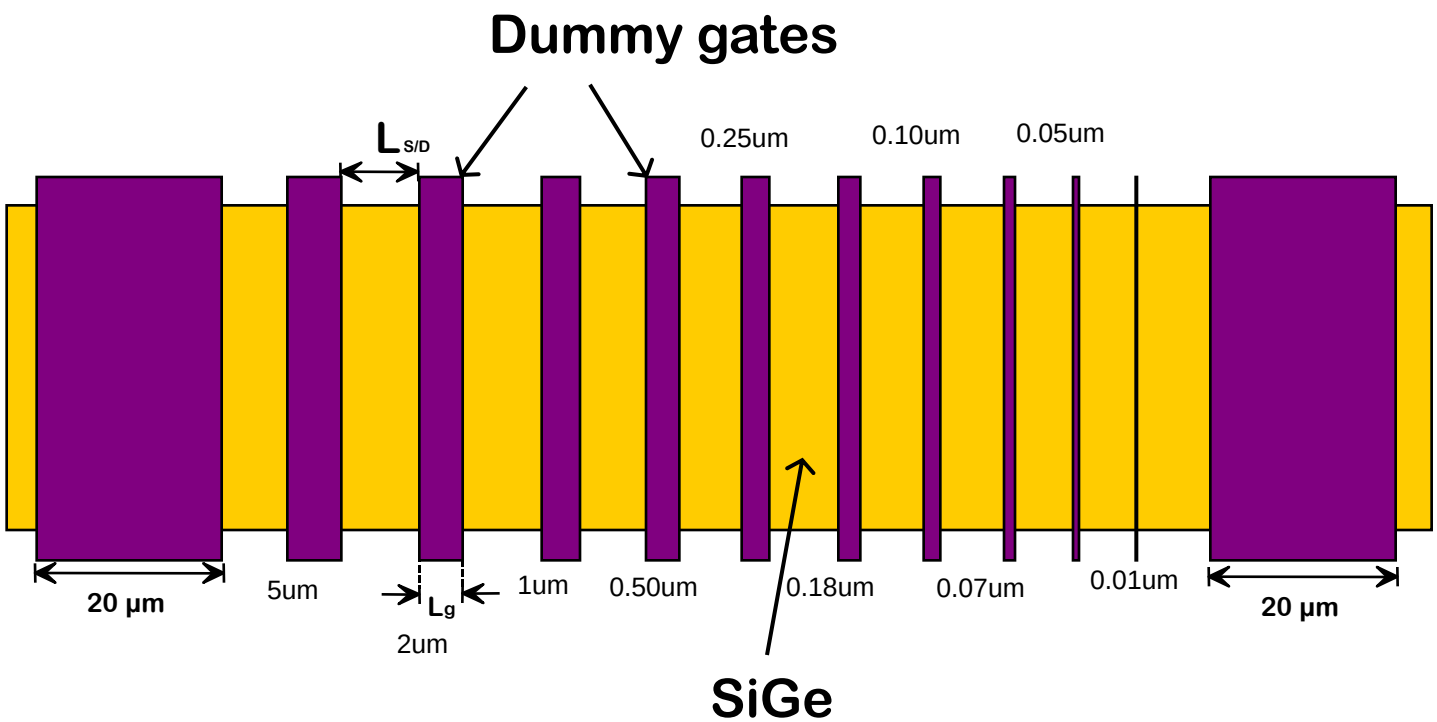
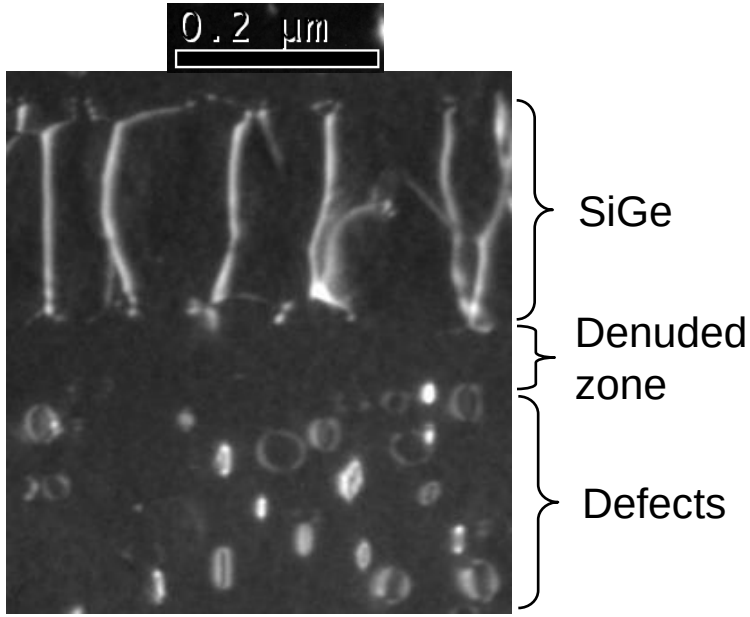
Experiments with the Si/SiGe Pattern



- Form stripes of 100 nm thick embedded SiGe with 20% Ge
- Implant 3e15 cm^{-2} As^+ @40 keV
- Anneal at 800°C or 900°C

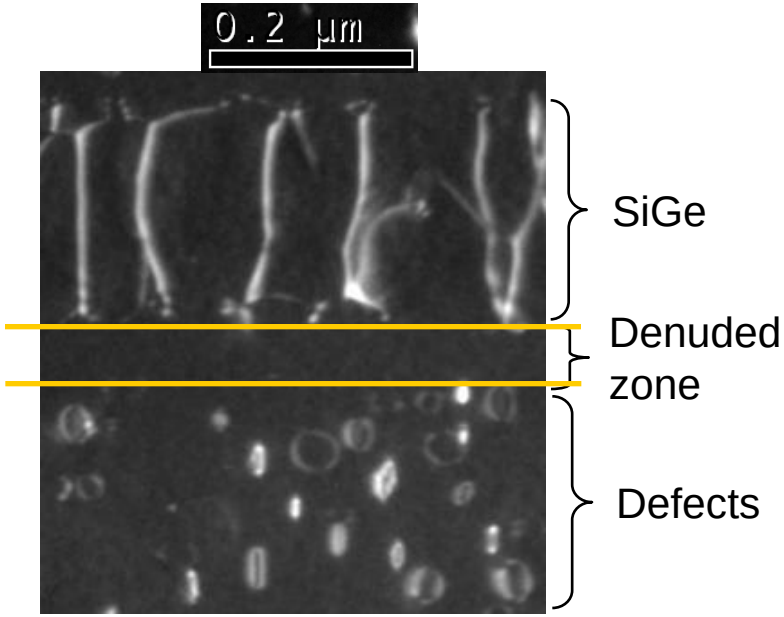
Plan View TEM: Narrow SiGe, Wide Si



10 s @900°C

V. Moroz et al., INSIGHT 2007

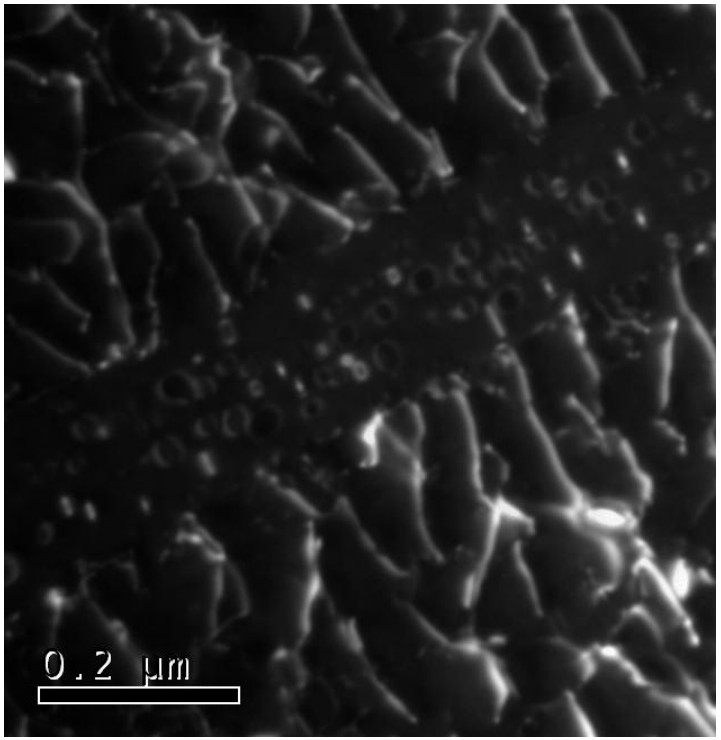
Plan View TEM: Narrow SiGe, Wide Si



10 s @900°C

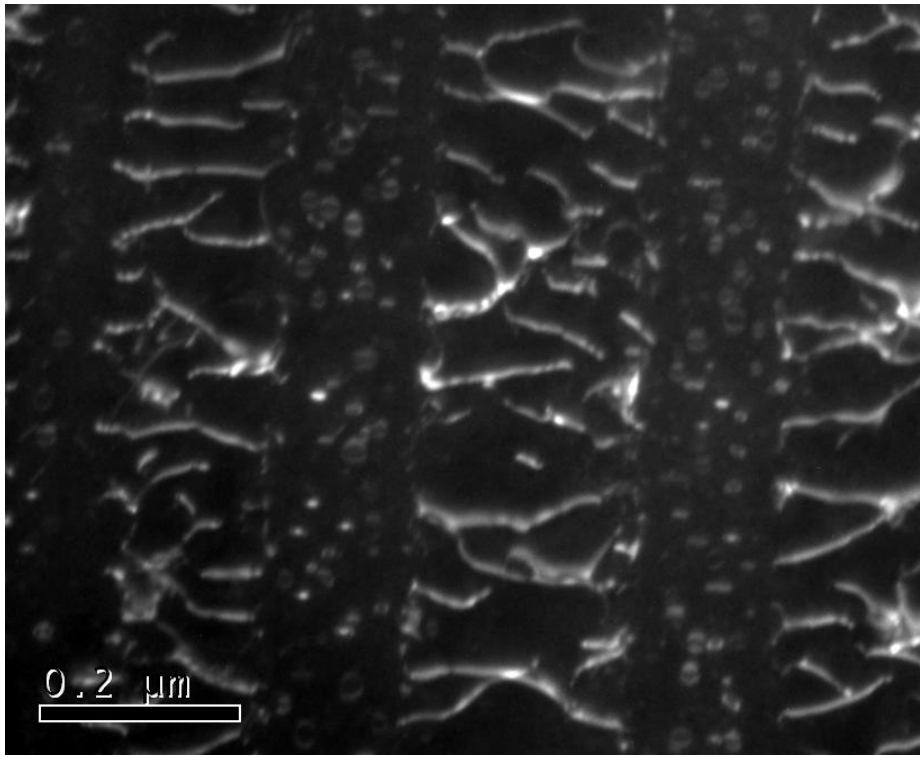
V. Moroz et al., INSIGHT 2007

Plan View TEM: Wide SiGe, Narrow Si



200 min @800°C

Plan View TEM: Narrow SiGe and Si



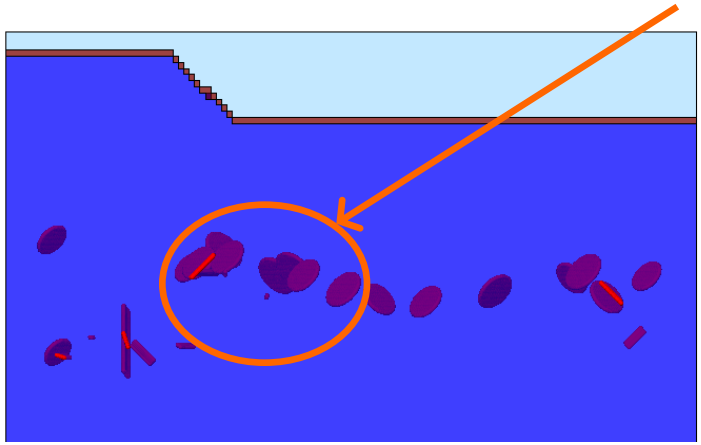
25 min @800°C

Assume That Tensile Stress is Favorable

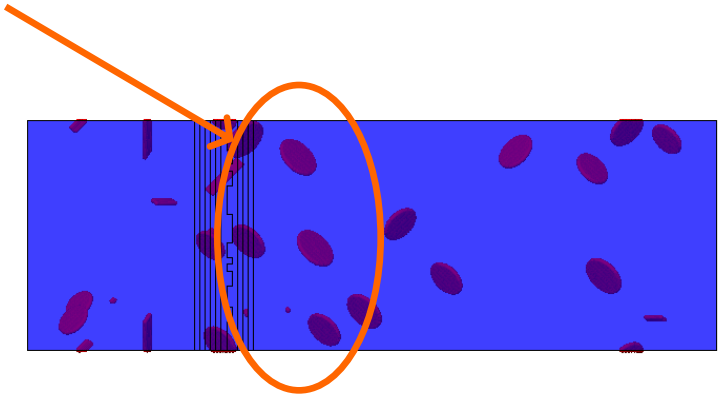
$$E_b = E_b^{relaxed} \exp(-P\Delta V / kT)$$

$$\Delta V = +0.02\, nm^3$$

Wrong behavior!



Side view



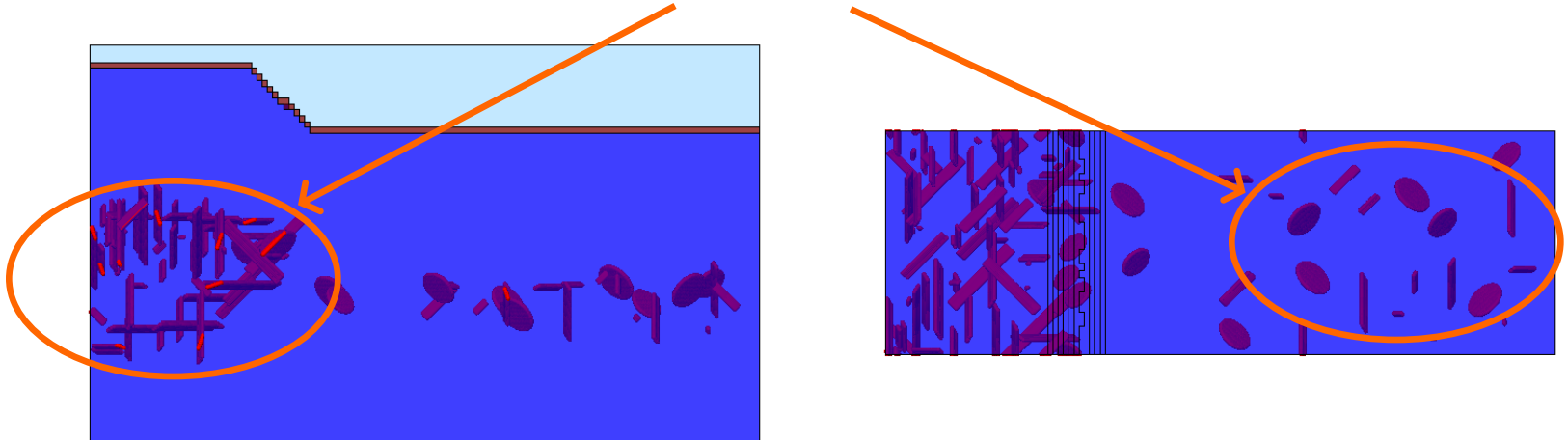
Top view

Assume Compressive σ is Favorable

$$E_b = E_b^{relaxed} \exp(-P\Delta V / kT)$$

$$\Delta V = -0.02\, nm^3$$

Wrong behavior!



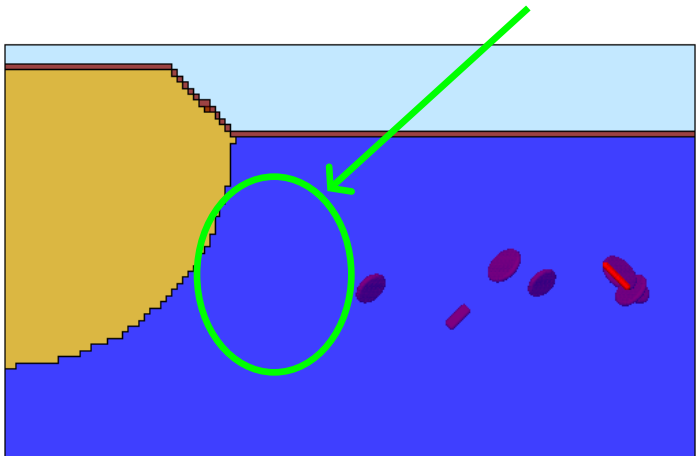
Side view

Top view

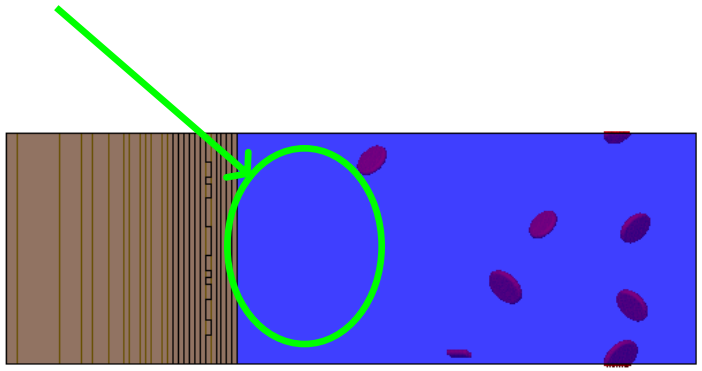
Assume I Recombination at Si/SiGe

Interstitials have non-zero recombination probability at the Si/SiGe interface

Correct behavior!



Side view



Top view

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- **Reliability**
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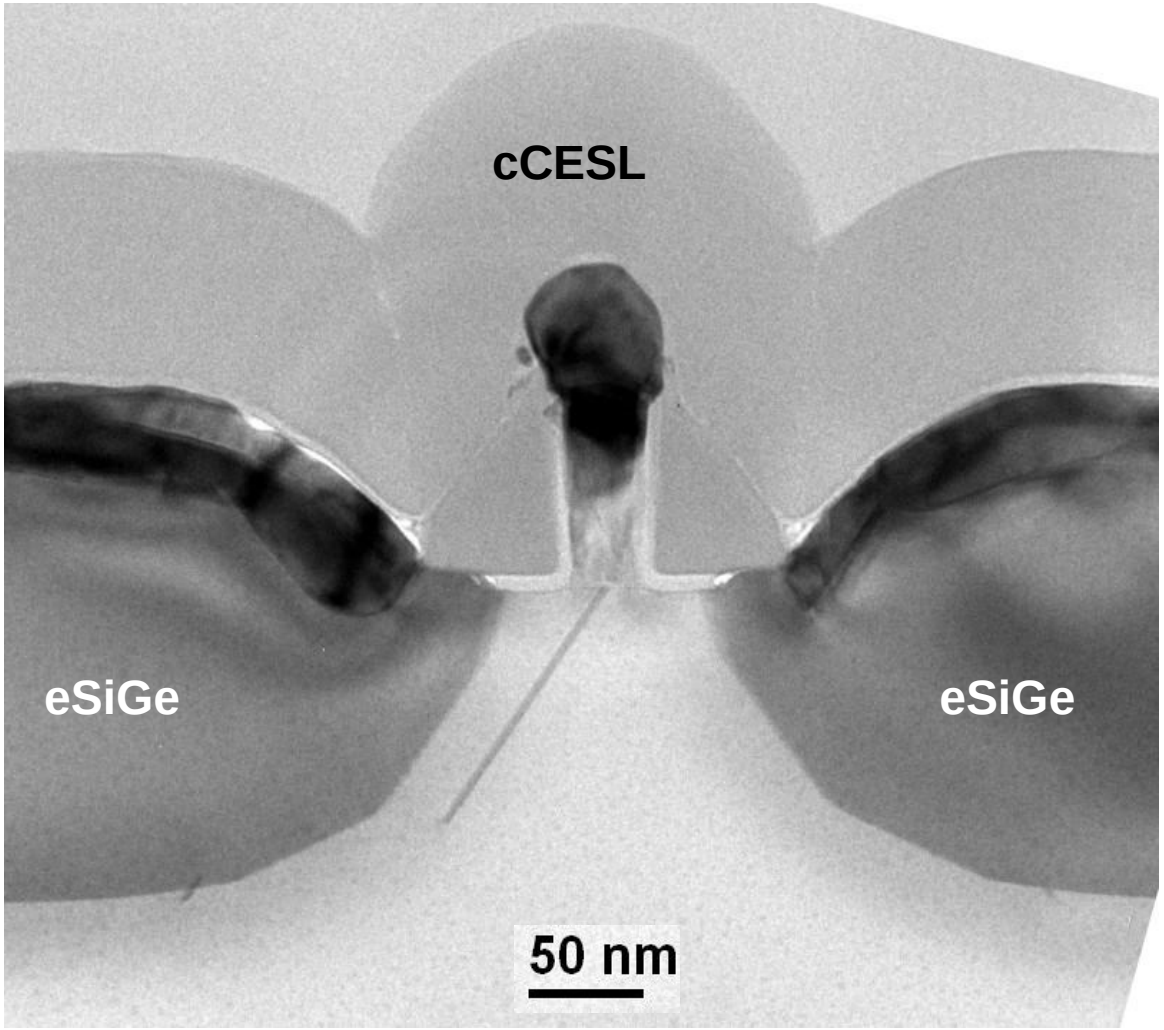
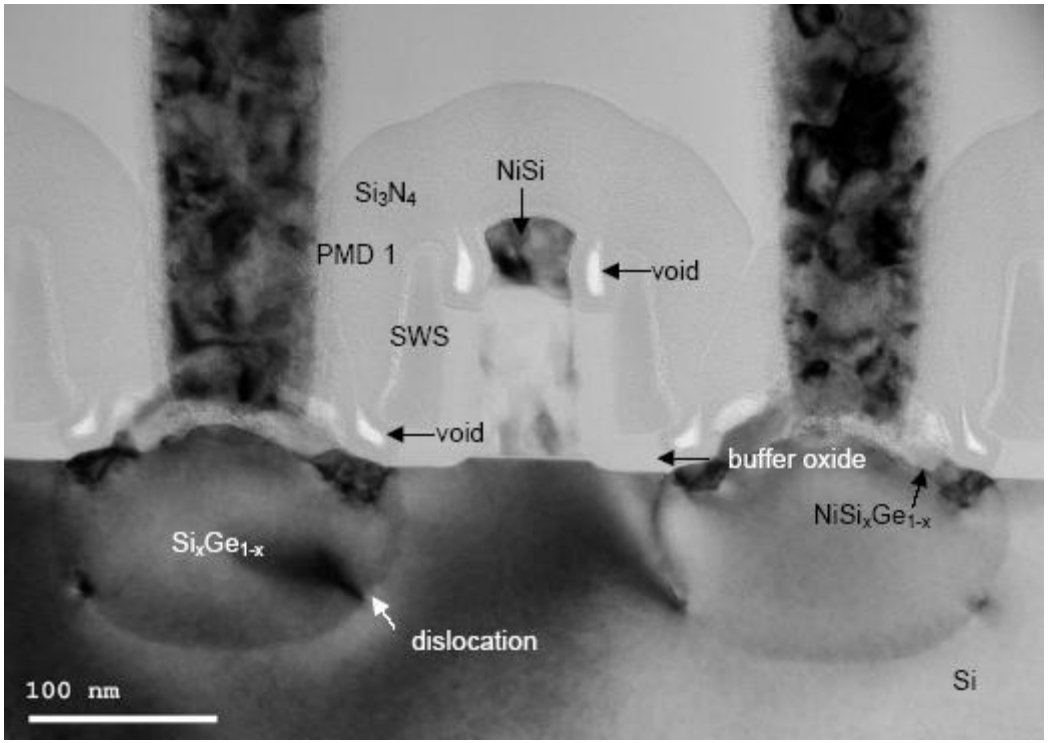
Stress-Induced Dislocations



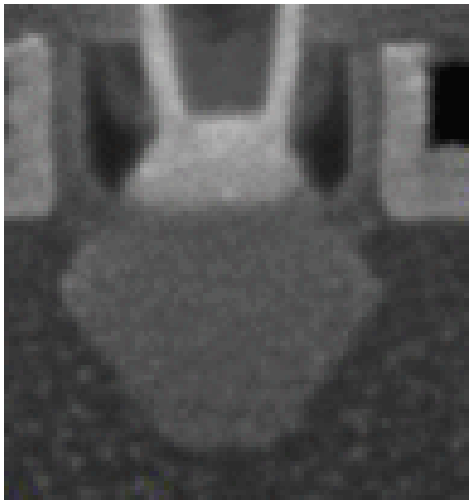
(111) vacancy disk squeezed out by eSiGe?

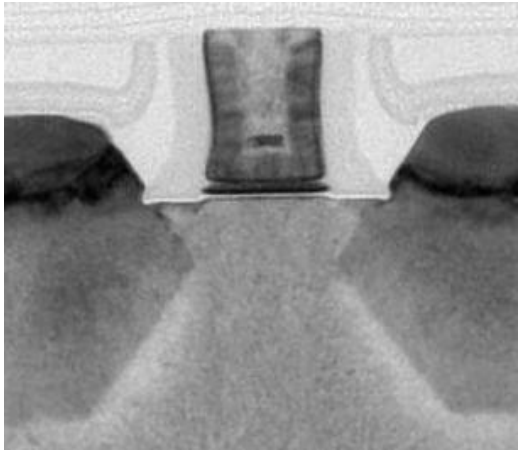
Stress-Induced Dislocations

90nm pMOS: full of dislocations



45nm dislocation- free pMOS





Is this due to (111) SiGe facets?

Impact of Stress on Transistor Reliability

Poly Gate

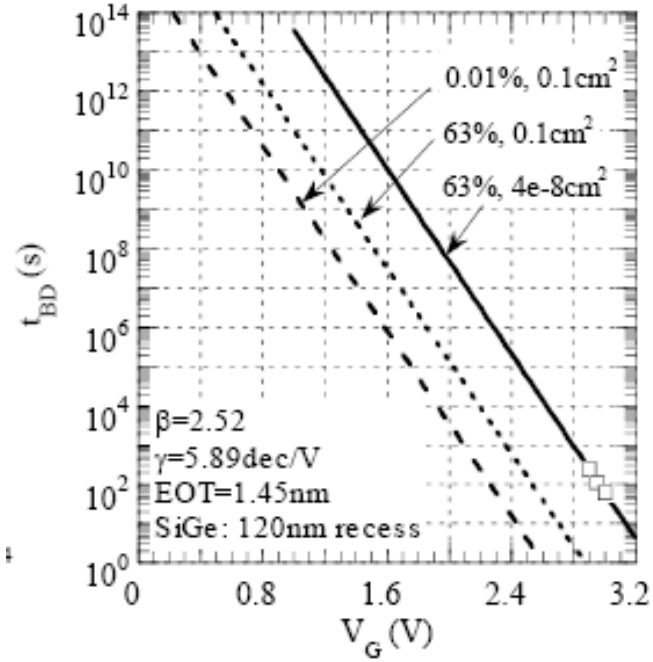


Fig. 16: TDDB time-to-breakdown vs. gate voltage for SiGe S/D transistors with 120nm recess depth and Area=4e-8cm²

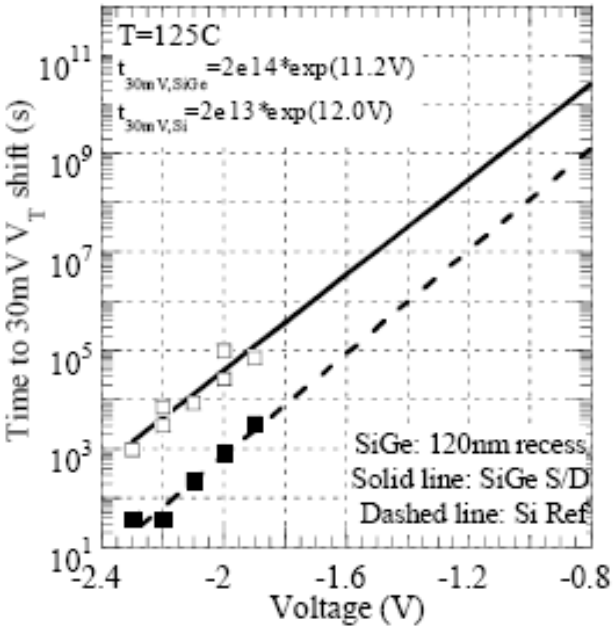


Fig. 17: Extrapolated time-to-30mV threshold voltage shift with W=1μm, L_{poly}=150nm, vs. applied voltage, obtained via NBTI measurements

G. Eneman et al., VLSI 2005

Impact of Stress on Transistor Reliability

High-K + Metal Gate

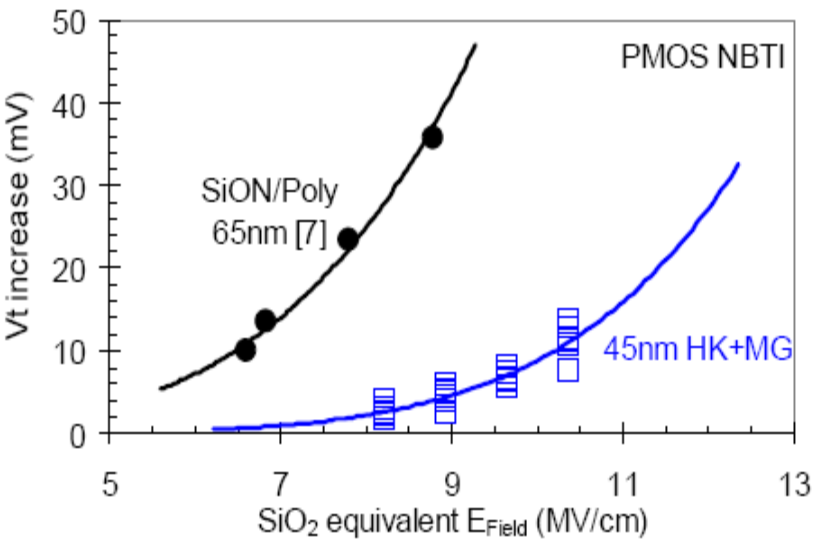


Fig. 14 PMOS NBTI V_T shift vs. electric field

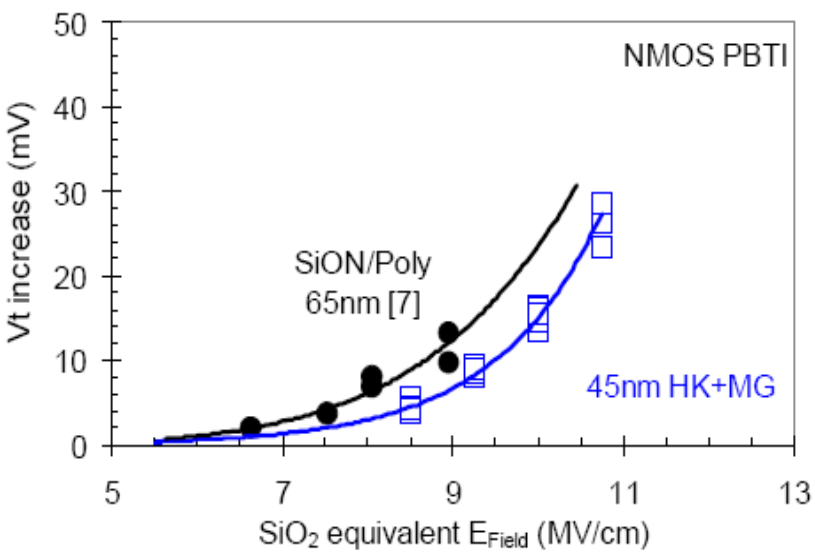


Fig. 15 NMOS PBTI V_T shift vs. electric field

K. Mistry, IEDM 2007

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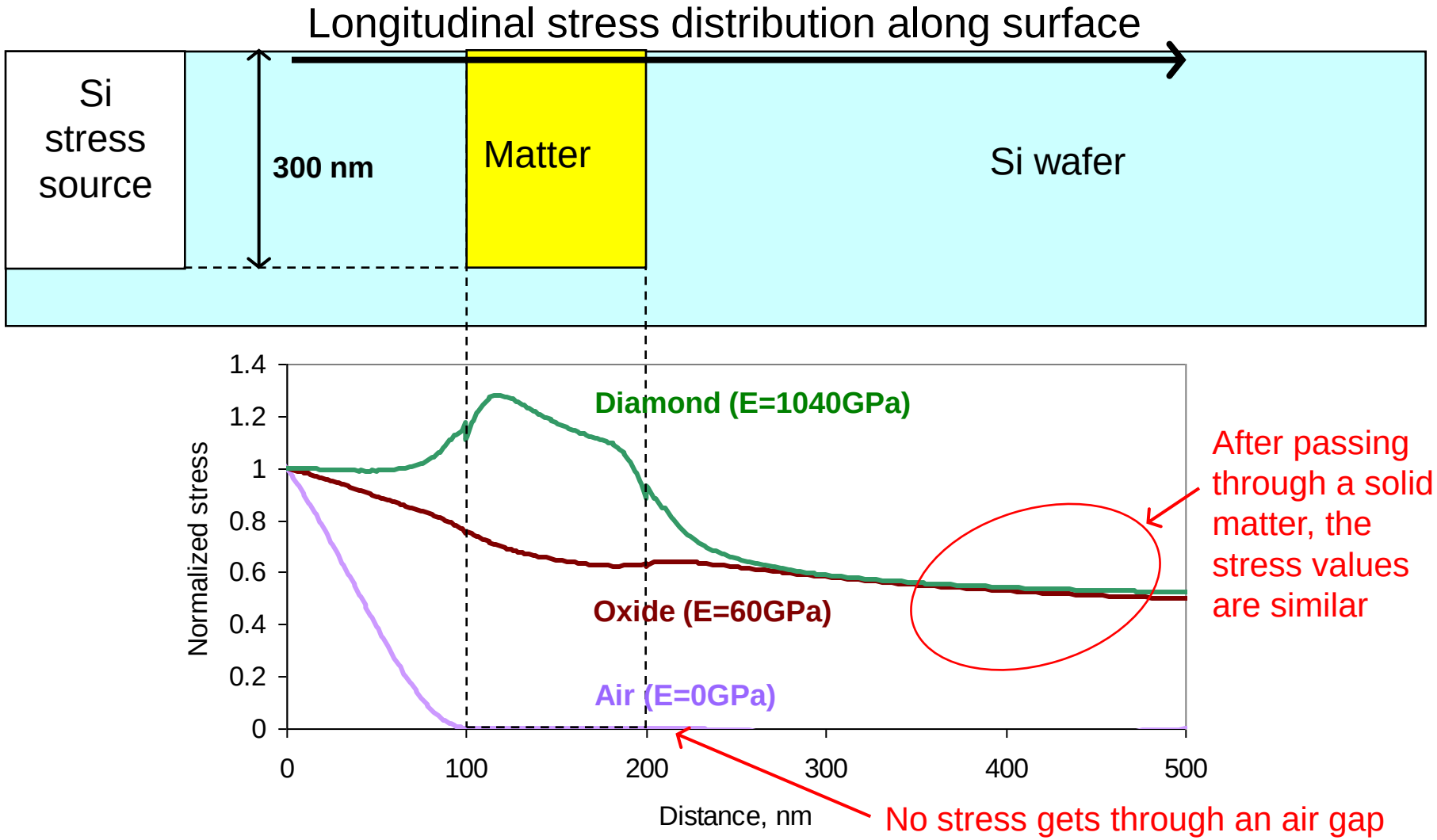
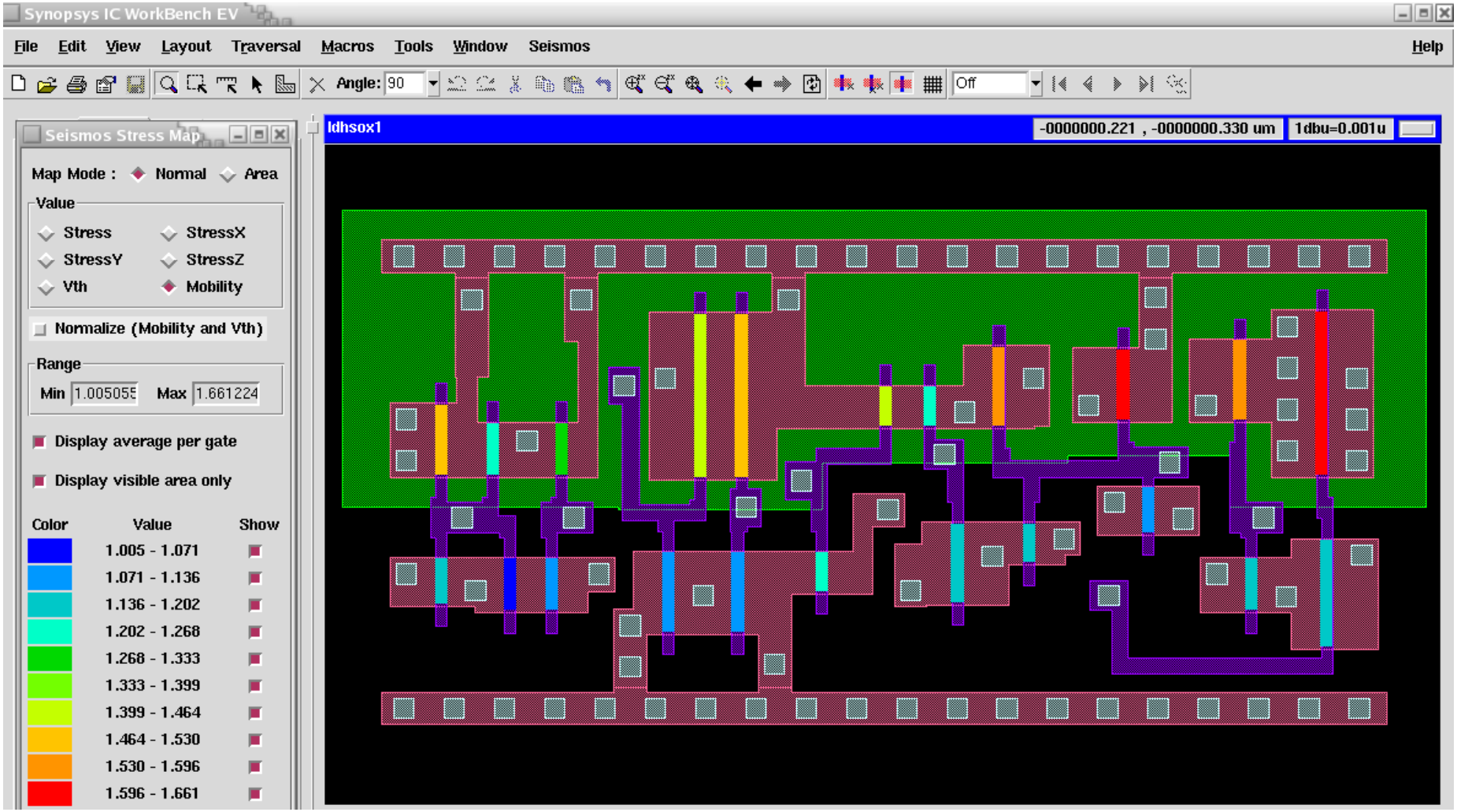
Stress Propagation Through Matter



Proximity Effects: Mobility +1% to +66%



Conclusions

- Reviewed the evolving stress engineering techniques
- Discussed millisecond annealing induced stress
- Analyzed interaction of carbon with stress and implant damage
- Discussed insensitivity of extended defects to stress
- Reviewed stress-related reliability issues
- Discussed stress proximity effects