Phase Change Memory: A Memory Technology for All Applications

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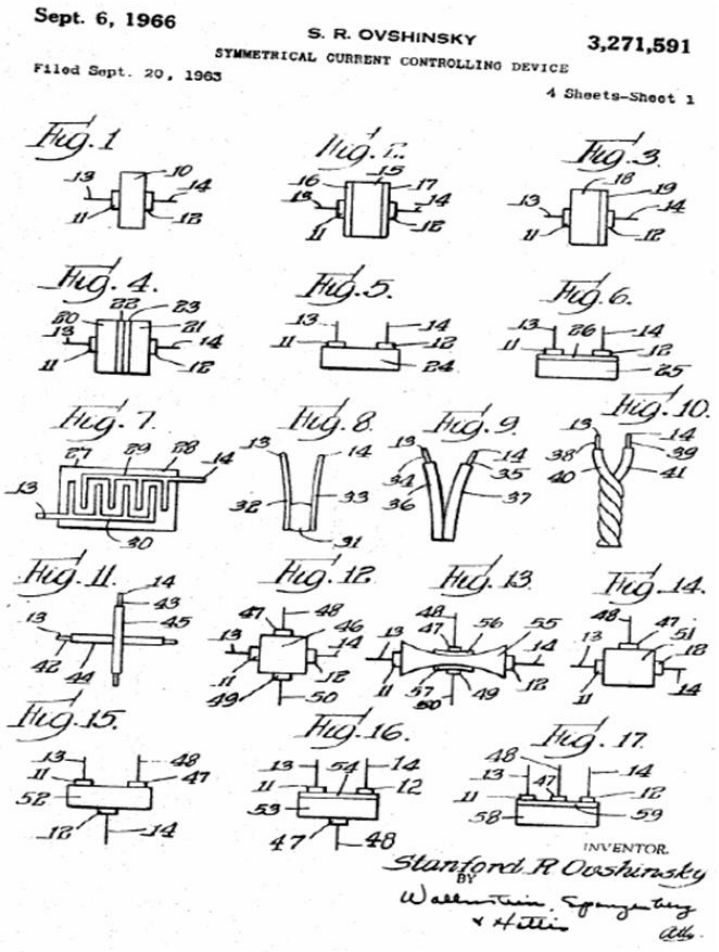
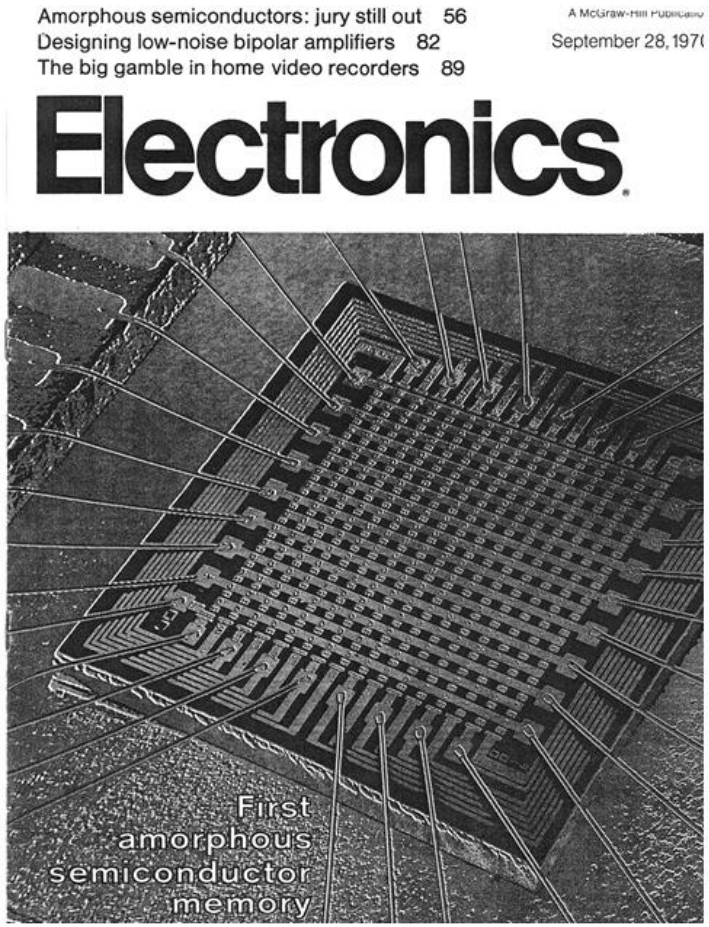
History of Phase Change Memory

The Concept



- Stan Ovshinsky first filed a patent on June 21, 1961 on the switching between high and low resistance states for electrical circuits.
- In the first granted patents 3271591, he demonstrated the many different ways the circuits could be fabricated.
- Reversible electrically induced changes in the resistance of thin films of chalcogenide alloy amorphous semiconductors were first reported in the technical literature in 1968.
  - S. R. Ovshinsky, Phys. Rev. Letters 21(1968) 1450.

One of the First Attempt



1970

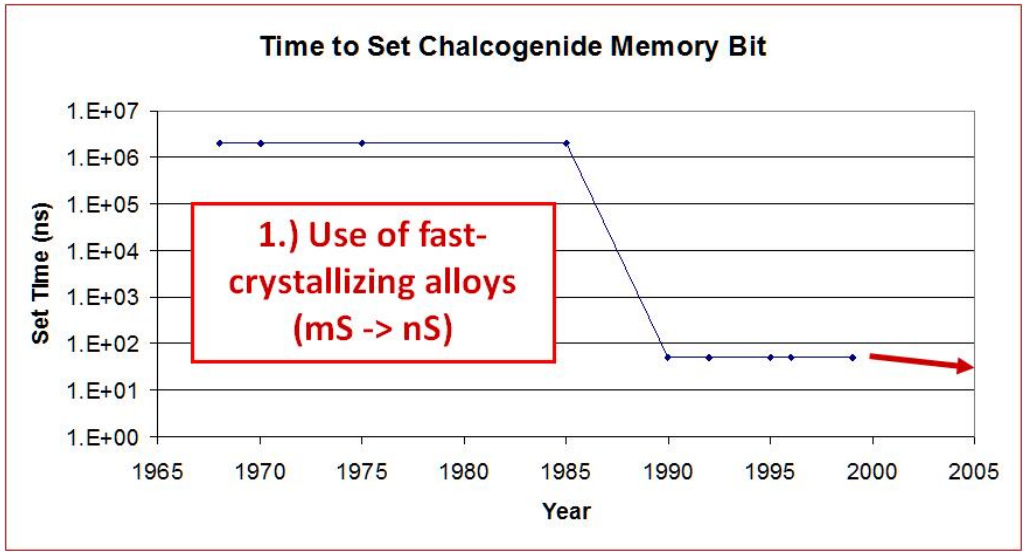
Die:	**122 mil X 131 mil**
Capacity:	**256 bits**
Reset:	**~200 mA, < 25V, 5 μs**
Set:	**5 mA, ~ 25V, 10 ms**
Read:	**2.5 mA, < 5V**

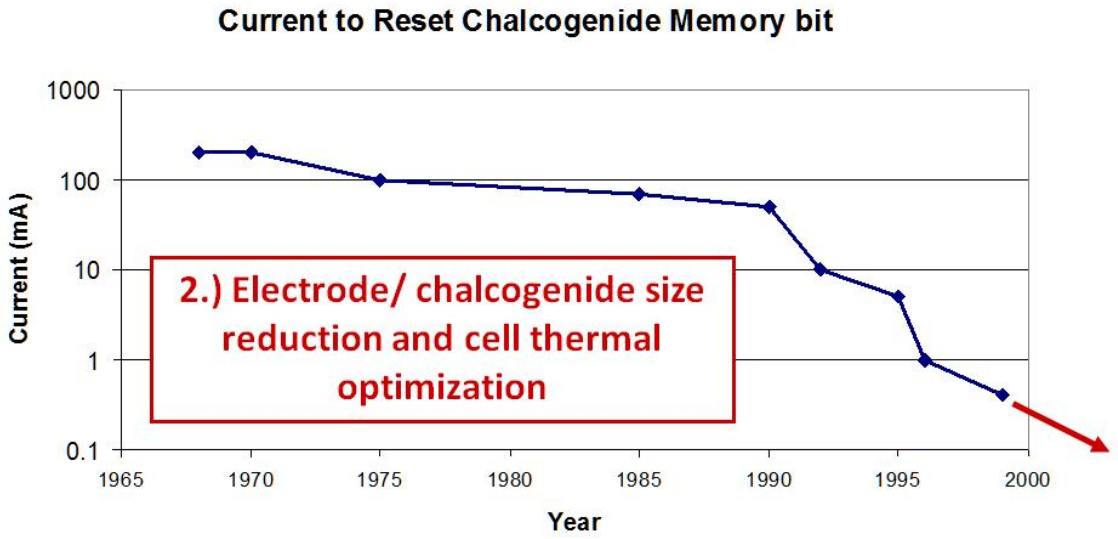
"Nonvolatile and Reprogrammable, the Read-Mostly Memory is Here," R. G. Neale, D. L. Nelson, and Gordon E. Moore, *Electronics* (Sept. 1970) p. 56.

Detour in Phase Change Memory

- With the large current and slow switching, phase change memory was not competitive with EPROM, and the semiconductor memory industry lost interest
- Optical memory application of laser-initiated reversible phase-change in chalcogenide alloy films was reported in 1971.
  - J. Feinlieb, S. Iwasa, S.C. Moss, J. deNeufville, and S.R. Ovshinsky, J. Non-Crystalline Solids, 8-10 (1971) 909.
- In the 80's and 90's, there was intense effort in Japan for development of RW CD/DVD which perfected the GST material
- In 1999, Ovonyx was founded to take a fresh look at the new material in electrical memories

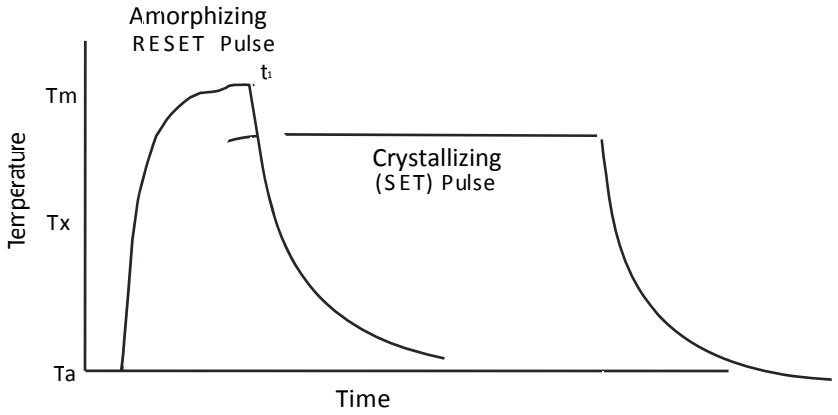
Progress in Phase Change Memory

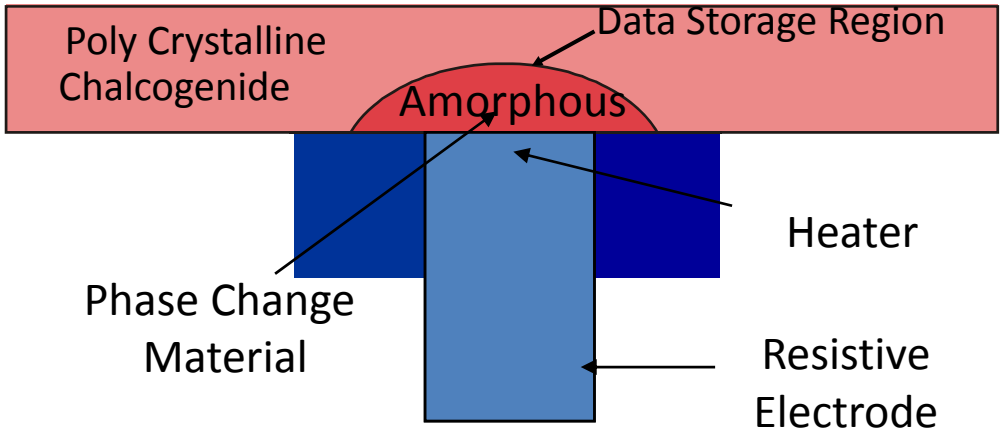




Phase Change Memory Capability

Basic Memory Concept





Amorphous Phase *Crystalline Phase*

TEM Images

Electron Diffraction Patterns

- Short-range atomic order
- Low free electron density
- High activation energy
- High resistivity

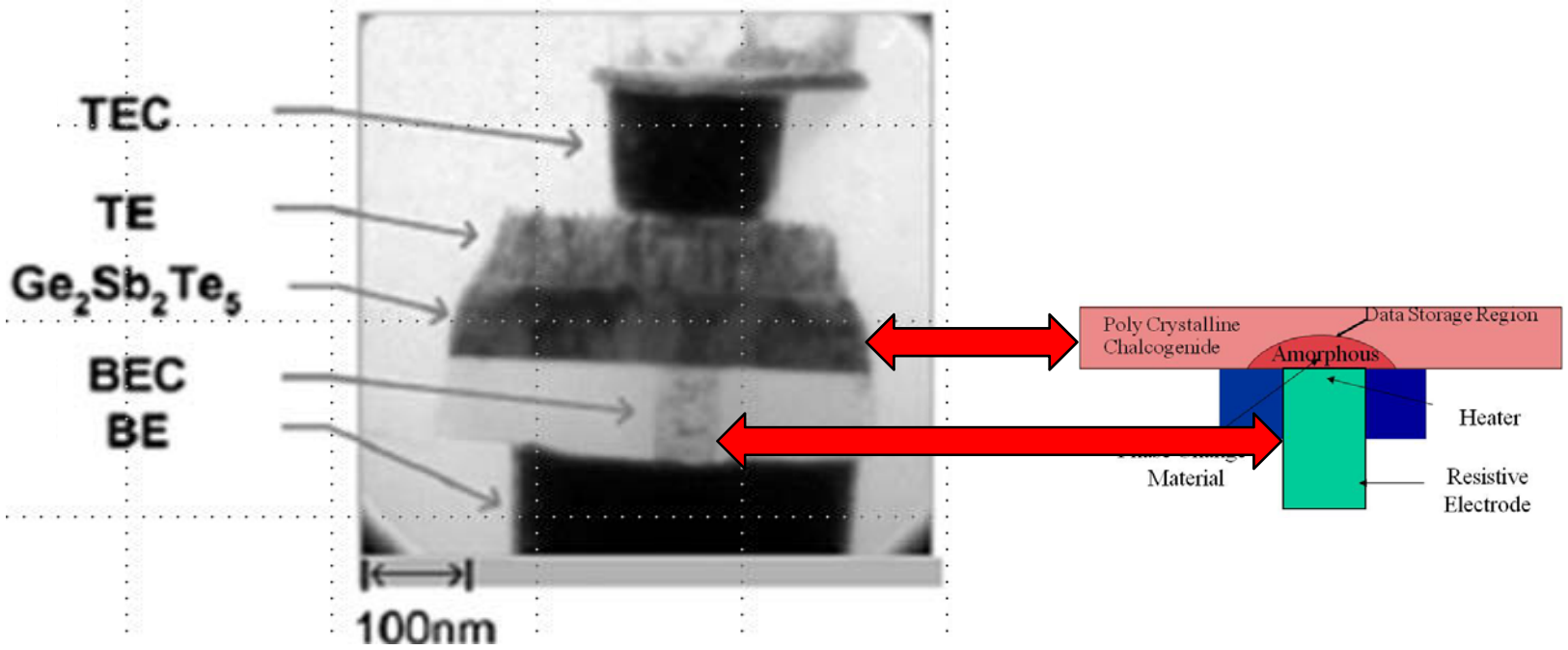
- Long-range atomic order
- High free electron density
- Low activation energy
- Low resistivity

- **Operation**
  - Chalcogenide material alloys used in re-writable CDs and DVDs
  - Current provides heat that converts the material between crystalline (conductive) and amorphous (resistive) phases
- **Attributes**
  - Non-volatile & high density
  - Direct fast write & bit alterable
  - ~10^{12} write/erase cycles
  - Non-destructive fast read
  - Low voltage operation
  - Integrate-able w/ CMOS logic

Technology Capability

- Direct write capability (no erase before write) as well as byte function (no block flash erase) makes it RAM like, easing significantly system implementation
  - For flash, changing a byte involves saving the current data, erasing a whole block (>100 mSec) and writing back old data + new byte (total ~1 sec)
  - For PCM, changing a byte involves writing the new data: (total < 100 nSec, can be less than 50 nSec with new alloy)
  - Endurance >> 10^8 cycles
- With read current > 10 μA, read speed is expected to be comparable to NOR and DRAM

Basic Memory Element

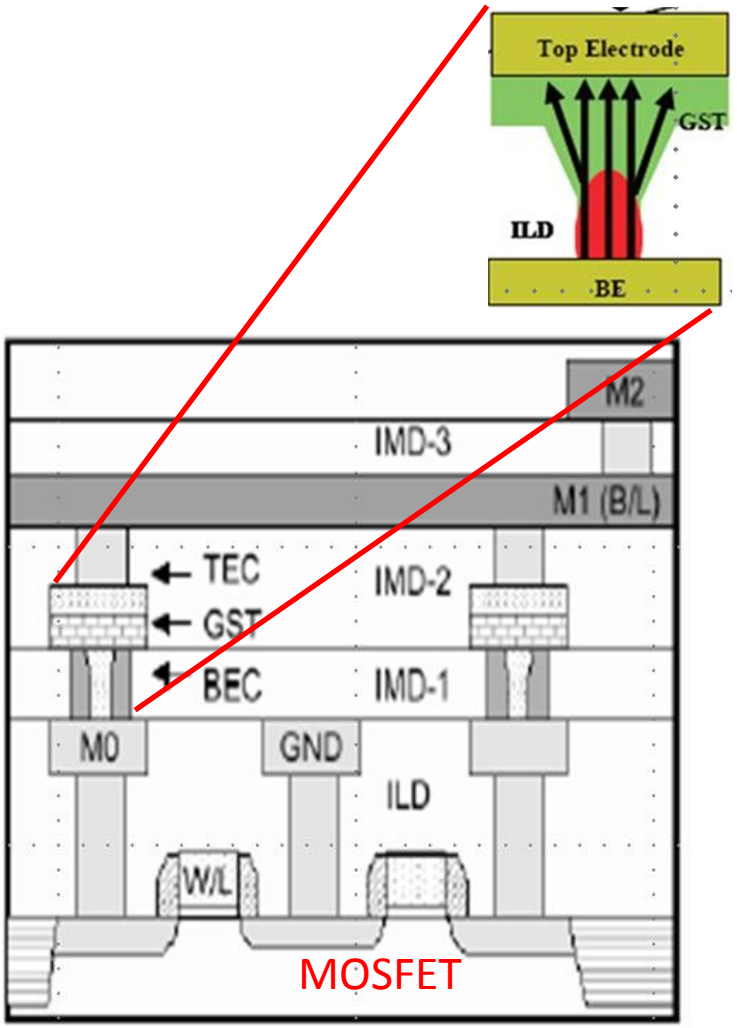


- Memory cell = memory element (variable resistor) + selector
- Selector can be MOSFET, BJT, Diode or other switches

A Memory For Everybody

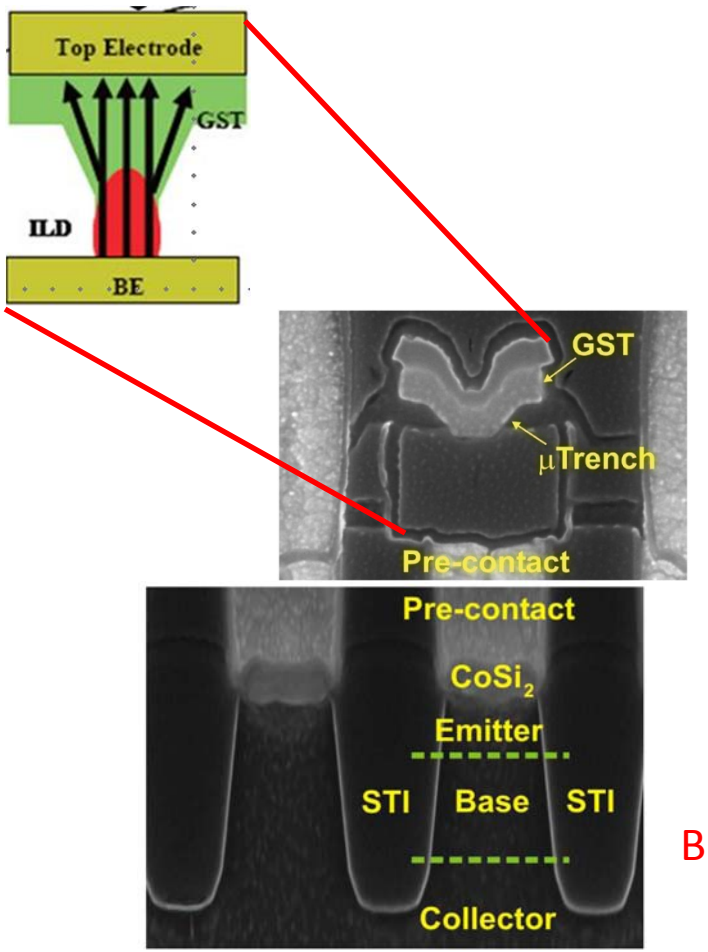
- Even though Phase Change Memory is not an universal memory in all respects, it comes close to an universal memory on how it can be used
- For embedded with the smallest amount of process change, one can get a high cycle EEPROM equivalent at lower cost.
- By using the same process but changing the alloy, one can get a high temperature memory suitable for the most demanding automotive application
- For dedicated high density memory, one can get a memory cell that is smaller than DRAM and has multi-level cell capability. Using high performance alloys, programming speed similar to DRAM are available.
- Using special switched selectors, one can get multi-layer memory than can rival NAND memory in cost

Embedded Memory



- Standard CMOS
- Add PCM element above contact
- Continue with normal metal layers
- Low operating voltage (~3V) simplifies based CMOS requirement
- Cell size ~ 20 λ^2

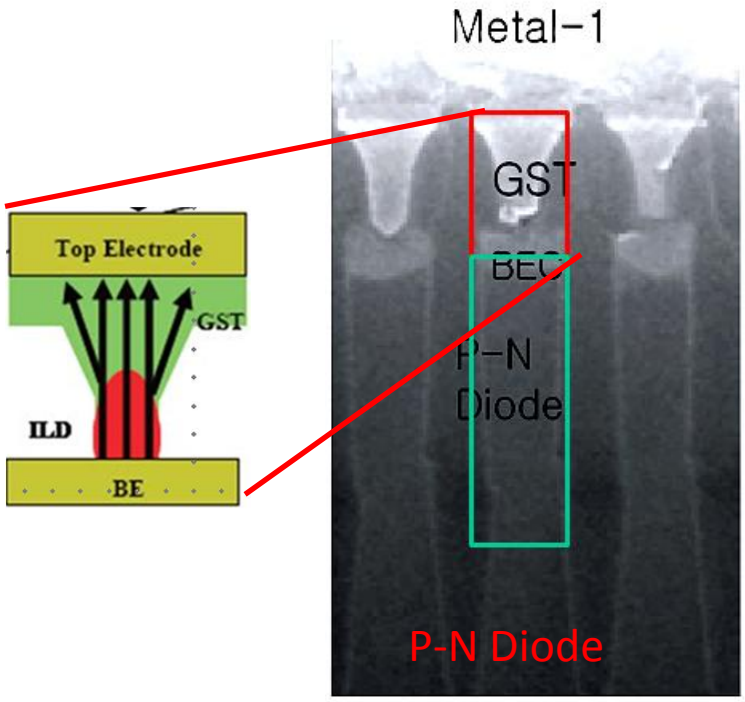
NOR Replacement



- BiPolar select diode smaller in area but more special process
- Can carry more current
- Cell size ~10 λ^2

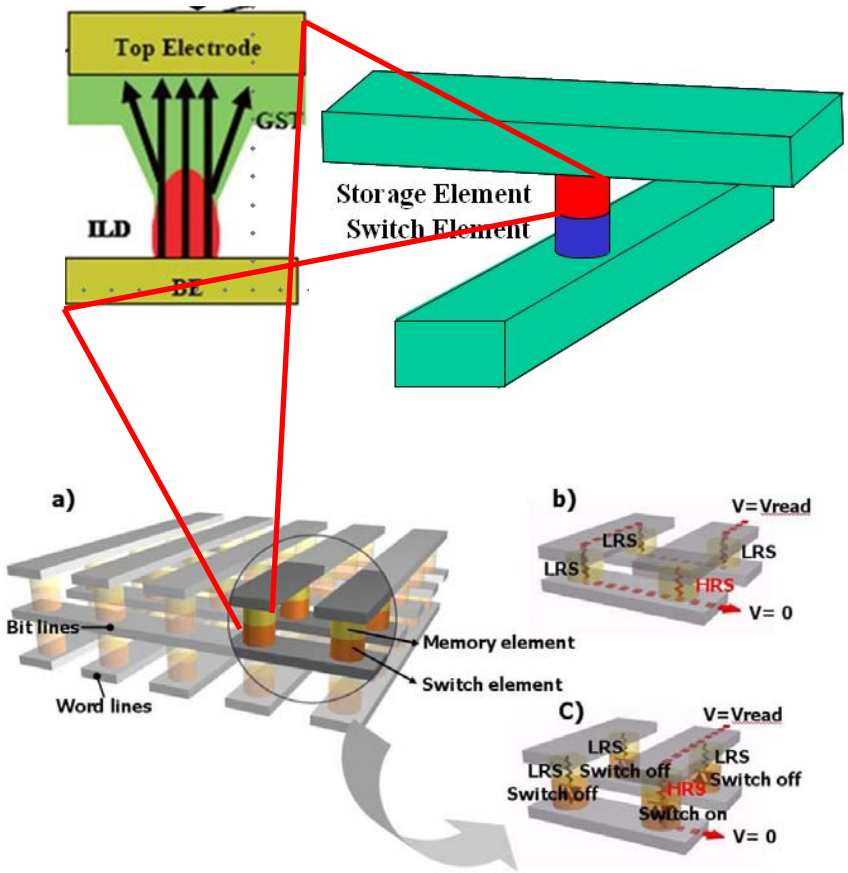
BiPolar select diode

DRAM Cost



- Epitaxial PN diode smaller in area, special process and circuits
- Carry more current
- Cell size < 6 λ^2

Multi-Layer Memory



- Thin film PN diode or selector allows stacking of memory layers
- Cell size 4 λ^2/ N layer
- Together with multi-level capabilities: lowest cost memory rivals NAND

Intel / STM PCM Demonstration

Intel and STMicroelectronics demonstration of a 128-Mbit, 90-nm phase-change memory in use with a mob phone to the Mobile World Congress at Barcelona, Spain.
Reproduced from EE Times Europe, February 18, 2008

Samsung 512 Mb

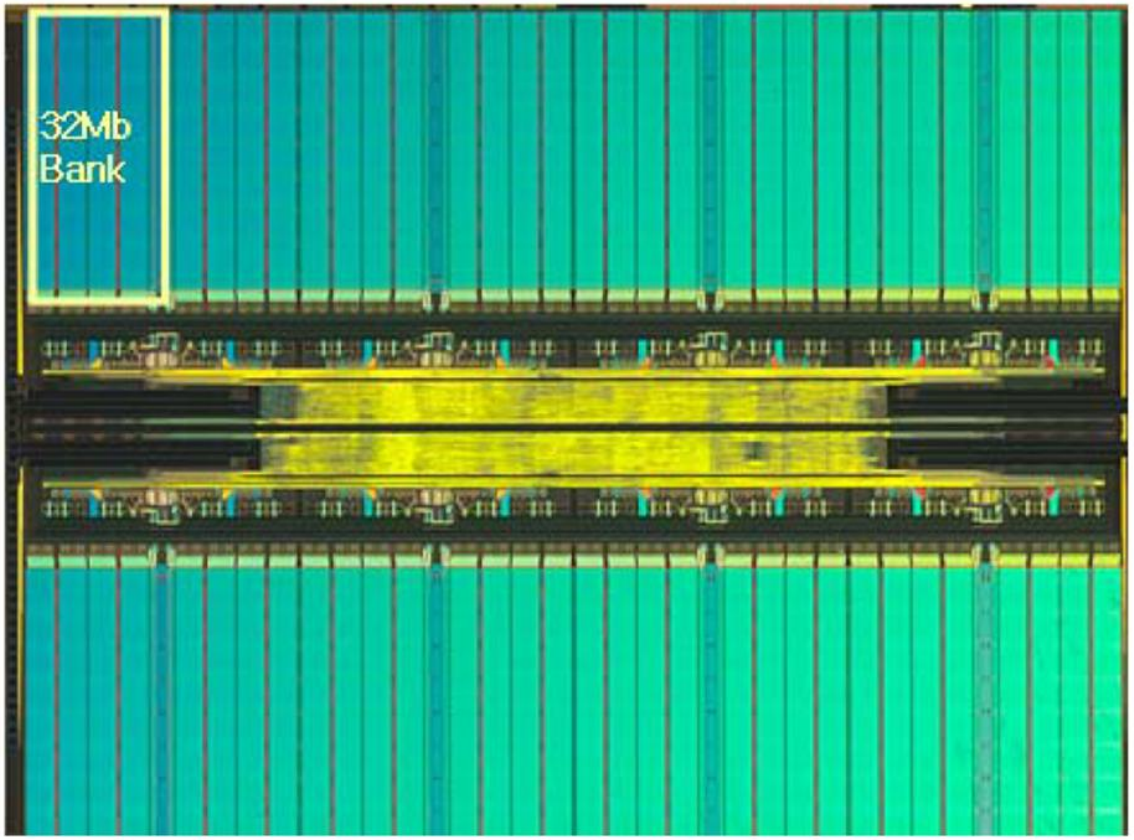


Figure 2. A photograph of 512Mb PRAM chip.

J. Oh et al, “Full Integration of Highly Manufacturable 512Mb PRAM based on 90nm Technology”, IEDM Tech Digest, 2007.

Scalable Diode Select Cell

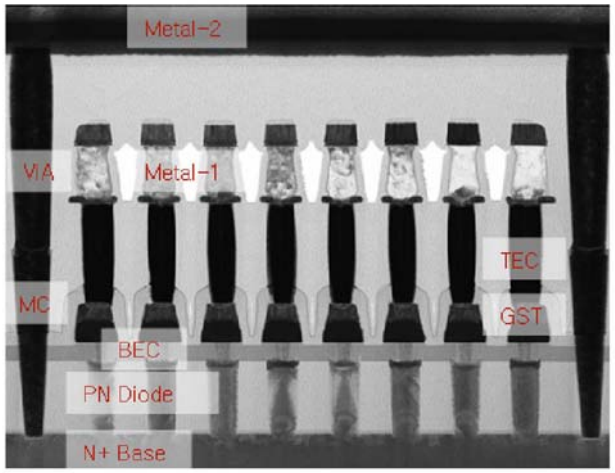


Figure 3. Vertical view of a 512Mb PRAM cell array.

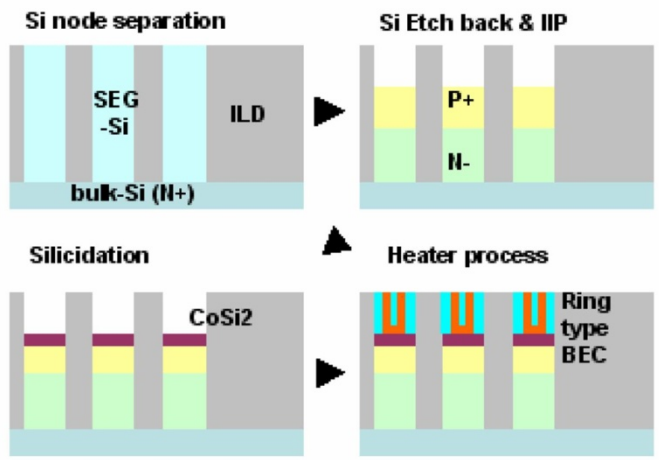


Figure 5. Schematic diagram of process sequence for vertical diode and SABEC.

- Samsung has demonstrated a 5.8 λ^2 memory cell using selective epi diode as selector.
- The simple memory cell structure scales directly with lithography

J. Oh et al, "Full Integration of Highly Manufacturable 512Mb PRAM based on 90nm Technology", IEDM Tech Digest, 2007.

Samsung PCM Roadmap

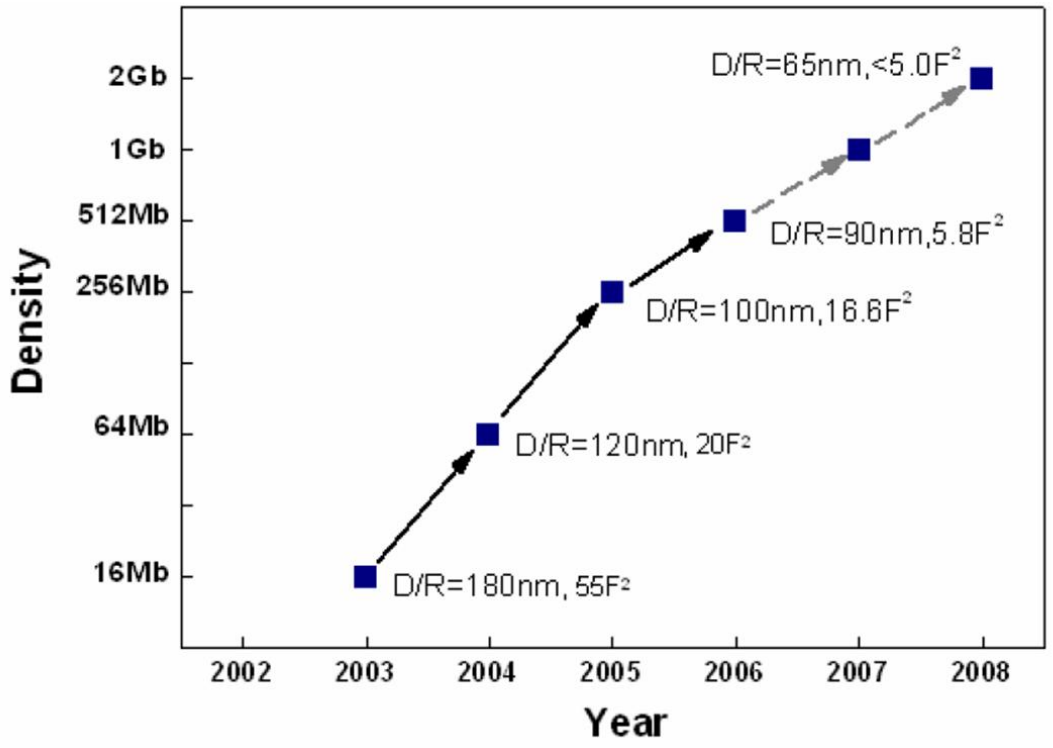


Figure 1. PRAM development roadmap with design rule and unit cell size.

J. Oh et al, "Full Integration of Highly Manufacturable 512Mb PRAM based on 90nm Technology", IEDM Tech Digest, 2007.

Confined Cell

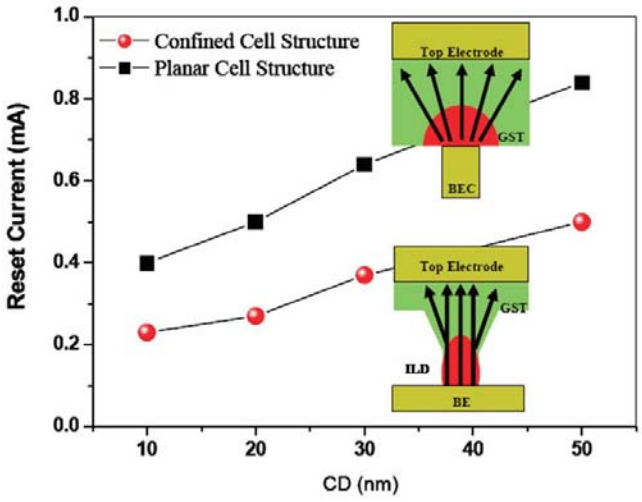


Fig.1 Comparison of reset current between confined and planar cell structure along with contact diameter [Ref 2].

- Samsung has reported that by confining the GST into the pore, the reset current is reduced by ~50%
- It also reduces the horizontal spread of the heated region, further facilitating scaling
- Integrated with a diode, the cell structure is highly scalable

J. Lee et al., "Highly Scalable Phase Change Memory with CVD GeSbTe for Sub 50 nm Generation", 2007 Symp on VLSI Tech, pp 102.

TEM of Confined Cell + Diode Select

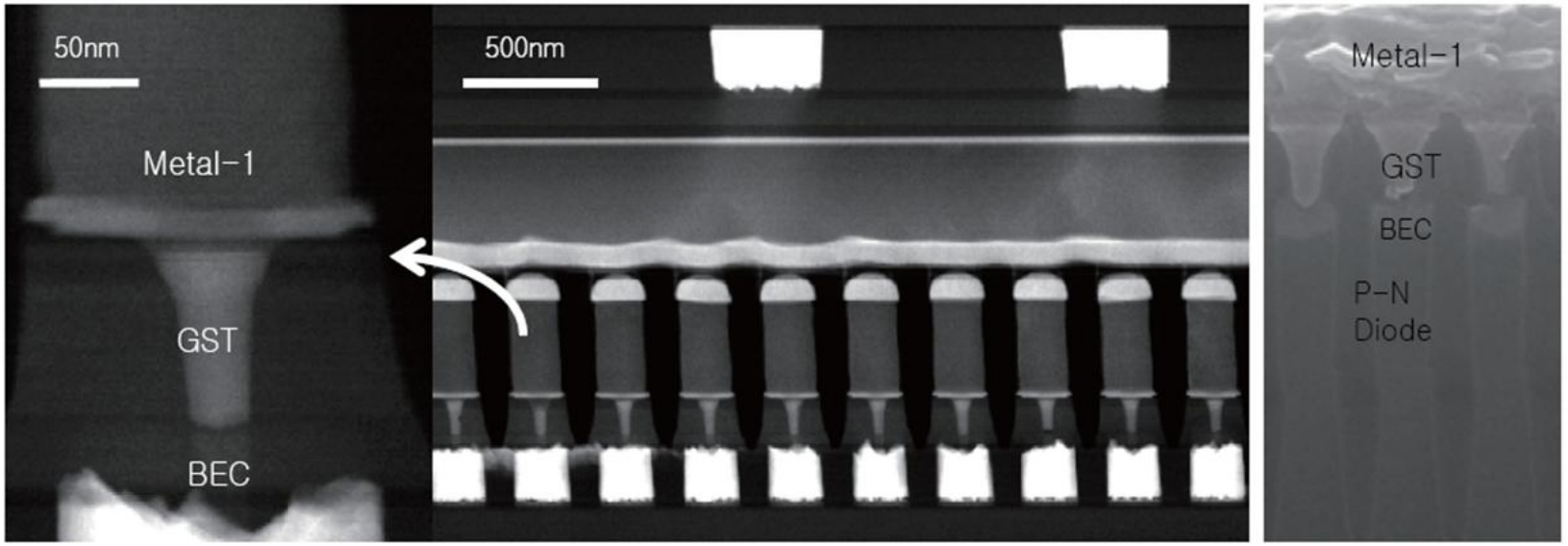


Fig.11 (a) Magnified TEM images of GST on 50nm contact device, (b) SEM image of fully integrated confined cell structure on diode.

Simple Cell Layout

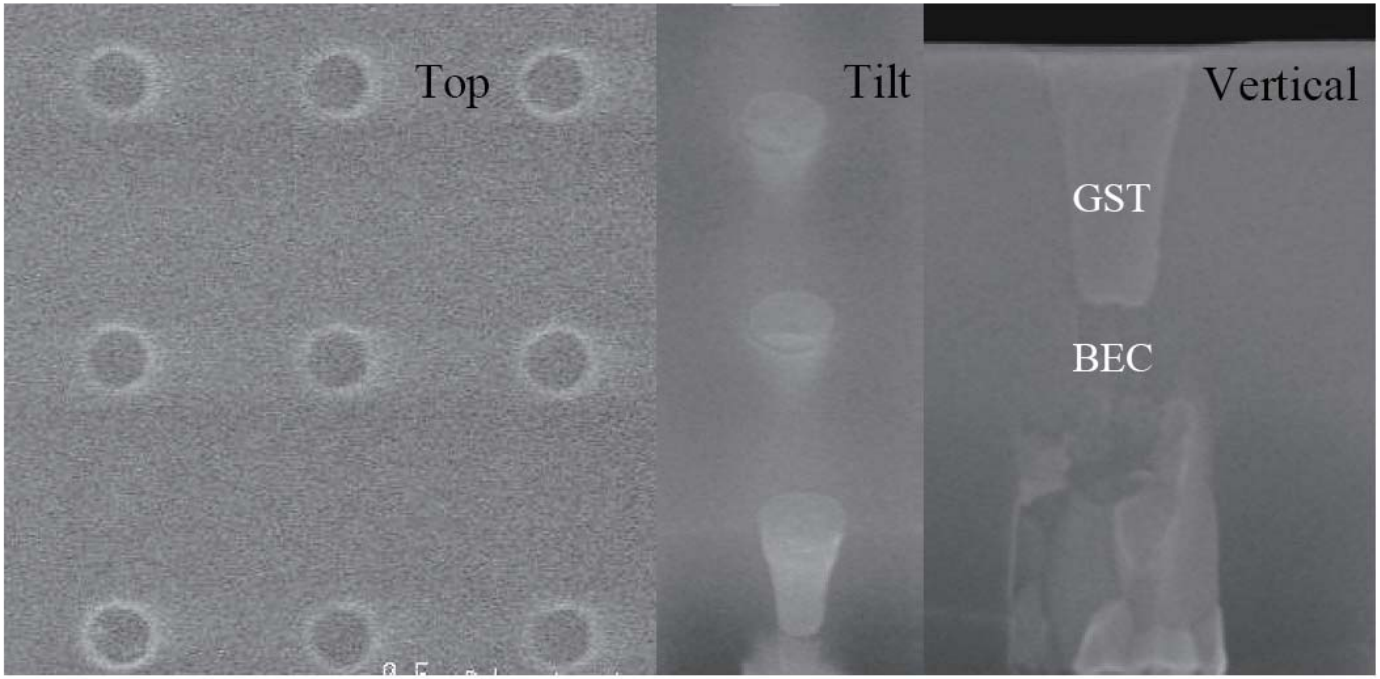
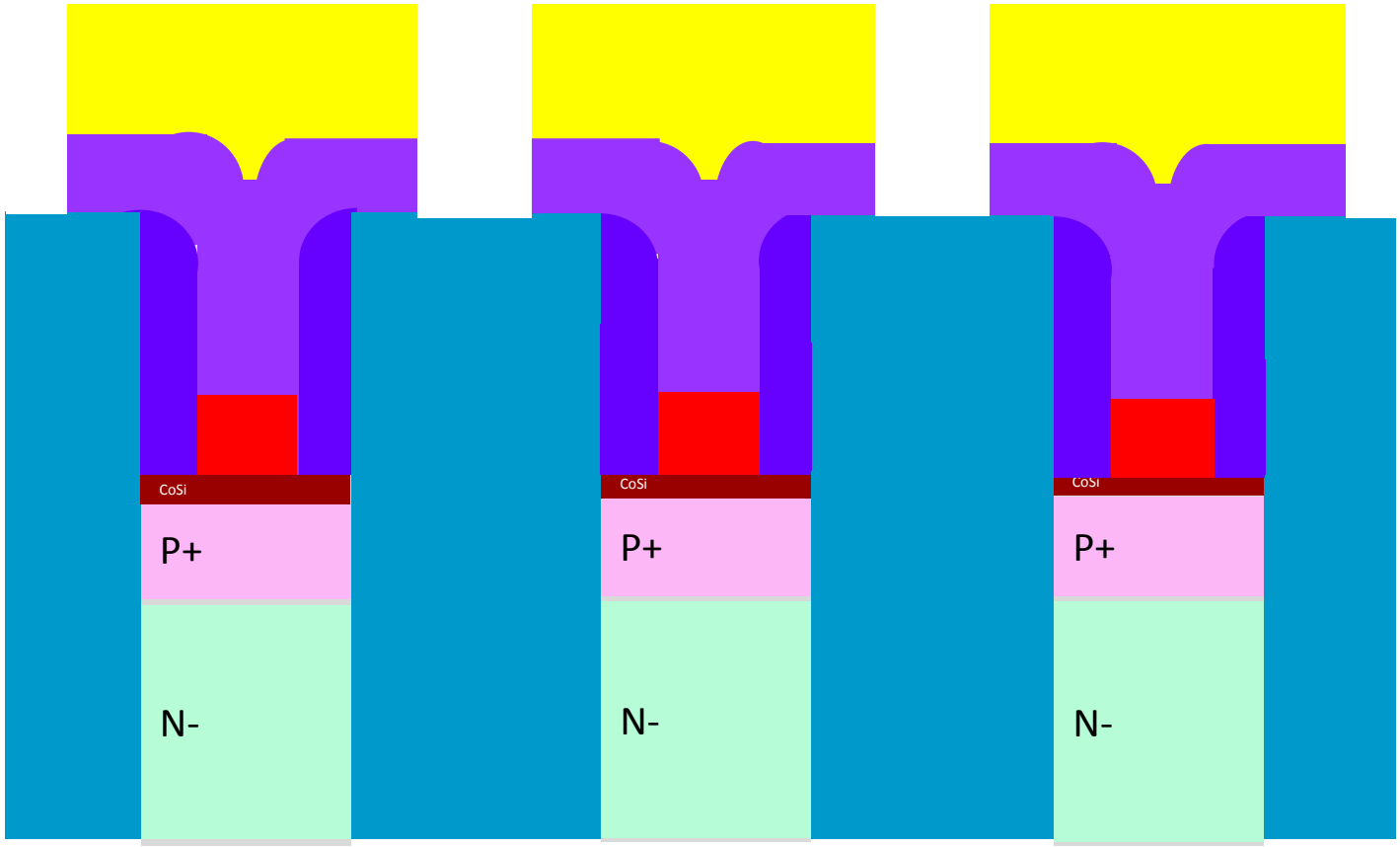


Fig. 6 Top, tilt, and vertical SEM images after CMP.

Technology Enabler

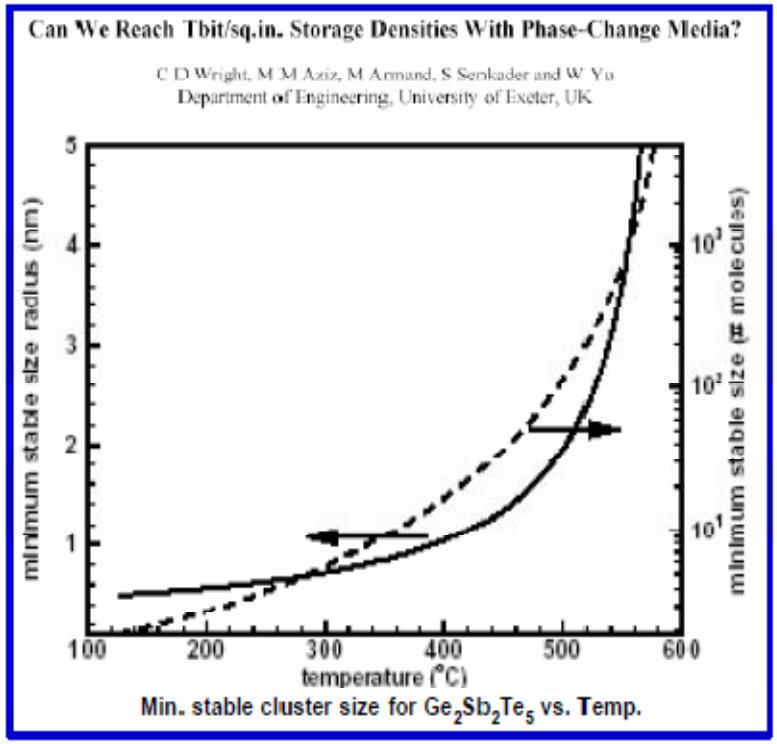
- The cell is cylindrically symmetrical and scaled directly with lithography
- Key Technologies
  - Litho technology for small pore (hole) formation
  - CVD metal and CVD GST processes
  - Small hole etch back and clean

Single Memory Cell Structure

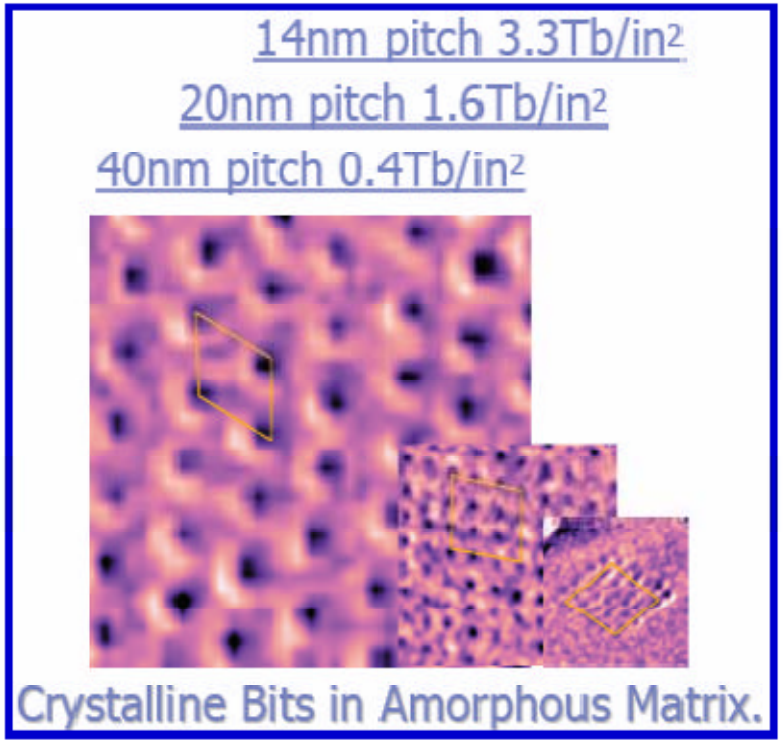


Material Scaling Limit

Phase Change Mechanism Appears Scalable to at Least ~5nm



Source: C.D Wright et al., EPCOS 2004



Source: C. Lam, SRC NVM Forum 2004

Summary

- Phase change memories based on Chalcogenide accepted by industry as leading candidate for new NV memories
  - Ovonyx licensees: Intel, STM, Elpida, Samsung, Qimonda & Hynix
- Near term: higher functionality (easy CMOS add on, direct byte write instead of block, > 10^6 Cycles) makes a better flash
- Longer term: more scalable, cost cross over NOR, then DRAM, then NAND as NOR/DRAM/NAND slow down in scaling