

# Multi-Gate MOSFETs

## Front-End Process and Materials Needs

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**August 20, 2008**

*NCCAUS THIN FILM USER GROUP MEETING*

# Outline

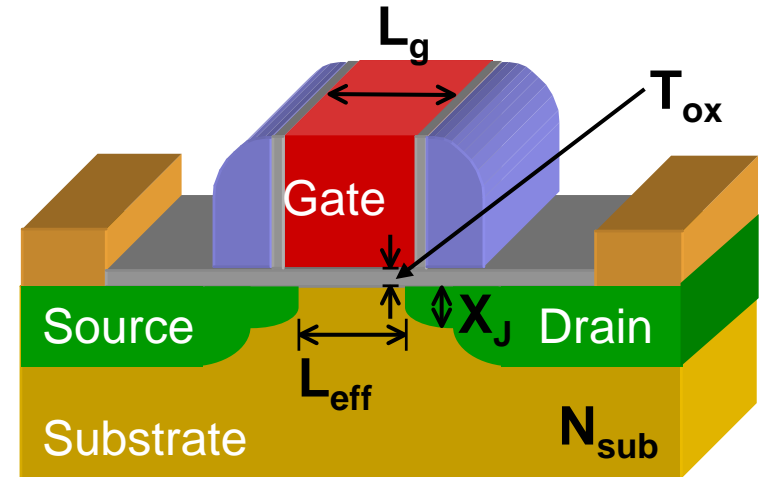
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- **Introduction**
  - MOSFET scaling challenges
- **Multi-gate MOSFET structures**
- **Front-end processes and materials**
- **Summary**

# MOSFET Scaling Challenges

## Leakage

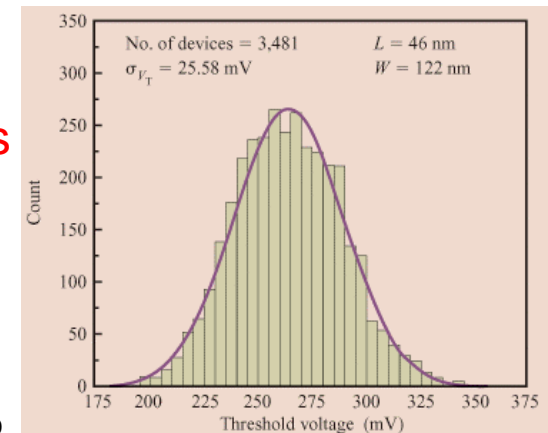
- » drain current  
→ reduce  $T_{ox}$  and  $X_J$
- » gate current  
→ use high- $\kappa$  gate dielectric



## Incommensurate gains in $I_{ON}$ with scaling

- » limited carrier mobilities  
→ strain Si to enhance  $\mu_{eff}$
- » parasitic resistance  
→ use metallic (silicide) source/drain extensions

## Performance variation...

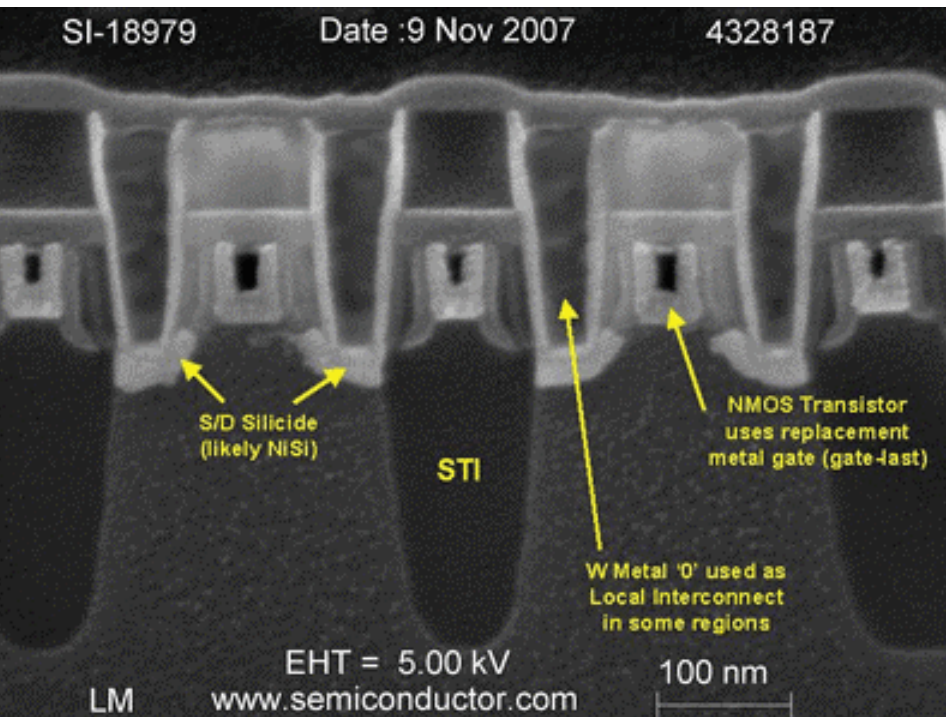


K. Bernstein *et al.*, IBM  
*J. Res. Dev.* 50-4/5, 2006

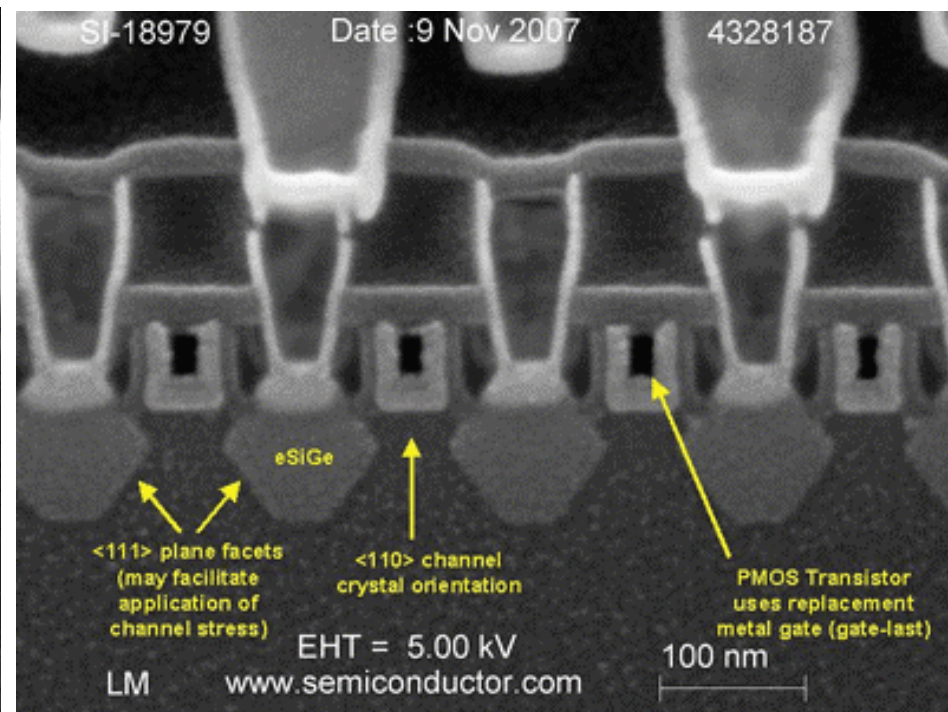
# Modern MOSFET Structures

(Intel Penryn©, from [www.semiconductor.com](http://www.semiconductor.com))

## N-channel MOSFETs



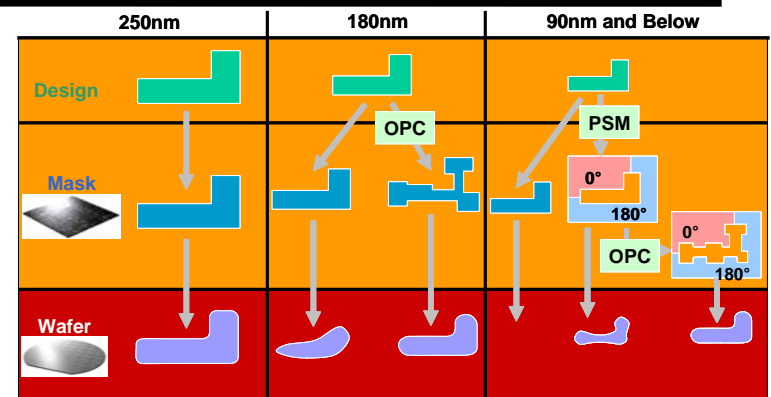
## P-channel MOSFETs



- **45nm CMOS technology features:**
  - high-permittivity gate dielectric and metal gate electrodes
  - strained channel regions
  - aggressive silicidation of n+ source/drain regions

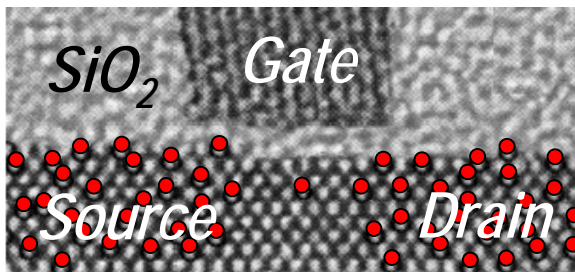
# Sources of Variability

- Sub-wavelength lithography:
  - Resolution enhancement techniques are costly and increase process sensitivity

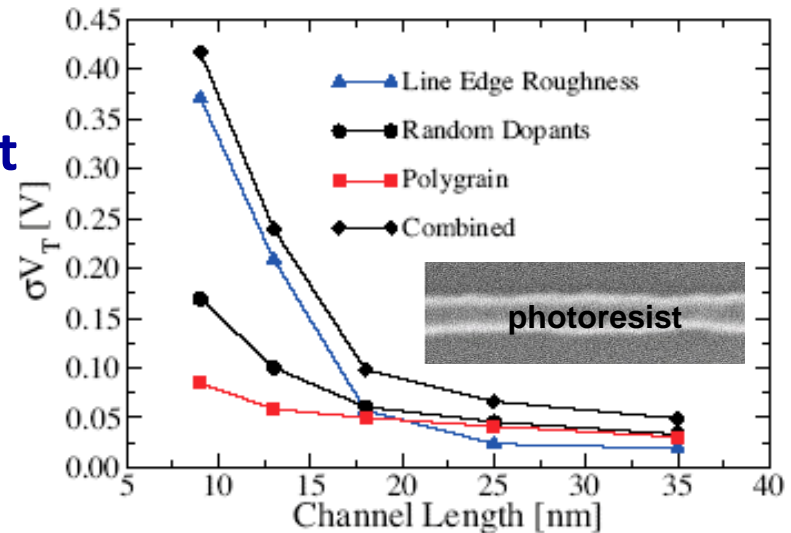


- Layout-dependent transistor performance:
  - Process-induced stress is dependent on layout

- Random dopant fluctuations (RDF):
  - Atomistic effects become significant in nanoscale FETs

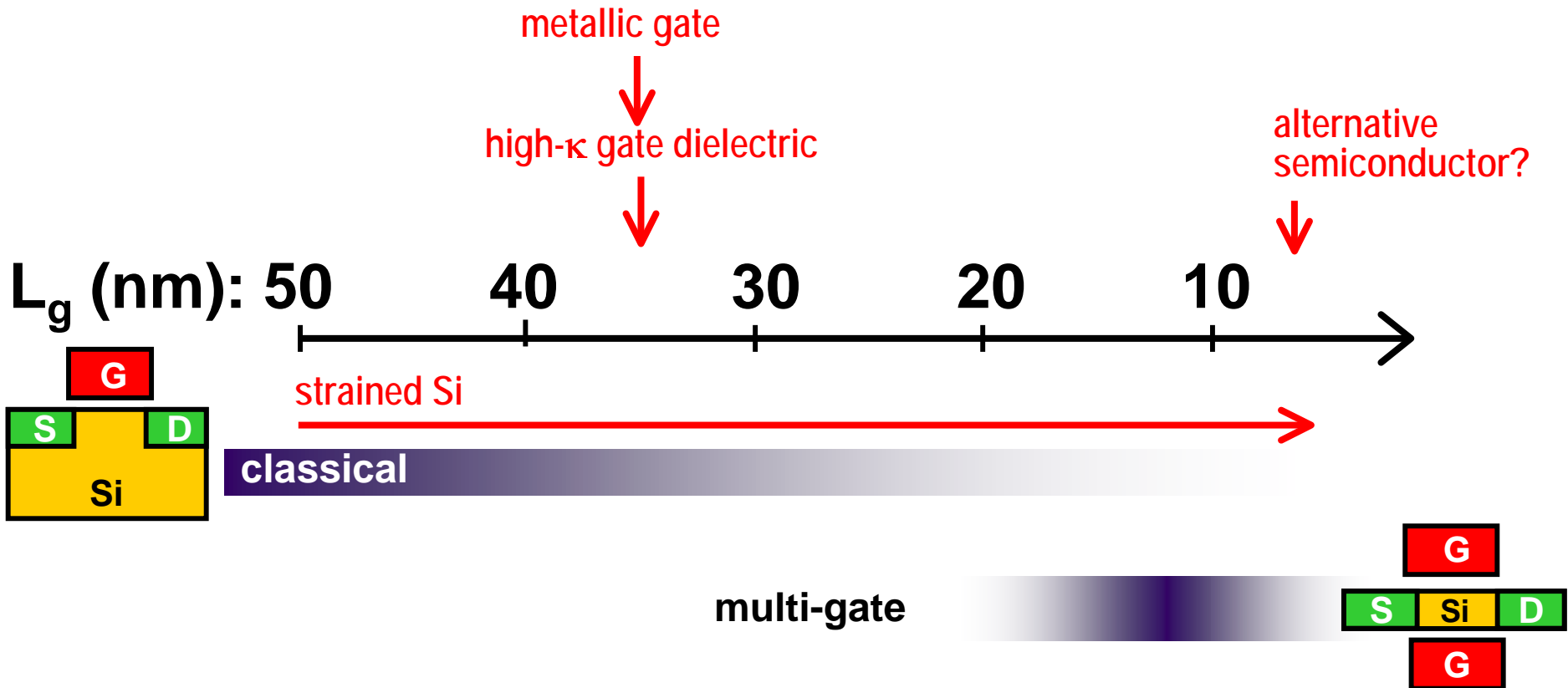


A. Brown *et al.*,  
*IEEE Trans. Nanotechnology*,  
p. 195, 2002



A. Asenov, *Symp. VLSI Tech. Dig.*, p. 86, 2007

# MOSFET Scaling Scenario



- Advanced structures will be needed for scaling to  $L_g < 20$  nm.

# Outline

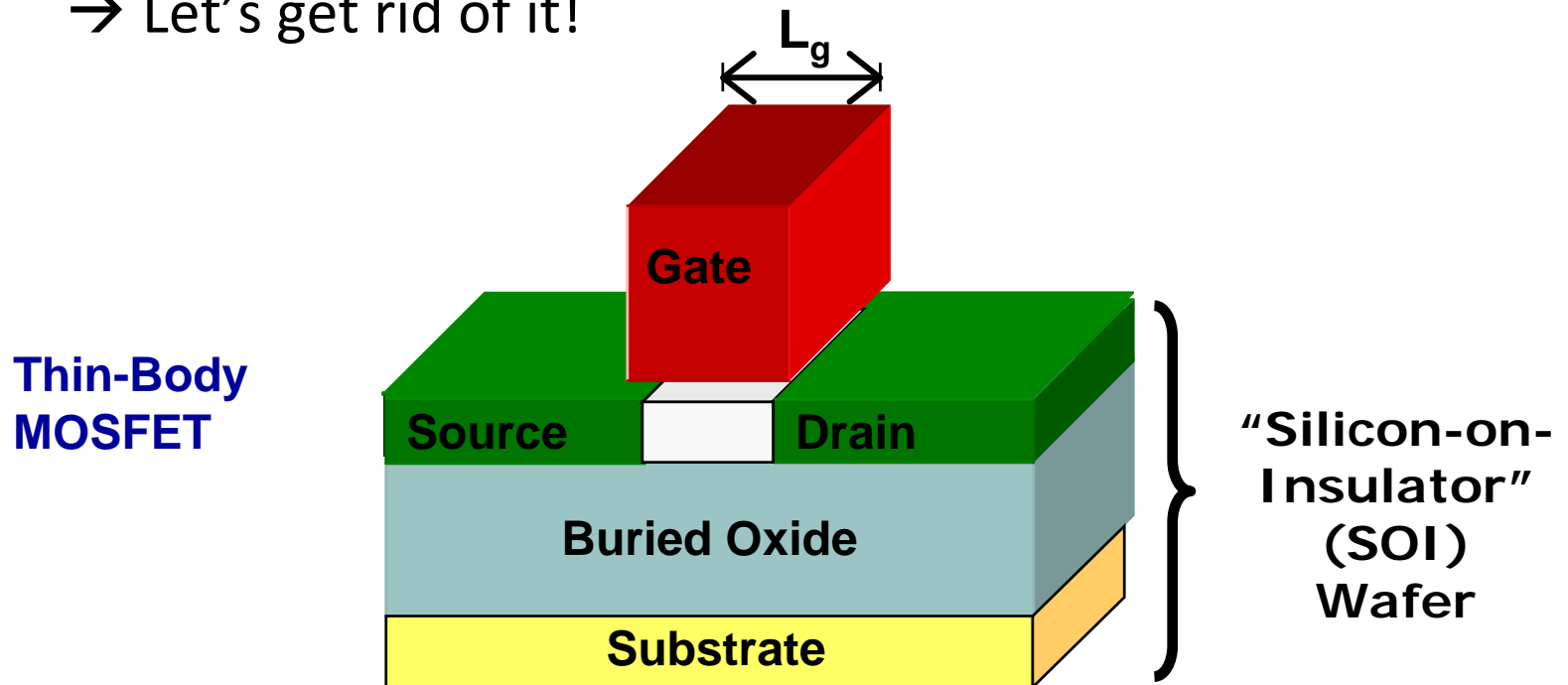
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- Introduction
- **Multi-gate MOSFET structures**
- Front-end processes and materials
- Summary

# Why New Transistor Structures?

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- Leakage must be suppressed to scale down  $L_g$
- Leakage occurs in region far from channel surface  
→ Let's get rid of it!

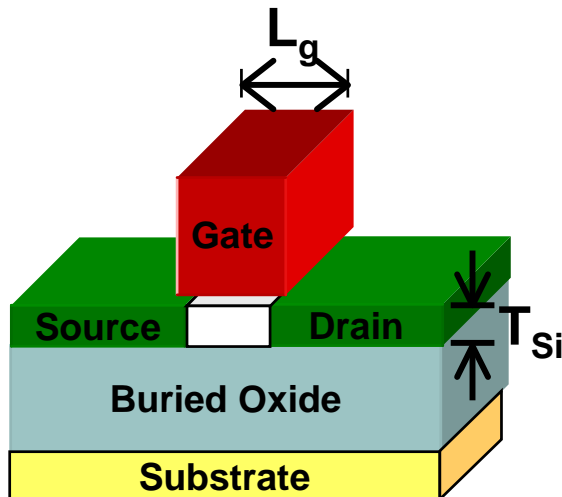




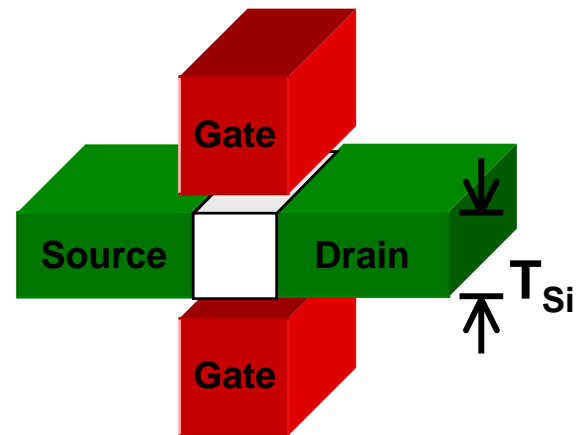
# Thin-Body MOSFETs

- Leakage is suppressed by using a thin body ( $T_{Si} < L_g$ )
  - Channel doping is not needed  $\rightarrow$  higher carrier mobility
  - Aggressive gate-oxide scaling is not needed
- The double-gate structure is more scalable (to  $L_g < 20\text{nm}$ )

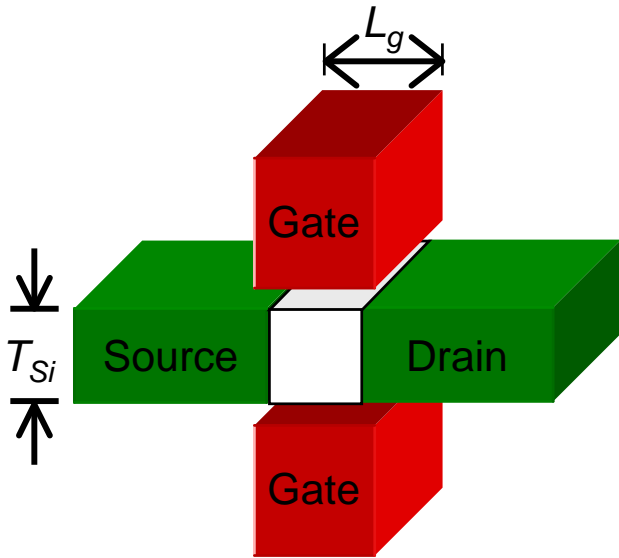
## Ultra-Thin Body (UTB)



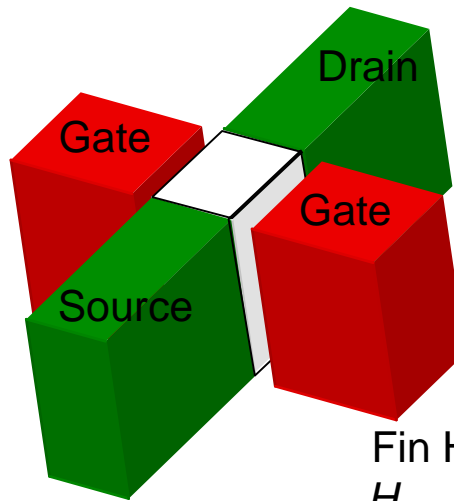
## Double-Gate (DG)



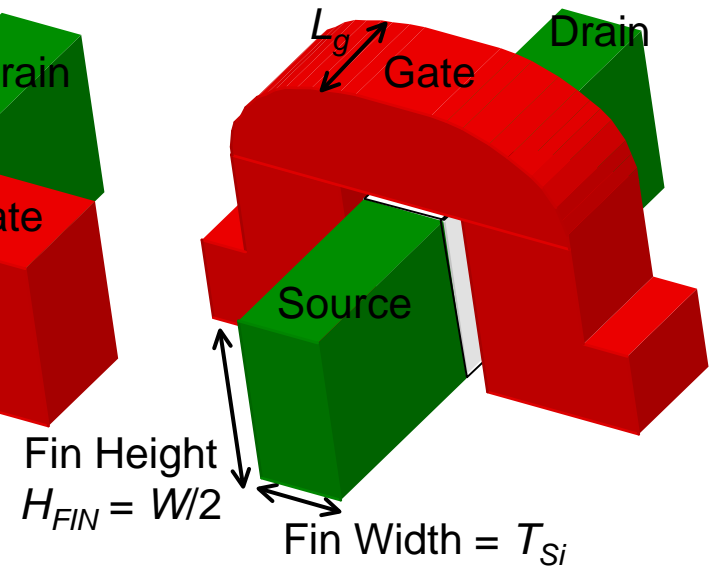
# Double-Gate “FinFET”



**Planar  
Double-Gate FET**



**(90° rotation)**



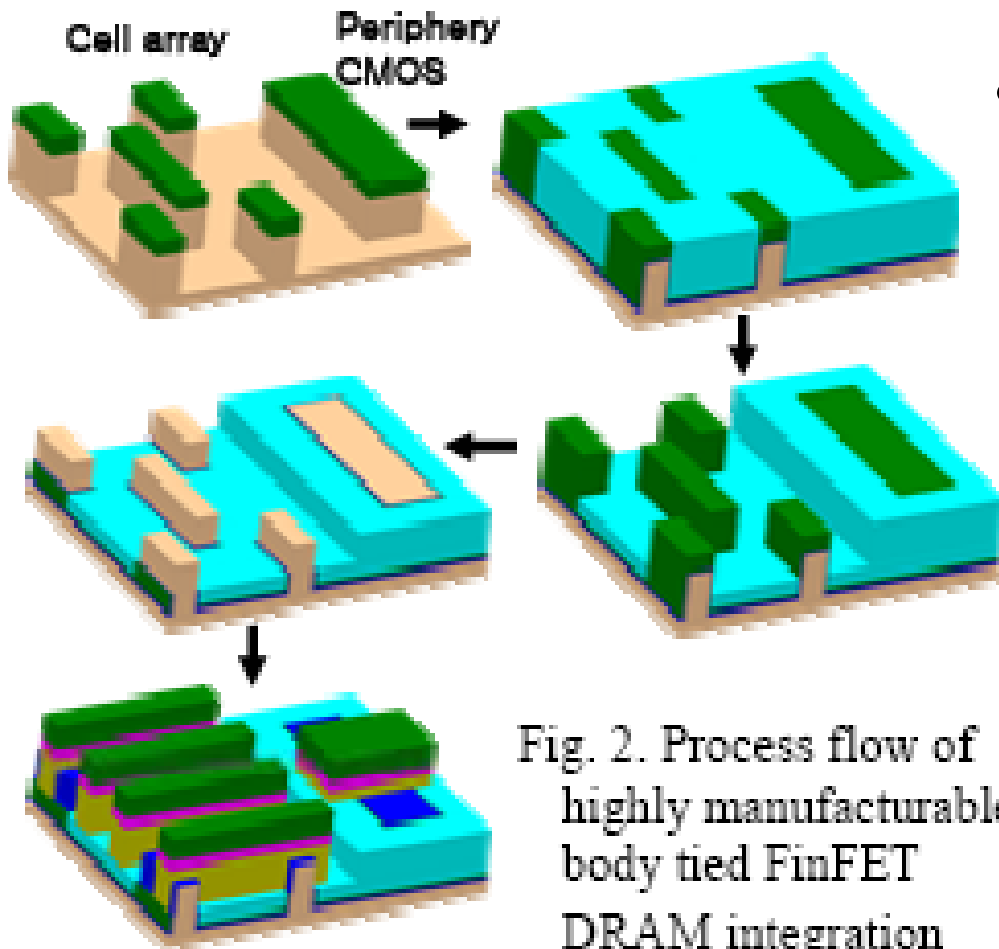
**“FinFET”**

D. Hisamoto *et al.*, *IEDM*, 1998  
N. Lindert *et al.*, *IEEE Electron  
Device Letters*, p.487, 2001

- Rotation allows for self-aligned gate electrodes
- FinFET layout is similar to that of a planar FET

# Bulk-Si FinFETs

C.-H. Lee *et al.*, *Symp. VLSI Technology Digest*, pp. 130-131, 2004

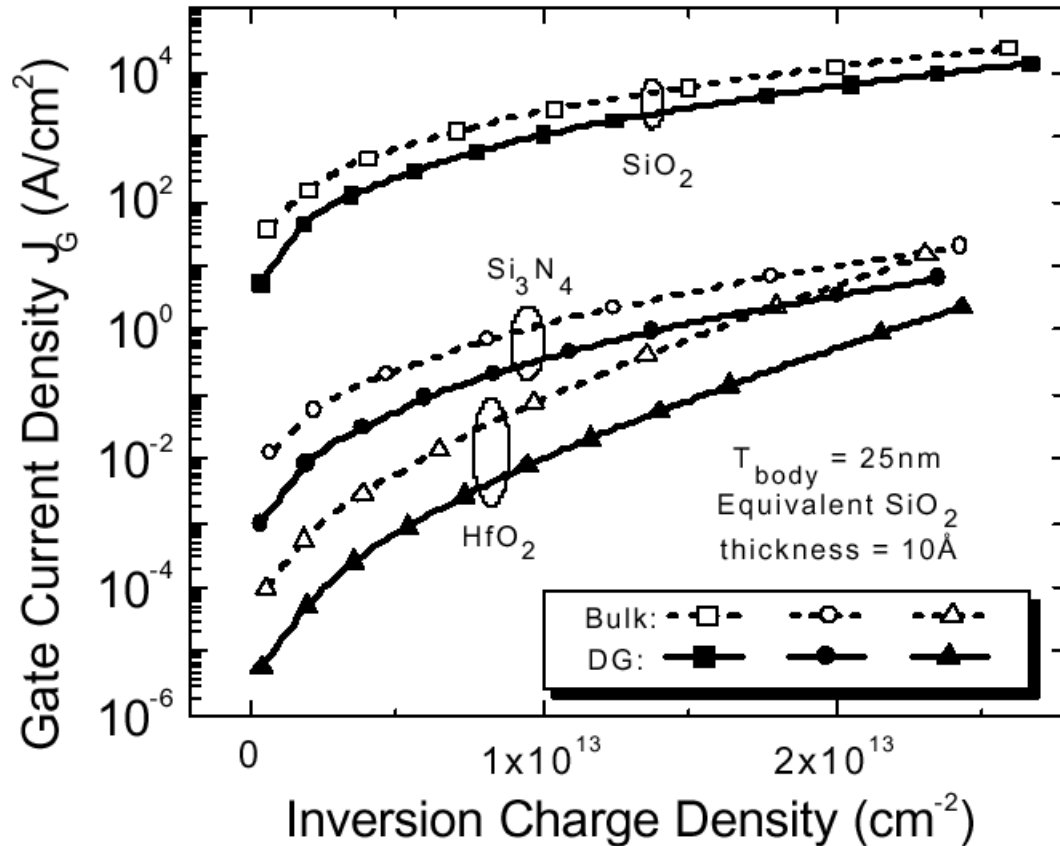


- FinFETs can be made on bulk-Si wafers
  - ✓ lower cost
  - ✓ improved thermal conduction to mitigate self-heating effects
  - ✓ integration with bulk-Si devices is possible

Fig. 2. Process flow of highly manufacturable body tied FinFET DRAM integration

# Gate Leakage Reduction

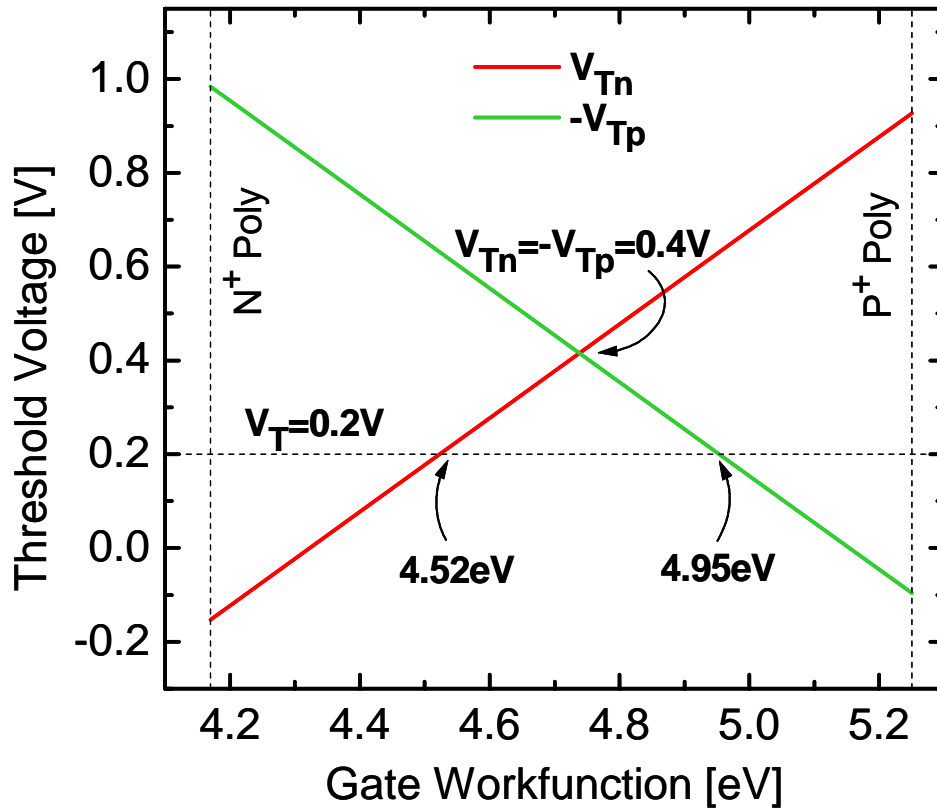
L. Chang *et al.*, *IEDM Technical Digest*, pp. 99-103, 2001.



- DG-MOSFET provides for less gate leakage
- ➔ T<sub>ox</sub> can be more aggressively scaled for improved I<sub>ON</sub>

# Thin-Body MOSFET $V_T$ Control

$V_t$  vs.  $\Phi_M$  for thin-body MOSFET



- For low body doping, desired  $\Phi_M$  values are:

~ 4.5 eV for NMOS

~ 5.0 eV for PMOS

⇒ Different metal gate materials are optimal for thin-body FETs than for bulk-Si MOSFETs.

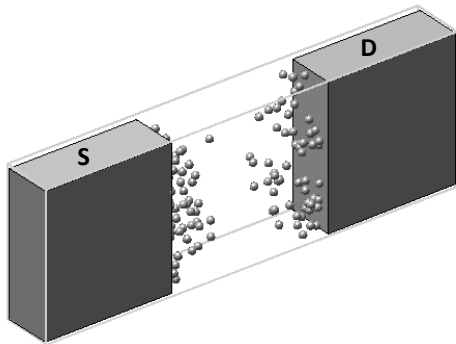
L. Chang *et al.*, *IEDM Technical Digest*, pp. 719-722, 2000

# Impact of RDF on FinFETs

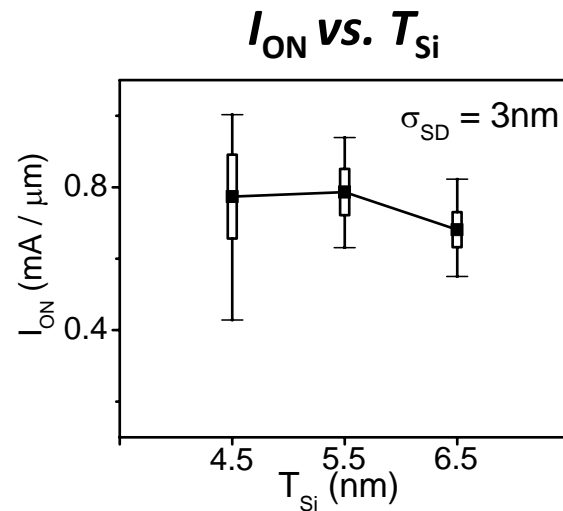
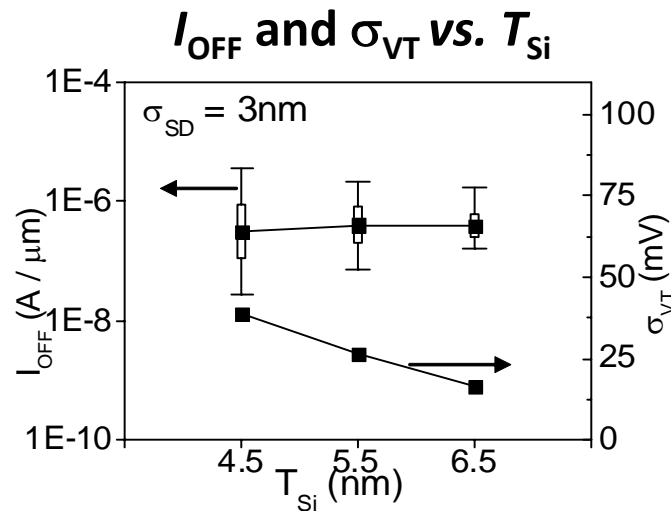
V. Varadarajan *et al.*, *Proc. IEEE Silicon Nanoelectronics Workshop*, pp. 137-138, 2006.

- Channel doping can be eliminated in thin-body FETs such as the double-gate FinFET, to mitigate RDF effects.
- However, due to source/drain doping, a trade-off exists between performance & RDF tolerance for  $T_{Si} < 10\text{nm}$ :

FinFET with atomistic  
S/D gradient regions:



$L_G = 9\text{nm}$ ,  $EOT = 0.7\text{nm}$

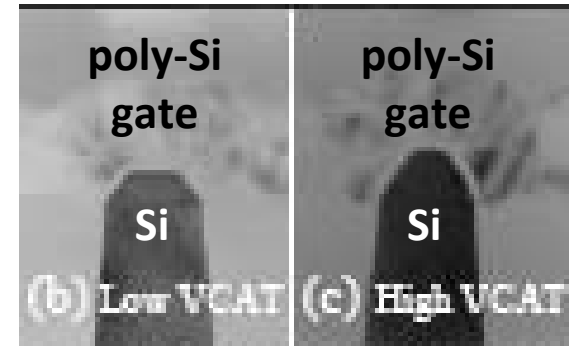


# Tri-Gate Bulk FET

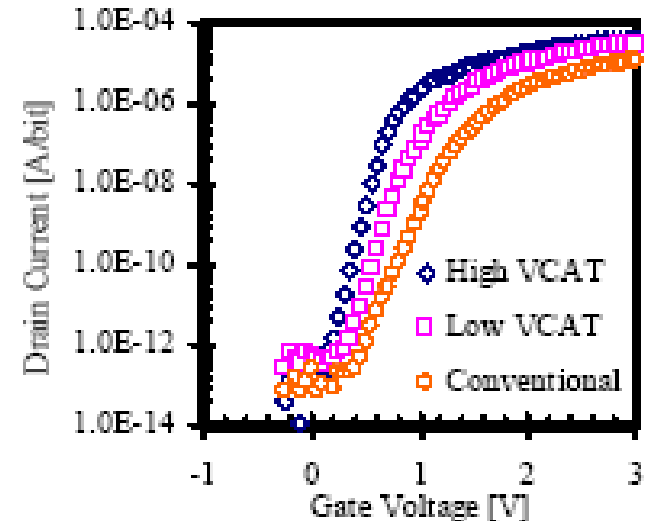
M. Kito et al. (Toshiba Corp.), 2005 Symp. VLSI Technology

- A tri-gate structure is easily achieved by slightly recessing the STI oxide (or by selective epitaxial growth) just prior to gate-stack formation
- Superior electrostatic integrity is achieved with the tri-gate structure
  - Smaller  $S$  and DIBL

## XTEM images

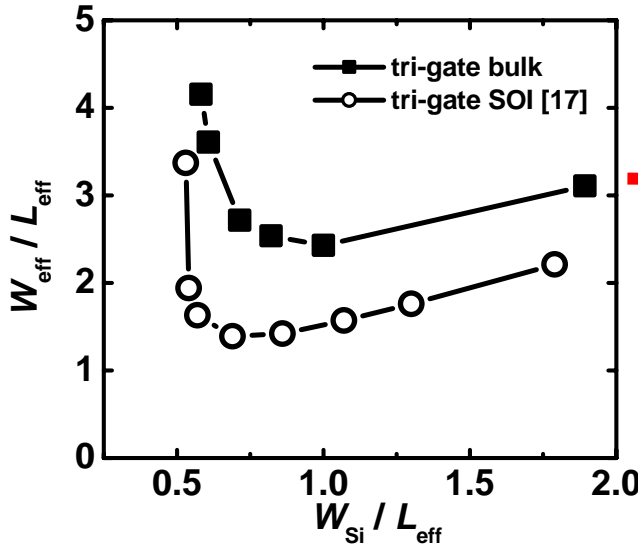
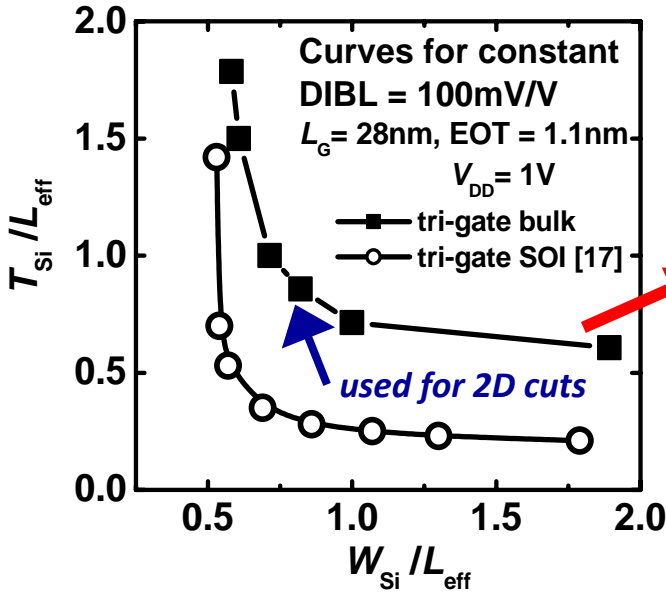


## Measured I-V Characteristics



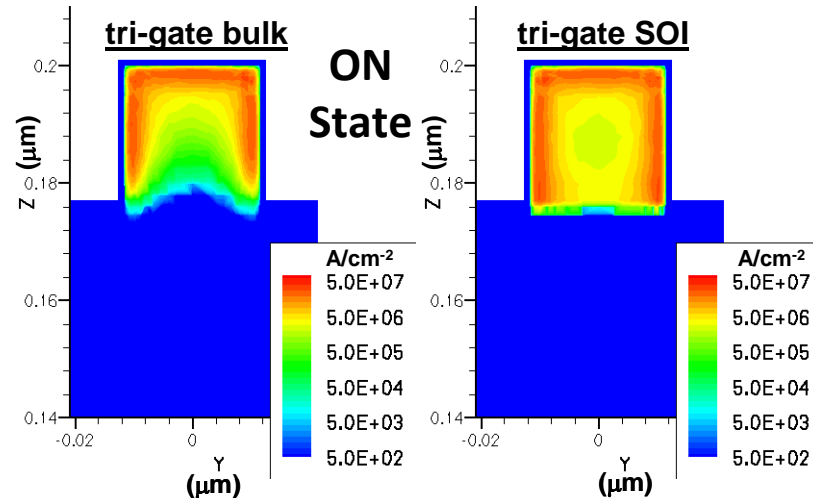
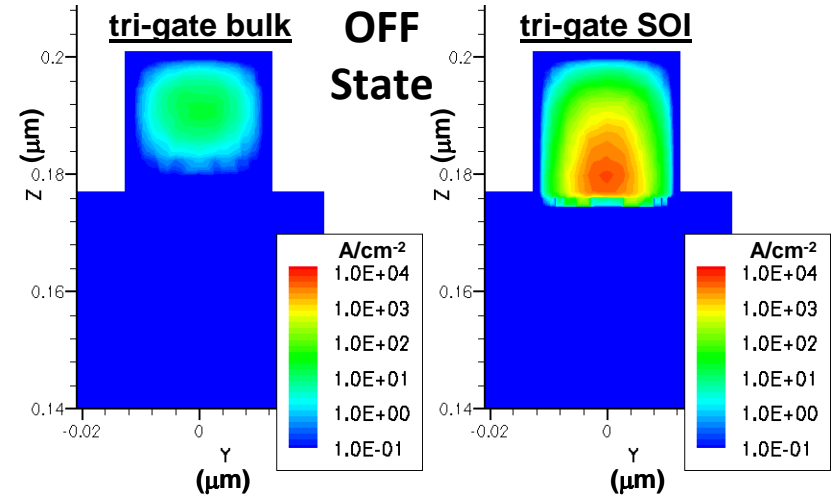
# Bulk vs. SOI Tri-Gate FET Design

X. Sun *et al.*, *IEEE Electron Device Letters* vol. 29, pp. 491-493, May 2008.



[17] J.G. Fossum *et al.*, *IEDM Tech. Dig.*, pp. 613-616, 2004.

## Current Contour Plots

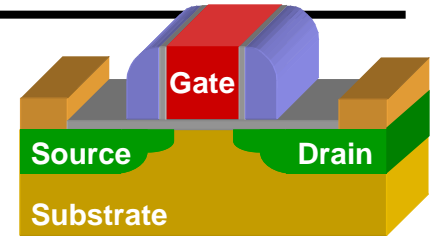




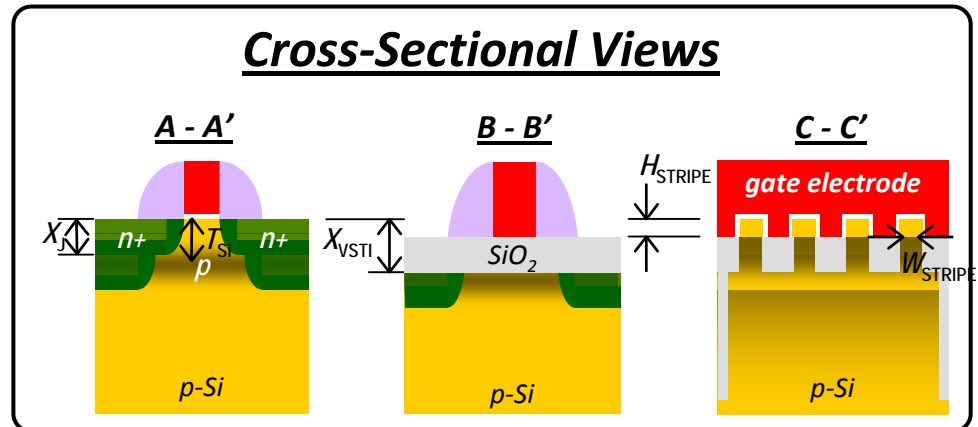
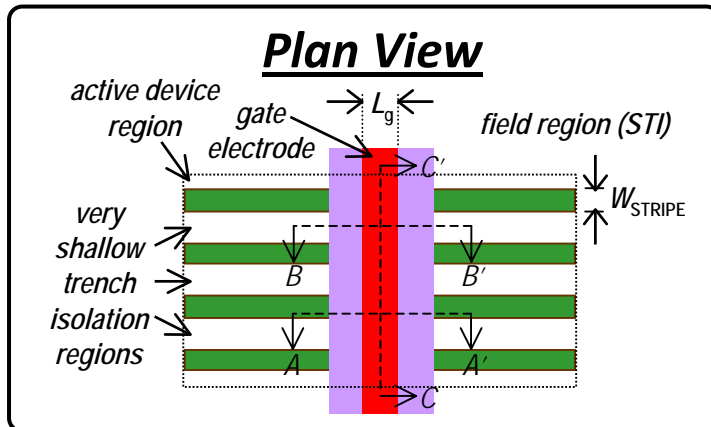
# The Segmented Bulk MOSFET

T.-J. King and V. Moroz, U.S. Patent 7,247,887

*Planar Bulk  
MOSFET:*



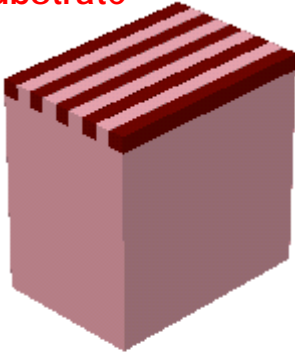
- Channel consists of stripes of uniform width  $\geq L_g$ 
  - geometrical regularity for reduced variations
- Very shallow trench isolation (VSTI) in-between the stripes
  - low aspect ratio stripes, for ease of fabrication
- Gate electrode wraps top portion of each stripe (tri-gate structure)
  - good control of short-channel effects and improved layout area efficiency



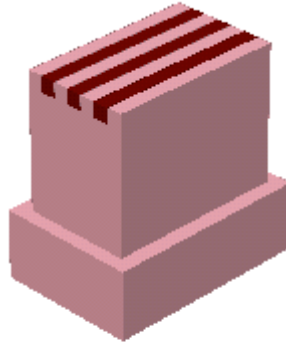
# SegFET Fabrication Process

T.-J. King and V. Moroz, U.S. Patent 7,265,008

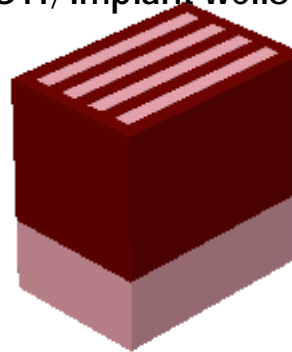
1. Start with corrugated substrate



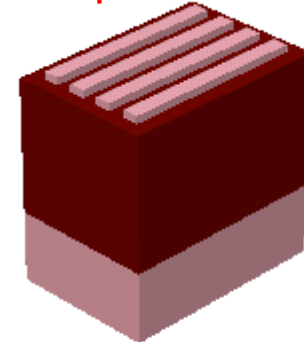
2. Define active areas



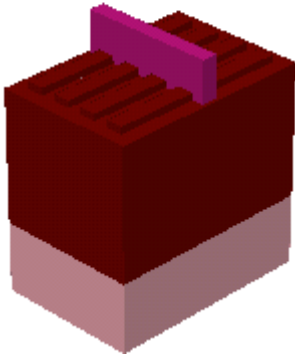
3. Fill trenches to form STI; Implant wells



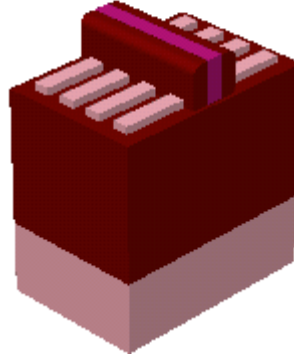
4. Slightly elevate the stripe surfaces (optional)



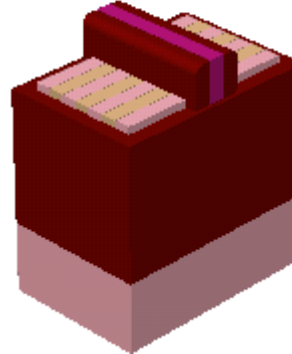
5. Implant channels; Form gate stack



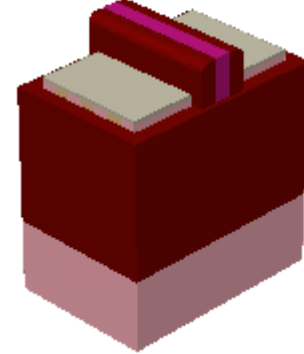
6. Form S/D extensions, then sidewall spacers



7. Grow epitaxial material in S/D regions (optional)



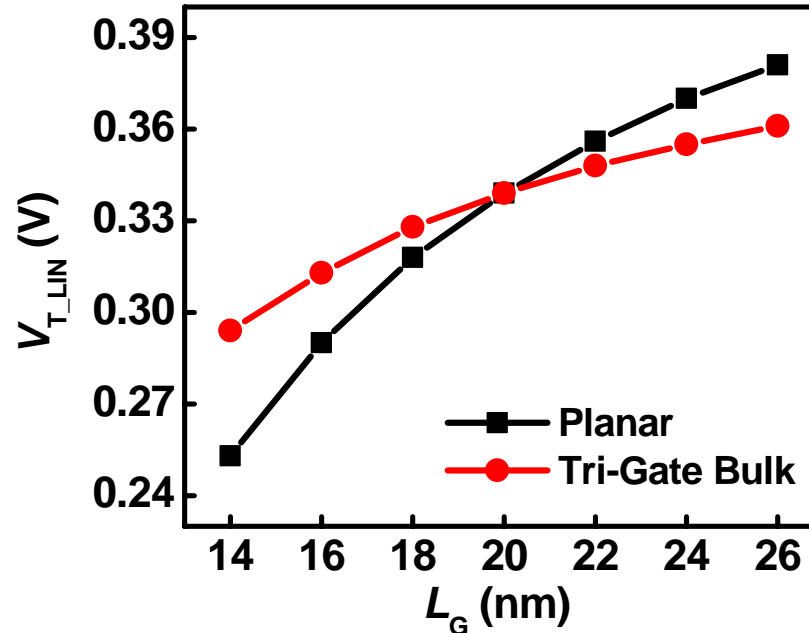
8. Dope S/D regions; Form silicide



# Impact of $L_g$ Variations

X. Sun *et al.*, to be published

EOT = 0.9nm,  $W_{\text{STRIPe}} = 20\text{nm}$ ,  $H_{\text{STRIPe}} = 7\text{nm}$ ,  $T_{\text{Si}} = 14\text{nm}$ ,  $X_j = 7\text{nm}$



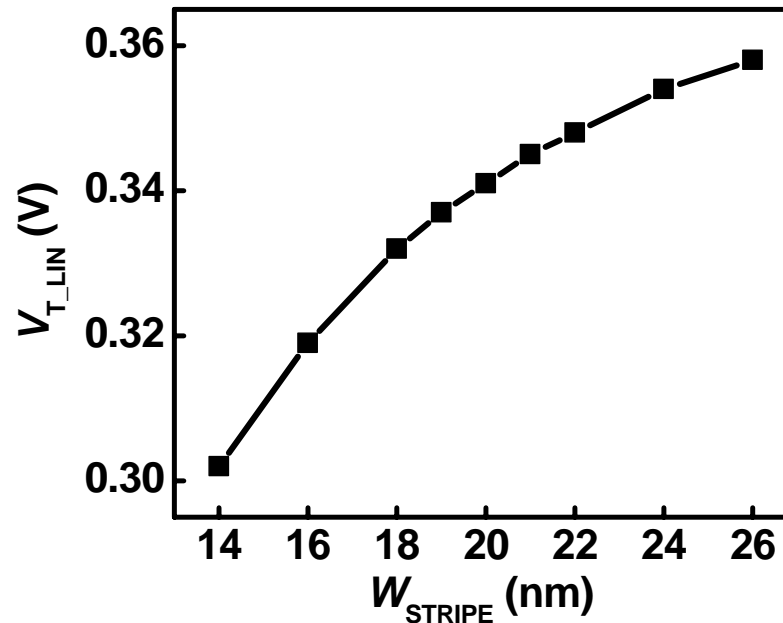
(Channel- and source/drain-doping profiles are identical for the planar and tri-gate MOSFETs)

- The tri-gate bulk MOSFET is less sensitive to gate-length variations, due to improved gate control.

# Impact of $W_{\text{STRIPE}}$ Variations

X. Sun *et al.*, to be published

$L_G = 20\text{nm}$ ,  $EOT = 0.9\text{nm}$ ,  $H_{\text{STRIPE}} = T_{\text{Si}} = X_J = 14\text{nm}$

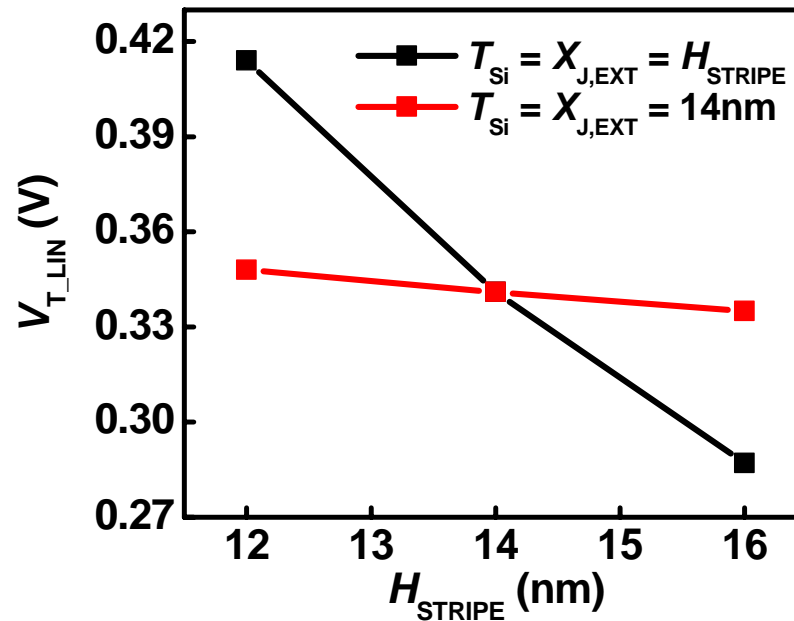


- Smaller  $W_{\text{STRIPE}} \rightarrow$  stronger gate control  $\rightarrow$  smaller  $V_T$   
 $\rightarrow W_{\text{STRIPE}}$  should be tightly controlled to minimize  $\sigma_{V_T}$

# Impact of $H_{\text{STRIPE}}$ Variations

X. Sun *et al.*, to be published

$L_G = 20\text{nm}$ ,  $EOT = 0.9\text{nm}$ ,  $W_{\text{STRIPE}} = 20\text{nm}$

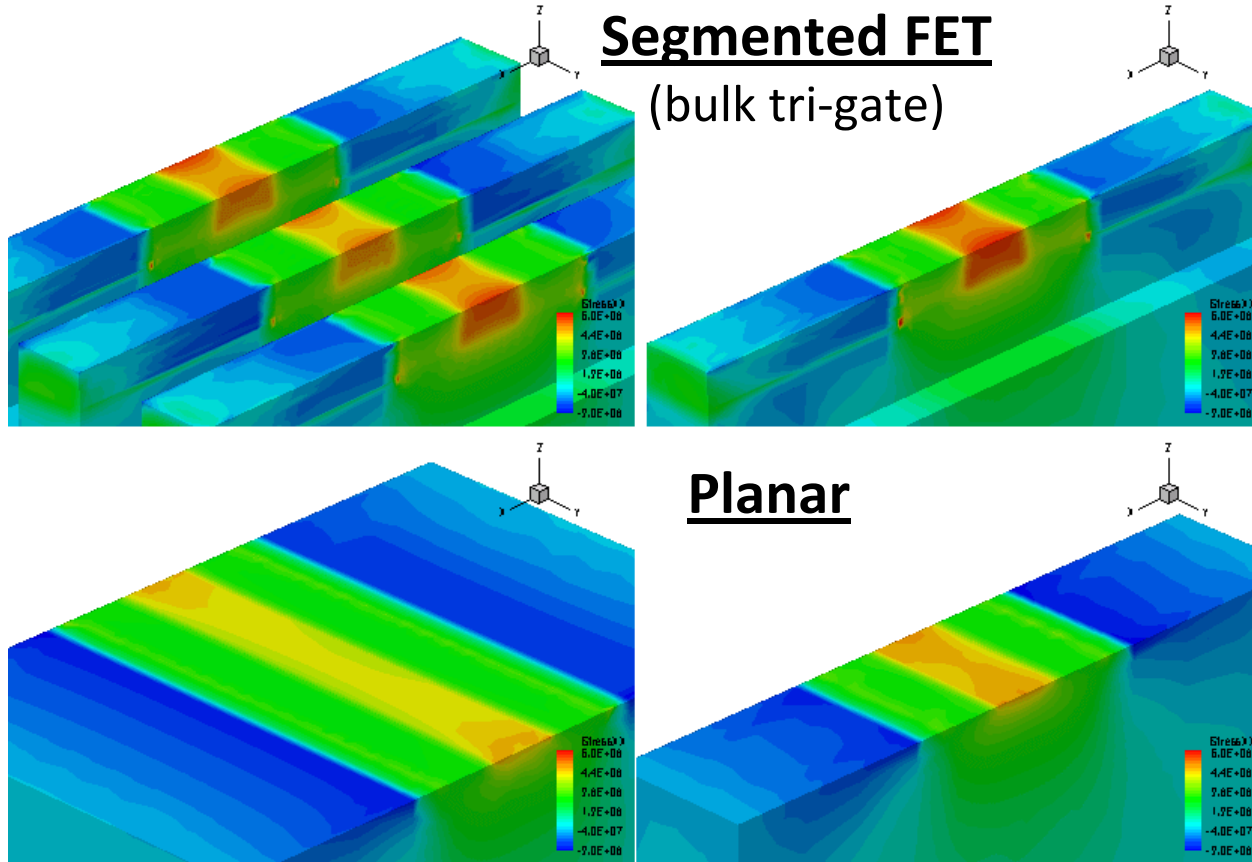


- If  $T_{\text{Si}}$  is fixed,  $V_T$  is not sensitive to  $H_{\text{STRIPE}}$  variation.
- $V_T$  can be tuned by adjusting  $T_{\text{Si}}$  rather than  $N_{\text{peak}}$   
→ reduced  $\sigma_{V_T}$  due to RDF

C. Shin *et al.*, 2008 Silicon Nanoelectronics Workshop

# Capping-Layer-Induced Strain Along Channel

(Contact etch stop liner is assumed to be a 30nm-thick silicon nitride with 2GPa tensile stress)



- SegFET parameters:

$$W_{\text{STRIPE}} = 20\text{nm}$$

$$W_{\text{SPACING}} = 20\text{nm}$$

$$H_{\text{STRIPE}} = 10\text{nm}$$

- $L_G = 20\text{nm}$
- $EOT = 0.9\text{nm}$
- $T_{\text{GATE}} = 40\text{nm}$
- $L_{\text{SPACER}} = 20\text{nm}$

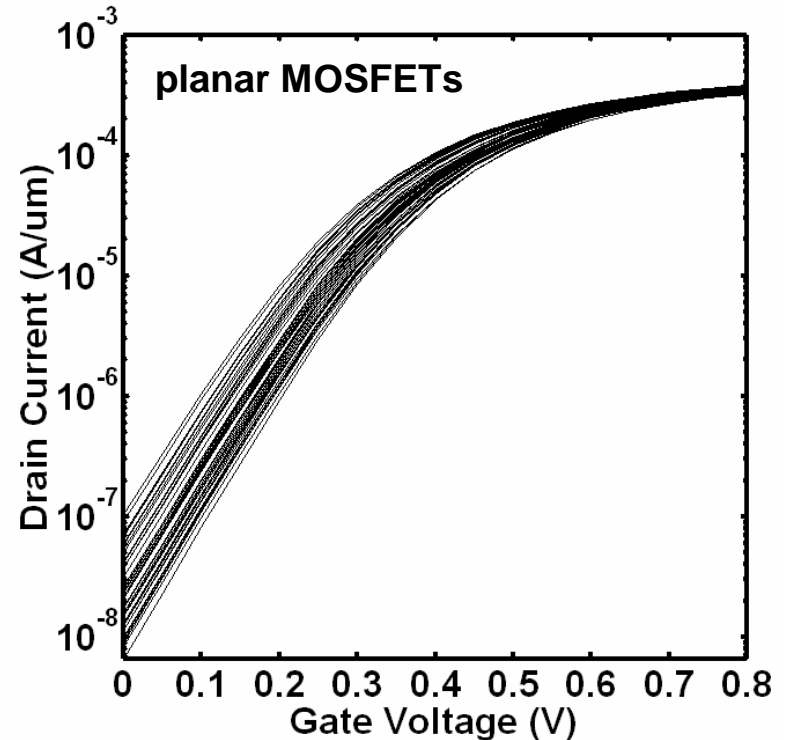
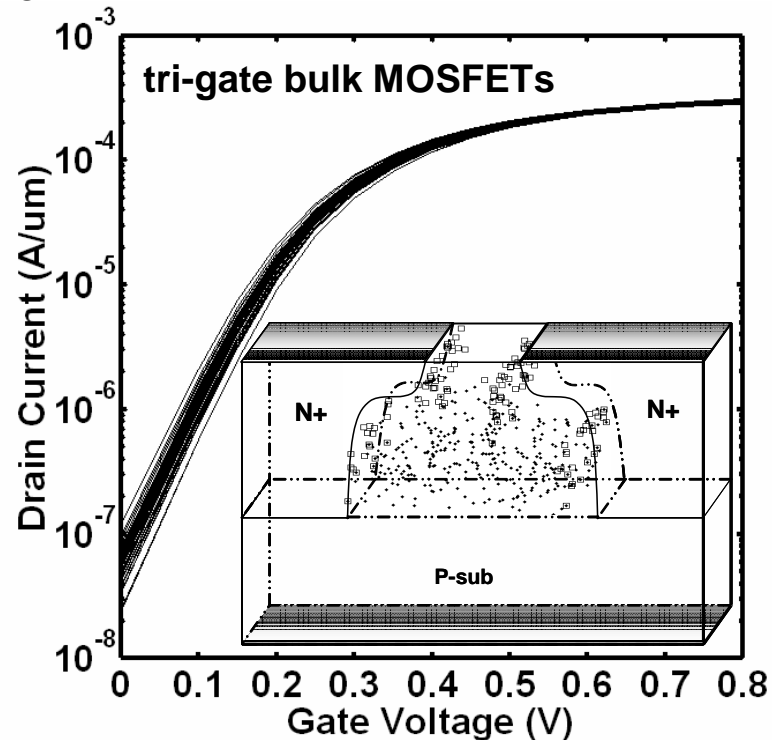
- More stress is induced in SegFET  $\rightarrow$  More mobility enhancement
- Reduced variation with  $W_{\text{eff}}$  for SegFET  $\rightarrow$  Reduced  $\mu$  variation

# Impact of RDF

X. Sun *et al.*, *IEEE Electron Device Letters* vol. 29, pp. 491-493, May 2008.

## Monte Carlo simulations, 100 cases each

$L_G = 20\text{nm}$ ,  $EOT = 0.9\text{nm}$ ,  $W_{\text{STRIPE}} = 20\text{nm}$ ,  $H_{\text{STRIPE}} = 14\text{nm}$ ,  $T_{\text{Si}} = 14\text{nm}$ ,  $X_J = 14\text{nm}$



- The tri-gate bulk FET structure has superior gate control and reduced depletion charge density per unit effective width.  
→ RDF induced variations are significantly reduced.

# Outline

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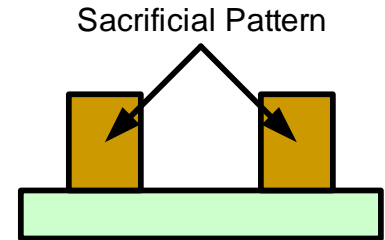
- Introduction
- Multi-gate MOSFET structures
- **Front-end processes and materials**
  - Spacer lithography
  - Steep retrograde doping
  - Advanced channel materials
- Summary



# Spacer Lithography Process

1. Begin with a patterned sacrificial layer

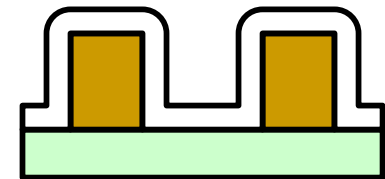
①



2. Deposit spacer layer by CVD

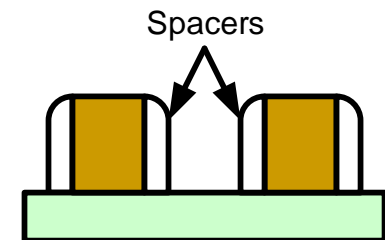
- Very uniform deposition
- Thickness determines CD

②



3. Etch anisotropically to leave spacers

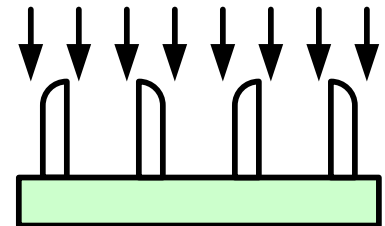
③



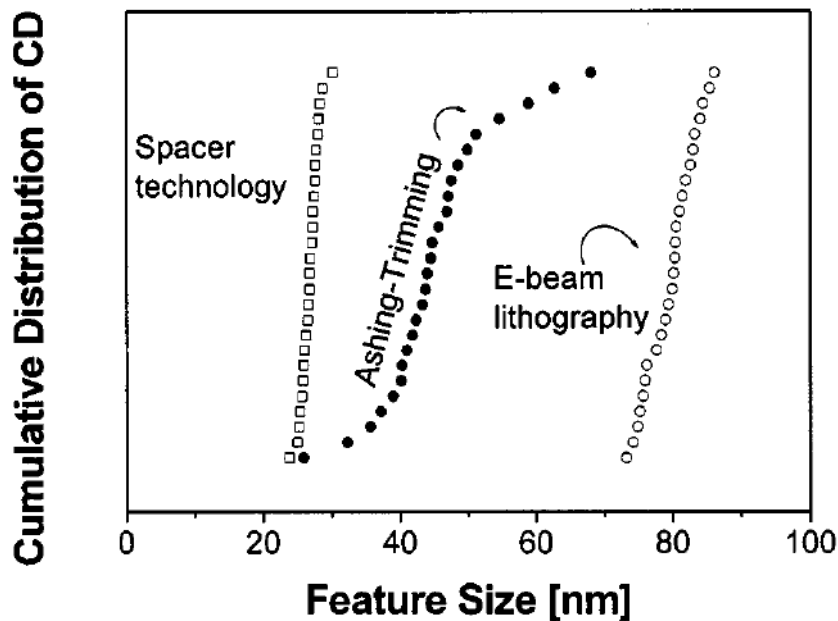
4. Remove the sacrificial layer

- Note that the pitch is halved

④



# Benefits of Spacer Lithography

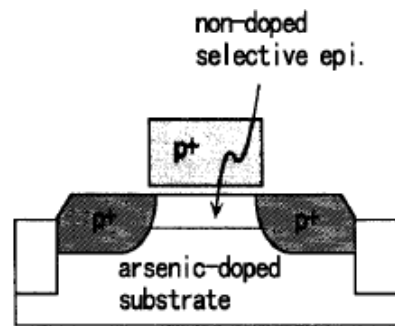


- Tighter CD control  
→ uniform  $W_{\text{STRIPE}}$  for tight  $V_T$  control
- Reduced pitch  
→ Improved layout area efficiency

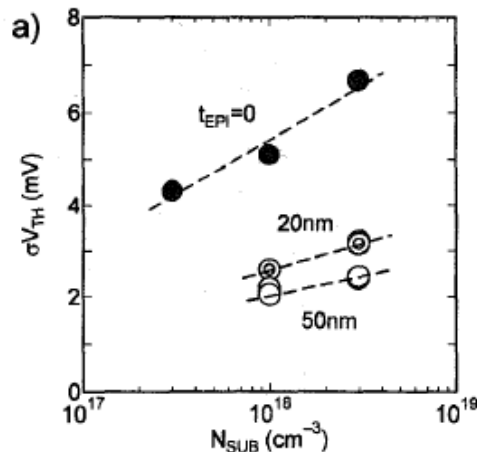
Y.-K. Choi *et al.*, *IEEE Trans. Electron Devices*, Vol. 49, pp. 436-441, 2002.

# Steep Retrograde (S-R) Doping

- In order to maximize  $I_{ON}$ , heavy doping in the channel region should be eliminated.
- Steep retrograde channel doping reduces  $V_T$  variation due to random dopant fluctuations



double As I/I  
anneal (850C,20min)  
selective epi. (@650C)  
gate oxidation (@750C)  
gate formation  
BF<sub>2</sub> I/I for S/D and gate  
RTA (1000C,10s)



K. Takeuchi *et al.*,  
*IEDM Technical Digest*,  
pp. 841-844, 1997

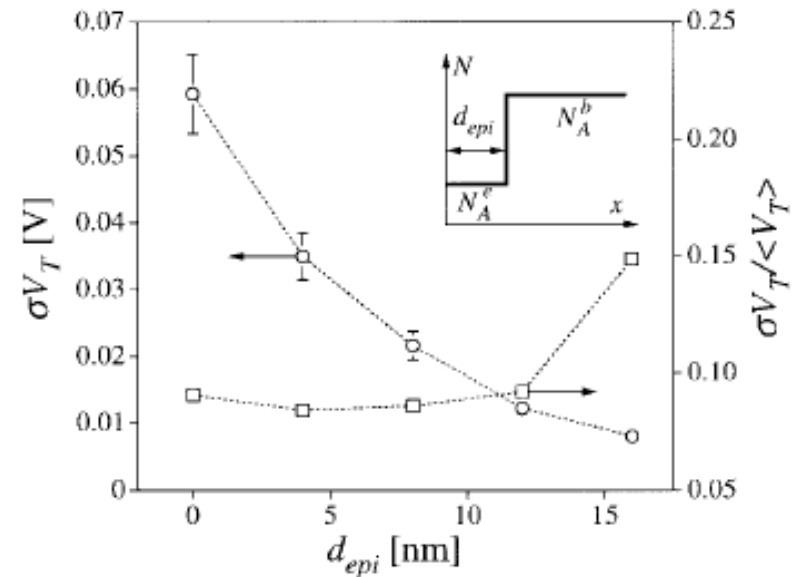
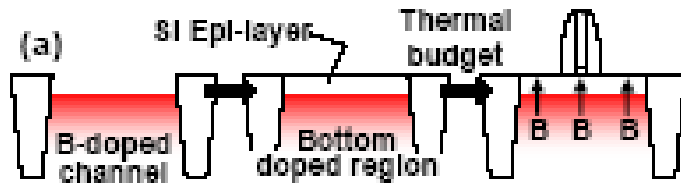


Fig. 3. Standard deviation of the threshold voltage  $\sigma V_T$  as a function of the thickness of the epitaxial channel layer  $d_{epi}$  for a set of MOSFET's with  $L_{eff} = 0.05 \mu\text{m}$ ,  $W_{eff} = 0.05 \mu\text{m}$ ,  $N_A^a = 1 \times 10^{15} \text{cm}^{-3}$ ,  $N_A^b = 5 \times 10^{18} \text{cm}^{-3}$ , and  $t_{ox} = 3 \text{nm}$ . Samples of 200 transistors.

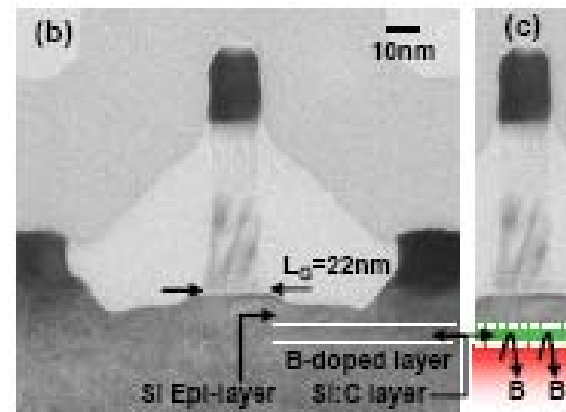
A. Asenov and S. Saini, *IEEE Trans. Electron Devices*, Vol. 46, 1718-1724, 1999

# Process Needs for S-R Doping

- Low-temperature selective epitaxial growth is ideal for achieving a steep retrograde doping profile
  - Material can be engineered to confine dopants, *e.g.* use Si:C layer to block B diffusion



A. Hokazono *et al.*, 2008 Symp. VLSI Technology



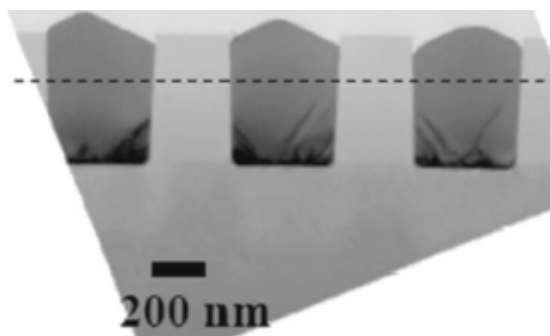
- Low-thermal-budget processes are also desirable for
  - gate-stack formation
  - embedded S/D ( $\text{Si}_{1-x}\text{Ge}_x$  for PMOS,  $\text{Si}_{1-y}\text{C}_y$  for NMOS)
  - S/D doping
  - passivation/etch-stop layers

# Advanced Channel Materials

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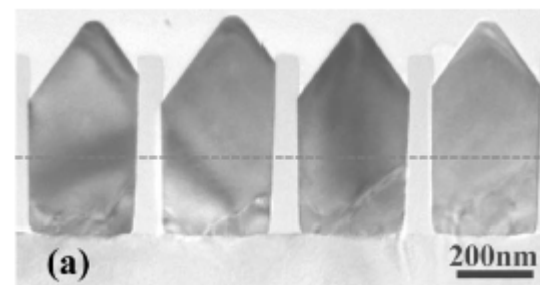
- High-mobility semiconductor materials can potentially provide for improved performance
  - Ge for PMOS
  - (In)GaAs for NMOS
- Selective epitaxial growth directly on Si is possible:

## Ge on Si



J.-S. Park *et al.*, *Appl. Phys. Lett.* 90  
052113, 2007

## GaAs on Si



J. Z. Li *et al.*, *Appl. Phys. Lett.* 91  
021114, 2007

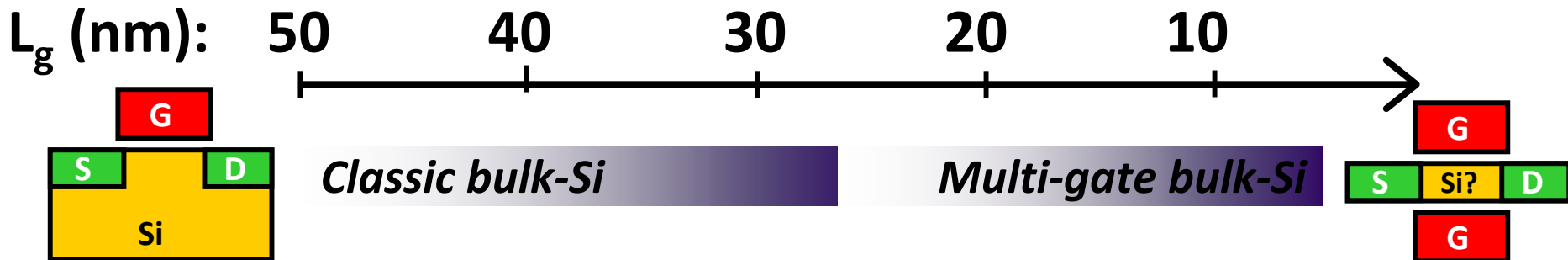
# Outline

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- Multi-gate MOSFET structures
- Advanced processes and materials
- **Summary**

# Summary

- CMOS scaling will continue with advances in
  - transistor design (for reduced leakage and variability)
  - fabrication techniques (for reduced variability)
  - materials (for enhanced performance)
- Highly uniform thin-film deposition, good anisotropy and selectivity in etching, precise dopant profile engineering, and low-temperature selective epitaxy will be needed to sustain MOSFET scaling to the fundamental limit.



# Acknowledgements

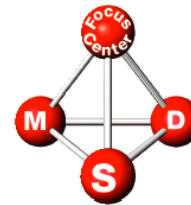
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- **Collaborators:**

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- Current students: Xin Sun, Changhwan Shin
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