TFUG Seminar

AMD Smarter Choice

Resistive Switching Memory Technologies

An Chen

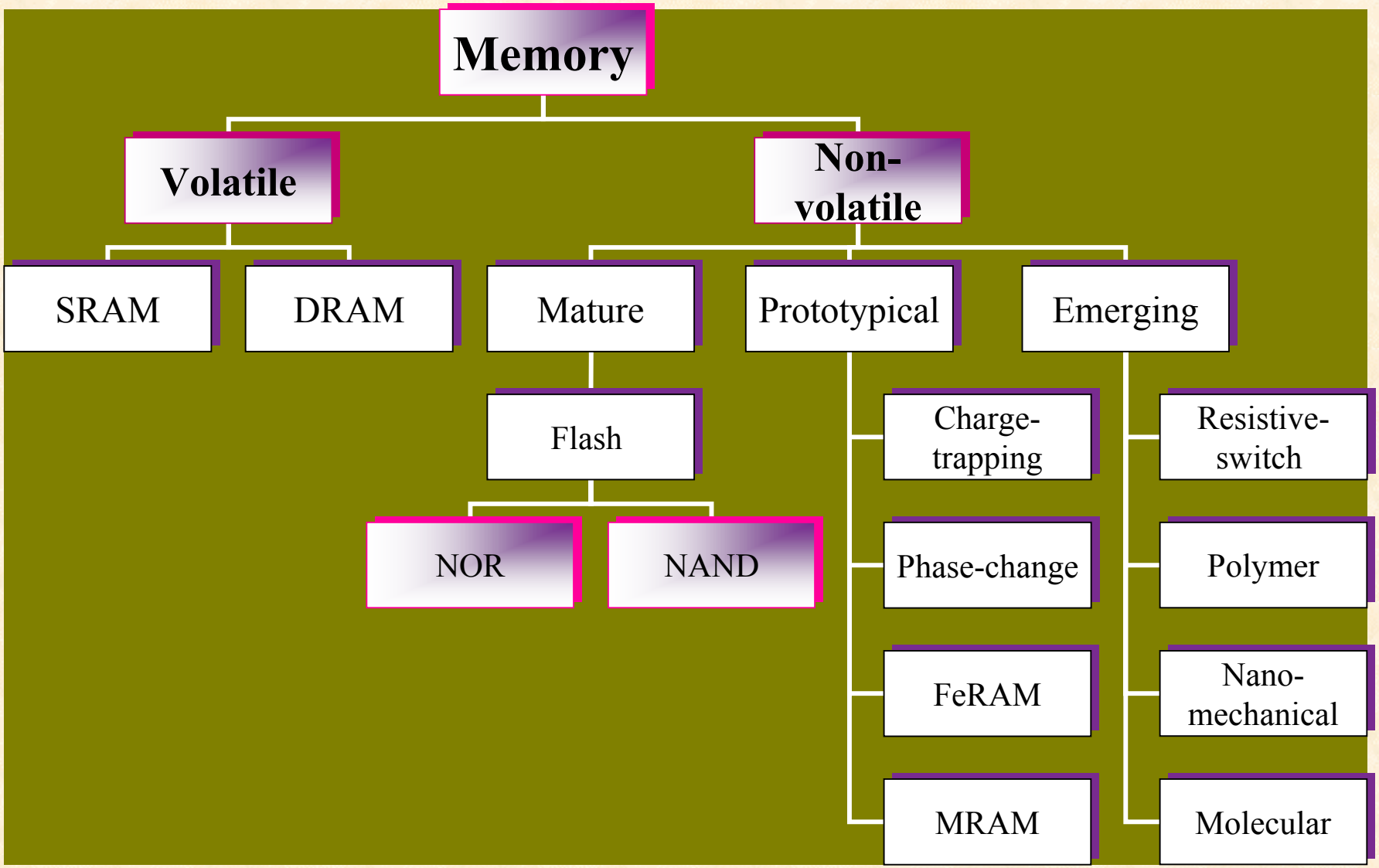
Strategic Technology Group

Advanced Micro Devices (AMD)

Outline

- Memory technologies
  - Category and characteristics
- Resistive switching memories
  - Resistive switching mechanisms
  - Device characteristics
- Ionic memory
  - Resistive switching in solid-state electrolytes
  - Device and array characteristics
  - Advantages *vs*. challenges
- Resistive switching devices for logic applications
- Summary

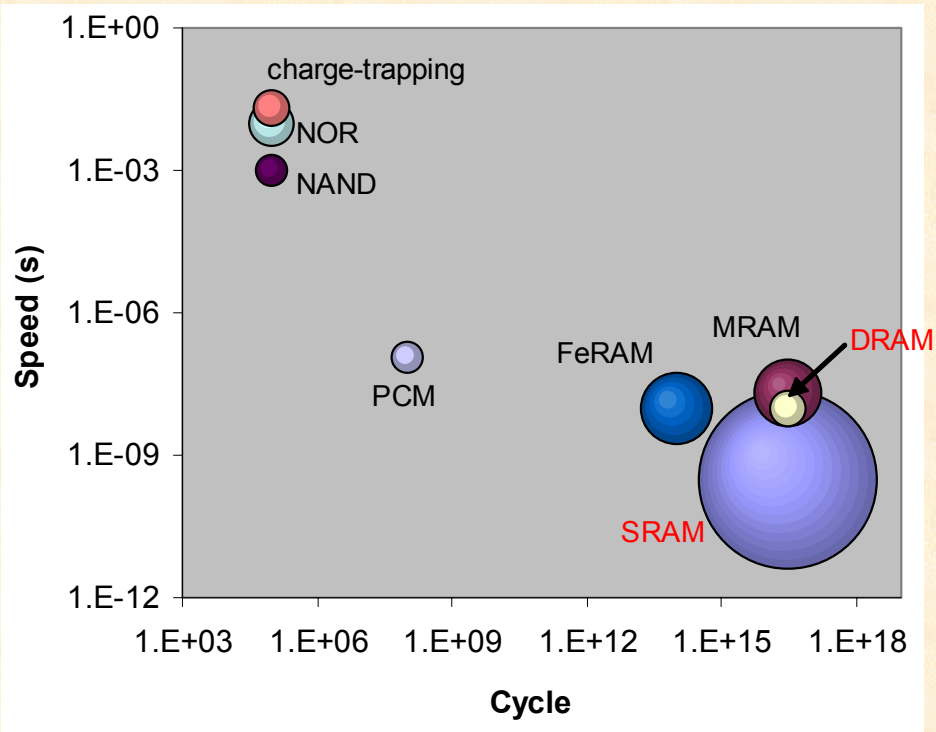
Memory Technologies

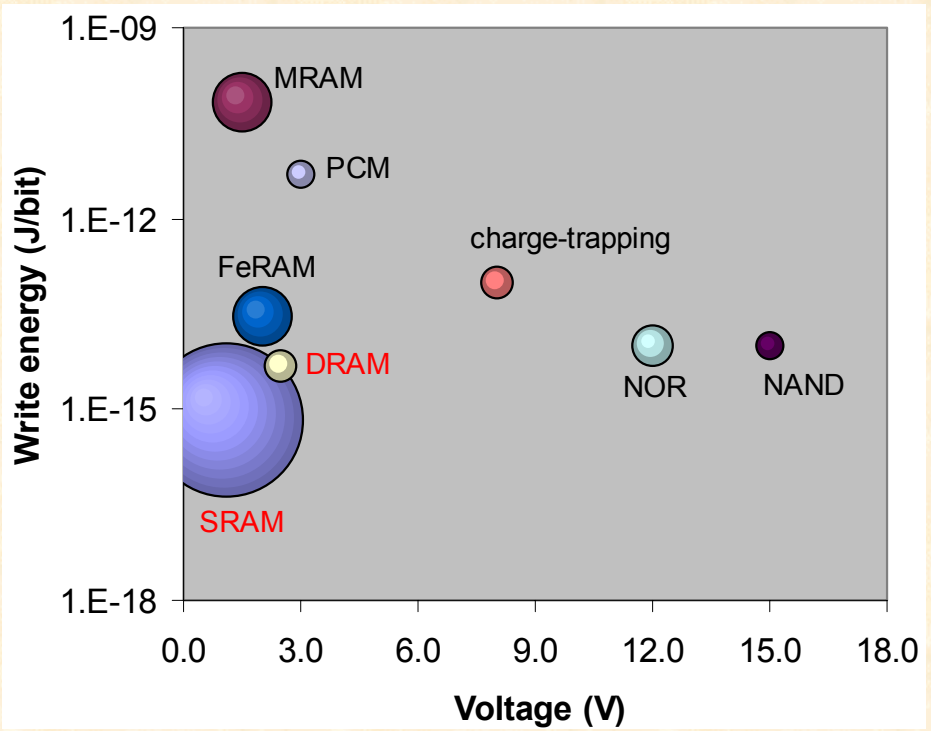


Baseline and Prototypical Memory Technologies

- Mature non-volatile memories (e.g., NAND, NOR) are relatively slow in speed, have limited cycling endurance, and high operating voltage
- Novel memory technologies have certain advantages, but also face challenges

speed – cycling endurance – write energy – operation voltage – size



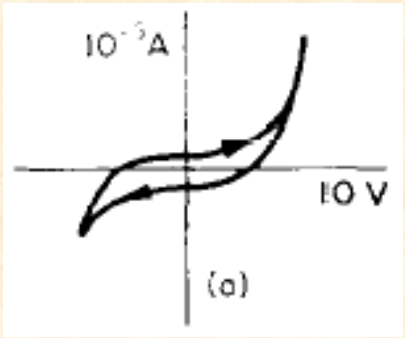


** The symbol size is proportional to the cell size of each memory device*

ITRS Emerging Research Device Report (2007)

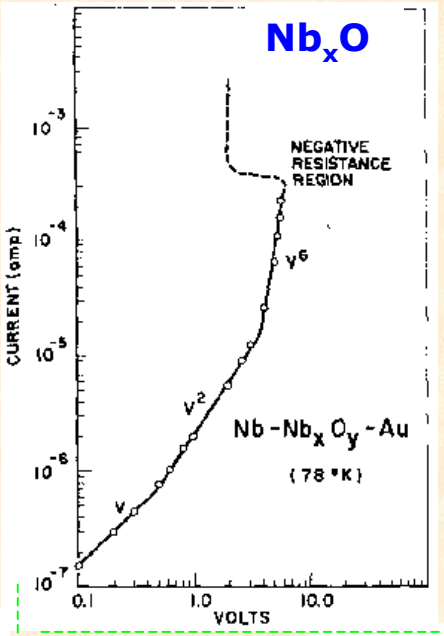
Early Report of Resistive Switching in Oxides

TiO_x



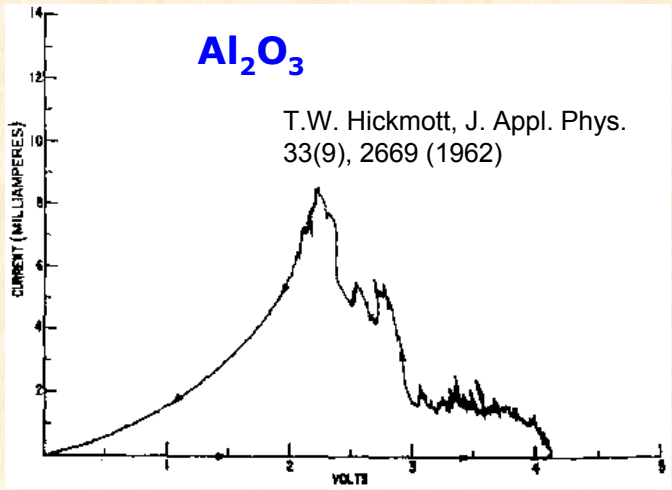
F. Argall, Solid State Electron. 11, 535 (1968)

Nb_xO



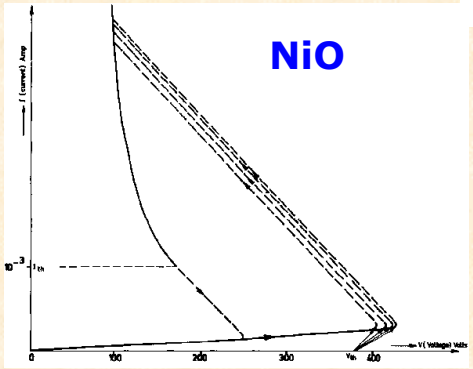
K.L. Chopra, J. Appl. Phys. 16(1), 184 (1965)

Al_2O_3



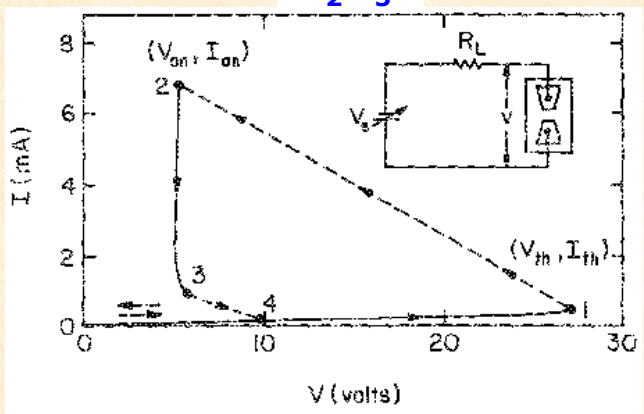
T.W. Hickmott, J. Appl. Phys. 33(9), 2669 (1962)

NiO



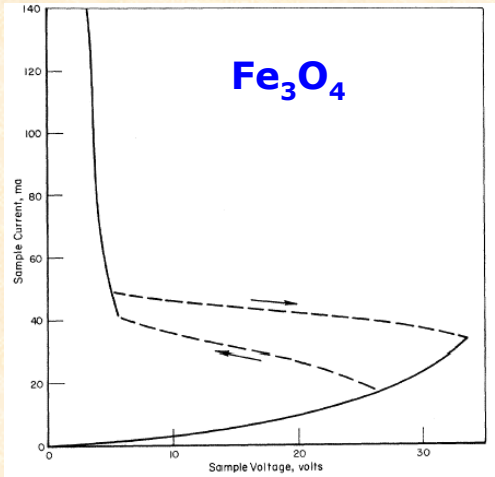
J.C. Bruyere, et al., Appl. Phys. Lett. 16(1), 40 (1970)

V_2O_5



J.G. Zhang, et al., J. Appl. Phys. 64(2), 729 (1988)

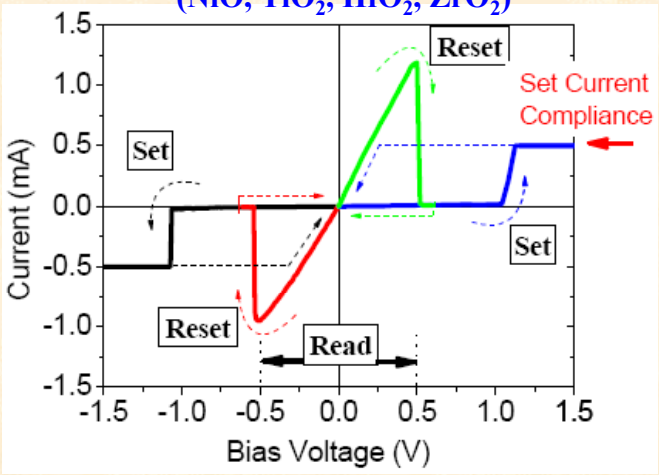
Fe_3O_4



P.J. Freud, et al., Phys. Rev. Lett. 23(25), 1440 (1969)

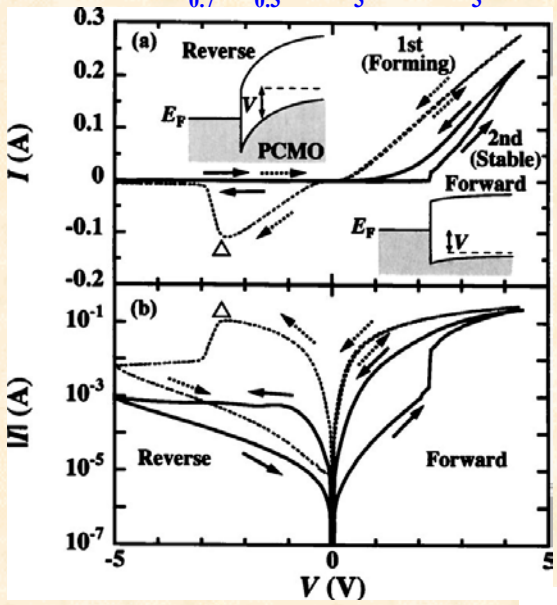
Recent Progress in Resistive Switching Devices

Transitional metal oxide (NiO, TiO_2, HfO_2, ZrO_2)



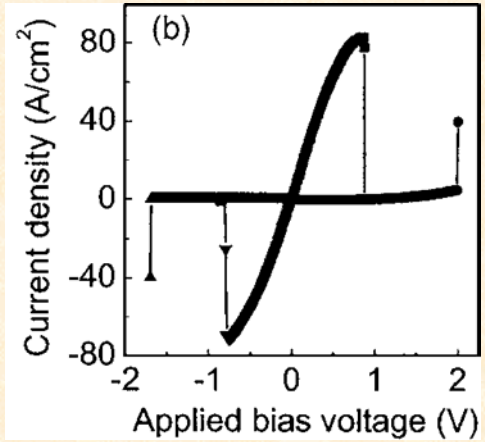
I.G.Baek, et al, IEDM 2004

$Ti/Pr_{0.7}Ca_{0.3}MnO_3/SrRuO_3$



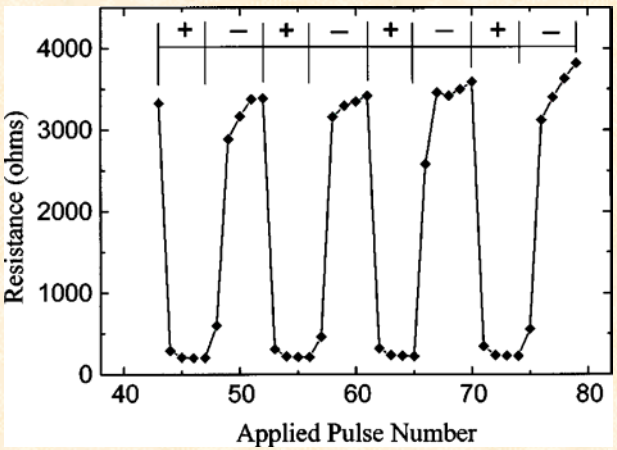
A. Sawa, et al, APL 85, 4073 (2004)

$Pt/TiO_2/Ru$



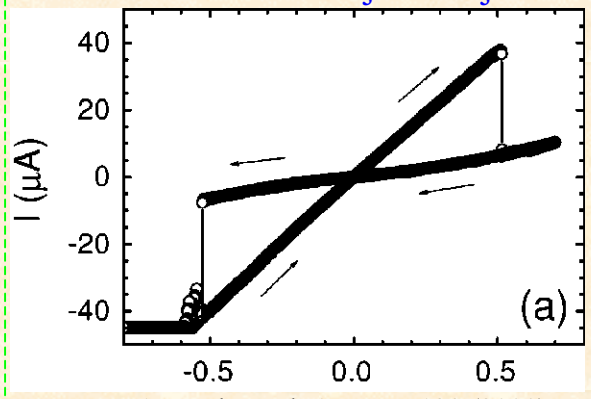
B. J. Choi, et al, JAP 98, 033715 (2005)

$Ag/Pr_{0.7}Ca_{0.3}MnO_3/YBa_2Cu3O_{7-x}$



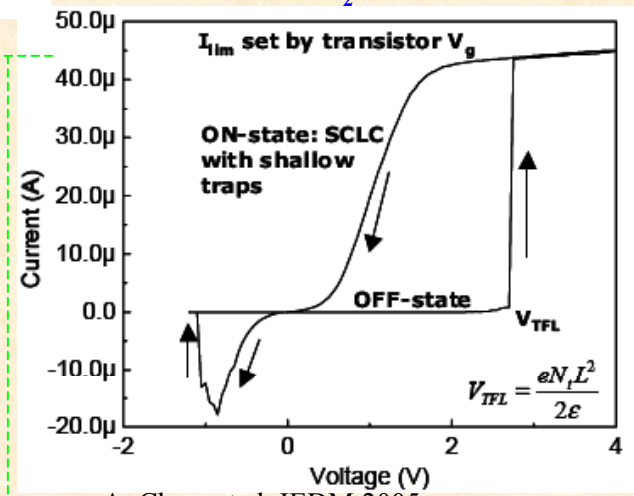
S.Q. Liu, et al, APL 76, 2749 (2000)

$Au/SrZrO_3/SrRuO_3$



A. Beck, et al, APL 77, 139 (2000)

$Ti/Cu_2O/Cu$



A. Chen, et al, IEDM 2005

Signatures of Switching Mechanisms

Materials

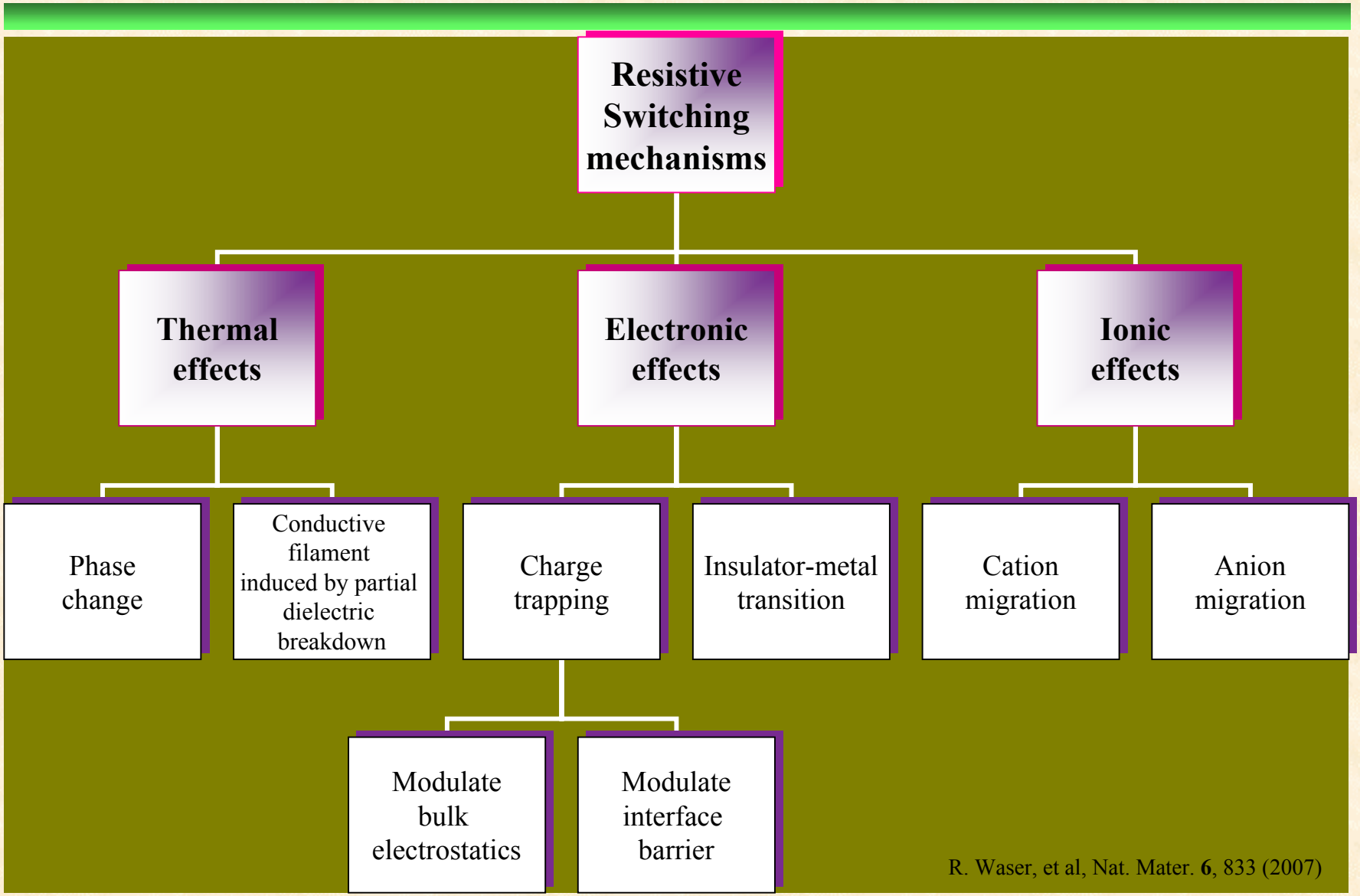
- Composition/processing effect on switching
- Electrode-dependence

Operation

- Forming process
- Switching polarity-dependence (bipolar vs. unipolar)
- Symmetry in I-V and switching characteristics
- Interface effect (rectifying *vs*. ohmic I-V)
- Frequency-dependence
- Device size-dependence
- Temperature effect

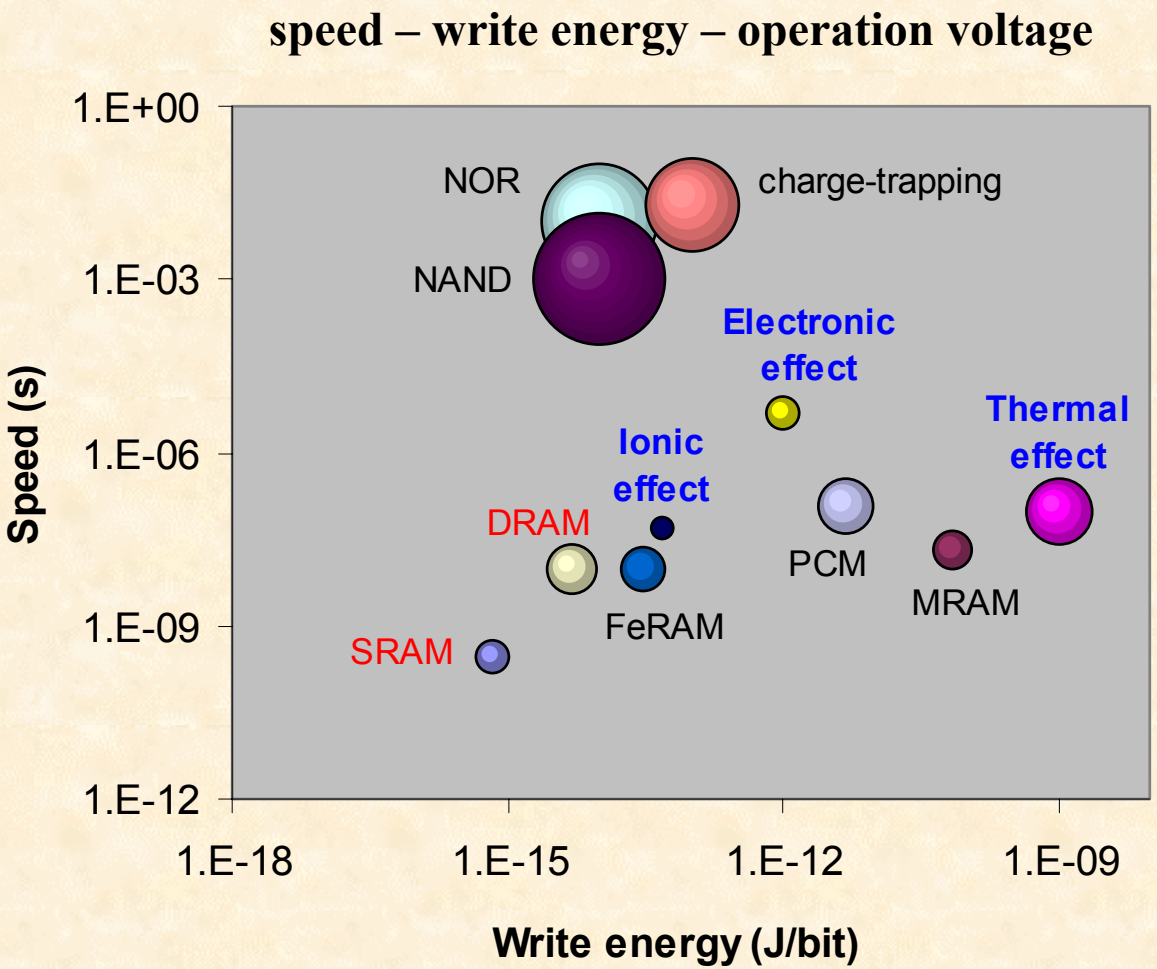
……

Resistive Switching Mechanisms



R. Waser, et al, Nat. Mater. **6**, 833 (2007)

RRAM Comparison with Other Memories



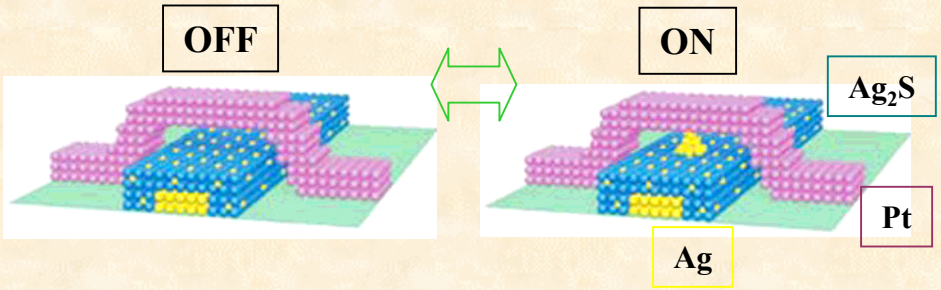
** The symbol size is proportional to the operation voltage of each memory device*

ITRS Emerging Research Device Report (2007)

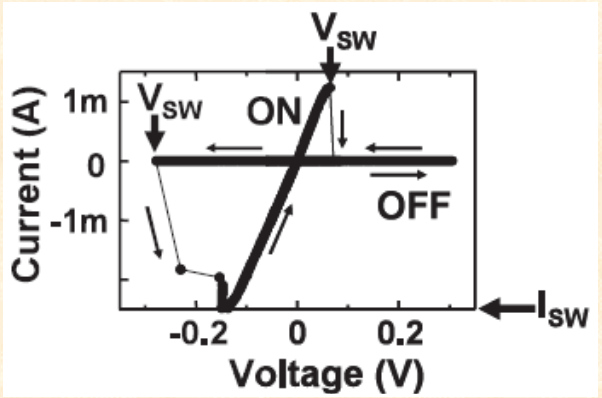
RRAM advantages:

- Non-volatile
- Low voltage
- Low energy
- Fast speed
- Scalable
- Stackable
- CMOS compatible

Resistive Switching in Solid-State Electrolytes

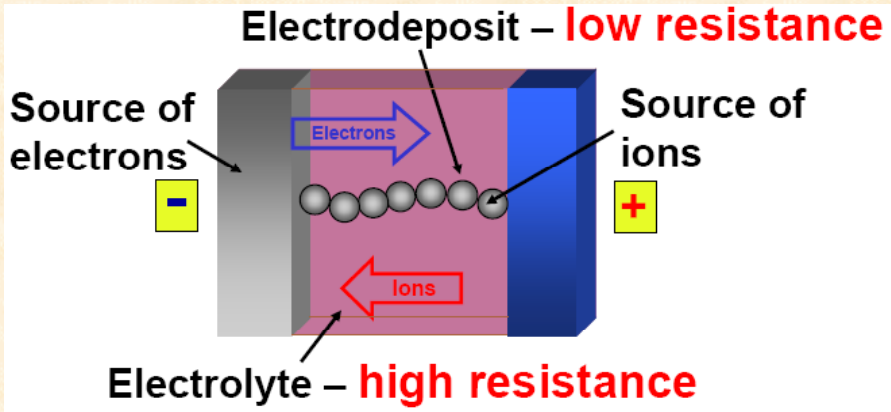


Typical switching I-V



N. Banno, et al, IEIC Trans. Electron. **E89**, 1492 (2006)

A quantized conductance switch is formed by electrochemical formation and annihilation of an atomic bridge between an inert electrode and an oxidizable electrode.

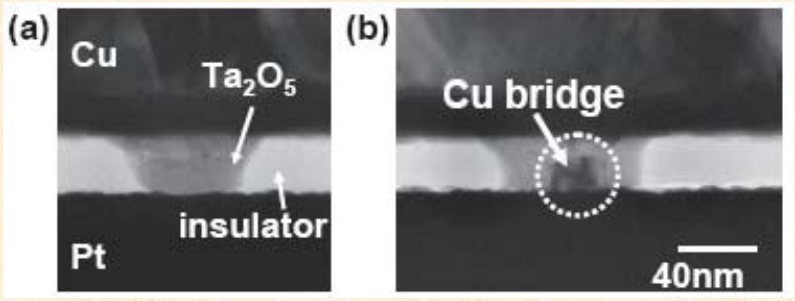


Source: M. Kozicki, ASU

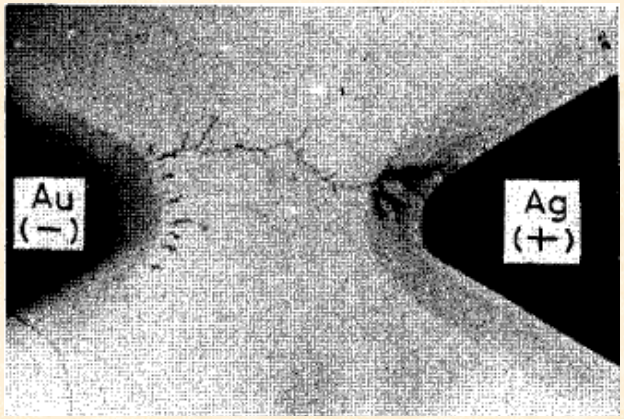
Multiple names for this type of devices

- **Atomic switch**
- **Ionic Memory**
- **NanoBridge** (NEC/JST)
- **Solid-State Electrolytic Memory** (Sony)
- **Programmable Metallization Cell** (ASU)
- **Conductive Bridging RAM** (Qimonda)

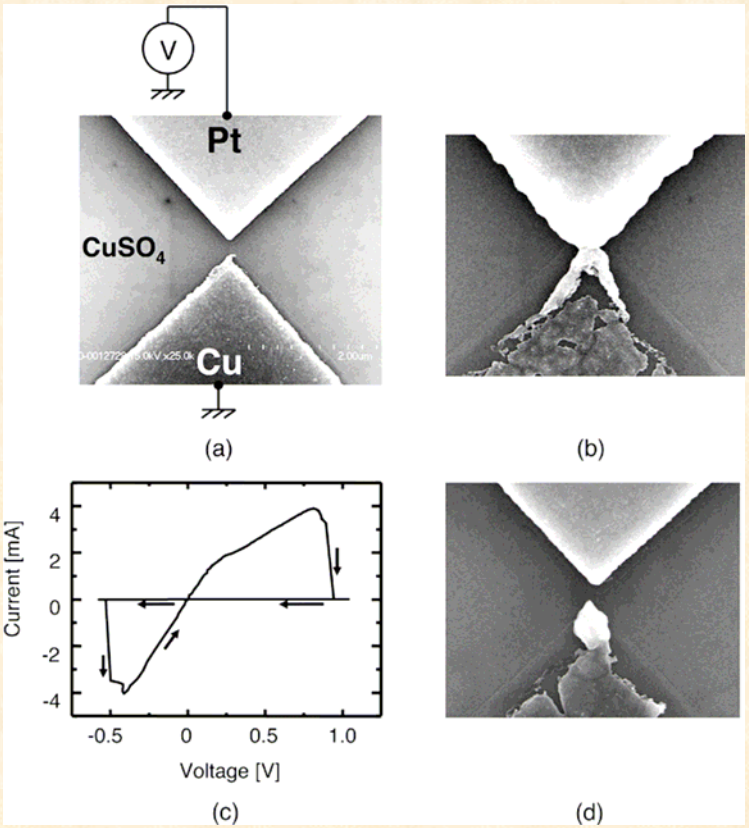
Images of Formation and Annihilation of Conductive Channels



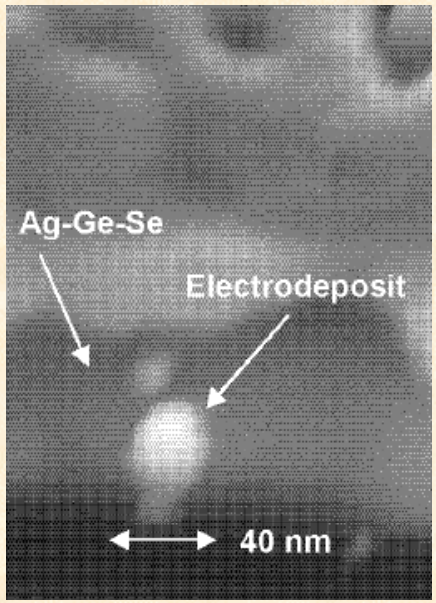
T. Sakamoto, *et al*, Symposium VLSI Tech., pp.38 (2007)



Y. Hirose, et al, JAP 47, 2767 (1976)

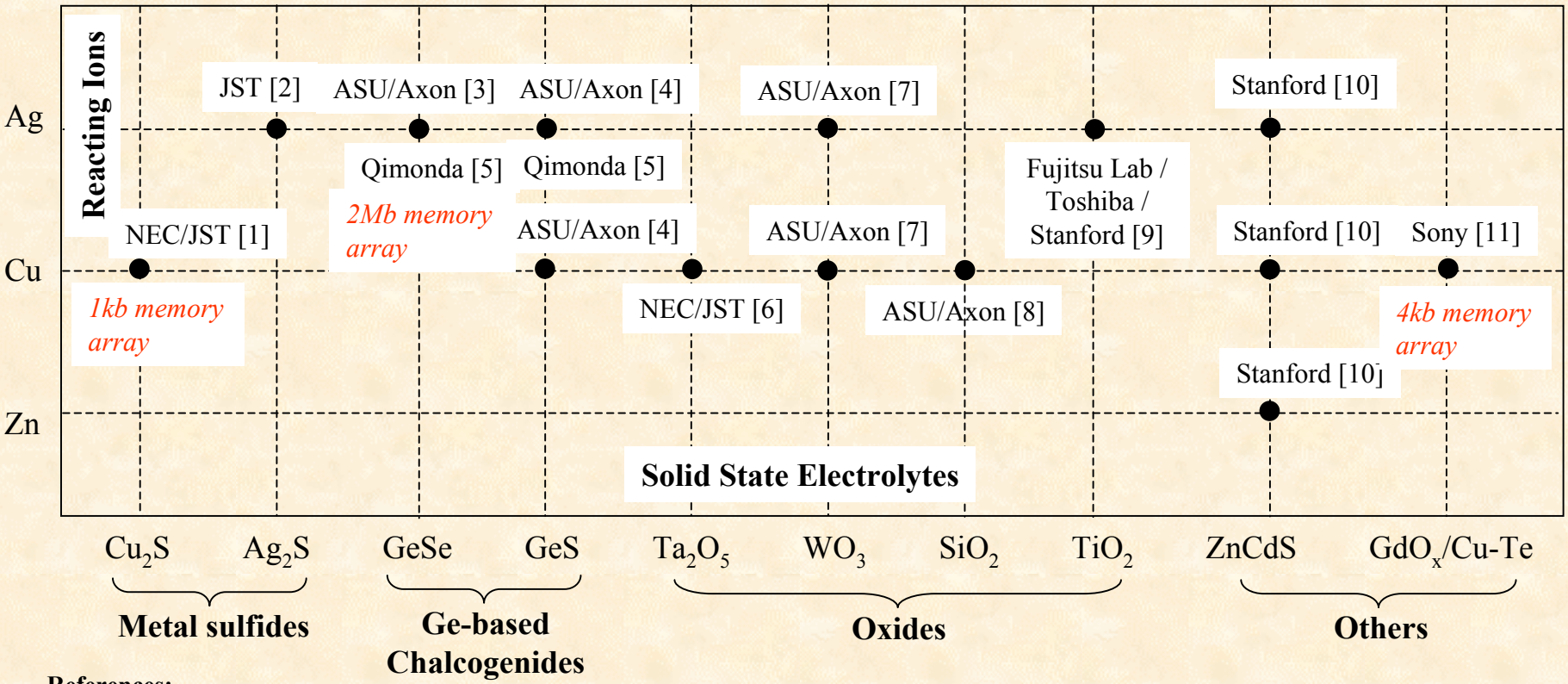


M. Kozicki, et al, NVMTS Proceedings, 111 (2006)



S. Kaeriyama, et al, IEEE J. Solid-State Circuits **40**, 168 (2005)

Ionic Memory Based on Cation-Migration



References:

1. S. Kaeriyama, *et al*, IEEE J. Solid-State Circuits **40**, 168 (2005);
2. K. Terabe, *et al*, Nature **433**, 47 (2005);
3. M.N. Kozicki, *et al*, IEEE Trans. Nanotech. **4**, 331 (2005);
4. M.N. Kozicki, *et al*, NVMTS proceeding, pp.83 (2005);
5. S. Dietrich, *et al*, IEEE J. Solid-State Circuits **42**, 839 (2007);
6. T. Sakamoto, *et al*, Symposium VLSI Tech., pp.38 (2007);
7. M.N. Kozicki, *et al*, NVMTS, pp.10 (2004);
8. C. Schindler, *et al*, IEEE Trans. Electron Dev. **54**, 2762 (2007);
9. K. Tsunoda, *et al*, Appl. Phys. Lett. **90**, 113501 (2007);
10. Z. Wang, *et al*, IEEE Electron Dev. Lett. **28**, 14 (2007);
11. K. Aratani, *et al*, IEDM Tech. Dig., pp.783 (2007).

Ionic Memory: Device Characteristics

Materials		Sulfides		Chalcogenides			Oxides		
		Ag/Ag_2S [1]	Cu/Cu_2S [2]	Ag/GeSe [3]	Ag/GeS [4]	Cu/GeS [4]	Cu/Ta_2O_5 [5]	Cu/WO_3 [6]	Cu/SiO_2 [7]
Thickness (nm)		----------	~ 40	~ 50	60	60	15	50	12
Device size		$150\times100nm^2$	d =30nm	d = 75nm	d=240nm	d = 300nm	d=0.2-10μm	d=240nm	d = 1μm
HRS → LRS (DC)	**V_{SW} (V)**	< 0.4	~ 0.3	~ 0.2	~ 0.45	~ 0.3	~ 2.5	0.4	~ 0.9
	I_{SW} (μA)	----------	2500	10	10	10	100	1	5
LRS → HRS (DC)	**V_{SW} (V)**	< 0.4	~ 0.1	< 0.5	~ 0.25	< 0.1	~ 1.0	0.2	~ 0.15
	I_{SW} (μA)	----------	1000	< 10	< 10	< 2	~ 1000	< 1	~ 2
Switching time (s)		$< 10^{-6}$	$< 10^{-4}$	$< 10^{-7}$	$< 10^{-7}$	$< 10^{-7}$	10^{-5}-10^{-4}	----------	$< 10^{-6}$
R_{on} (Ω) / R_{off} (Ω)		$10^3/10^5$	$10^2/10^4$	$10^4/10^7$	$10^4/10^{11}$	$10^4/10^{10}$	$10^2/10^6$	$10^5/10^9$	$10^4/10^7$
Retention		----------	0.25 yrs	---------	> 10^5 s	----------	10 yrs	>10^4 s	> 10^5 s
Cycle		10^5	> 10^3	10^{11}	----------	----------	10^4	10^5	10^7

* *HRS: high resistance state; LRS: low resistance state*

References:

1. K. Terabe, *et al*, Nature **433**, 47 (2005);
2. S. Kaeriyama, *et al*, IEEE J. Solid-State Circuits **40**, 168 (2005);
3. M.N. Kozicki, et al, IEEE Trans. Nanotech. **4**, 331 (2005);
4. M.N. Kozicki, *et al*, NVMTS proceeding, pp.83 (2005);
5. T. Sakamoto, *et al*, Symposium VLSI Tech., pp.38 (2007);
6. M.N. Kozicki, *et al*, IEEE Trans. Nanotech. **5**, 535 (2006);
7. C. Schindler, *et al*, IEEE Trans. Electron Dev. **54**, 2762 (2007).

Ionic Memory: Array Characteristics

Company		**NEC/JSTA** [1]	**Qimonda** [2]	**Sony** [3]
Tested array size		1 kbit	2 Mbit	4 kbit
Material system		Cu / Cu_2S	Ag / GeSe or GeS	Cu-Te / GdO_x
Technology node		250 nm CMOS	90 nm CMOS	180 nm CMOS
Minimum tested cell size		D ~ 30 nm	D = 20 nm	D = 20 nm
Memory structure		1T-1R	1T-1R	1T-1R
Programming (HRS → LRS)	**Voltage**	1.1 V	≥ 0.6 V	3 V
	Current	----------	10 μA	110 μA
	Pulse width	5 – 32 μs	≤ 50 ns	5 ns
Erasing (LRS → HRS)	**Voltage**	1.1 V	≤ 0.2 V	1.7 V
	Current	----------	20 μA	125 μA
	Pulse width	5 – 32 μs	≤ 50 ns	1 ns
Retention	**Measured**	10^3 s under 35 mV	10^5 s @ 70°C	100 hrs @ 130°C
	Projected	3 months	10 years	10 years
R_{on} / R_{off}		≤ 10^2 Ω / ≥ 10^3 Ω	10^4 Ω / 10^{11} Ω	10^4 Ω / 10^6-10^8 Ω
Endurance		10^3 – 10^4 cycles	10^6 cycles	10^7 cycles
Operating Temperature		----------	≥ 110°C	≥ 130°C

[1] S. Kaeriyama, IEEE JSSC **40**, 168 (2005); [2] S. Dietrich, IEEE JSSC **42**, 839 (2007); [3] K.Aratani, IEDM Tech. Dig., pp.783 (2007)

Compare with Other Resistive Switching Memories

Company		Samsung [1]	Spansion [2]	Sharp [3]	Many others
Tested array size		----------	64 kbit	64 bit	Many binary and complex metal oxides have been tested on resistive switching properties, e.g., TiO_x, ZrO, Nb_2O_5, V2O5, $SrTiO_3$, $SrZrO_3$, $LaMnO_3$, *etc*. The switching mechanisms are controversial.
Material system		TMO (e.g., NiO)	TMO (e.g., Cu_2O)	$Pr_{0.7}Ca_{0.3}MnO$	
Technology node		180 nm CMOS	180 nm CMOS	0.5 μm CMOS	
Minimum tested cell size		D ~ 70 nm	D ~ 180 nm	D = 0.8 μm	
Memory structure		1T-1R	1T-1R	1T-1R	
Programming (HRS → LRS)	Voltage	< 3 V	~ 3 V	~ 5 V	
	Current	< 1 mA	< 100 μA	< 200 μA	
	Pulse width	< 10 ns	< 50 ns	~ 20 ns	
Erasing (LRS → HRS)	Voltage	< 1 V	< 1.5 V	~ 5 V	
	Current	< 2 mA	< 100 μA	< 200 μA	
	Pulse width	< 5 μs	< 50 ns	~ 10 ns	
Retention	Measured	8 months	10^5 s @ 90°C	----------	
	Projected	10 years	10 years	----------	
R_{on} / R_{off}		~500 Ω / ~50 kΩ	< 50 kΩ / > 1 MΩ	< 100 kΩ / > 1M Ω	
Endurance		10^6 cycles	> 10^3 cycles	10^5 cycles (?)	
Operating Temperature		300°C	> 90°C	> 200°C	

[1] I.G. Baek, IEDM Tech. Dig., pp.587 (2004); [2] A. Chen, IEDM Tech. Dig., pp.765 (2005); [3] W.W. Zhuang, IEDM Tech. Dig., pp.193 (2002)

Ionic Memory: Advantages *vs.* Challenges

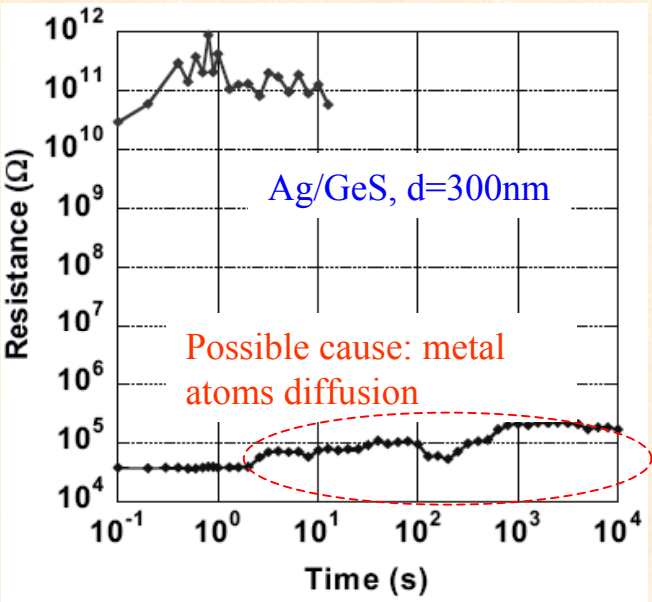
Advantages	**Challenges**
• Scalable • Compatible with CMOS • Low switching voltage/current • Nonvolatile switching states • Stackable for 3D IC • (Relatively) well-understood mechanism	• Reliability / endurance • Switching speed • Operating temperature • Defect/fault tolerance • Mixed mechanisms

Other features

- Low processing temperature
- Potential for novel architectures

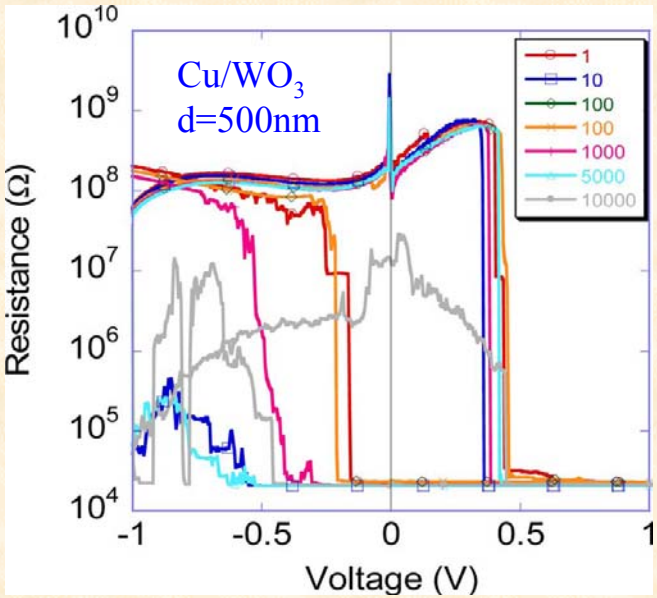
Ionic Memory: Reliability Issues

Reliability concerns	Possible effects
• Over-programming or over-erasing	• R_{on}/R_{off} variation; cycling failure
• Random diffusion of migrating ions	• Variation in switching parameters
• Diffusion of metal atoms	• R_{on} variation; retention failure
• Temperature sensitivity	• Material degradation; switching failure
• Inherent impurities	• Poor uniformity; instability



Retention

Endurance

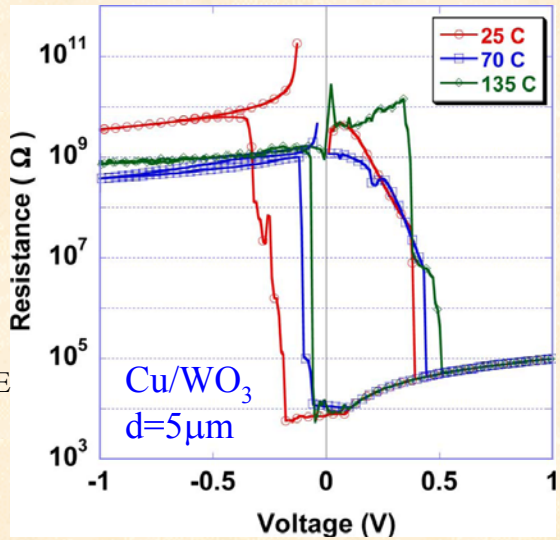


M.N. Kozicki, et al, NVMTS proceeding, pp.83 (2005)

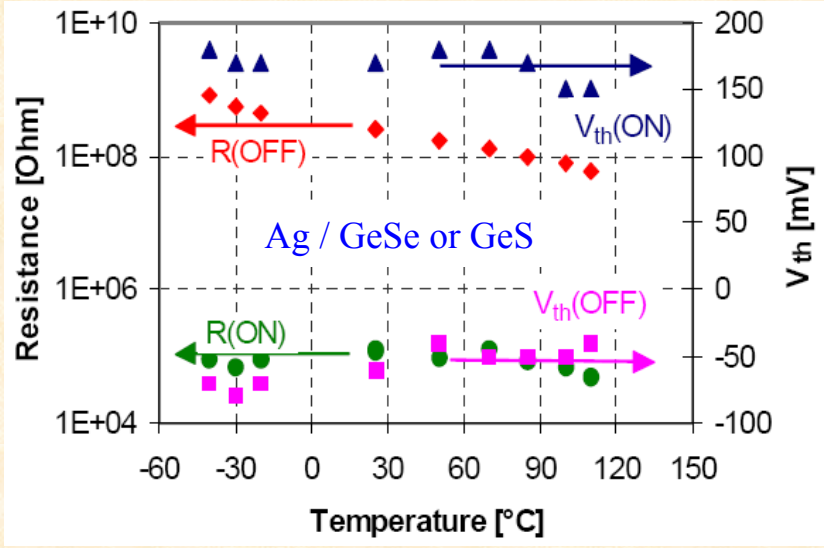
M.N. Kozicki, et al, IEEE Trans. Nanotech. **5**, 535 (2006)

Ionic Memory: Reliability Issues

Temperature effect

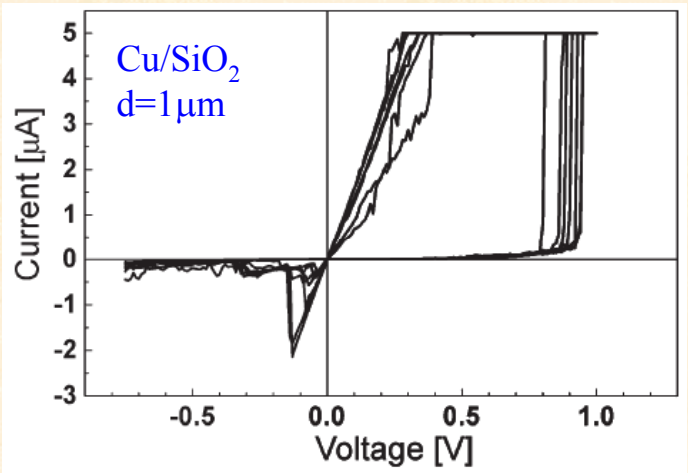


M.N. Kozicki, et al, IEEE Trans. Nanotech. 5, 535 (2006)

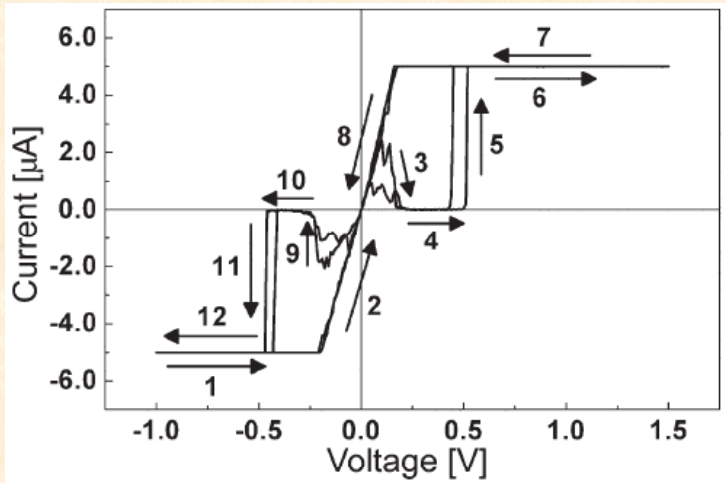


S. Dietrich, et al, IEEE JSSC **42**, 839 (2007)

Mixed switching types



Bipolar to unipolar

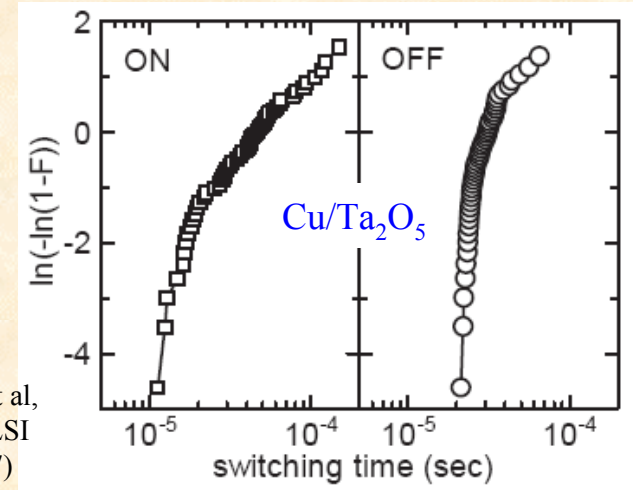


C. Schindler, et al, IEEE Trans. Electron Dev. **54**, 2762 (2007)

Ionic Memory: Switching Speed

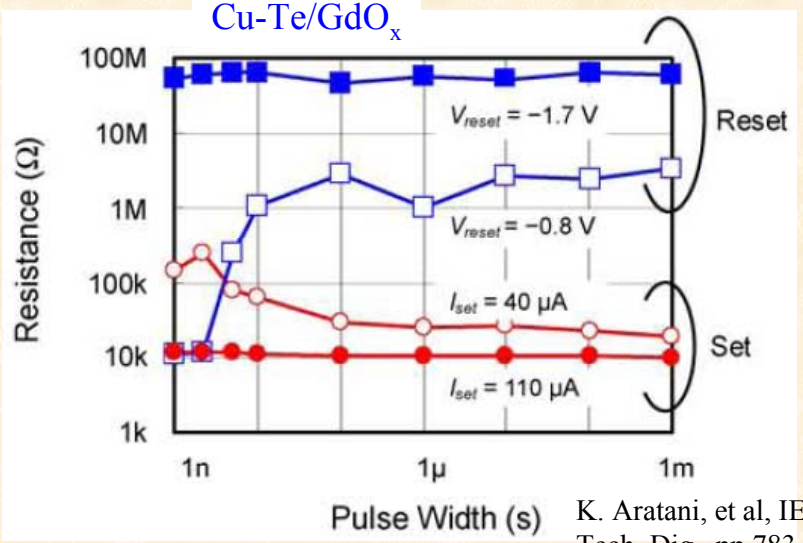
Switching = **Ion migration in solid electrolyte** + **Electrochemical reaction at cathode**

- Switching speed is determined by the speed of ion migration and electrochemical reaction
- Large variation on switching speed across different material systems (maybe due to parasitic RC delay)
- Switching speed on the order of ns has been demonstrated in chip-level measurement



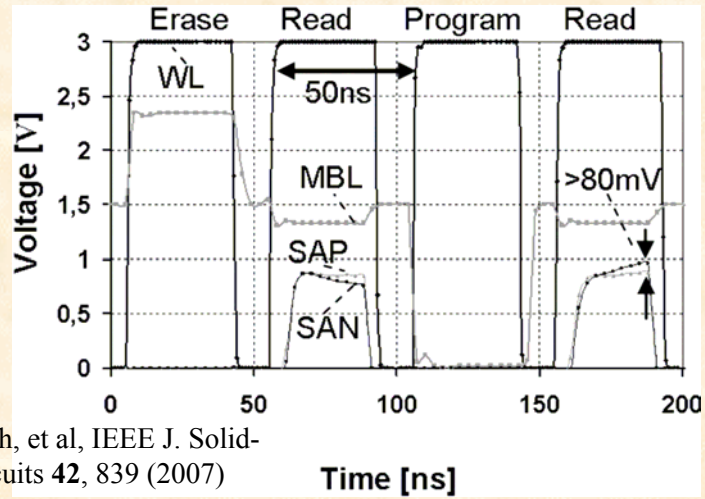
T. Sakamoto, et al, Symposium VLSI Tech., 38 (2007)

Cu-Te/GdO_x



K. Aratani, et al, IEDM Tech. Dig., pp.783 (2007)

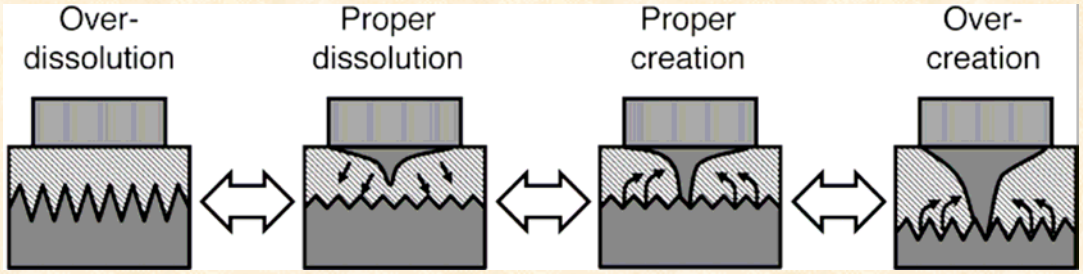
Ag / GeSe or GeS

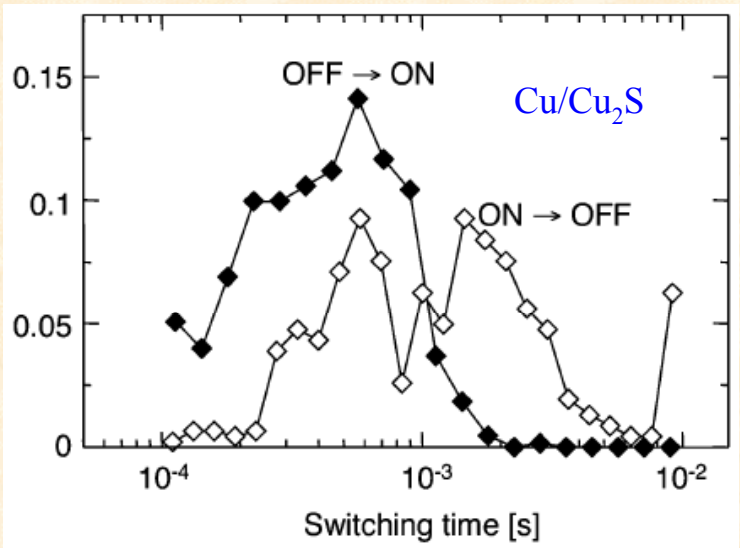


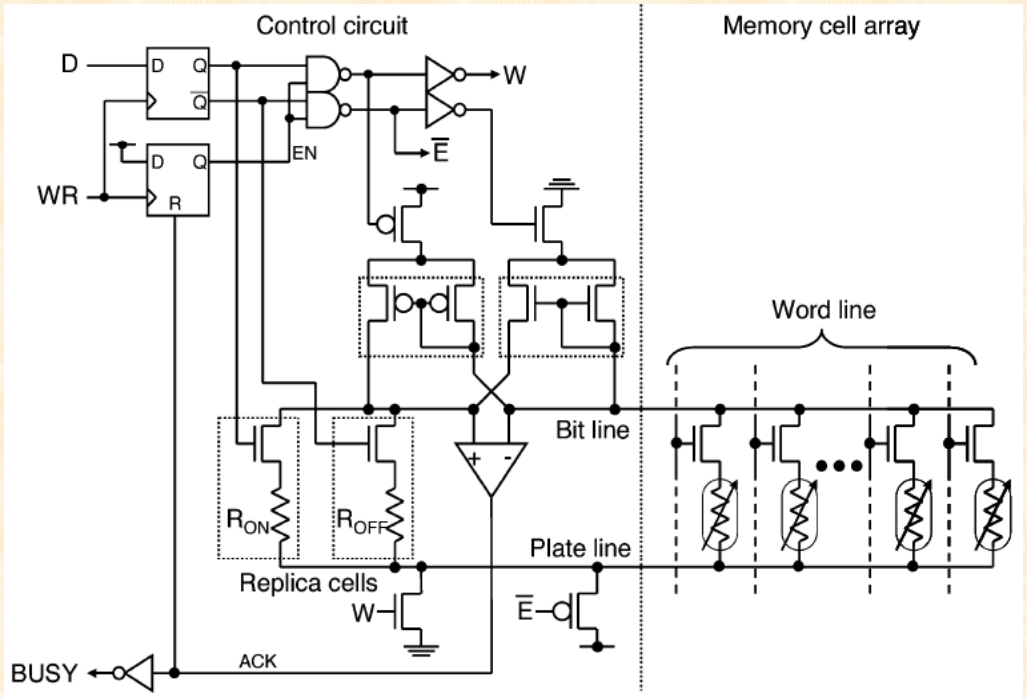
S. Dietrich, et al, IEEE J. Solid-State Circuits **42**, 839 (2007)

Ionic Memory: Over-Programming, Over-Erasing

Over-programming and over-erasing lead to long switching time, large variation on switching parameters, and short endurance. Sensing/control circuits are needed to alleviate this problem.

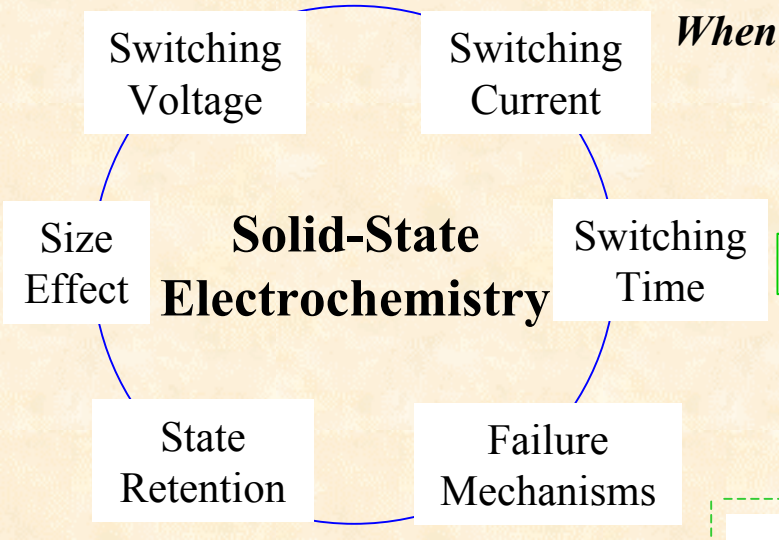






S. Kaeriyama, et al, IEEE J. Solid-State Circuits **40**, 168 (2005)

Quantitative Modeling of Ionic Memory



When nanoelectronics meet nanoionics …

- **Energy**
- **Speed**
- **Scalability**
- **Endurance**
- **Retention**

✓ **Benchmark and projection**

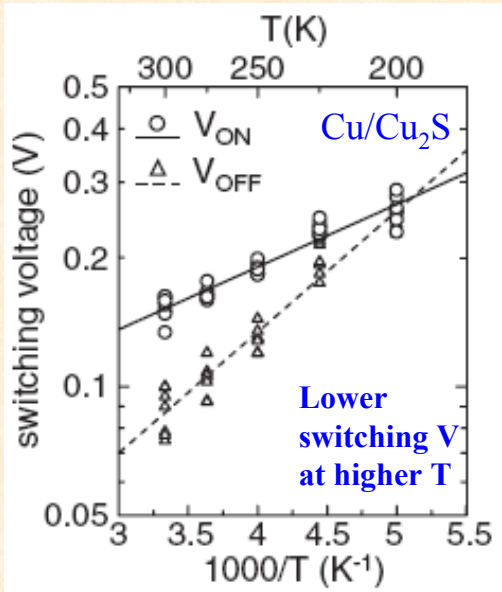
✓ **Device/process optimization**

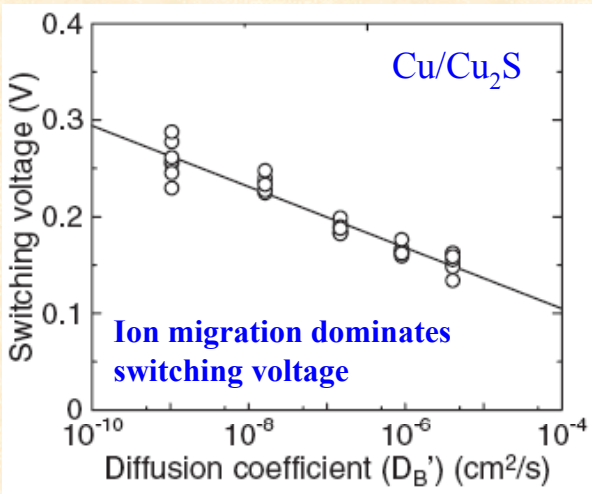
✓ **Architecture design**

Many questions to be addressed:

- Microscopic nature of the cation conduction paths?
- Details of electrode reactions?
- Impact of thermal effects?
- Fundamental speed limits?
- Fundamental scaling limits?
- Temperature effects?
- Failure mechanisms?

…

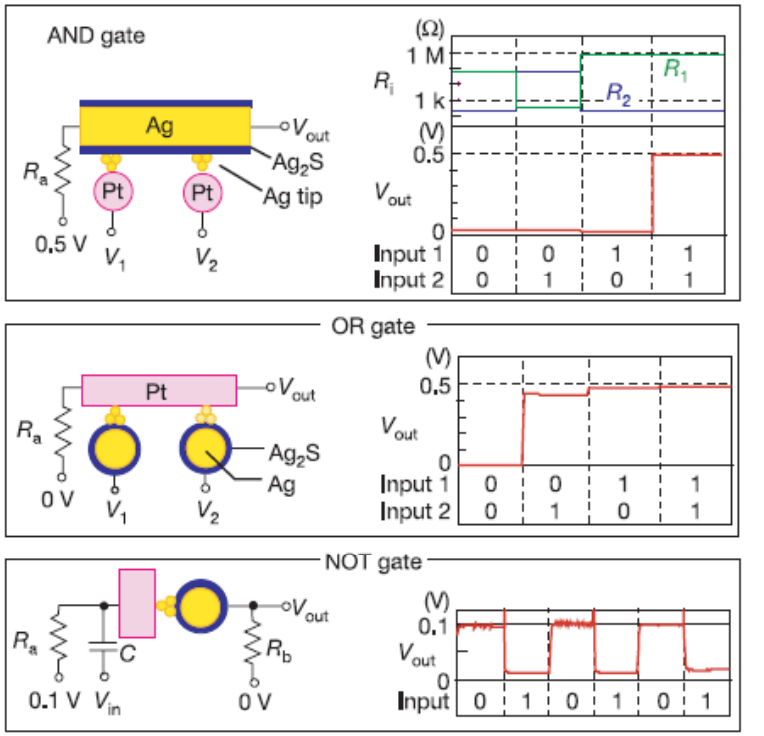




N. Banno, et al, Jpn J. Appl. Phys. **45**, 3666 (2006)

Novel Logic Gates Based on Hysteretic Resistors

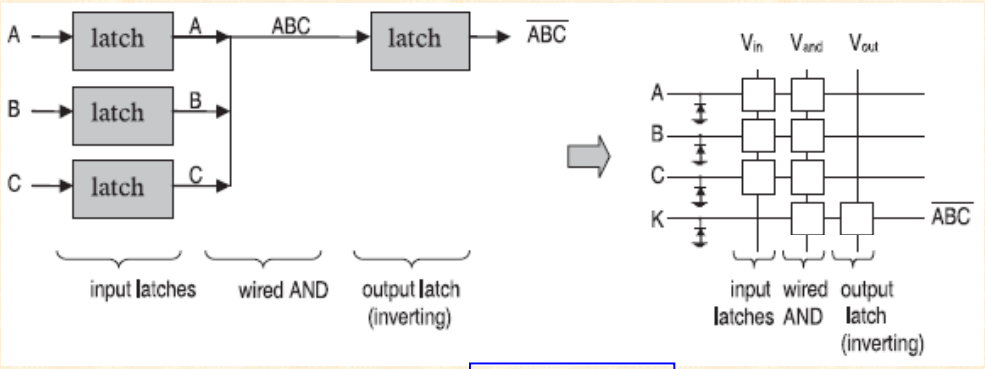
Logic gates based on atomic switch



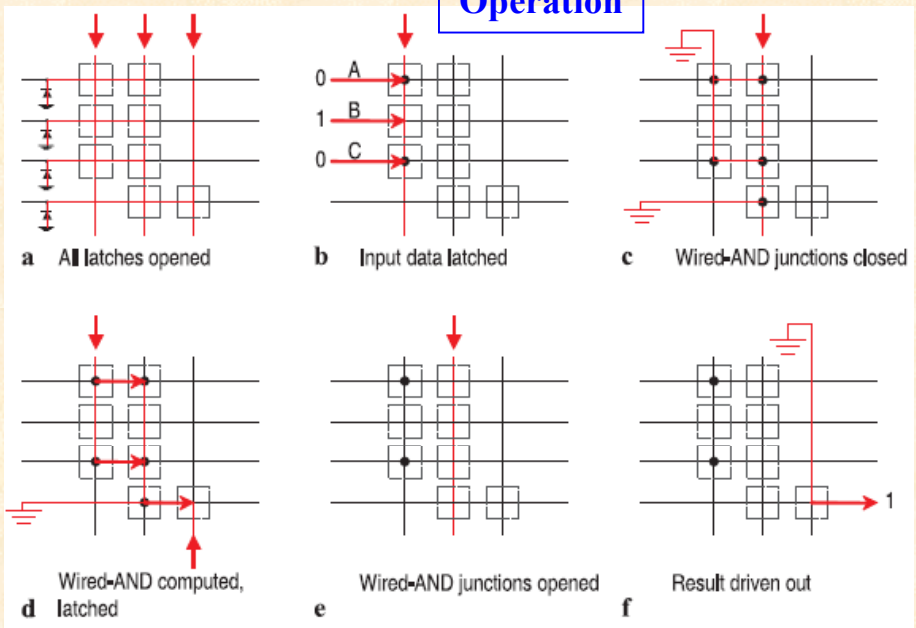
Logic gates configured with QCASs. **a**, Schematic diagram of an AND gate using QCASs (left) and its operating result (right). **b**, Schematic diagram of the OR gate (left) and its operating result (right). **c**, Schematic diagram of the NOT gate (left) and its operating result (right). Resistors R_a (10 kΩ) and R_b (1 kΩ), and a capacitor C (100 pF), are used. V_1 and V_2 are applied as input bias voltages. Input level 1 is 0.5 V for the AND and OR gates, and 1.5 V for the NOT gate. Input level 0 is 0 V for all gates. Input levels were changed every second.

K. Terabe, et al, Nature **433**, 47 (2005)

Crossbar NAND gate

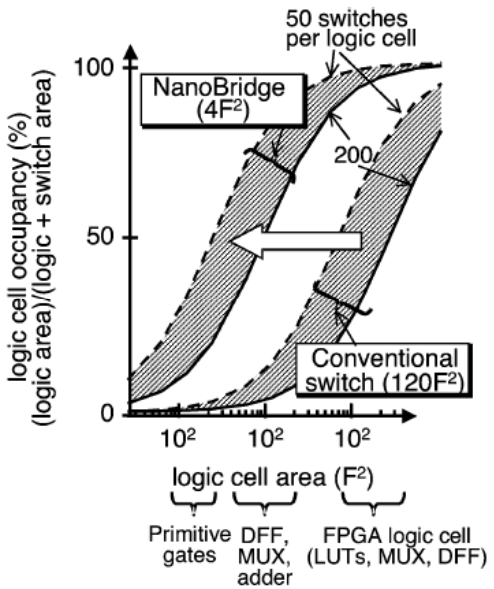


Operation

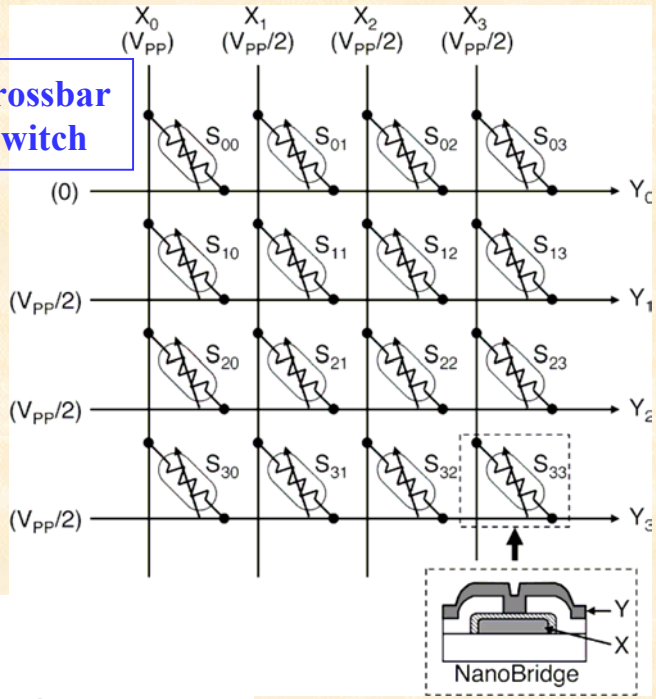


G. Snider, Appl.Phys. A **80**,1165 (2005)

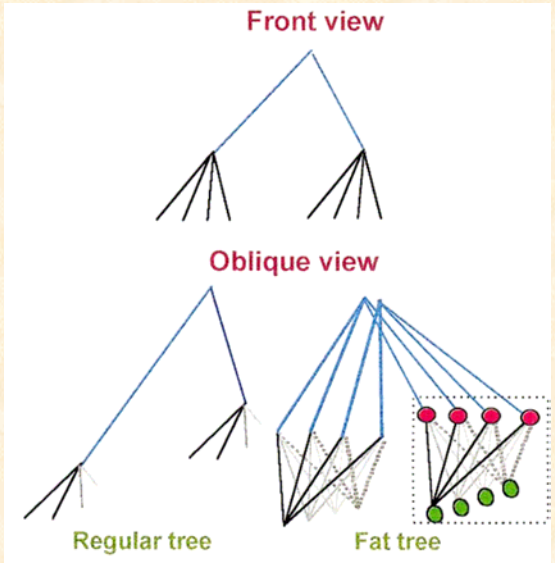
Novel Architectures



Crossbar switch

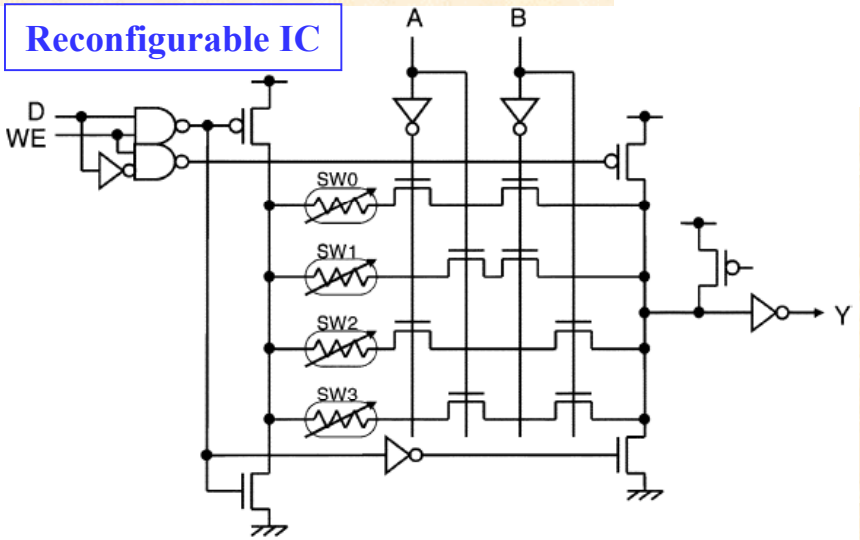


Defect-tolerant architectures



J.R. Heath, et al, Science 280, 1716 (1998)

Reconfigurable IC



	Inputs			Output	
WE	A	B	D	Y	Operation
1	0	0	0	-	Turns SW0 off
1	0	1	1	-	Turns SW1 on
1	1	0	1	-	Turns SW2 on
1	1	1	0	-	Turns SW3 off
0	0	0	-	0	Evaluates SW0 state
0	0	1	-	1	Evaluates SW1 state
0	1	0	-	1	Evaluates SW2 state
0	1	1	-	0	Evaluates SW3 state

Programming operations

Logic operations

- : don't care or unstable

S. Kaeriyama, et al, IEEE J. Solid-State Circuits **40**, 168 (2005);

Summary

- Resistive switching memories involves multiple switching mechanisms.
- Ionic memory devices have the advantages in scalability, energy efficiency, and compatibility with CMOS.
- The major challenges of ionic memory are reliability and speed.
- Novel logic gates and architectures may be possible for resistive switching devices, e.g., reconfigurable IC, stackable memory, defect-tolerant architecture, *etc* .