Wafer-Level Three-Dimensional ICs

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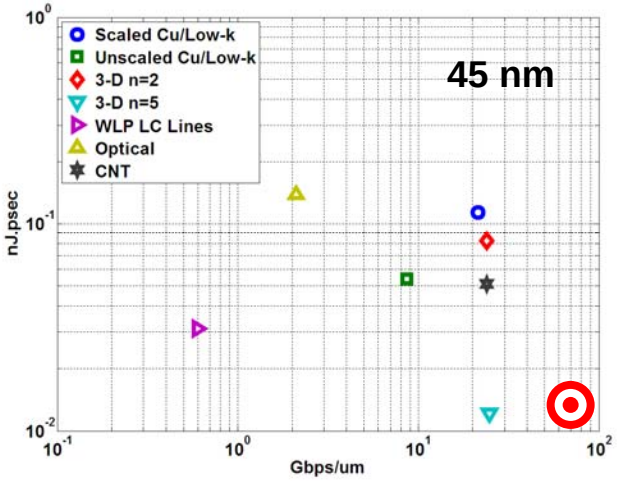

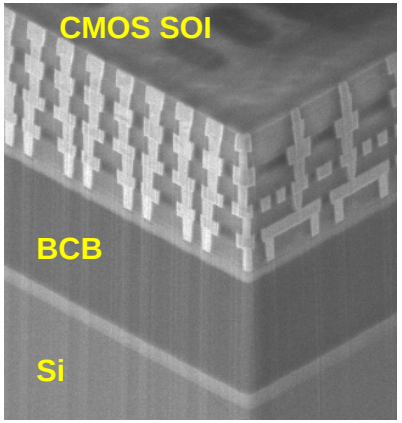

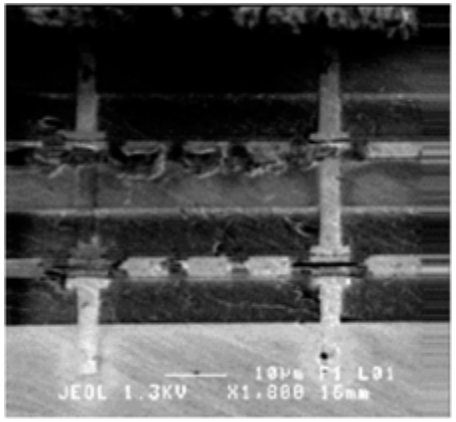

June 2007

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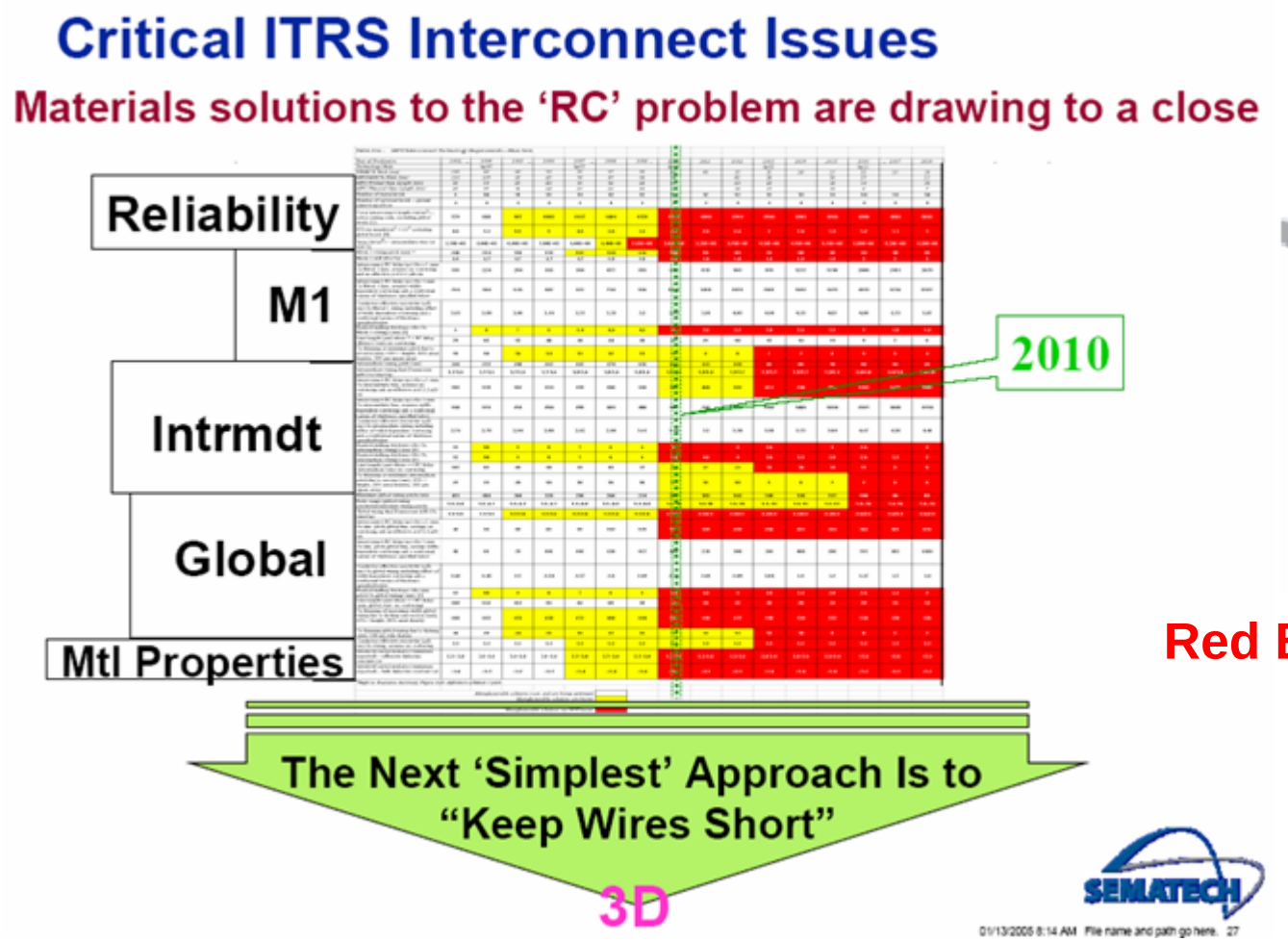
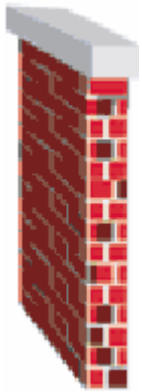
Outline

- Why Desirable (3-8)
  - Alternatives to On-Chip Interconnect Scaling Limits
  - Heterogeneous Component/Subsystem Integration
  - Highest Volume Density of Electronics/Photonics
- Wafer-Level 3D Platforms (9-36)
  - Generation 1 (11-23)
  - Generation 2 (24-30)
  - Reliability Status (31-36)
- Application Examples (37-45)
- Conclusions (46-47)

Interconnect Crisis: Is 3D Interconnects the Solution?



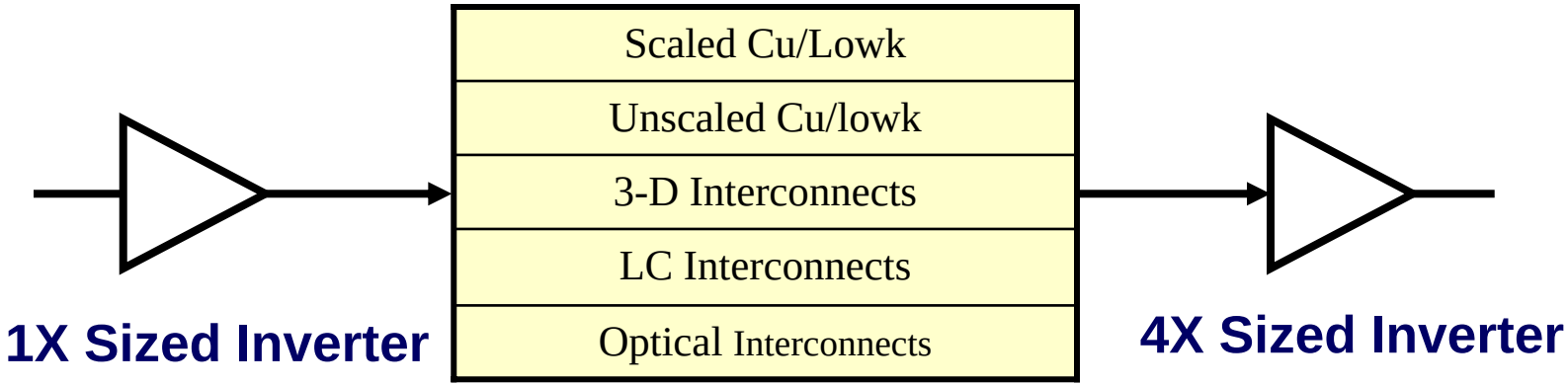


Red Brick Wall

Courtesy : Sematech

ITRS=International Technology Roadmap for Semiconductors

Benchmarking Methodology



Assumptions:

➔ Interconnect System is optimized only to minimize the latency

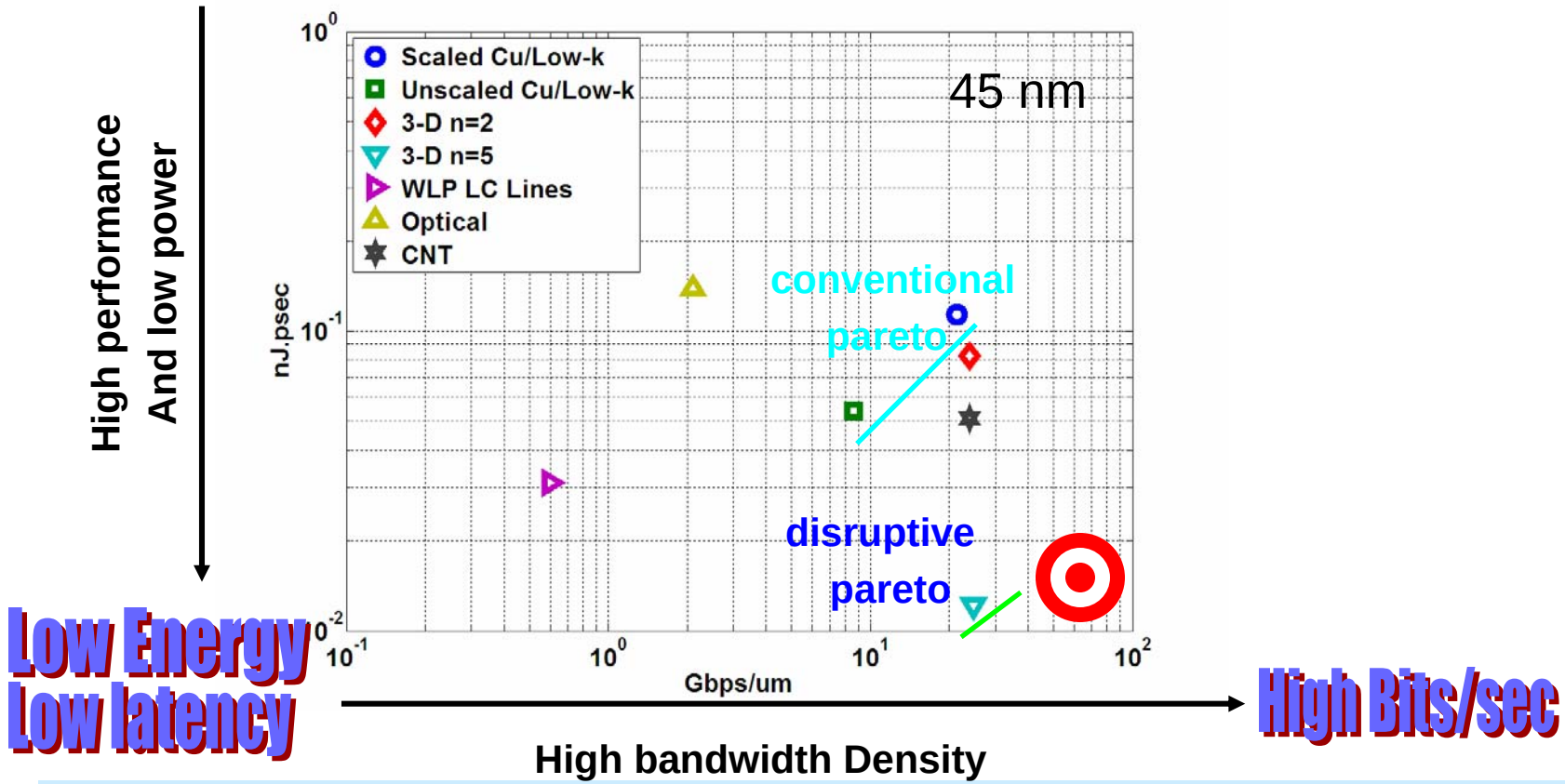
➔ All additional circuit components count towards power overhead

➔ HSPICE is used to perform circuit level simulations for all interconnect technologies. Berkeley PTM Models are used for the front end (45nm)

➔This benchmarking analysis calculates the benchmark metrics based on a unidirectional simple serial propagation of a pulse in an interconnect system. Neither any intelligent signaling strategies or system level optimization are considered nor any multiplexing is assumed (TDM,WDM etc.)

Scott List, IMEC
(M. Bamal, et al., IITC 2006.)

E-D product vs. Gbps/um for 1mm



- 3-D with 5 strata clearly gives the highest bandwidth density for the lowest energy delay product.
- No other technology options give significant advantages over conventional scaled or unscaled Cu/Low k.

Scott List, IMEC
(M. Bamal, et al., IITC2006.)

Summary Chart 1mm (45nm)

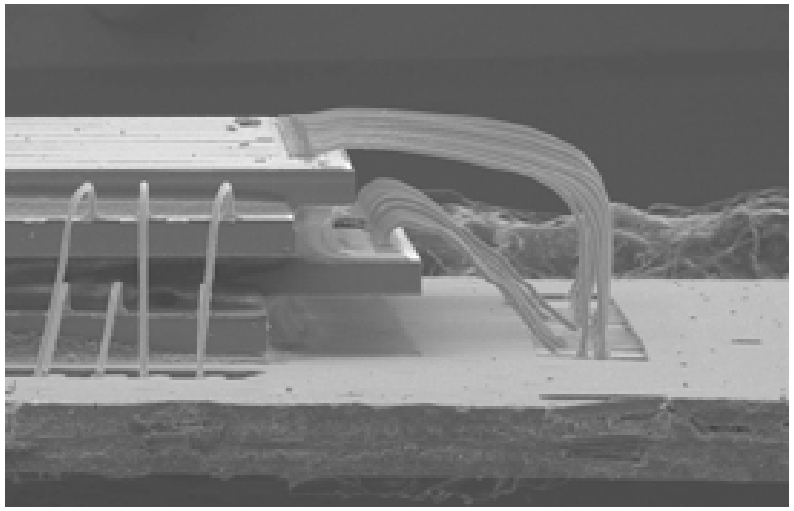
	Scaled Cu/Lowk	Unscaled Cu/Lowk	3-D n=2	3-D n=5	WLP T-Lines	Optical	CNTs
Delay (psec)	**246**	**171**	**201**	**147**	**138**	**195**	**171**
Energy (fJ)	**463**	**314**	**409**	**82.2**	**226**	**711**	**297**
Gbps	**5**	**5.8**	**5.8**	**5.8**	**6**	**4.2**	**5.6**
Pitch (nm)	**234**	**670**	**234**	**234**	**10000**	**2000**	**234**
Form Factor	+/-	-	+	++	-	-	+
Integration Flexibility	+/-	+/-	+ stacking	++ multiple stacking	+ chip to chip	+ chip to chip	+/-

Scott List, IMEC
(M. Bamal, et al., IITC2006.)

3D IC Technologies

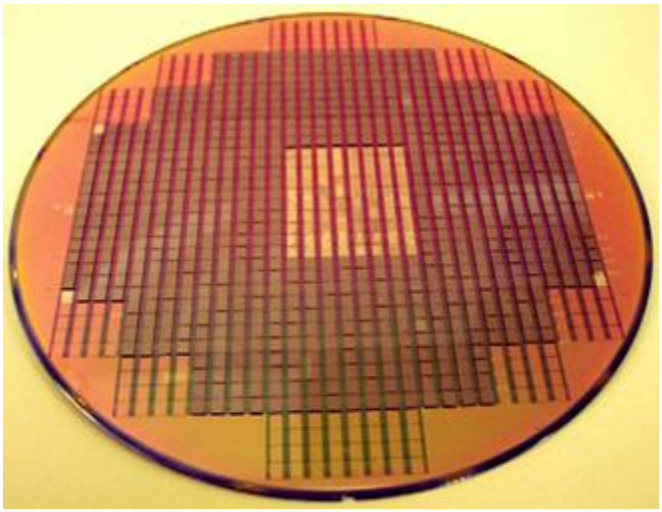
Die-to-Die, Hybrid Die-to-Wafer and Monolithic Wafer-to-Wafer

Die-to-Die / Multi-chip Packaging



(Intel)

Hybrid Die-to-Wafer



(Fraunhofer)

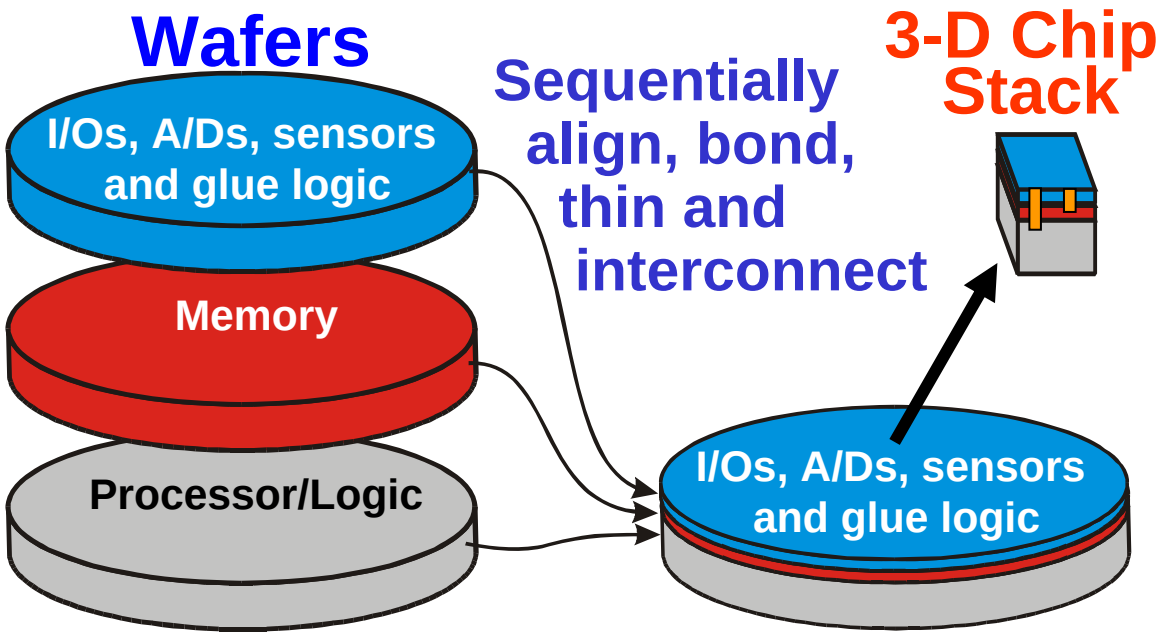
- Known-good-die (KGD)
- Assembly flexibility
- Pick-and-place assembly

- In production with short-term advantages
- Low interconnect density & performance

- Wafer-level process
- Performance improvement

Highest — Cost for High-Quantity Production — High

Monolithic Wafer-Level 3D Hyper-Integration



For a 3D SoC with N active IC layers:

- Increase in global clock **frequency**: **$N^{3/2}$**

  Ref. J.D. Meindl et al., p. 525, IEDM 2001

- Reduction in interconnect **power**: **~ $1/N^{1/2}$**

  Ref. J.W. Joyner and J.D. Meindl, p. 148, IITC 2002

- Shorten on-chip long wires (high performance)
- Small/short inter-chip via size (high density, low coupling)
- Function-specific processing (alleviating material/processing constraints)
- Lower high-volume interconnect cost (monolithic process)

Wafer-Level Integration Alternatives

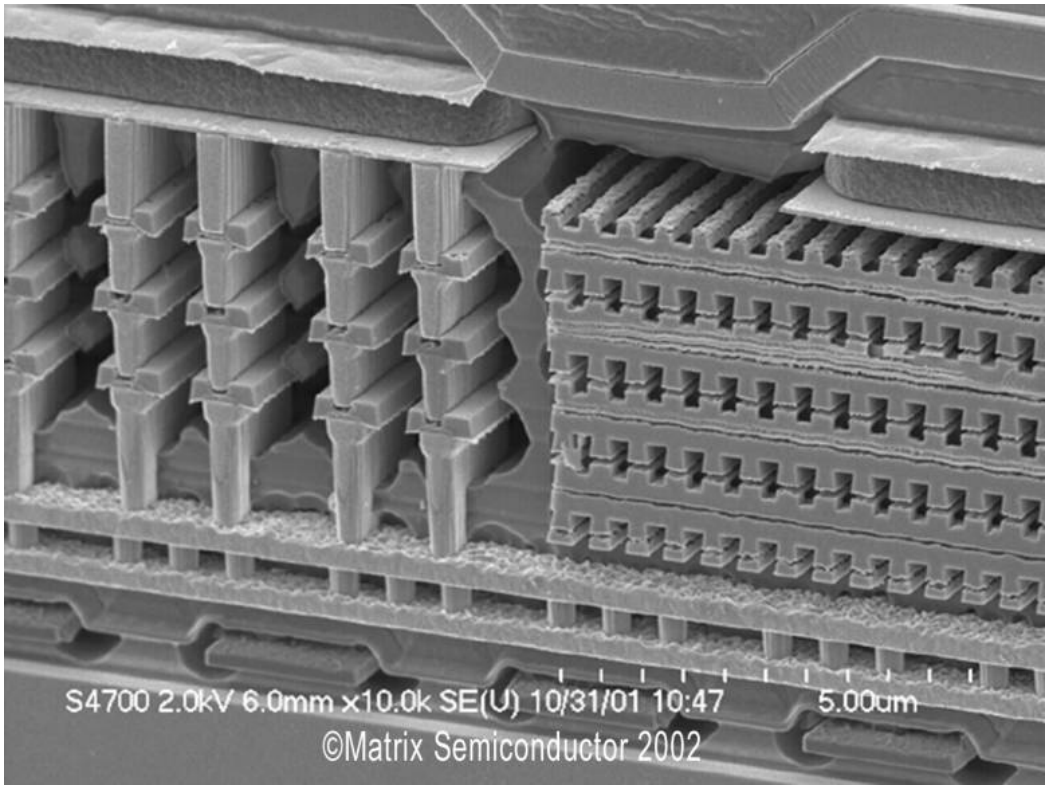
Front-End Based

- silicon-on-insulator
- recrystallized or large-grain poly
- compound semiconductors for electro-optics/photonics

Back-End Based (emphasis in talk)

- metal (copper) versus dielectric (low-k) bonding
- via-first versus via-last
- use or non-use of handling wafers

Front-End 3D Integration



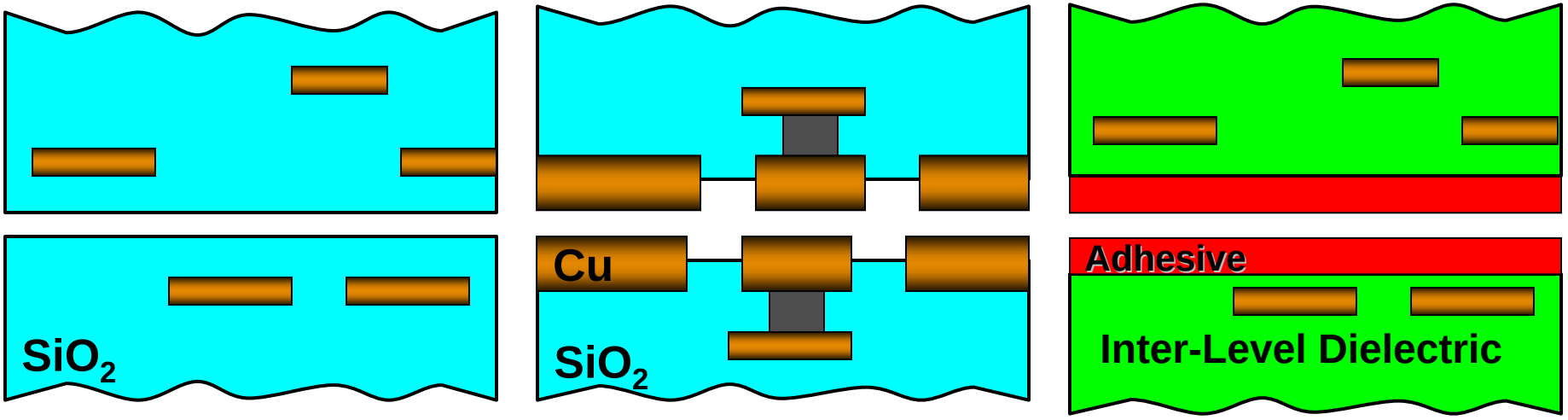
3D non-volatile memory (NVM) with polysilicon memory devices (Matrix Semiconductor)

Wafer-Level 3D Alternatives (BEOL-Based)

– IBM	high speed processors
– Infineon/ Fraunhofer	technology platform
– Intel	high speed processors
– Lincoln Laboratory/ R^3 Logic	imagers
– MIT	technology platform
– Rensselaer	technology platform
– Tezzaron	memory stacks
– Tohoku University/ ZyCube	memory stack/ imagers

- All provide micron-sized, through-die interconnects

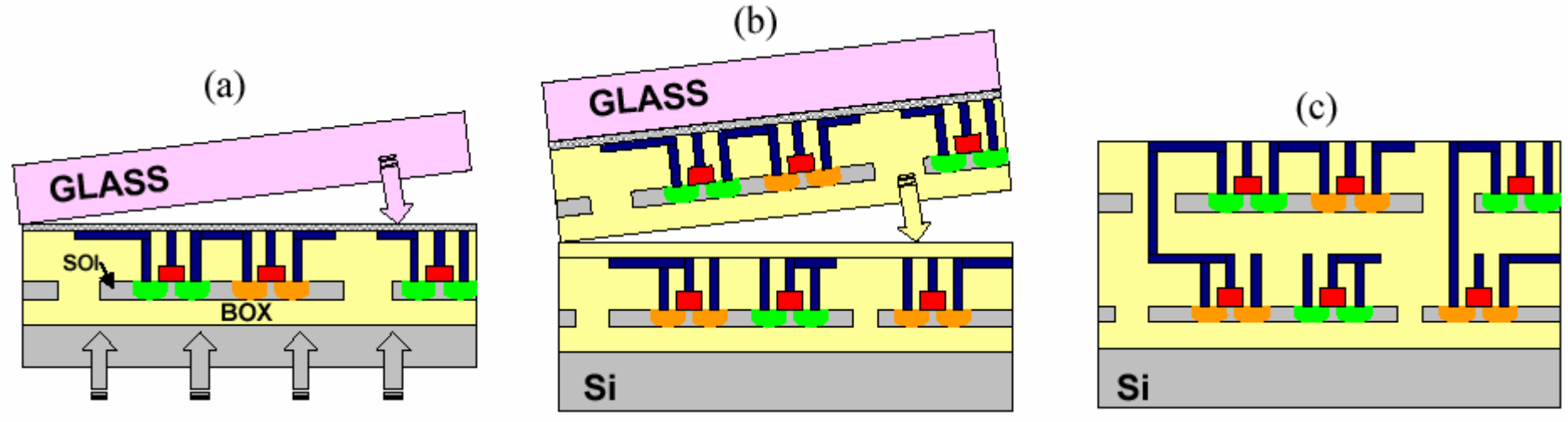
Bonding Approaches for Wafer-Level 3D ICs



Direct Oxide Bonding | Direct Metal Bonding | Adhesive Bonding

- **Common Issues**
  - BEOL IC Process Compatibility
  - Planarization and Interface Activation
  - Wafer Thinning and Leveling without Edge Chipping
  - Wafer-to-Wafer Alignment Approach
  - Inter-Wafer Interconnection Methodology

IBM 3D Approach



Schematic diagrams of layer transfer process for 3D IC fabrication:

(a) Circuit is attached to glass handle wafer and original substrate is removed

(b) Top circuit is aligned and bonded to second circuit

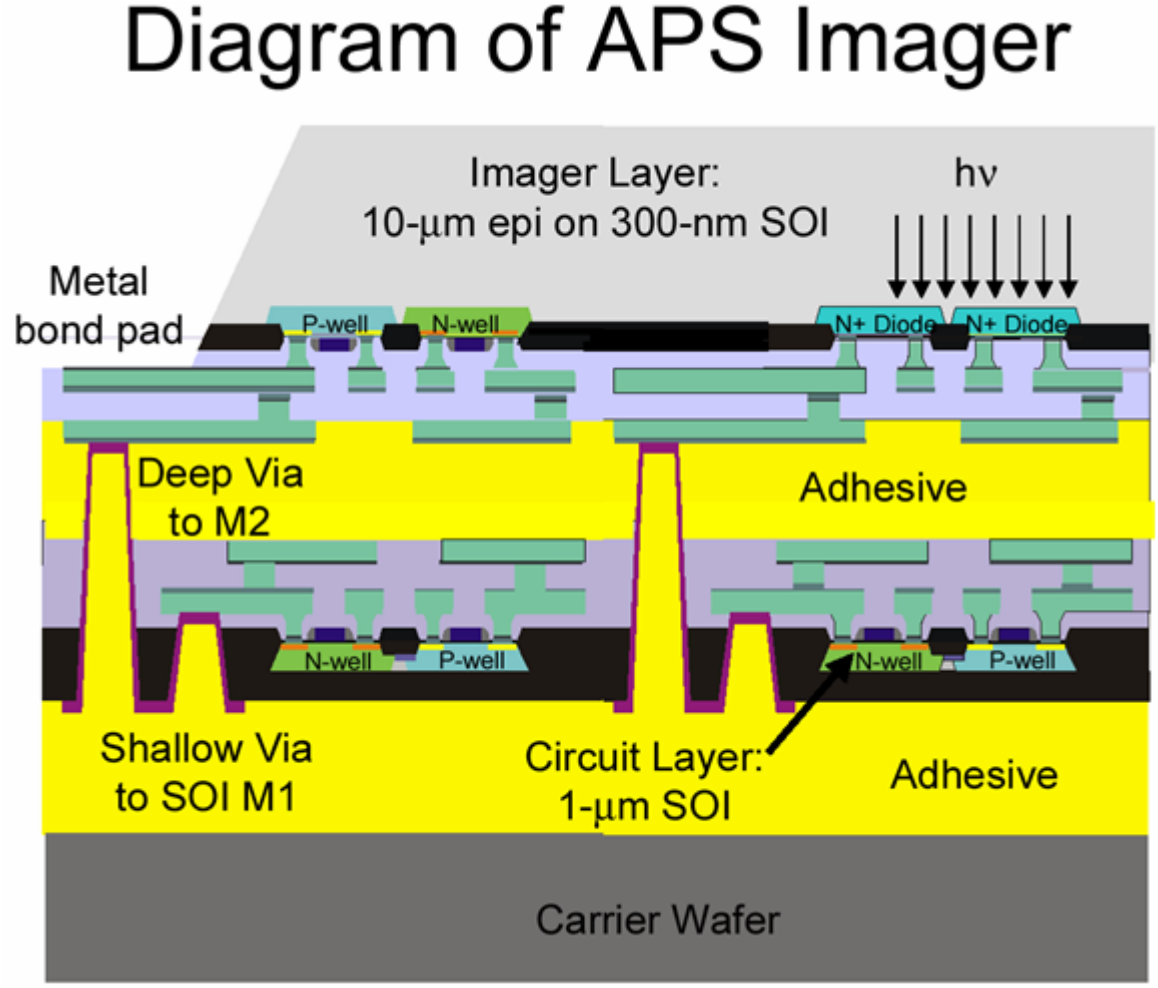
(c) Handle wafer and adhesives are removed, and vertical interconnects are formed between device layers

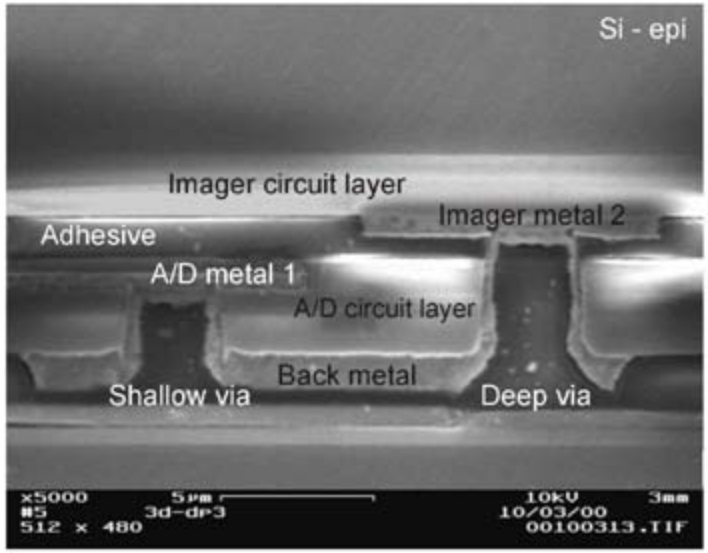
K.W. Guarini, et al., "Electrical Integrity of State-of-the-Art 0.13μm SOI CMOS Devices and Circuits Transferred for Three-Dimensional (3D) IC Fabrication," IEDM, pp. 943-945, 2002.

Three-Dimensional Integrated Circuits for Low-Power, High Bandwidth Systems-on-a-Chip

MIT Lincoln Laboratory, Lexington, MA and 3D-IC, Inc., Somerville, MA

J. Burns, L. McIlrath, C. Keast, C. Lewis, A. Loomis, K. Warner, P. Wyatt, "Three-Dimensional Integrated Circuits for Low-Power, High-Bandwidth Systems on a Chip", IEEE International Solid-State Circuits Conference, ISSCC 2001, pp. 268-270, Feb. 2001.

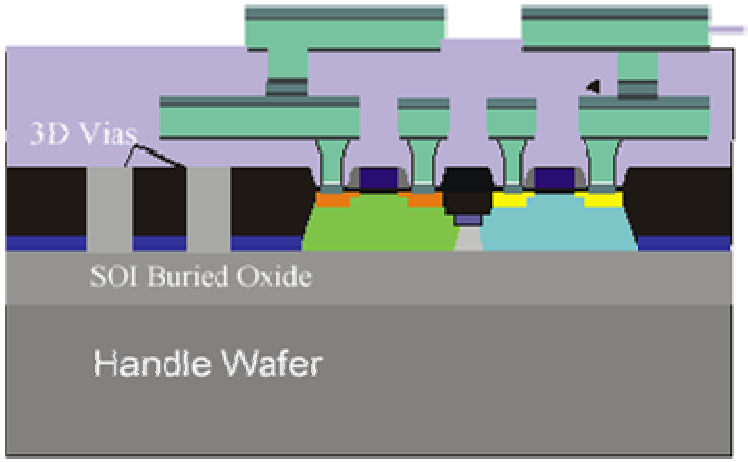




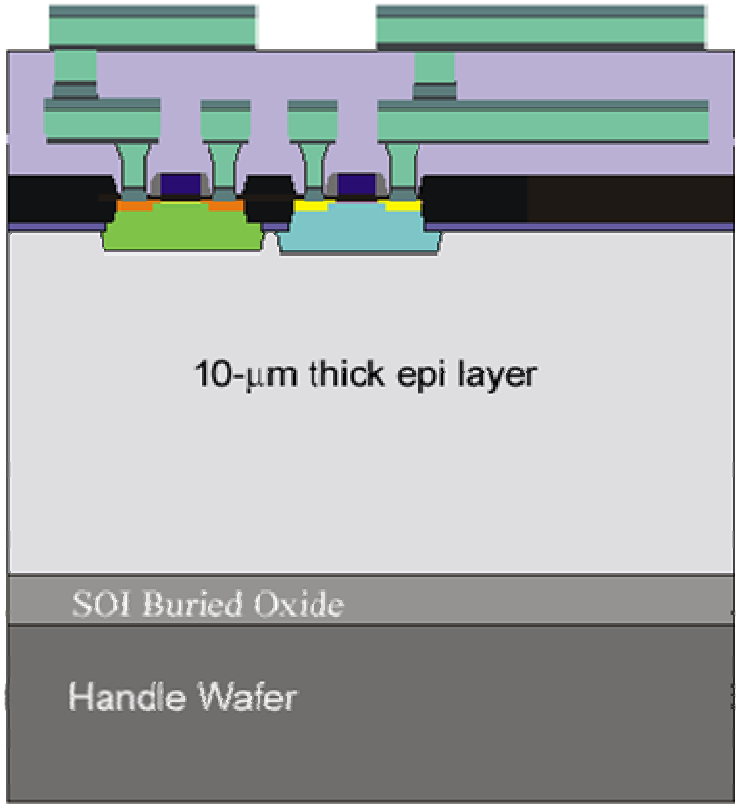
Lincoln Laboratory/ 3D-IC Inc. Approach

3D Interconnect Demonstration Vehicle

Circuit layer: 1-µm SOI CMOS



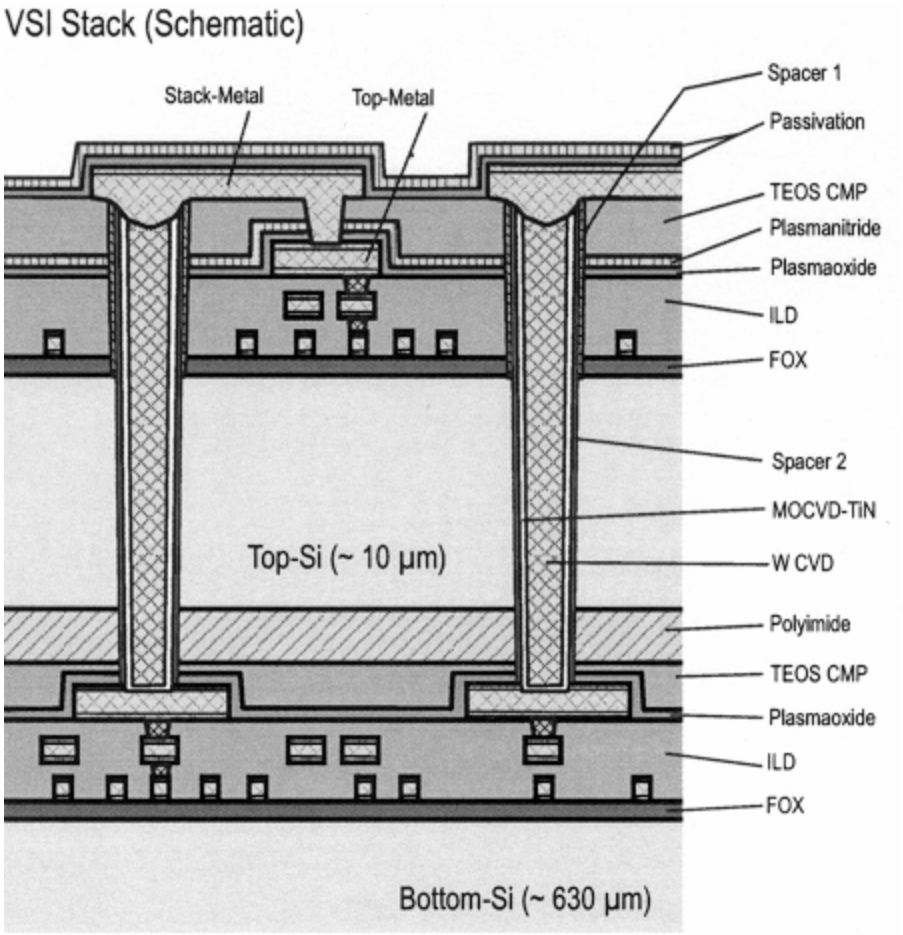
Photodetector layer: 10-µm SOI CMOS



- 0.8-µm CMOS process
  - SOI wafers
  - 10-µm epi required for imaging
- Three additional mask layers
  - 3D-Via insulation
  - 3D-Via etch
  - 3D metal

Infineon/Fraunhofer 3-D

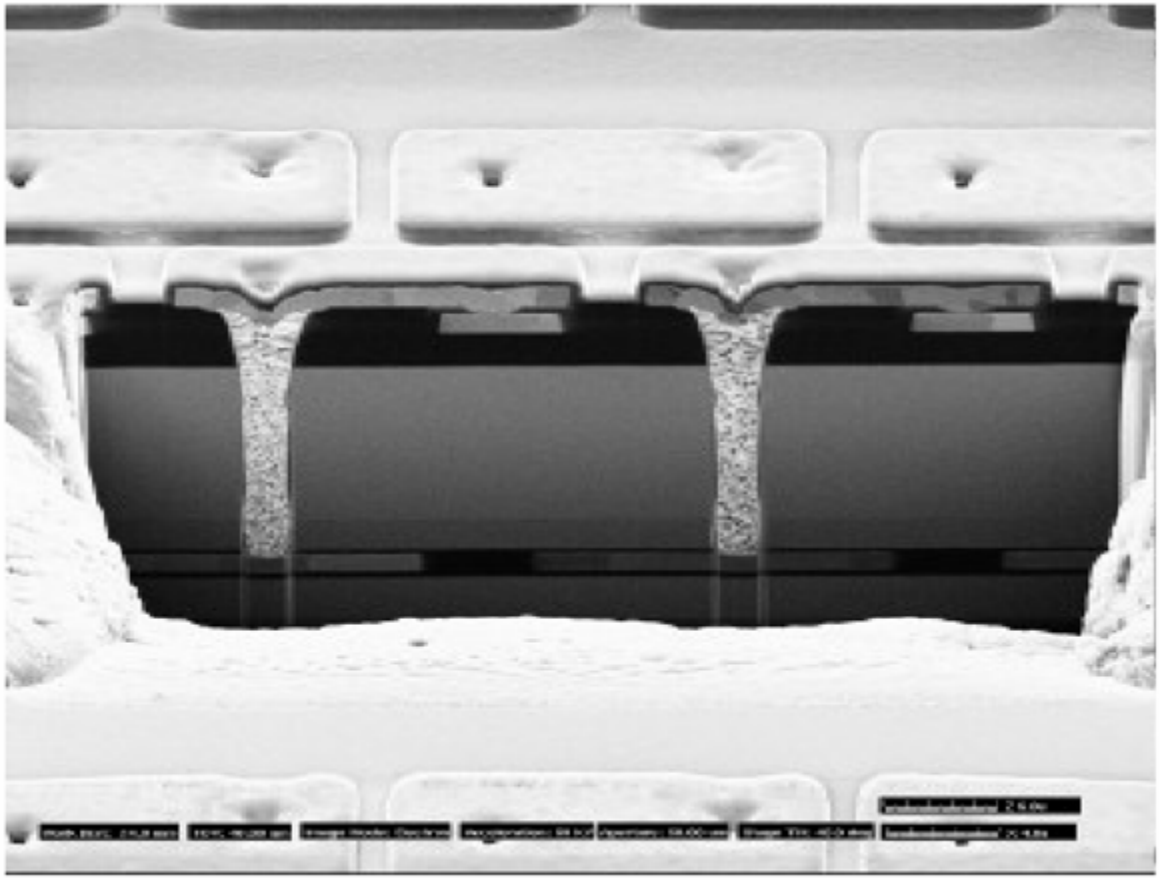
Vertical System Integration (VSI®)



- Back-to Face
- Glue: Polyimide
- Via: W CVD
- Via-Chain
- EEPROM

P. Ramm, D. Bonfert, H.Gieser, J. Haufe, F. Iberl, A. Klumpp, A. Kux, R. Wieland, 2001 IEEE International Interconnect Technology Conference (IITC), pp. 160-162, June 2001.

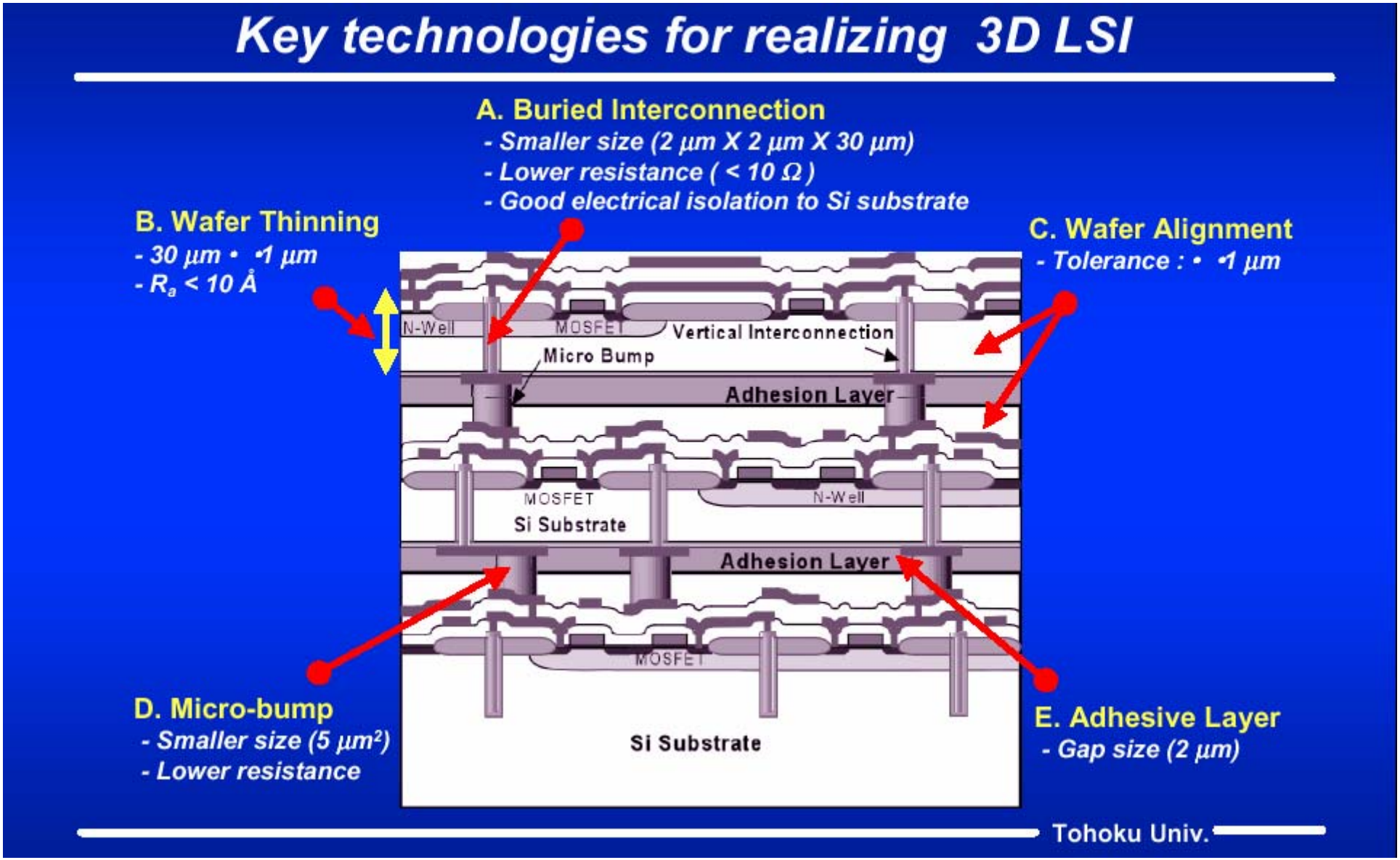
Infineon/Fraunhofer 3-D



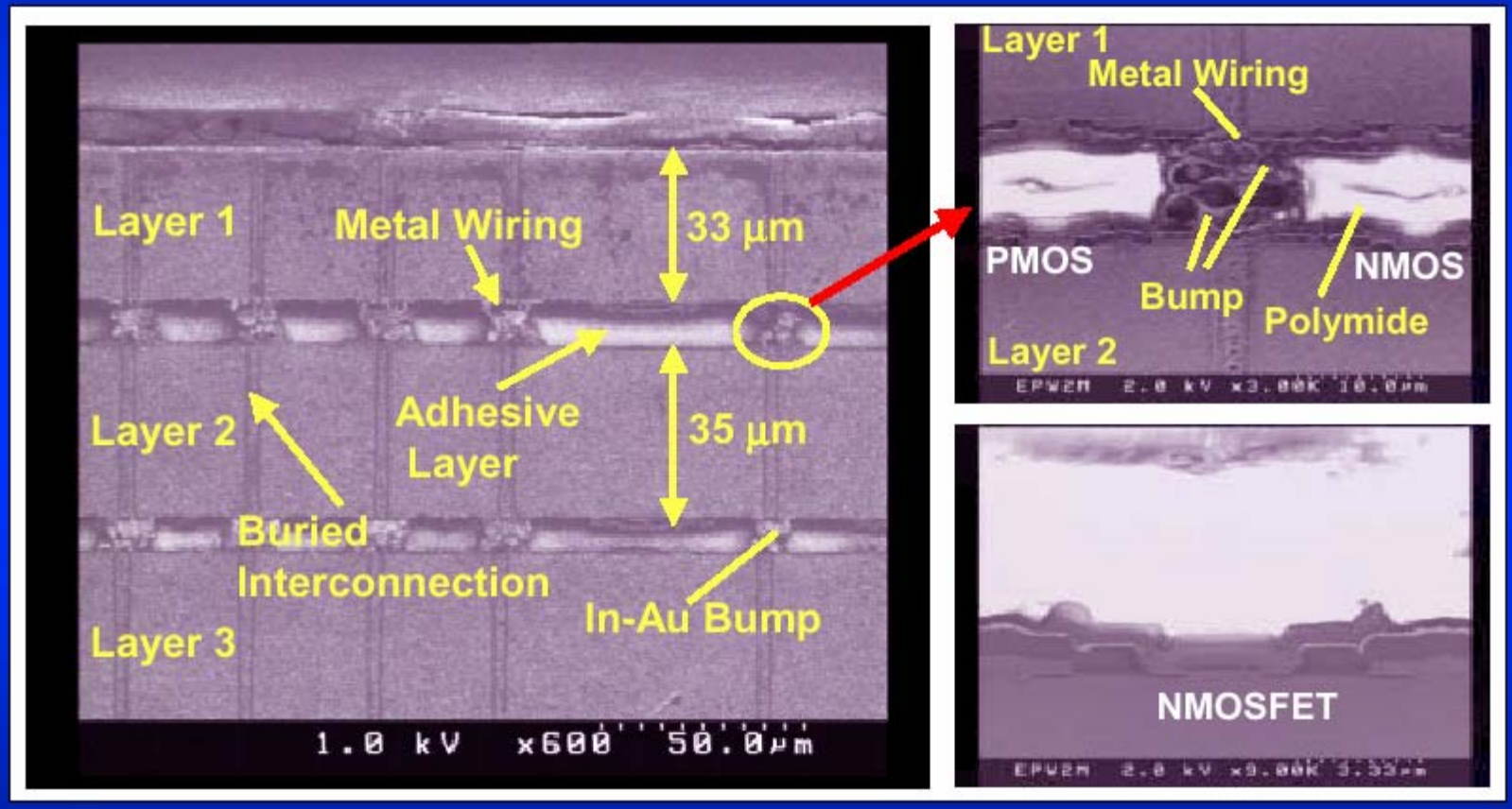
Cross section of a vertically integrated test chip structure, showing 2.5 x 2.5µm^2 interchip vias (FIB)

Three-Dimensional Shared Memory Fabricated Using Wafer Stacking Technology

K.W. Lee, T. Nakamura, T. One, Y. Yamada, T. Mizukusa, H. Hasimoto, K.T. Park, H. Kurino and M. Koyanagi, International Electron Devices Meeting (IEDM), pp. 165-168, Dec. 2000



SEM cross section of 3D shared memory chip



MIT 3-D Integration Approach: Cu-Cu Bonding with Handling Wafer

- **MIT 3D Integration**
  -- Back-to-face stacking using handle wafer release and copper bonding

Advantages:

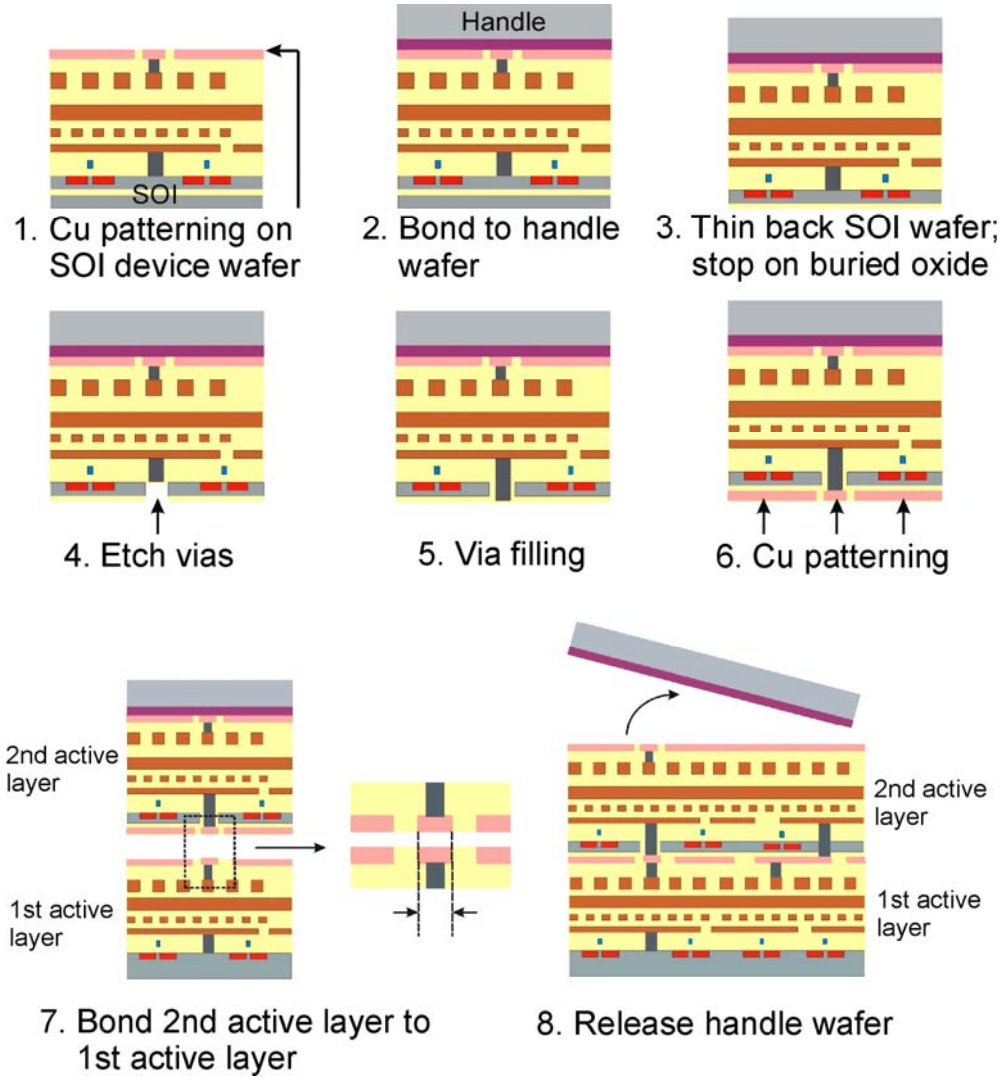
1. Low aspect ratio vertical vias

- Vertical vias are formed on both wafers and bonded

2. Handle wafer release

- Minimum damage to the stack : The 3-D stack does not see the SOI thinning step. This also explains the choice of back-to-face stacking

3. Copper Wafer Bonding

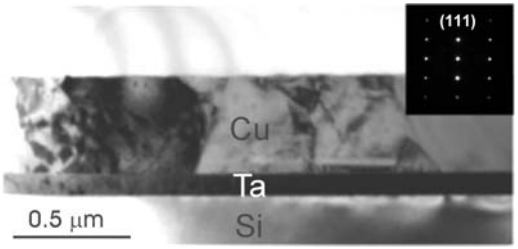


(Fan *et al.*, 2001 ECS meeting)

Evolution of Morphologies During Bonding

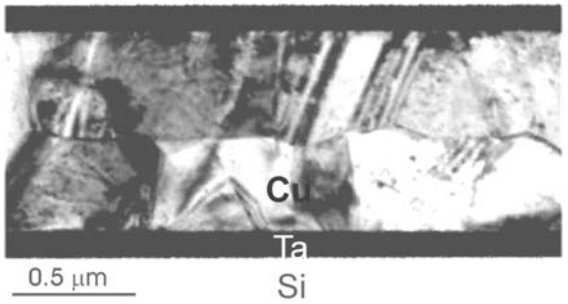
Bonding temperature: 400 °C

Before bonding



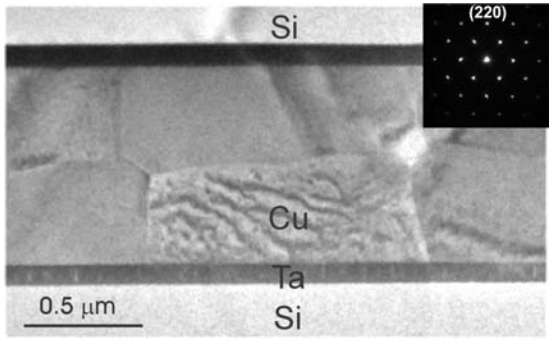
- (111) orientation

30 min bonding

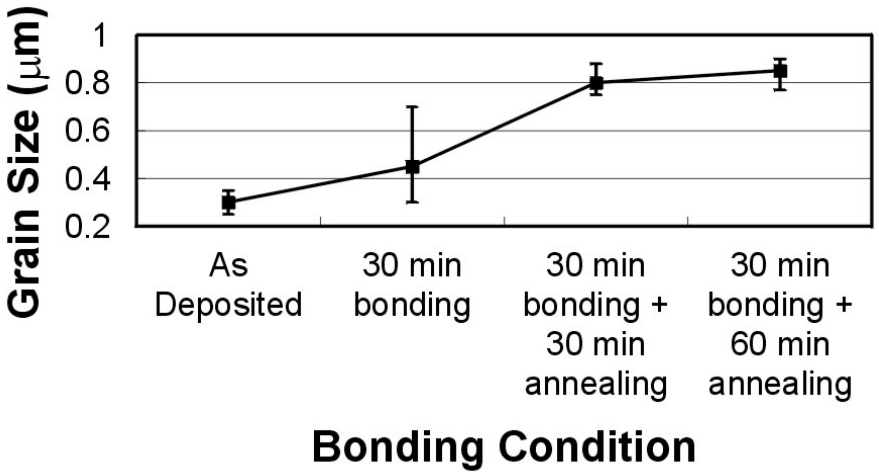


- Clear interface

30 min bonding +
30 min N2 anneal



- (220) orientation
- Grain structure



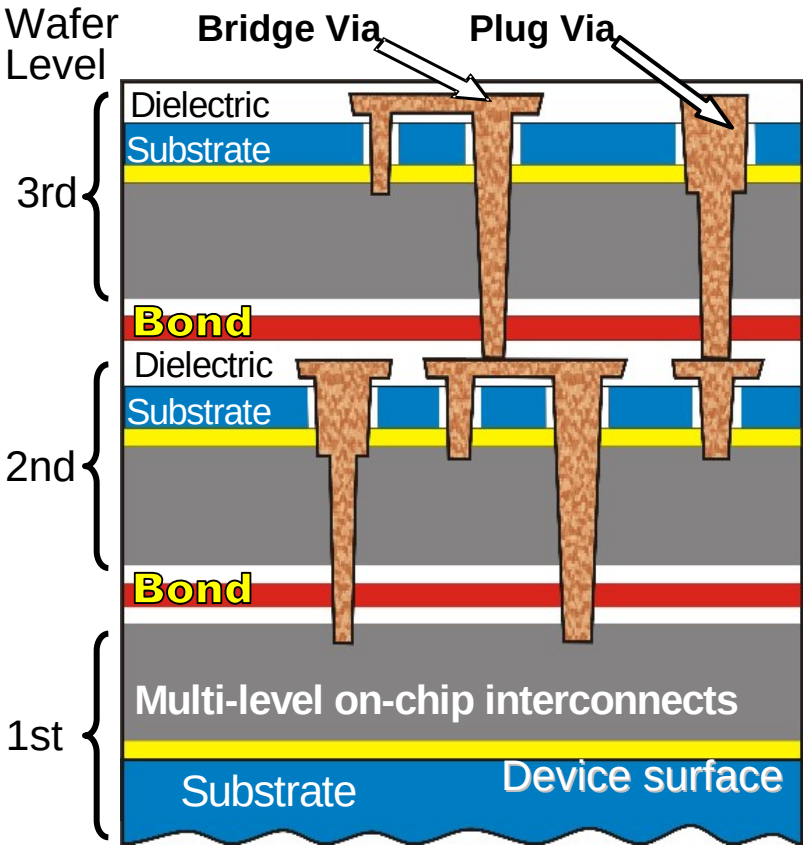
- Grain size saturates after 30 min of annealing
- Stable grain structures and bonded layers are observed after further annealing

-- Post-bonding anneal is suggested to improve the bonding quality.

*(Chen and Reif, Applied Physics Letters, **81**, 2002)*

RPI Wafer-Level 3D Hyper-Integration Platform

Using Adhesives Wafer Bonding and Cu Damascene Inter-Wafer Interconnect

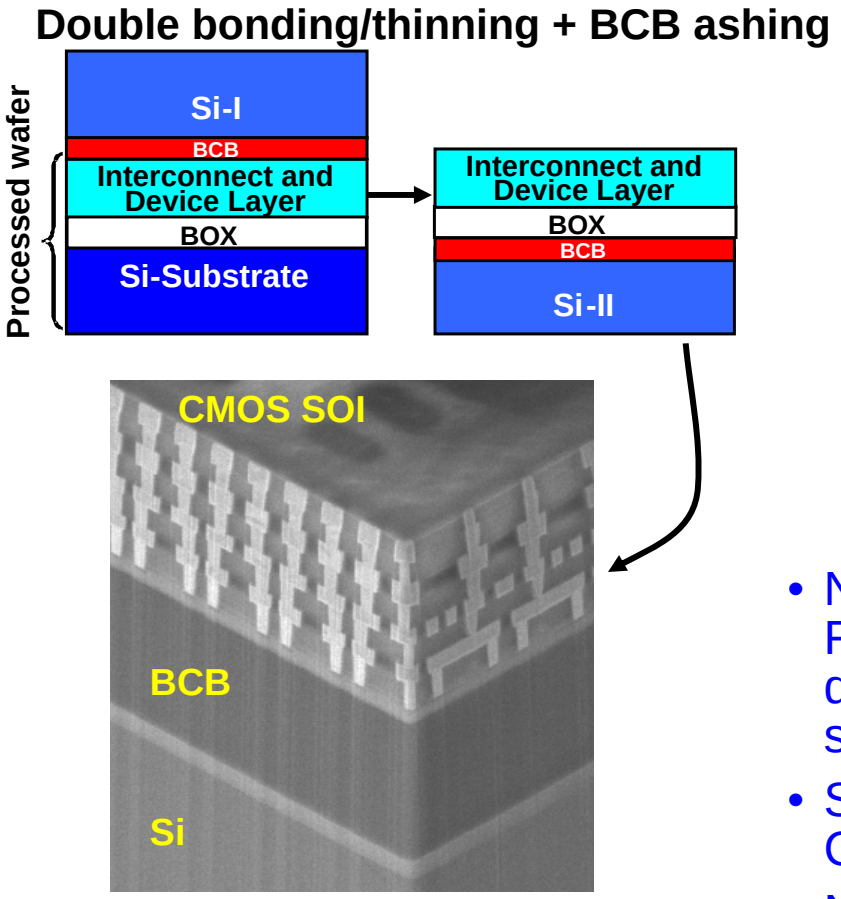


Key Accomplishments:

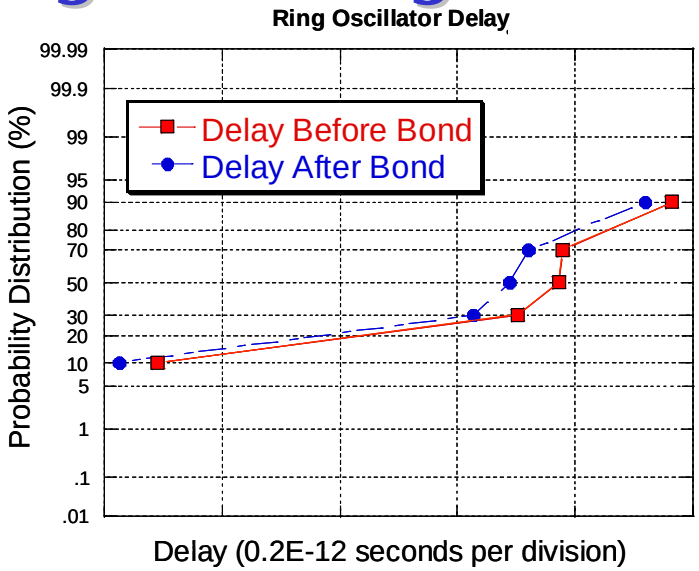
- Precise **alignment** of 200 mm wafers: 1 µm across wafer achieved; key concerns: within-wafer variations and bonding-induced changes
- Thin adhesive **bonding** at T ≤ 400 °C: Robust process with 2.6 µm thick BCB; 0.7 µm BCB bonding demonstrated; key concerns: impact of bonding on wafer alignment and spatial variations in BCB thickness after bonding
- Precision **thinning** and leveling of top wafer: Robust 3-step thinning established for SOI wafers; key concern: thinning uniformity for bulk wafers
- **Inter-wafer connection** by high-aspect-ratio vias: Via-chains demonstrated and process issues delineated (RPI and UAlbany collab); key concerns: high contact resistance

- BEOL and packaging compatible baseline process steps demonstrated
- Platform for hyper-integration with high performance, functionality and density
- Thermal heat sink and electrical isolation with extra copper vias (design rule needed)

Thermal-Mechanical-Electrical Robust Wafer Bonding/Thinning



FIB image of bonded Freescale's 130nm CMOS SOI Cu/low-k wafer

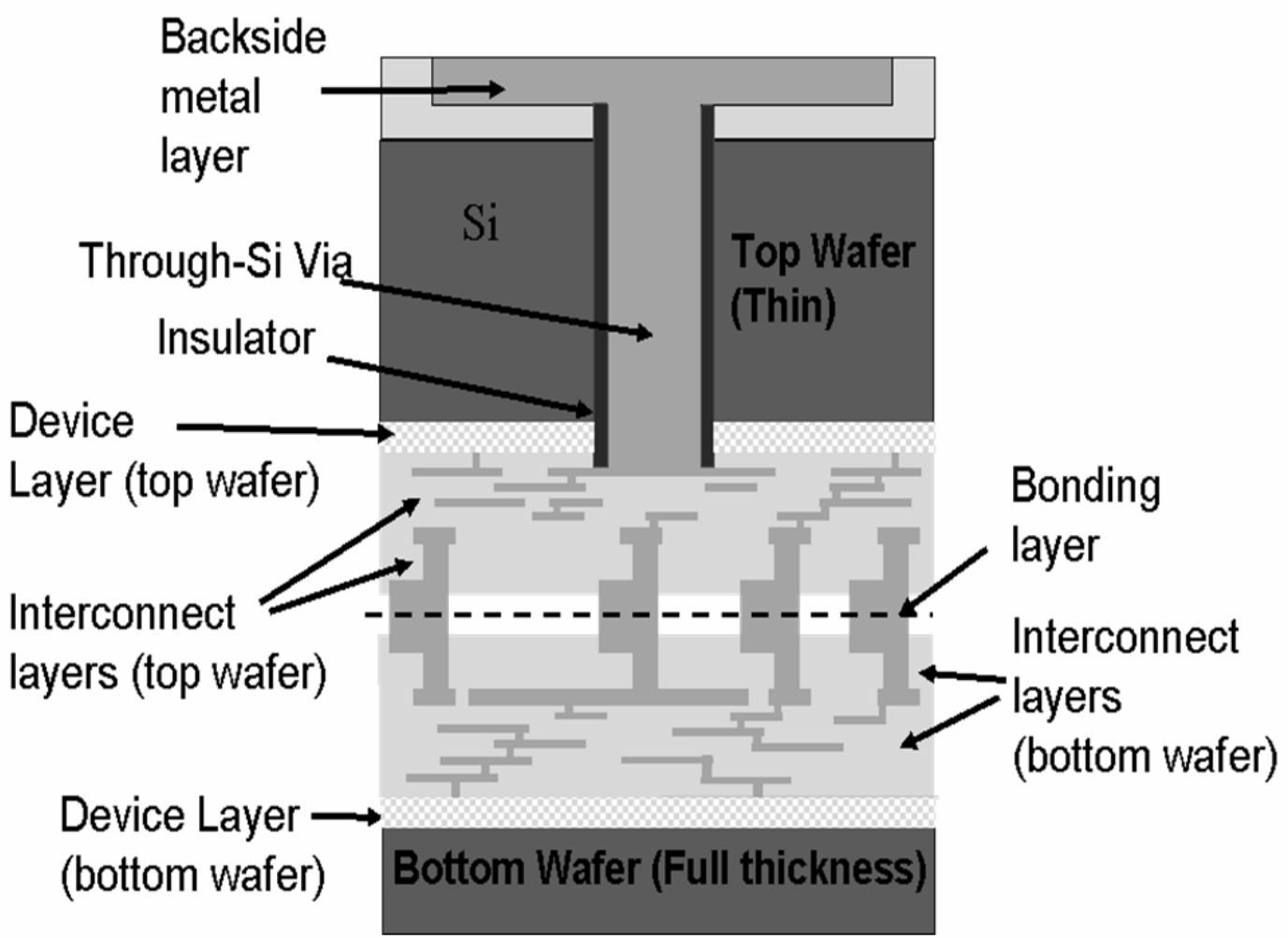


- No degradation of electrical characteristics on Freescale's CMOS SOI Cu/low-k wafer after double bonding/thinning and comparable sawing results to 2D IC wafer
- Similar EM test results on SEMATECH's Cu/low-k wafers after double bonding/thinning
- No degradation in bond strength after conventional die packaging reliability tests (autoclave test and thermal-shock LLTS)

R.J. Gutmann, J.-Q. Lu, S. Pozder, Y. Kwon, A. Jindal, M. Celik, J.J. McMahon, K. Yu and T.S. Cale, ***AMC 2003****.*

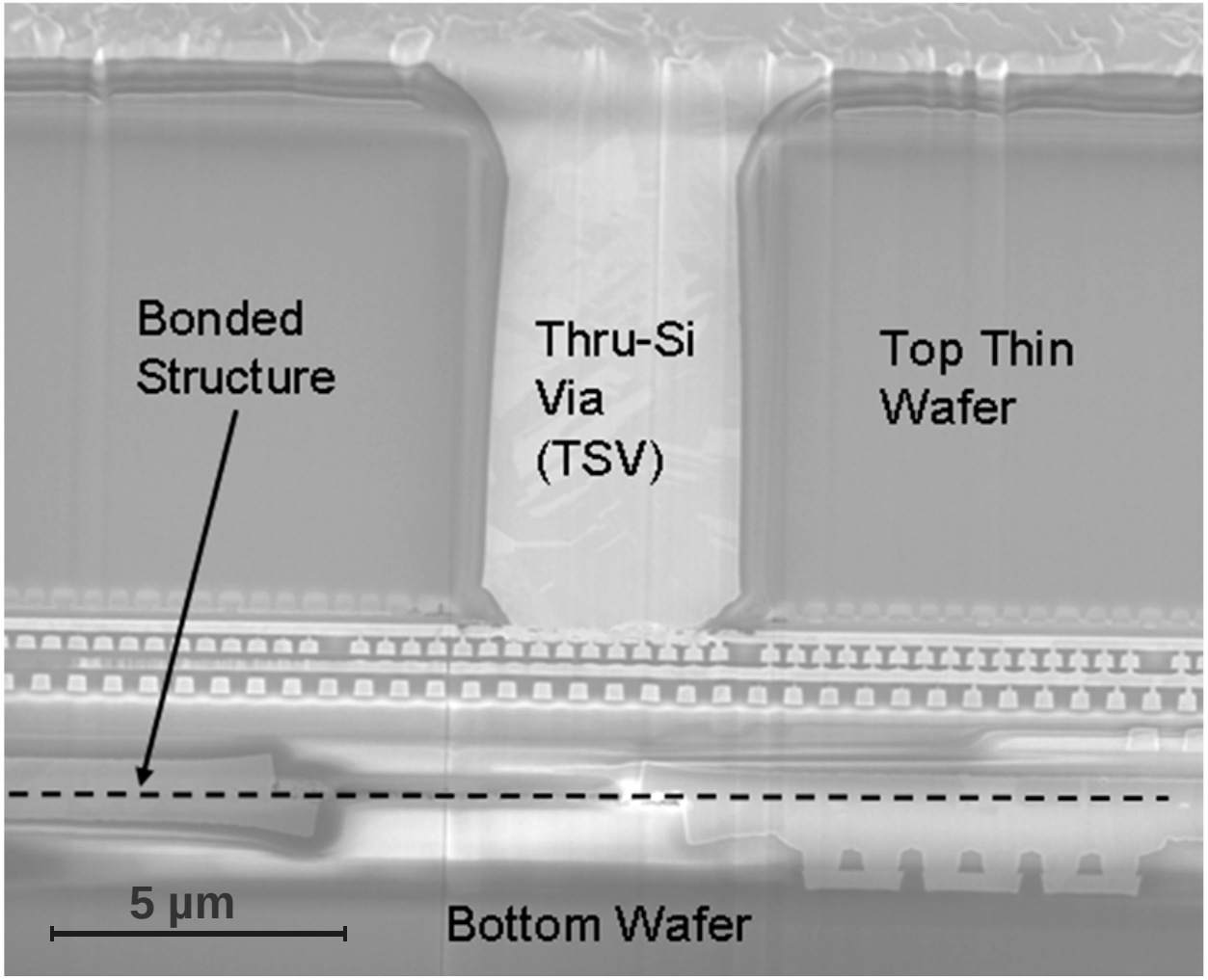
S. Pozder, J.-Q. Lu, Y. Kwon, S. Zollner, J. Yu, J.J. McMahon, T.S. Cale, K. Yu, and R.J. Gutmann, ***IITC 2004****.*

Intel Cu-Cu Interconnect Structure



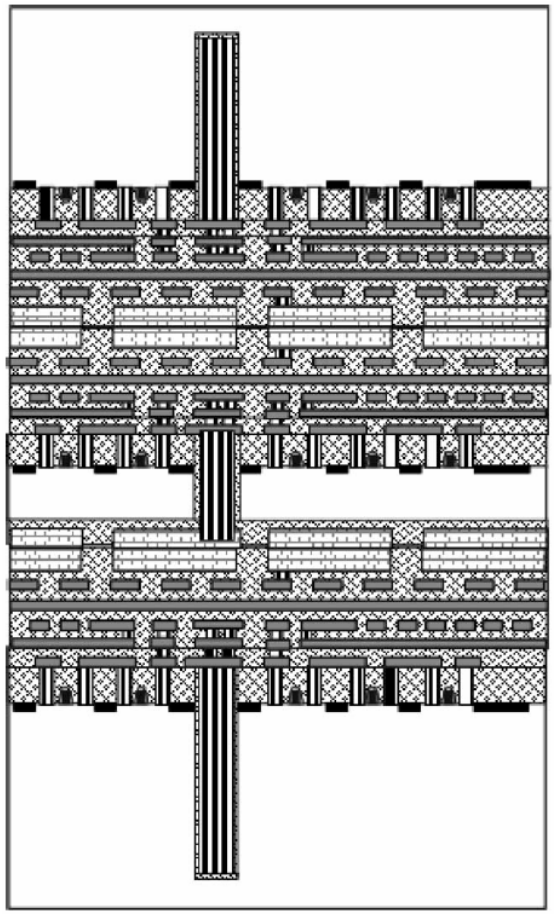
P. R. Morrow, et. al, IEEE EDL, Vol. 27, No. 5, p. 335, MAY 2006.

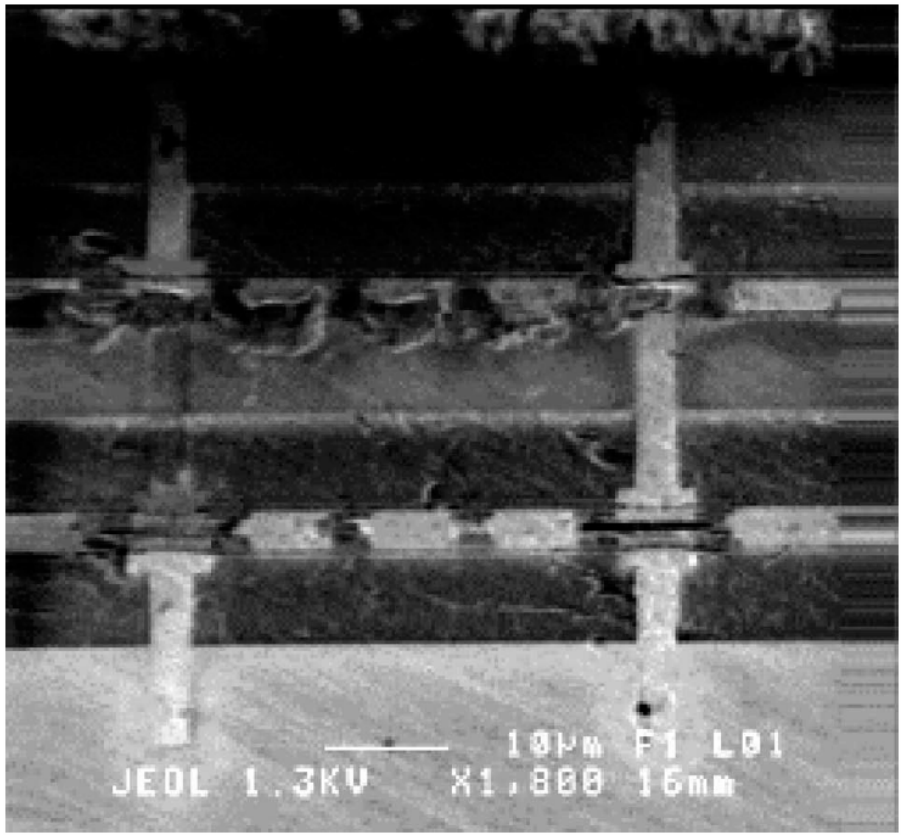
Cross Section of Cu-Stacked Wafer with Integrated TSV (Intel)



P. R. Morrow, et. al, IEEE EDL, Vol. 27, No. 5, p. 335, MAY 2006.

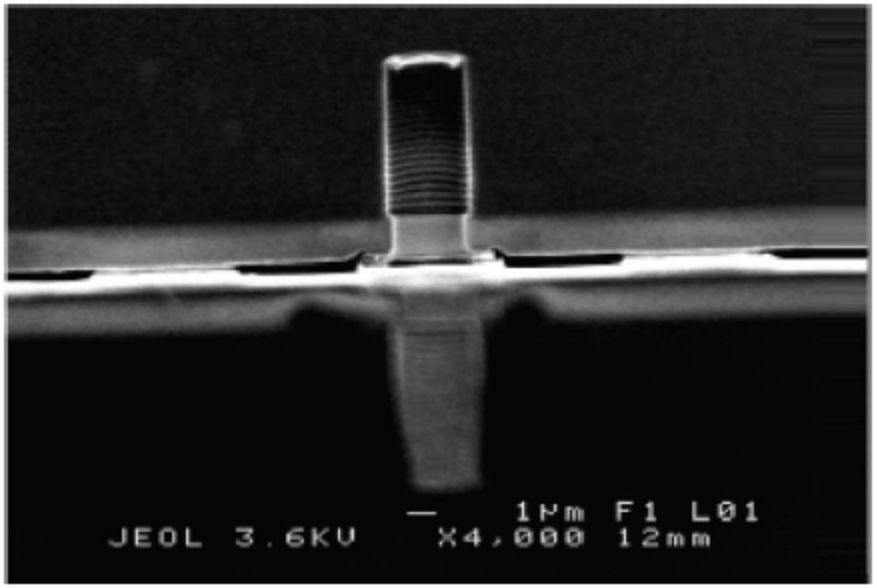
Tezzaron 3D Stack with vertical "Super-Contact"



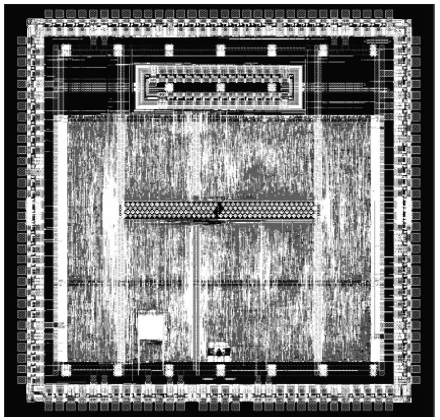


R.S. Patti, Proceedings of the IEEE, Vol. 94, No. 6, June 2006.

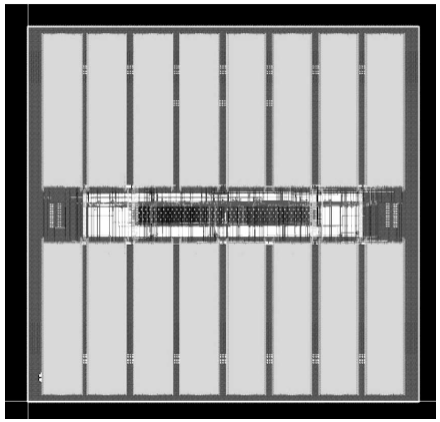
Tezzaron Alignment Tolerances of Super-Vias and Prototypes



Circuitry for a processor/memory stack



Processor (on top of the stack)

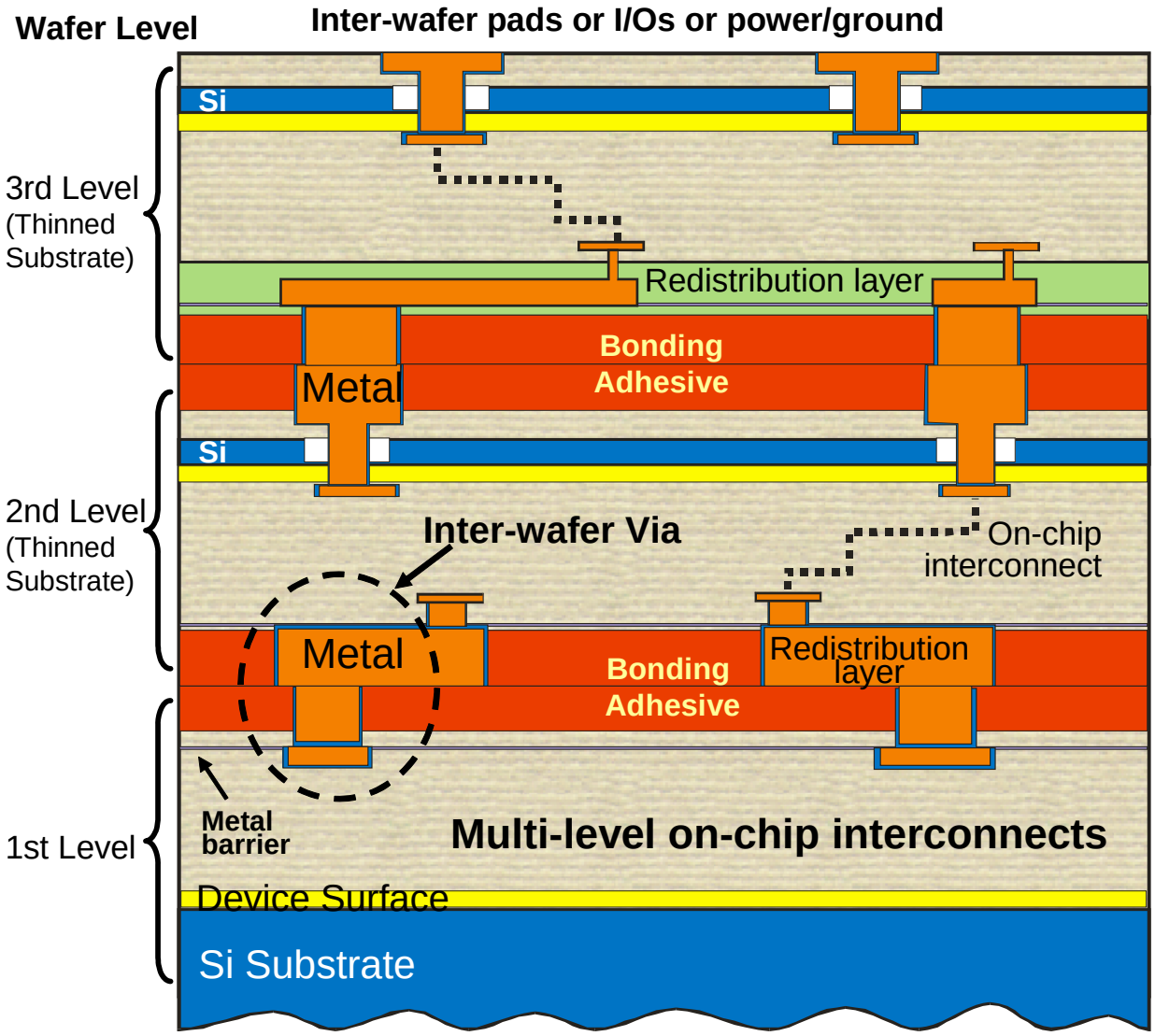


Memory (on bottom of the stack)

R.S. Patti, Proceedings of the IEEE, Vol. 94, No. 6, June 2006.

RPI Via-First Platform

Metal/Adhesive Via-First 3D Scheme



Patent filed

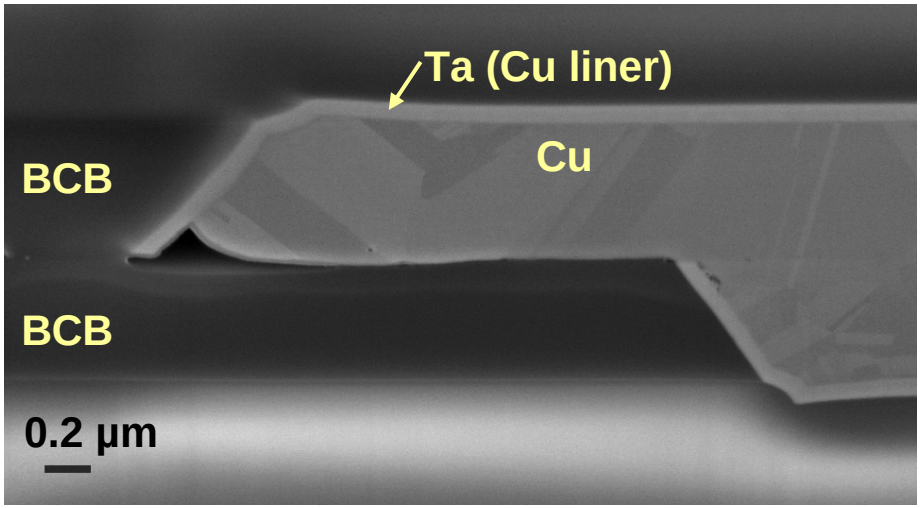
Distinctive Features:

- BCB bond strength (mechanical integrity)
- Metal direct bonding (high-density, short inter-wafer via)
- Redistribution layer (inter-wafer routing & large alignment tolerance)
- Thermal management options
- Optical interconnect ready

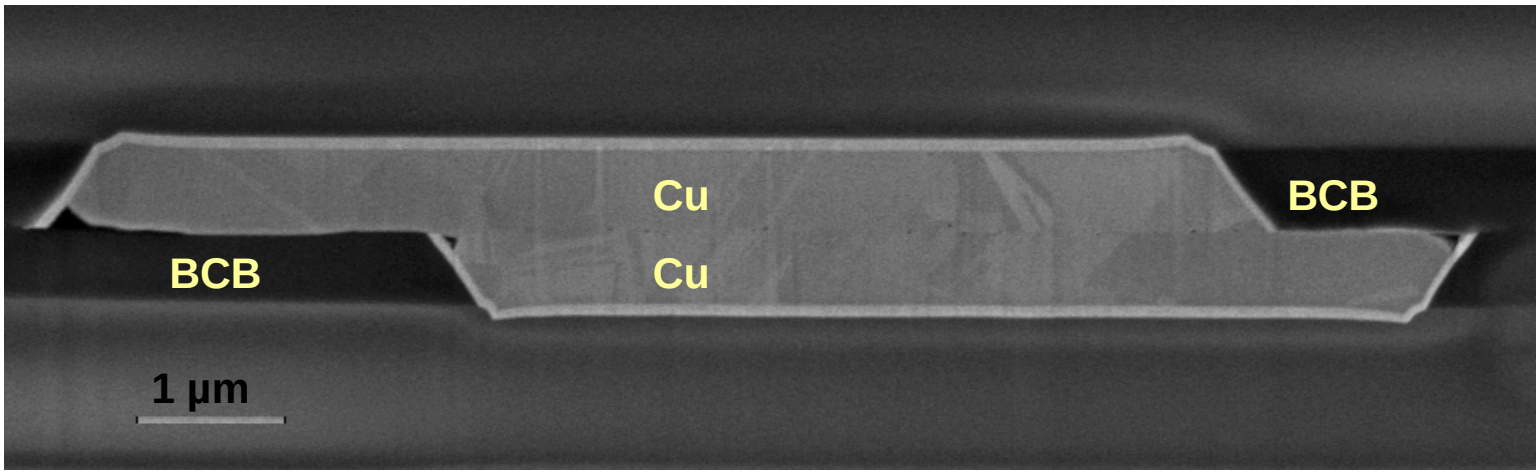
Process Challenges:

- Selection of metals and adhesives for damascene patterning
- Wafer-level feature-scale planarization (CMP)
- Post CMP treatment
- Bonding process & processing integrity

Cu/BCB Via-First 3D Approach

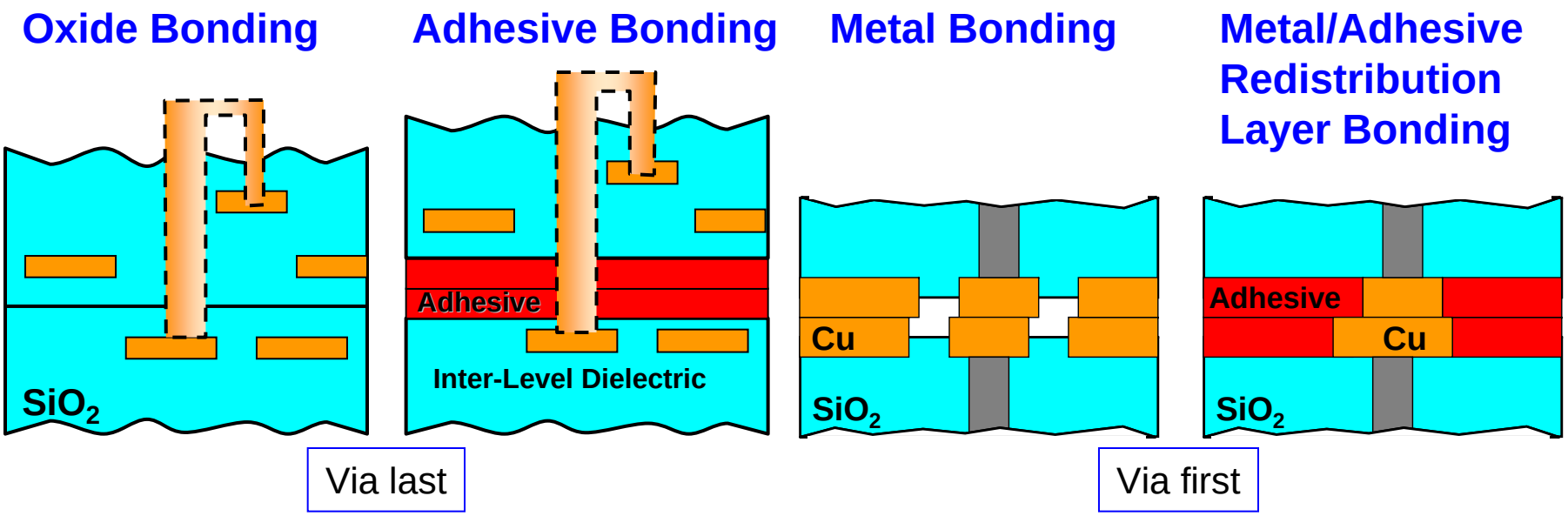


- **Feasibility demonstrated with *small portion* of bonding area**
- **Challenges:**
  - BCB partial-curing and patterning
  - Ta and Cu deposition
  - Wafer level feature-scale planarization (Cu/BCB CMP)
  - Post CMP treatment
  - Bonding process to form all bonds



J.J. McMahon, J.-Q. Lu and R.J. Gutmann, ***IEEE 55th ECTC, 2005.***

Approaches for Wafer-Level 3D ICs

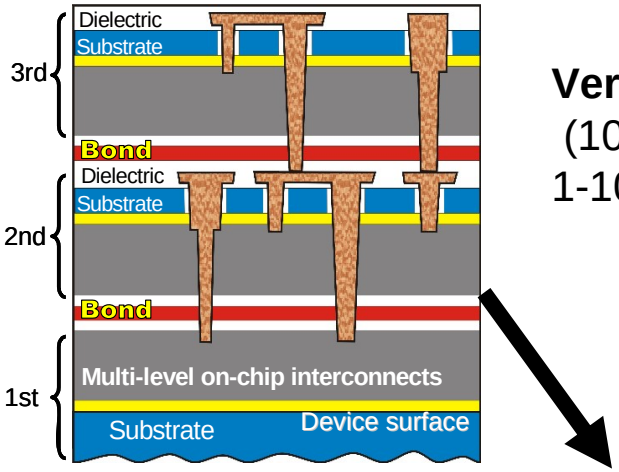


BEOL Issues	Oxide/Oxide	BCB/BCB	Cu/Cu	Redist Layer
Temperature	Challenging	Best	Good	Good
Surface planarity	Challenging	Best	Challenging	Good
Film stress	Good	Best	Good	Best
Si real estate usage	Challenging	Challenging	Good	Good
Bond strength	Good	Best	Good	Good
Thermal mgmt.	Good	Good	Very good	Best

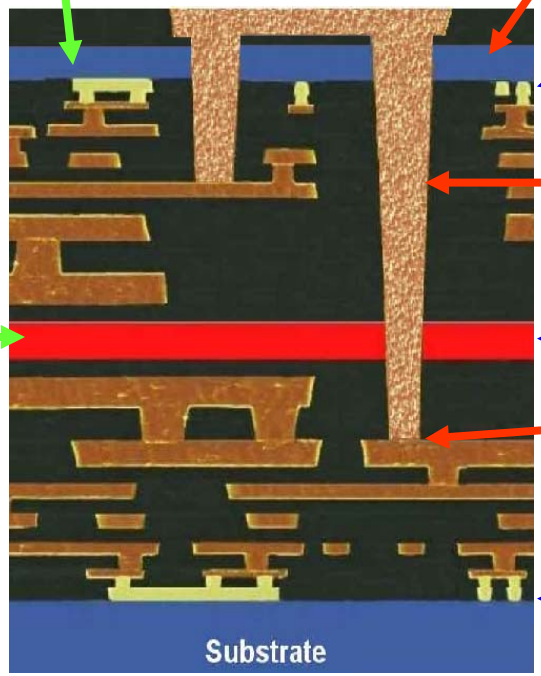
Wafer-Level 3D Technology Challenges

- **Platform** (Wafer-to-wafer alignment and bonding)
- **Thermal-mechanical stresses**
- **Yield**
  - Yield enhancement inherent to 3D scheme
  - Novel, flexible **architectures**
- **Thermal Power** dissipation (cooling solution)
- Consumption of **silicon** real estate (SiRE) by 3D inter-wafer interconnects
- Common **die size** (application-specific issue)
- Integration **architecture** and **CAD** design tools
- **Equipment (industry infrastructure)** qualified for 24/7 manufacturing

Potential Reliability Issues With 3D Integration



Very thin *active* Si layer
(10 – 140 nm for SOI wafer,
1-10 µm for bulk Si wafer)



Bonding Interface

Device reliability in the **bonded and thinned *active*** Si layer due to thermal-mechanical stress

Device degradation during 3D process

Via yielding and reliability due to thermal, mechanical, electrical stress

Wafer bond reliability

Via contact reliability

Device degradation

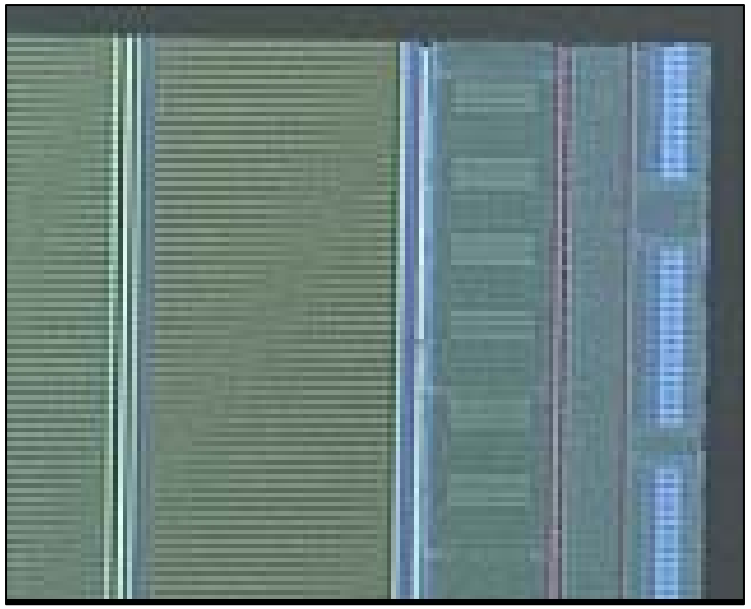
Compatibility with Conventional Die Packaging Reliability Tests

- Reliability Tests:
  1. Autoclave test #1: 100% humidity, 2 Atm., 120 ^{o}C, time = 48 hrs
  2. Autoclave test #2: 100% humidity, 2 atm., 120 ^{o}C, time = 144 hrs
  3. Thermal-Shock LLTS: -50 to 125°C (Large piece, 4x3 cm^{2})

✓ **No degradation in bond strength**

- Saw Edges of CMOS SOI Wafer after double bonding/thinning, BCB ashing and sawing

✓ **Comparable to 2D IC wafer**



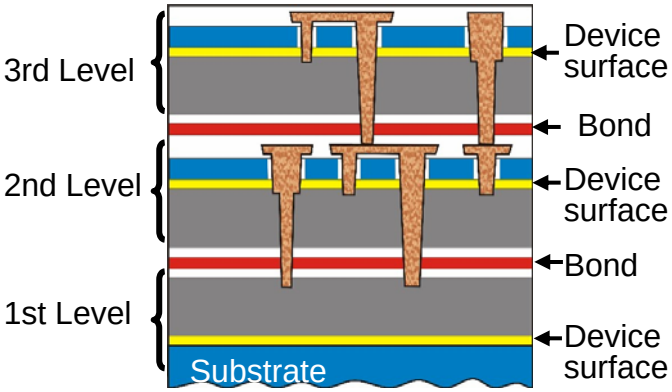
- EM test on SEMATECH Cu/Low-k wafers

✓ **No degradation after double bonding/thinning**

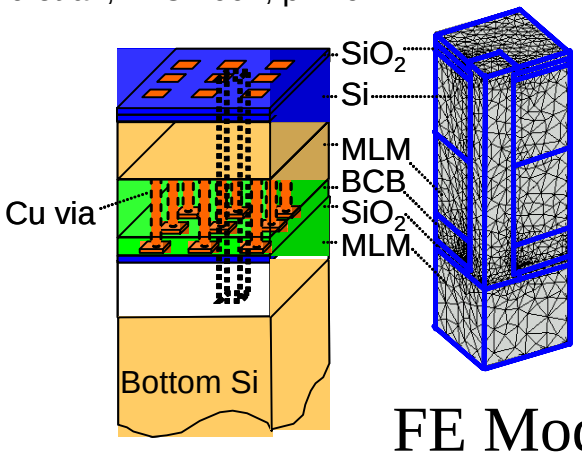
Collaborations: Rensselaer, Freescale and SEMATECH

Modeling Thermomechanical Stresses in 3D IC Inter-wafer Interconnects

Reliability data are not available

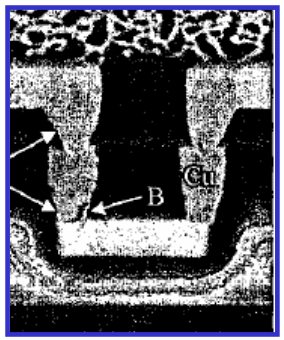


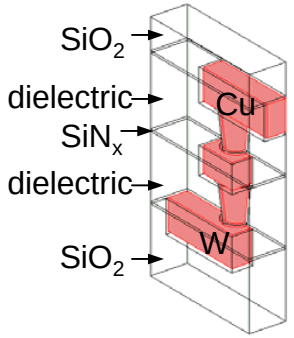
Lu *et al.*, IITC 2001, p.219



FE Model

Data exist for planar IC MLM structures

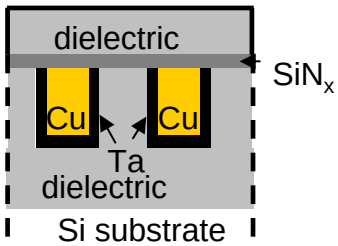


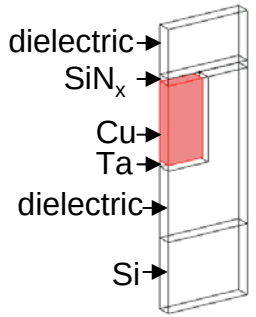


Filippi *et al.*, 42nd Rel. Phy. Symp., 2004, p.61

Edelstein *et al.*, 42nd Rel. Phy. Symp., 2004, p.316

Failure predictions agree with experiment: Cu vias fail when SiLK is used as the dielectric and they do not fail when SiCOH is used as the dielectric.





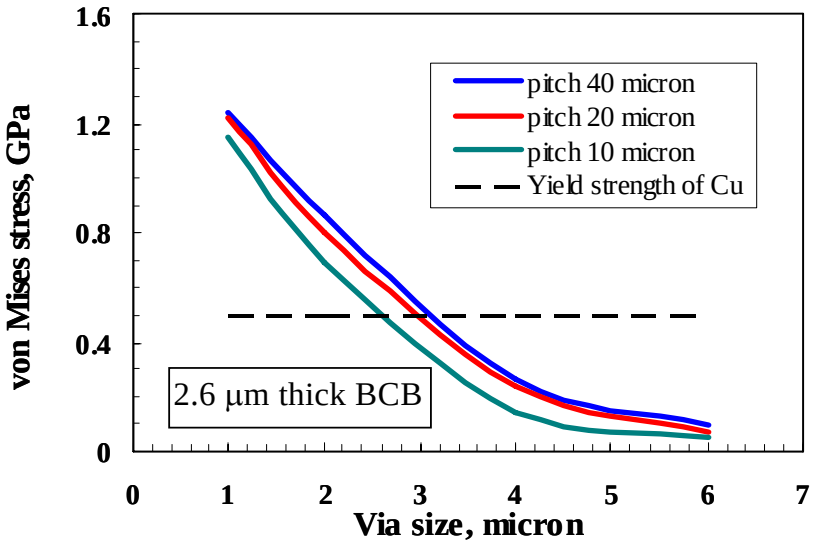
Rhee *et al.*, *J. Appl. Phys.* 93(7), 3926 (2003).

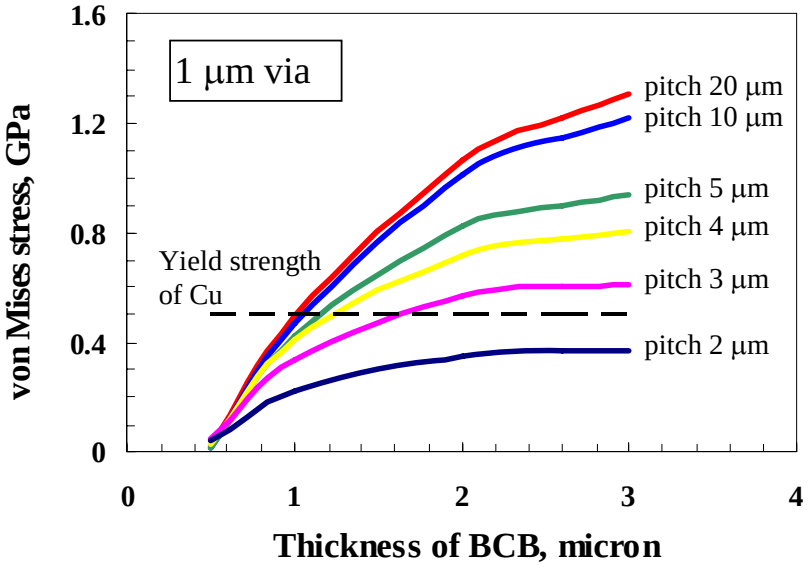
Computed stress values agree reasonably well with experimental values, as determined using XRD.

J. Zhang, M.O. Bloomfield, J.-Q. Lu, R.J. Gutmann, and T.S. Cale, "Modeling Thermal Stresses in 3D IC Inter-Wafer Interconnects", to be published in IEEE Trans. on Semiconductor Manufacturing, Nov. 2006.

Thermomechanical Modeling

Maximum von Mises Stresses





- Larger via size, smaller via pitch and thinner BCB thickness are desired to avoid plastic yield of Cu vias

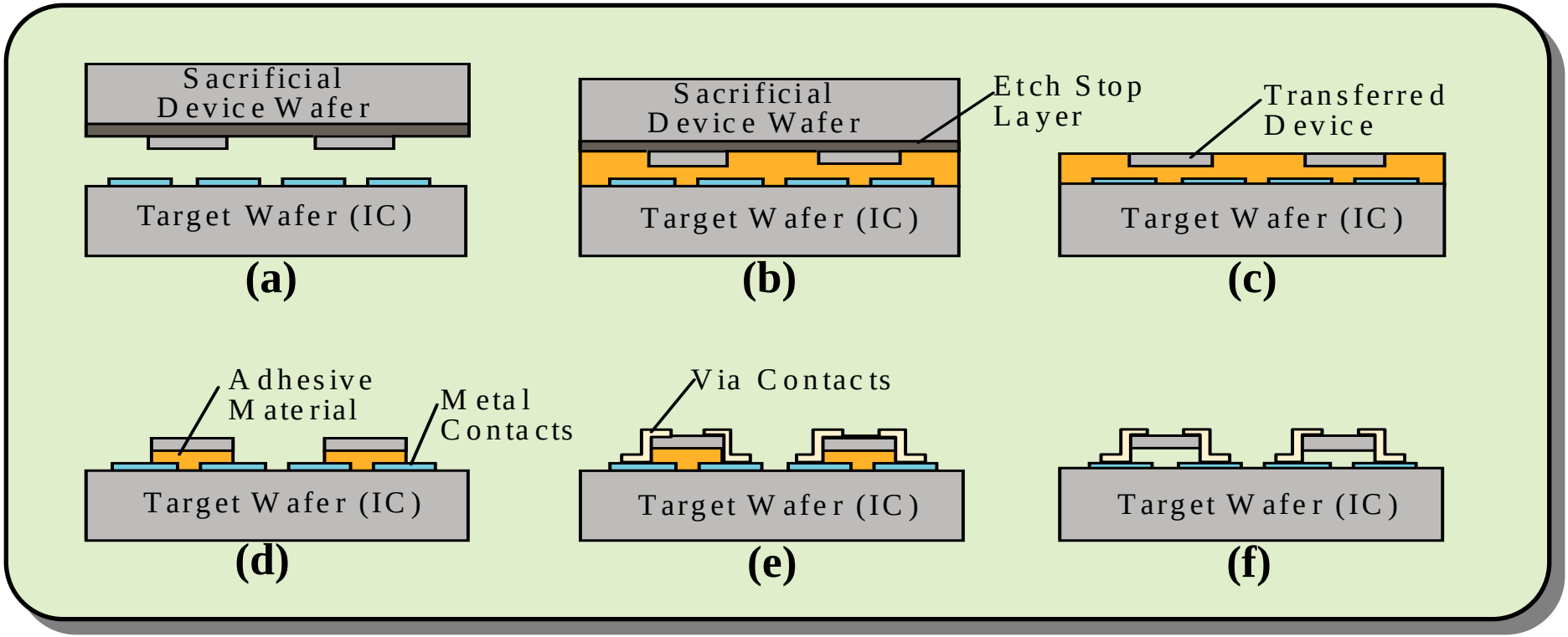
Zhang, Bloomfield, Lu, Gutmann, Cale, Microelectronic Engineering, 82, pp. 534-547, 2005.

Comparison of Wafer-Level 3D Integration with SoCs and SiPs

	SoCs	SiPs	3D ICs
Performance (speed, frequency, power)	😐	☹	☺
Signal process packing density	😐	☹	☺
Manufacturing cost in high quantities	😐	☹	☺
Heterogeneous Integration	☹	☺	😐
Manufacturing cost in low-medium quantities	☺	😐	☹
Manufacturing ready	😐	☺	☹

For high manufacturing quantities of high performance, heterogeneous products, wafer-level 3D ICs have a significant POTENTIAL advantage

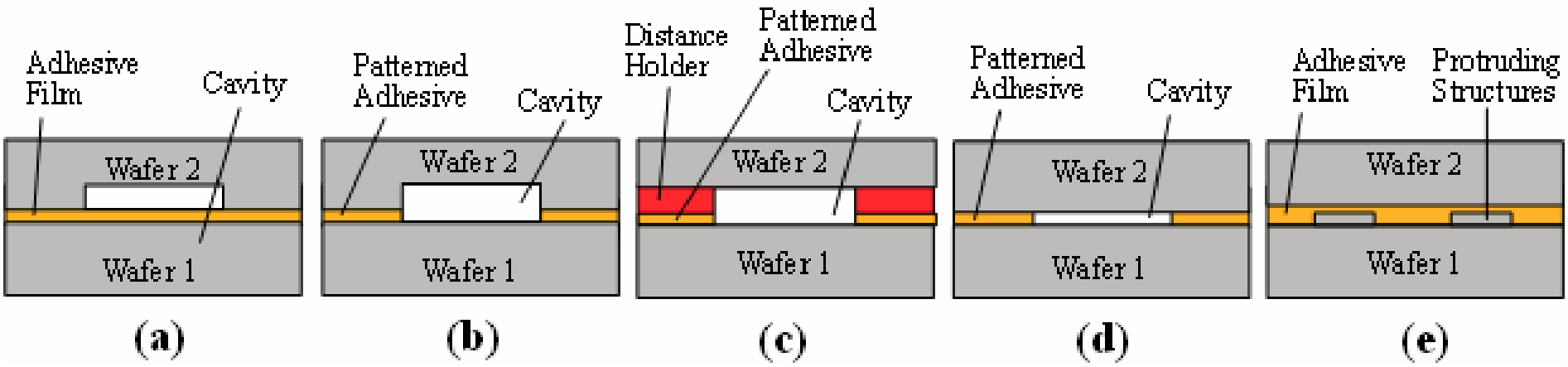
Integration of MEMS and ICs

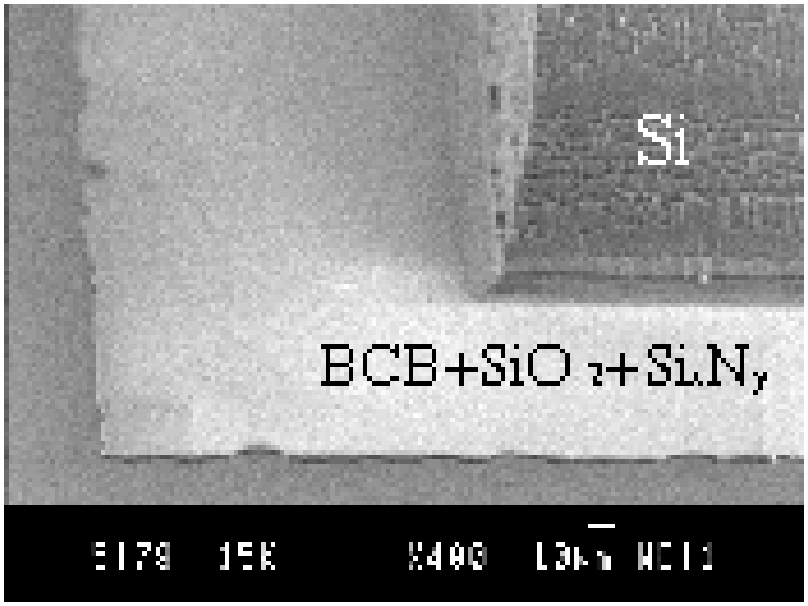


- **Extremely thin film (< 0.3 μm) structures with small feature sizes (< 1 μm) and small via contacts (< 3x3 μm²) can be integrated with CMOS wafers**

(F. Niklaus, Royal Institute of Technology, Sweden)

Manufacturing of Microfluidic Devices for bioMEMS

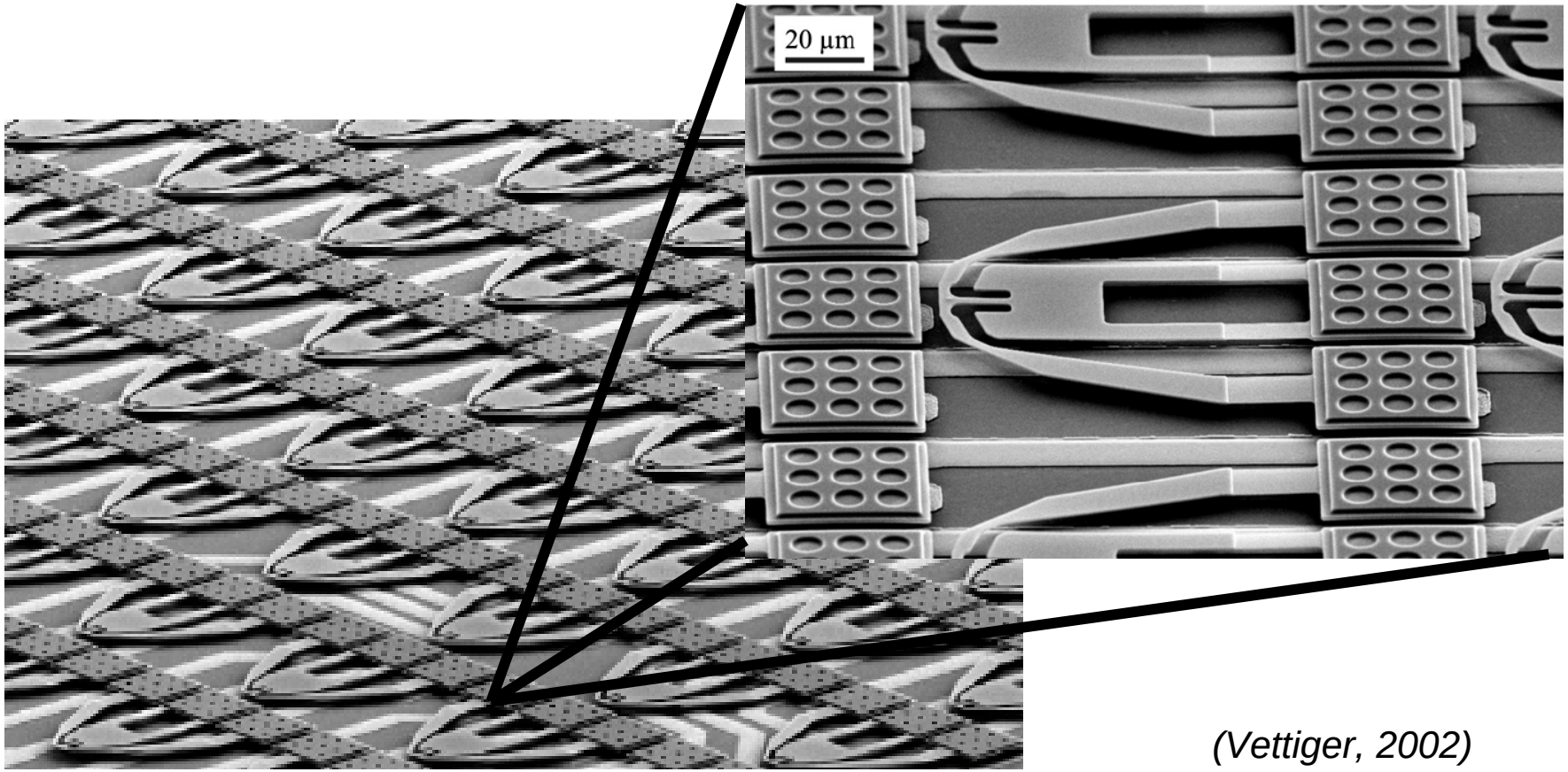




(Frank Niklaus, KTH)

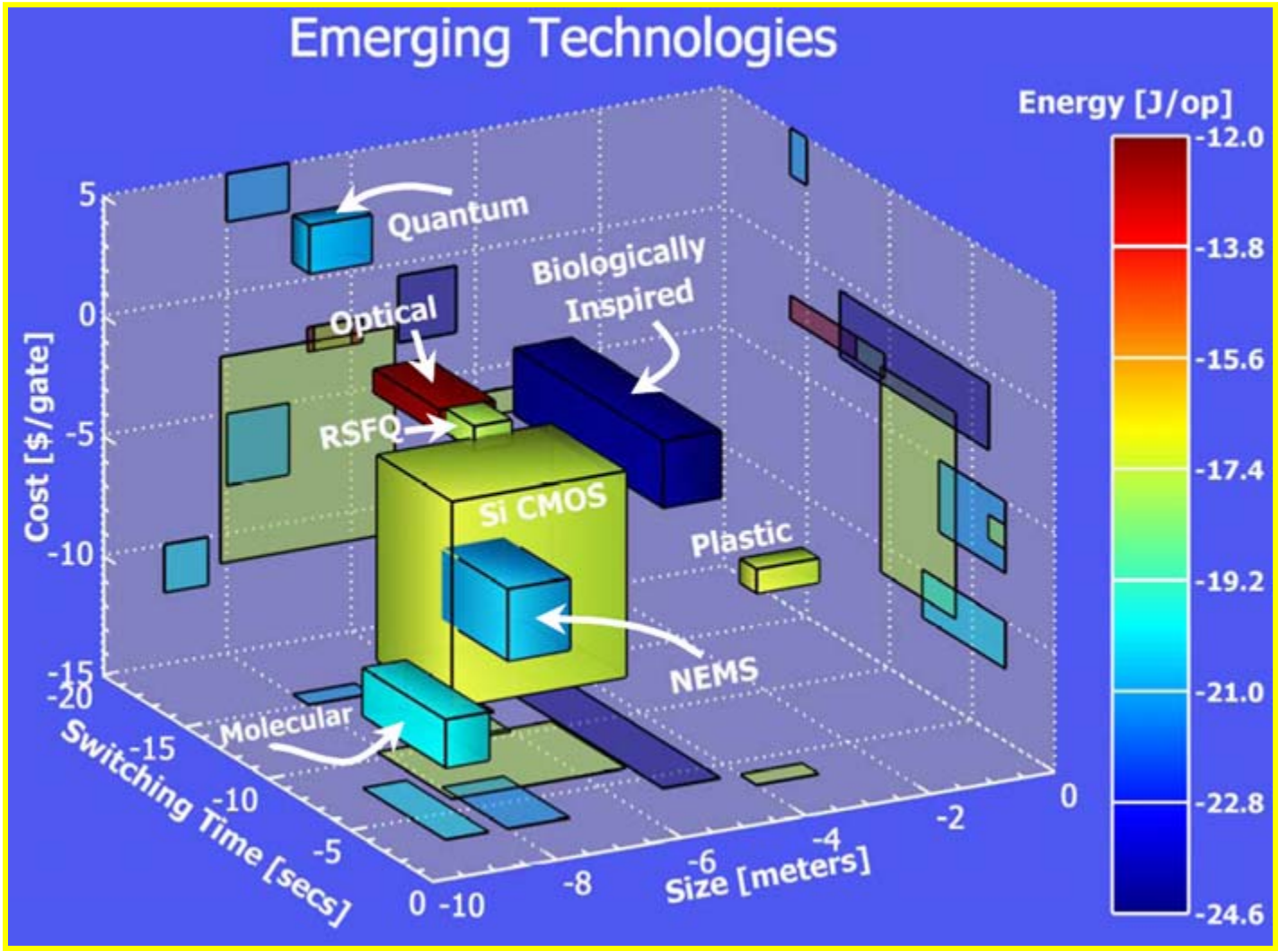
- PECVD SiNx as additional diffusion barrier material
- He leak tests show significantly less He absorbtion of sealed cavities as compared to non-sealed cavities

IBM's Millipede Data Storage:
Wafer Bonding to Fabricate Millipede Read-Write Head



(Vettiger, 2002)

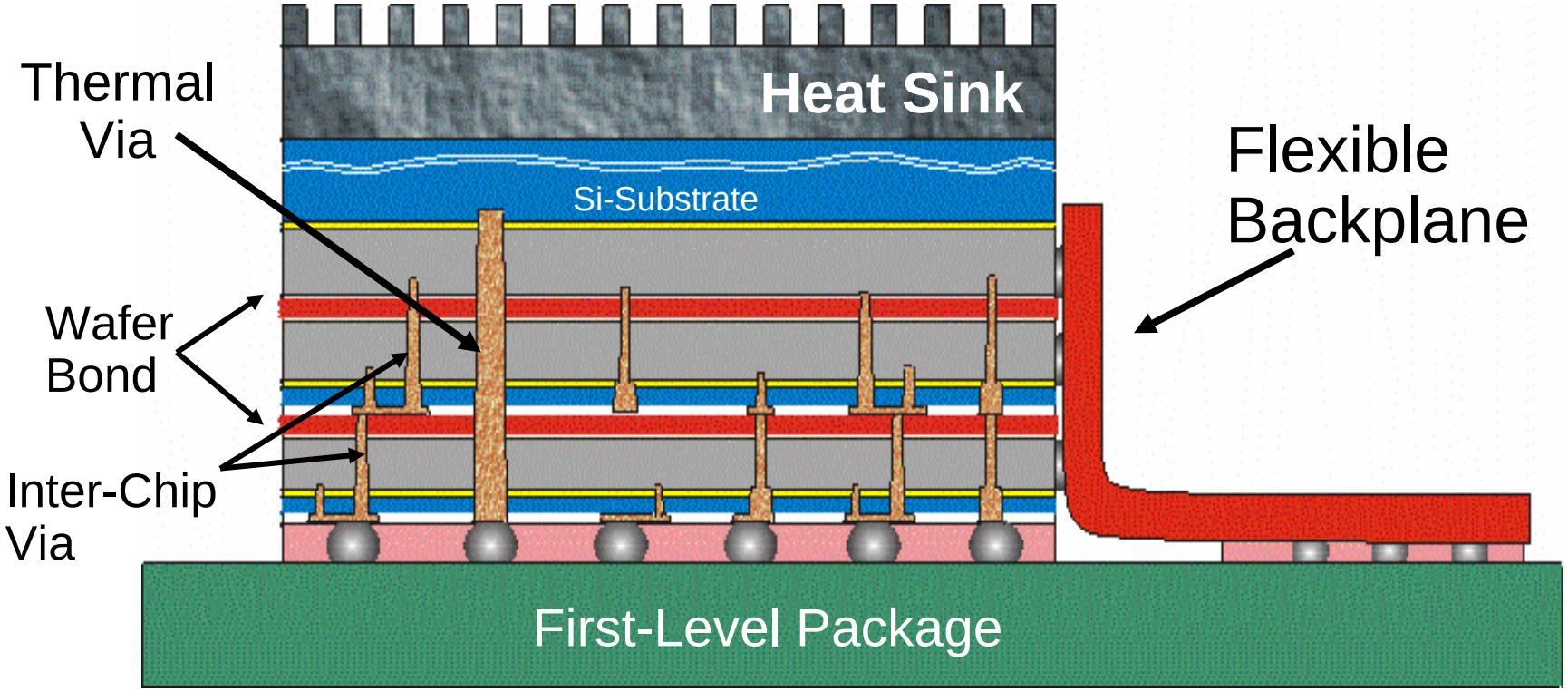
- **Arrays of membrane tips that can create pits with a side length of about 10 nm using heating of the polymer surface**
- **4000 tips on a 6.4 mm x 6.4 mm area can store the data of 25 DVD**



ITRS 2005

- The emerging devices, materials and processing are most likely incompatible with silicon processing technology
- 3D Integration is the natural choice for integrating future silicon CMOS with emerging devices and materials

3D Package with Thermal Vias and Flexible Backplane for Heterogeneous I/O Capability

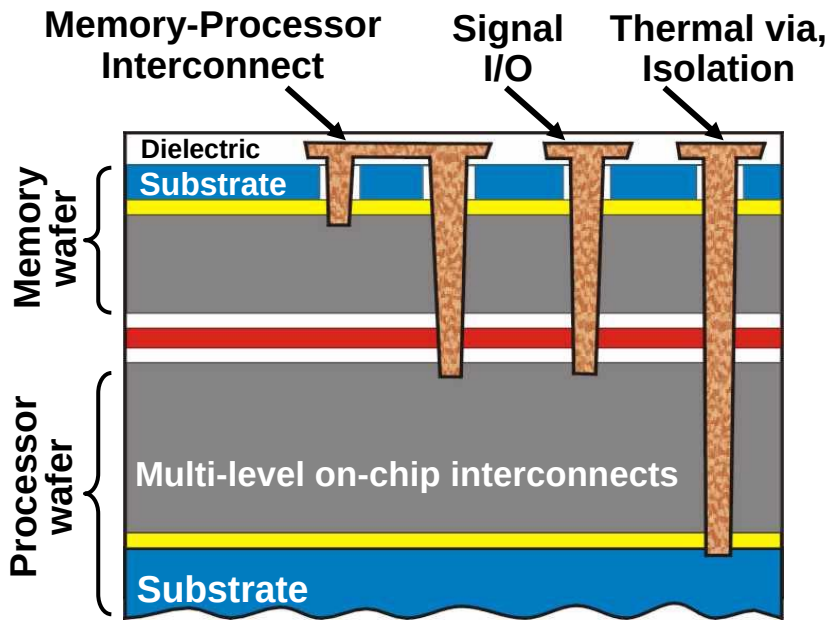


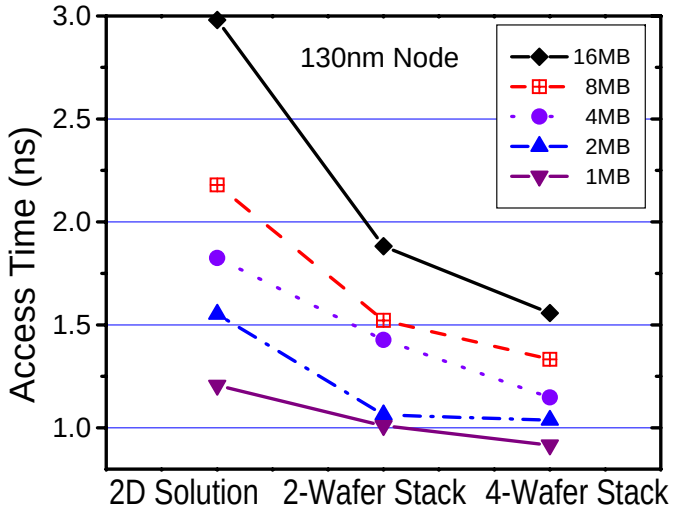
- Thermal/ ground vias enable cooling and electrical isolation
- Edge contracts offer additional I/O capability

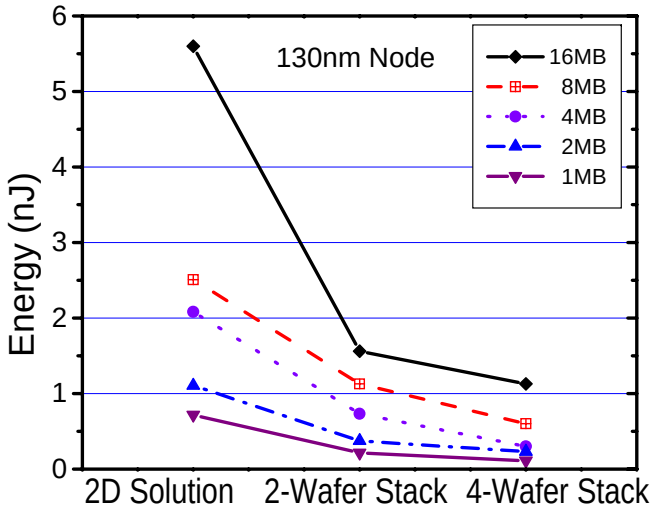
J.-Q. Lu, A. Jindal, P.D. Persans T.S. Cale, and R.J. Gutmann, 2003 Intern'l Conference on Compound Semiconductor Manufacturing Technology, pp. 91-94, May 19-22, 2003.

3D Integration of Memory with Processor

(for memory-intensive applications)



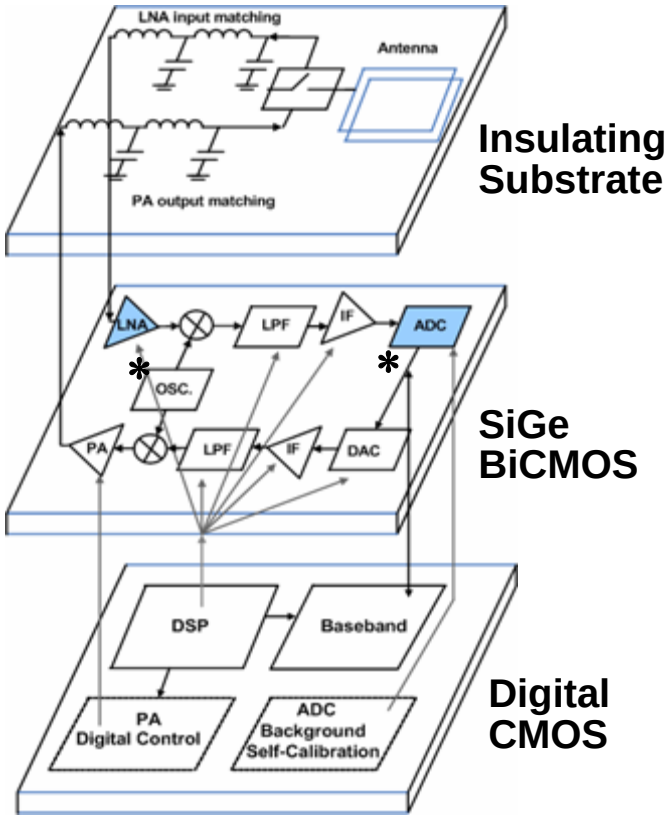




- Advantages Compared with 2D SoC or SiP:
  - Broad memory bandwidth and short cache latency
  - Power consumption reduction within interconnect network
  - Low inductance with low ΔI noise

A.Y. Zeng, J.-Q. Lu, K. Rose, and R.J. Gutmann, IEEE Design & Test of Computers, Vol. 22, No. 6, pp. 548-555, Nov/Dec. 2005.

3D Hyper-Integration of Next-Generation Transceivers for Wireless Communications

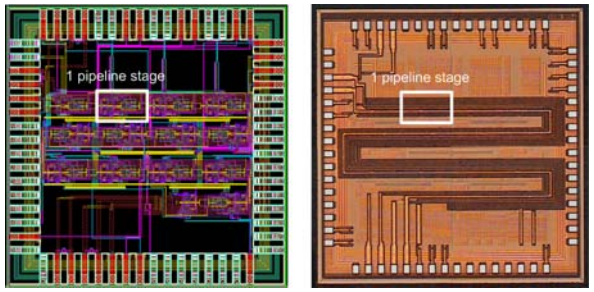


R.J. Gutmann, A.Y. Zeng, S. Devarajan, J.-Q. Lu and K. Rose, J. of Semiconductor Technology and Science, Vol. 4, No.3, pp. 196-203, Sept. 2004.

S. Devarajan, PhD. Thesis, RPI, 2006.

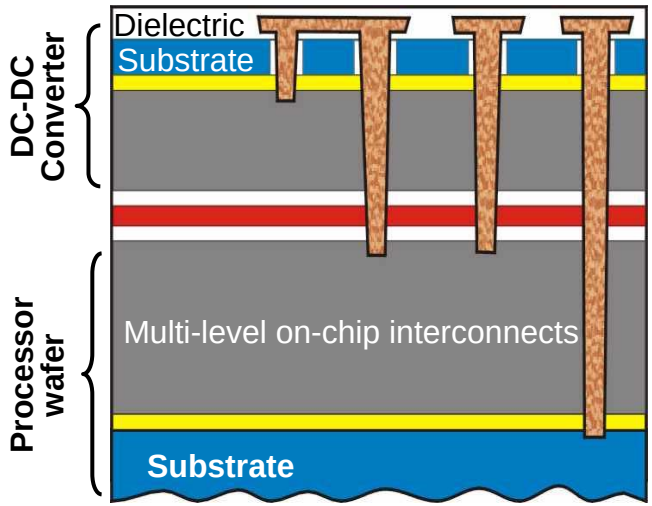
RF System Partitioning

- Hyper-integration with technologies optimized for realizing high-performance components.
  - Integrated antenna and high Q inductors
  - SiGe BiCMOS analog blocks
  - Digital CMOS processing
- ***Software-radio (SWR)*** requires a very high-performance ADC not currently possible.
- SiGe BiCMOS vs CMOS ADCs
  - Projections for realizing SWR ADCs
- Fabricated and/or simulated results:
  - SiGe BiCMOS ADC
  - SiGe HBT LNA

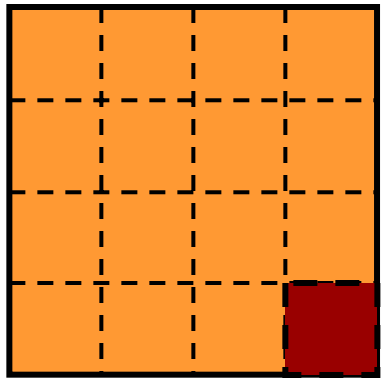


14-bit SiGe BiCMOS ADC chip layout & fabricated die

Monolithic 3D Hyper-Integration Approach to Power Delivery



Top View of DC-DC Converter Die
(Cellular Design)

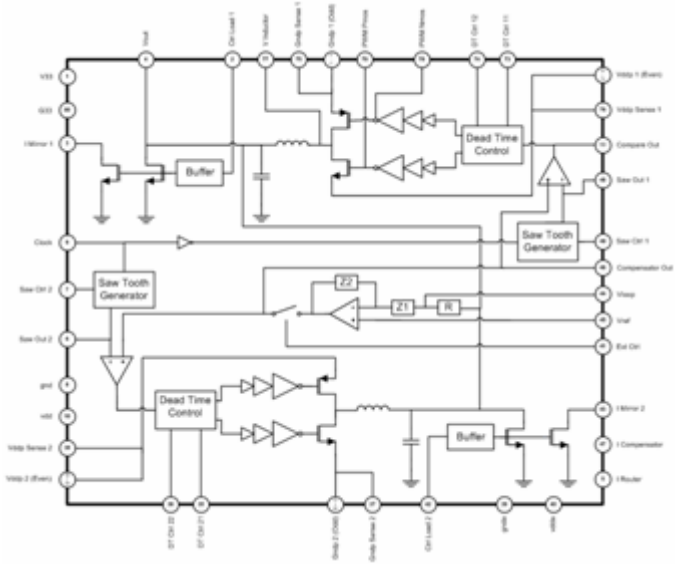


Prototype Converter Cell Design

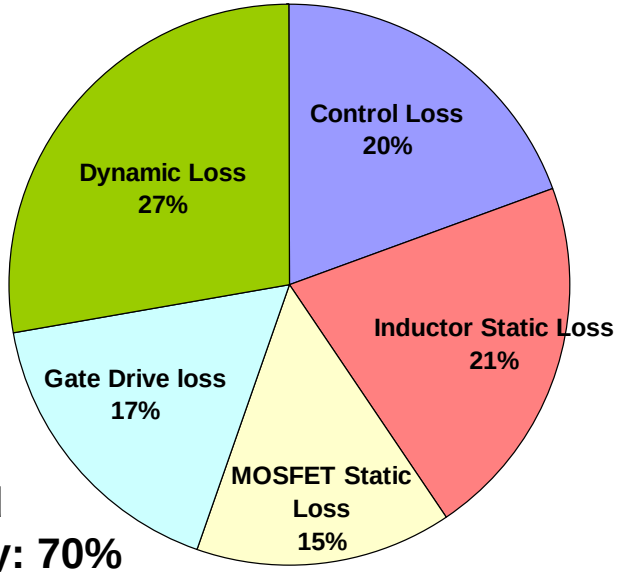
- Monolithic DC-DC Converter Vertically Integrated with Processor Chip
  - Minimize interconnect parasitic effects
  - Easy to supply and distribute multiple supply voltages
  - Flexible platform enables dynamic voltage scaling
  - Significantly reduced package pin counts (I/Os)
  - Uniform, high-density power/ground vias to processor
- High Switching Frequency, Wide Bandwidth Control

DC-DC Converter Design & Performance

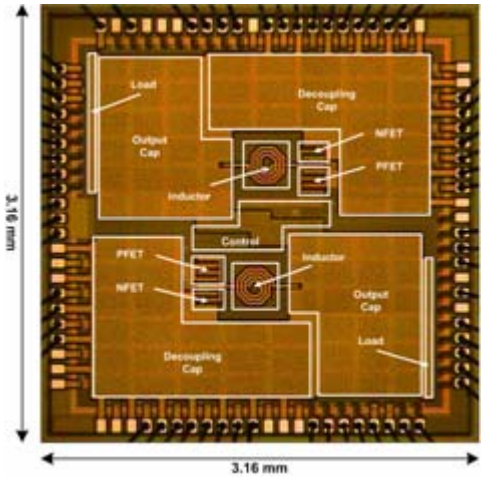
Die Block Diagram



Power Loss Breakdown



Projected Efficiency: 70%



Chip Micrograph

Fabricated through MOSIS

	Area Occupied (%)
Decoupling Capacitors	31
Output Capacitors	27
Converter / Control	11
Bond Pads / ESD	31

To be published.

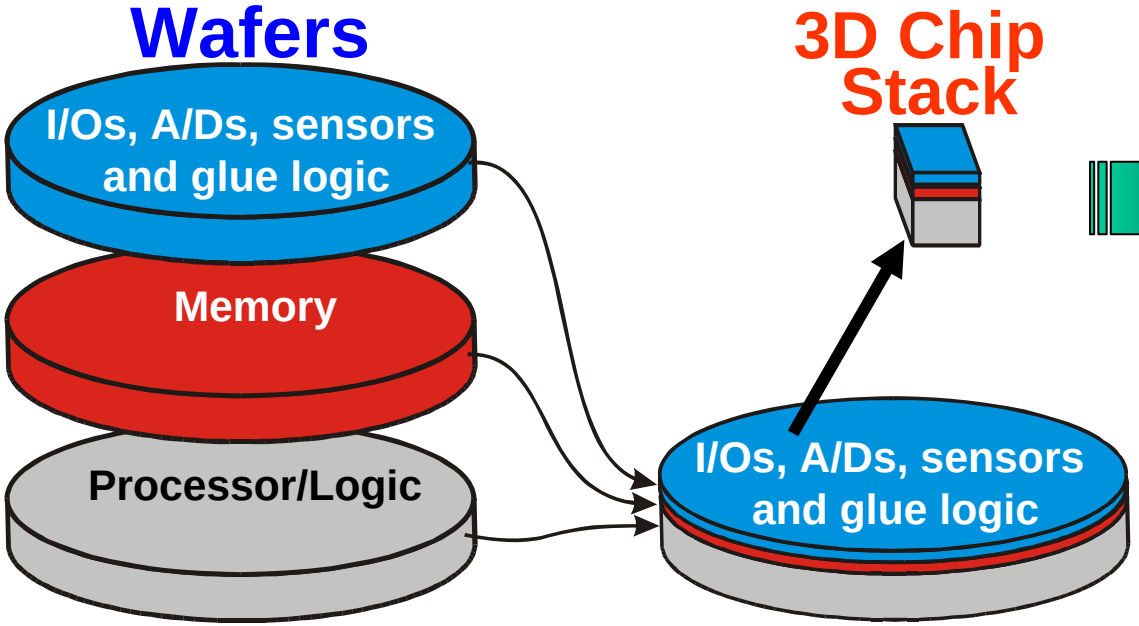
D. Giuliano, M.S. Thesis, RPI, 2006.

Conclusions

- Wafer-level 3D integration offers heterogeneous integration with micron-sized through-die interconnectivity, alleviates the interconnect bottleneck for complex ICs, and offers the highest volume density of any integration technology platform.
- A variety of technology platforms do not indicate any technology showstoppers.
- Cu-Cu bonding is favorable for applications that need highest density of inter-wafer vias, such as highest performance digital applications.
- Adhesive bonding is favorable for applications that need a more modest density of inter-wafer vias, such as heterogeneous integration of diverse technologies.
- Metal-adhesive via-first platform combines both Cu-Cu bonding and adhesive bonding advantages, and is attractive for wafer-level packaging (WLP) platforms.
- Wafer-level 3D is a disruptive technology, requiring major industry infrastructure commitments.

3D Hyper-Integration

An emerging architecture for future chips



ICs
- Improve performance
- Increase functionality
- Increase density/bandwidth

Heterogeneous Systems
- Mixed signal
- Wireless
- Terahertz
- Optical

Micro-Nano Interface

Bio-Chips/MEMS
(Microfluidics/sensing/logic)
- Parallel sensing/evaluation
- Reaction pathways
- Synthesis

- Utilizing vertical dimension to increase performance, bandwidth, functionality and density with micron-sized inter-wafer vias
- Enabling technology for future ICs and low-cost Micro/Nano/Electro-Opto/Bio heterogeneous systems