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Direct Bond Interconnect for Advanced Packaging Applications

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Outline

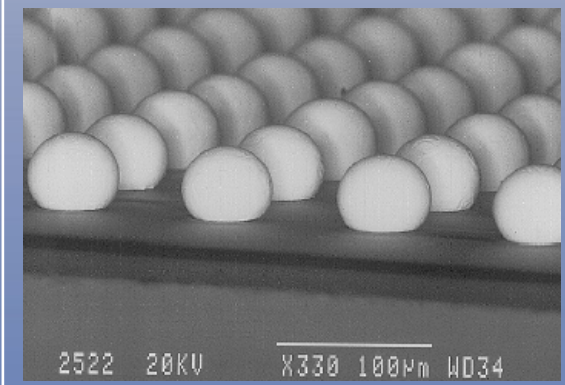
- Advanced Assembly & Packaging Requirements
- Direct Bond Interconnect
  - Process Flow
  - Process Capability
    - Mechanical
    - Electrical
    - Reliability
- DBI Application to Advanced Assembly & Packaging

Assembly and Packaging Difficult Challenges *

- Wafer Level CSP
  - Reduced I/O pitch for small die with high pin count
  - Solder joint reliability
  - Wafer thinning
  - TCE mismatch compensation for large die
- Close Gap Between Chip and Substrate
  - Silicon I/O density increasing faster than the package substrate technology
  - Production techniques will require silicon-like production and process technologies
- High Current Density Packages
  - Electromigration will become a more limiting factor

* International Technology Roadmap for Semiconductors 2006 Update

Wafer Level CSP Criteria

Technology	Wafer Bumping / PCB	Next Generation
	 *P.A. Magill, Unitive, 1998*	?
Pitch	Non-Planar	Planar
Solder Joint Reliability	Solders (Alloys)	No Solders (Alloys)
Electro-migration	Solders (Alloys)	No Solders (Alloys)
Wafer Thinning	Before Assembly	After Assembly
TCE Mismatch	Silicon vs. PCB	Eliminate PCB TCE
Silicon Scaleable Package	NO	YES
Silicon-like Production	NO	YES

Will Next Generation Assembly & Packaging Technology be Required to Meet Upcoming Challenges ?

Direct Oxide Bonding

- Spontaneous Bond Initiated by Contact
- Does Not Require
  - Adhesives
  - Anodic Voltage, Pressure, and Temperature
  - Solders and Reflow
  - Thermo-compression or Fusion Temperature and Pressure
- Requirements
  - Planar, Low RMS Surface
  - Appropriate Surface Activation / Passivation
- Capabilities
  - High Direct Oxide Bond Strength w/out High Temperature
  - 3D Electrical Interconnections (Direct Bond Interconnect)

Direct Oxide Bond Process Flow

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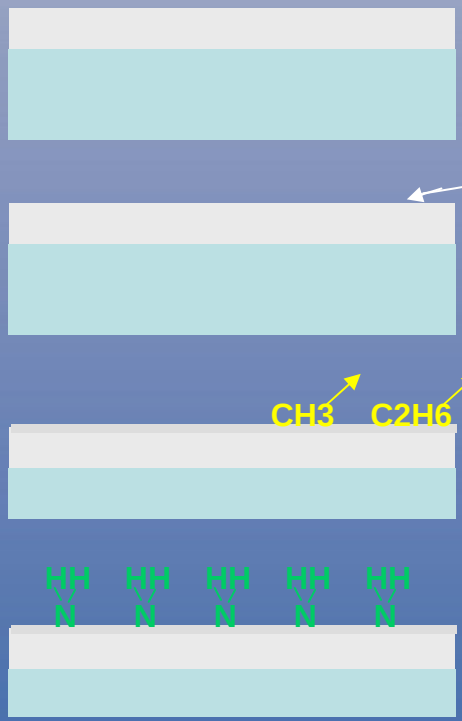
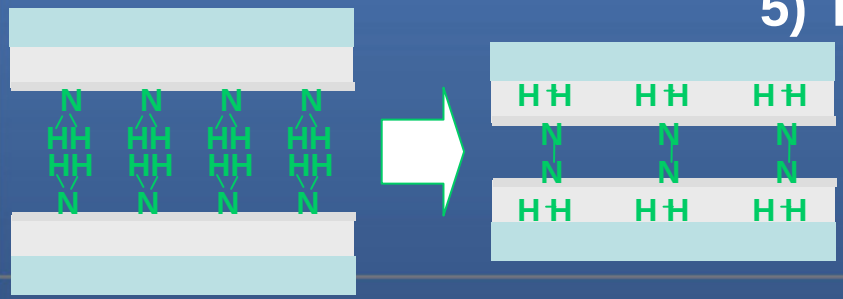


1) Deposit Silicon Oxide

2) Chemo-Mechanical Polish
   - < 0.5 nm RMS Specification
   - < 25 um Bow and Warp

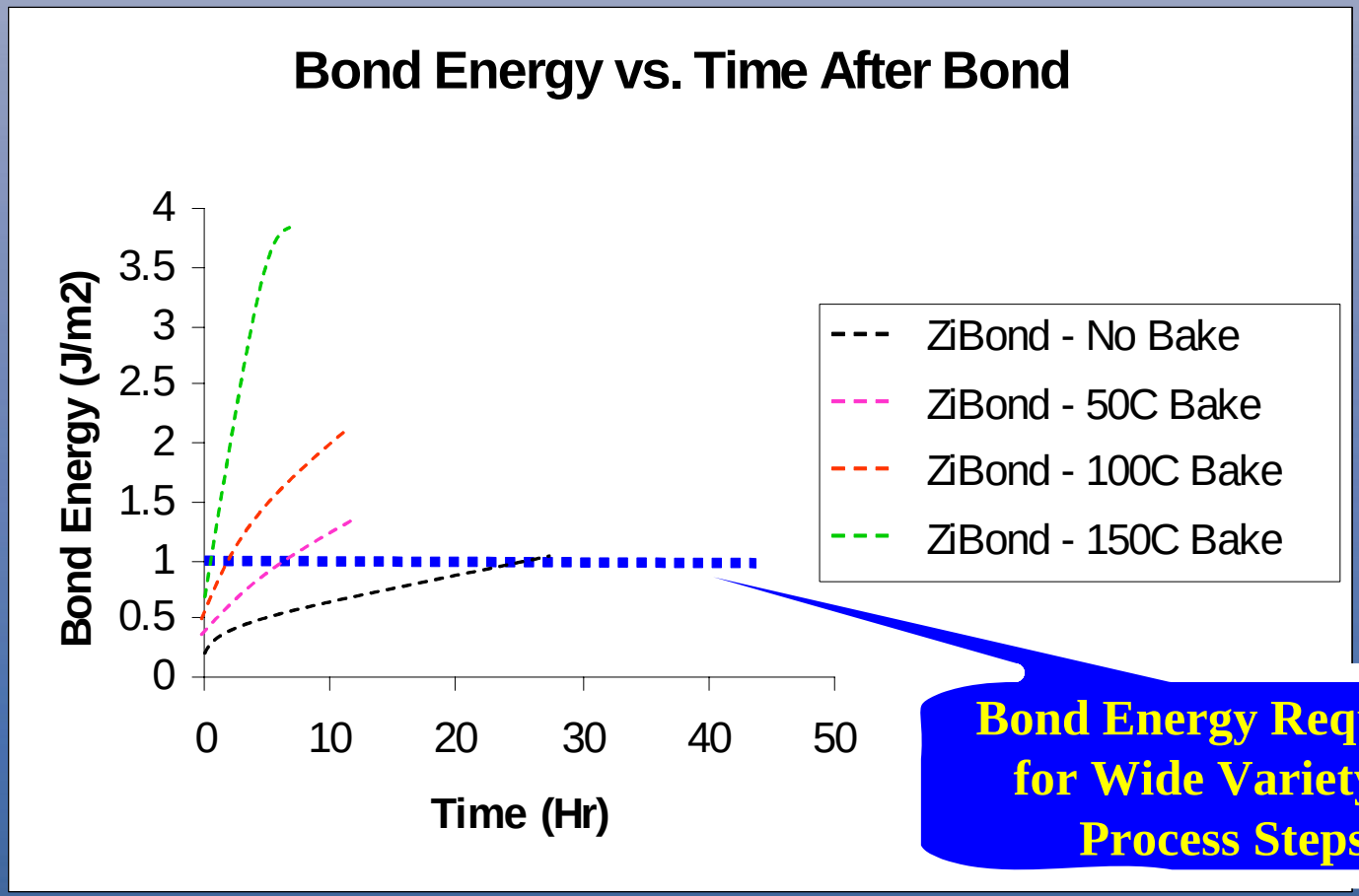
3) Inert RIE
   - Regenerate Uncontaminated Surface
   - "Activate" (Enhance SiO_2 Porosity)

4) Ammonia-based Dip
   - Terminate Surface with Amine Groups



5) Place Surfaces Together
   - Spontaneous Chemical Reaction
   - $Si\text{-}NH_2 + Si\text{-}NH_2 = Si\text{-}N\text{-}N\text{-}Si + 2H_2$
   - H_2 Diffusion from Bond Fixes Reaction

Direct Oxide Bond Kinetics



Very High Bond Energy Possible at Low Temperature…..
but no Electrical Interconnections with Bond

Direct Bond Interconnect Process Flow

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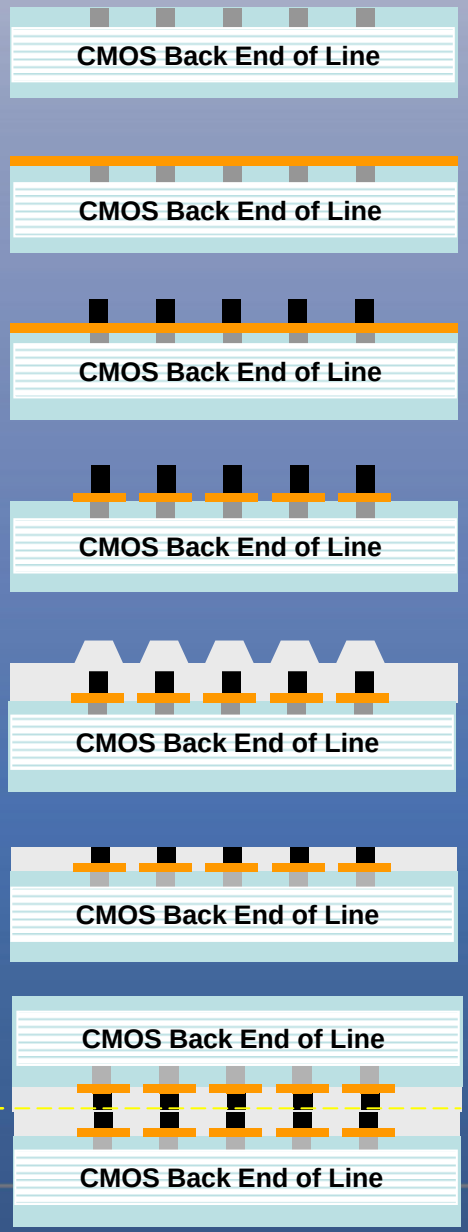


1) **Starting Wafer**
   - Planar Surface
   - Exposed Filled Vias

2) **Deposit Seed**

3) **Plate DBI Metal**

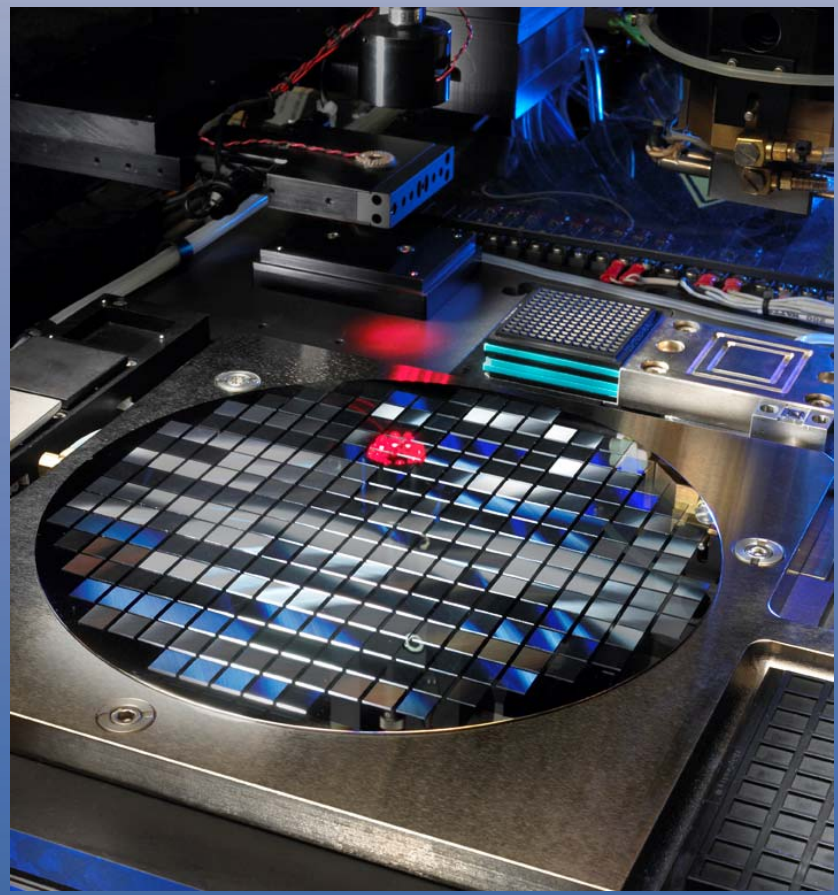
4) **(Blanket) Etch Seed**

5) **Oxide Deposition**

6) **Planarization**
   - Oxide Bonding Mechanical Spec < 0.5nm

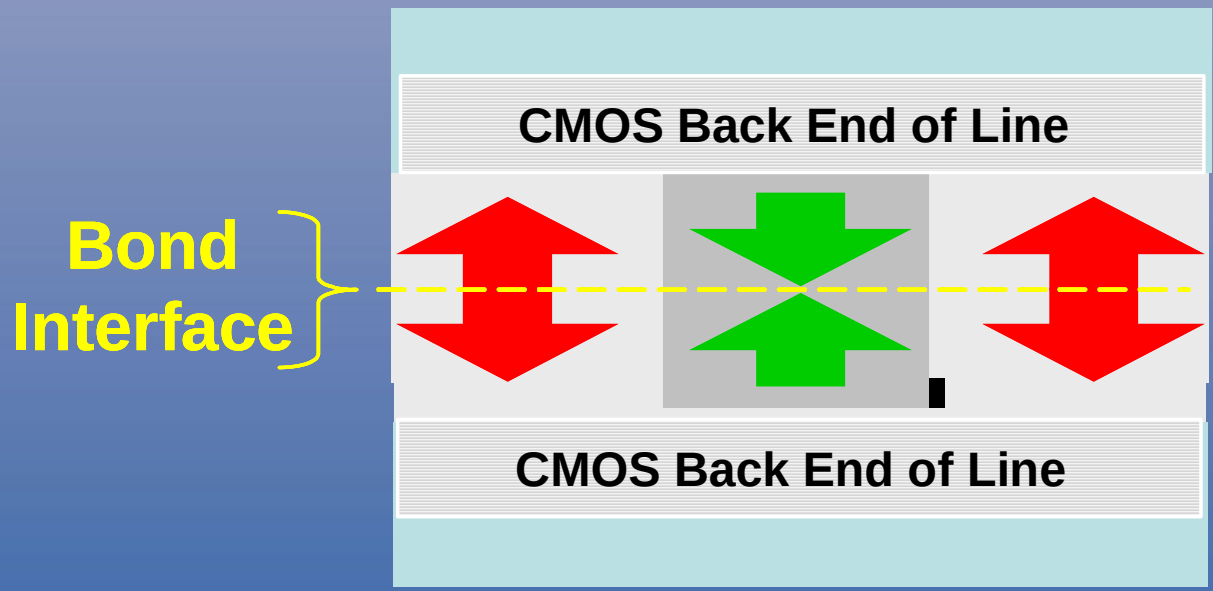
7) **Place 2 DBI Surfaces into Contact**
   - Conventional Pick-&-Place
   - Room Temperature, Direct Oxide Bonding

Die Alignment / Placement



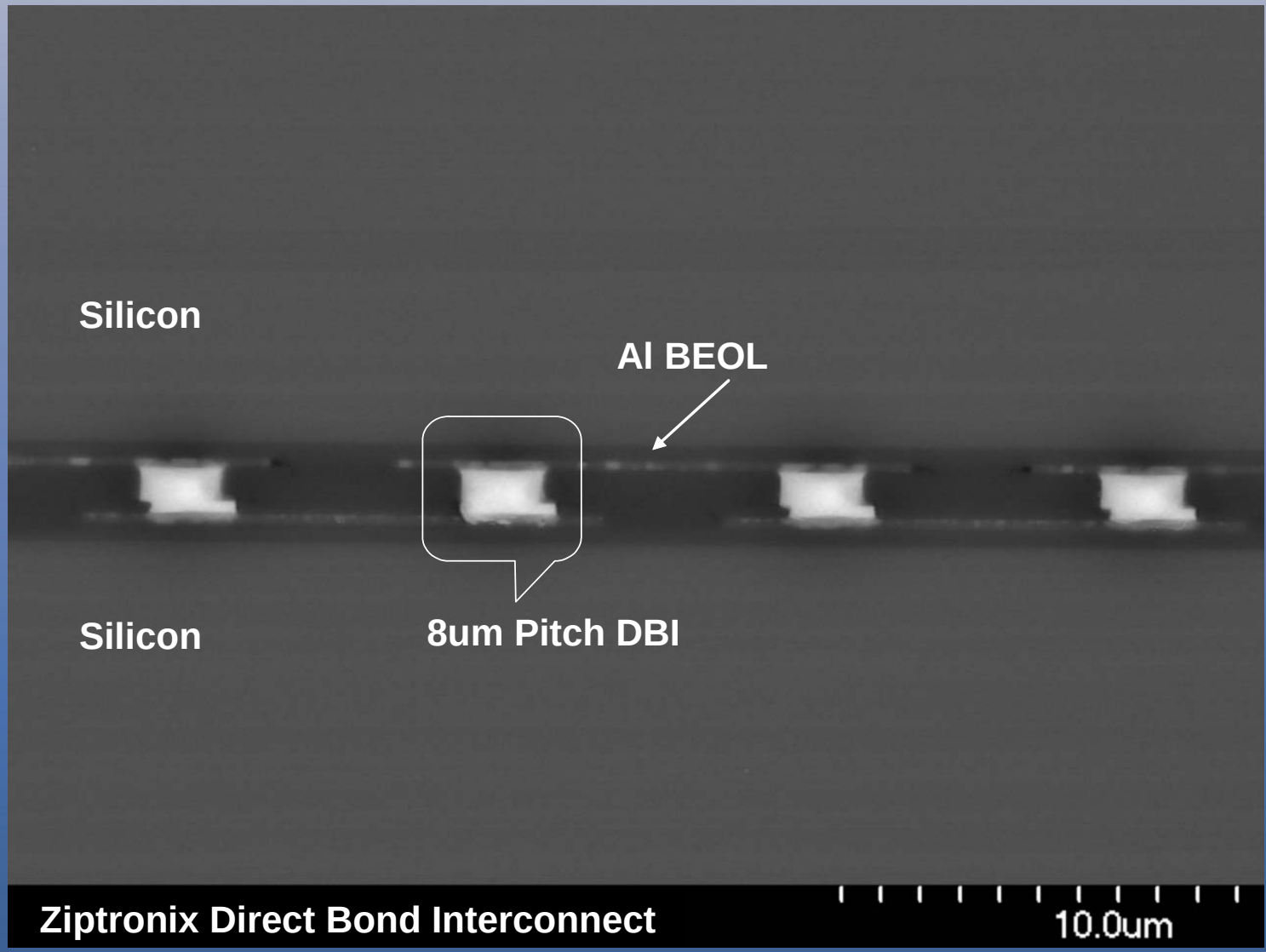
Alignment / Placement Compatible with Conventional Tools
Demonstrated Placement Accuracy < +/- 1 um over 3 σ

Direct Bond Interconnect Electrical Interconnections



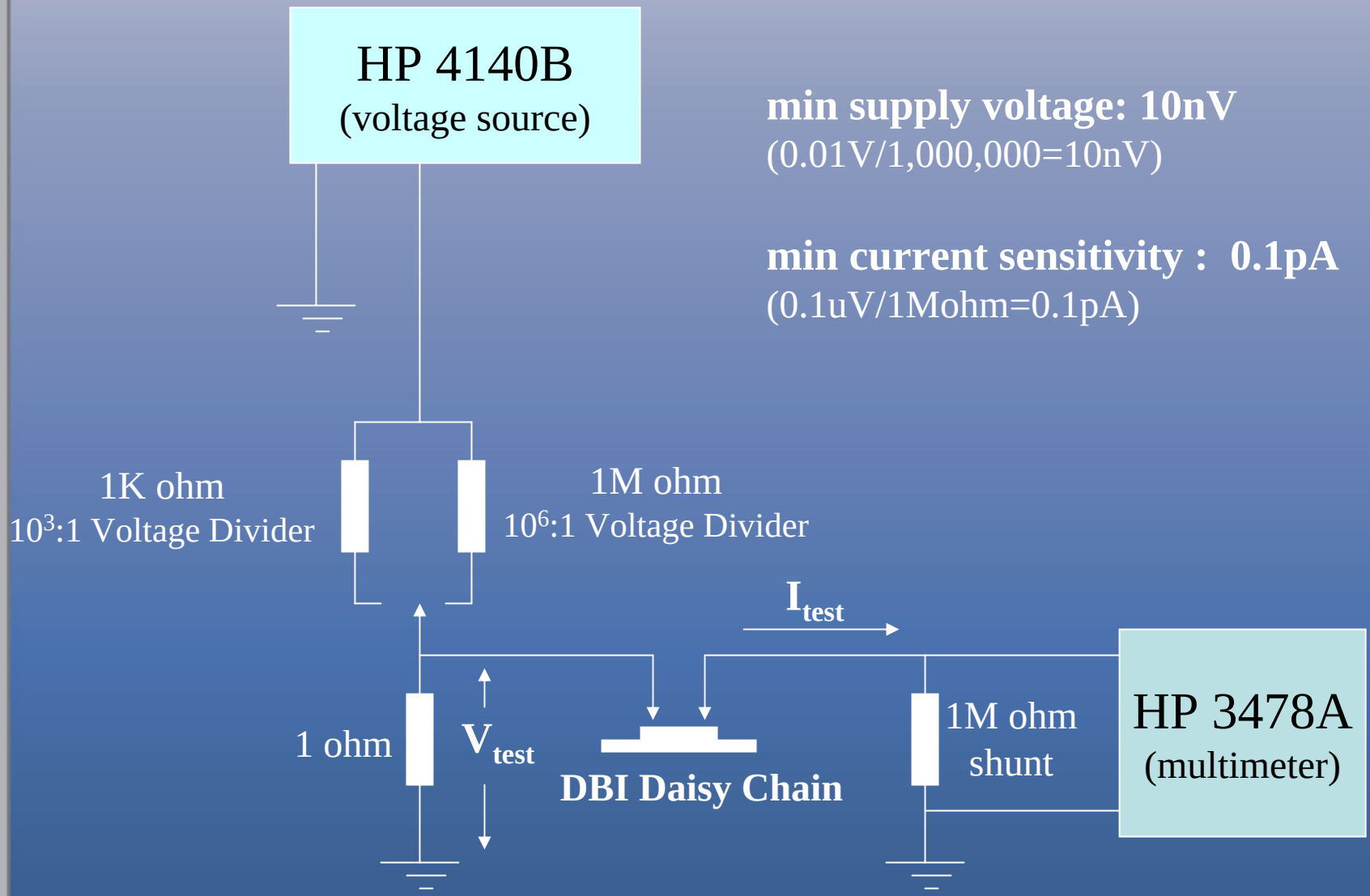
300-350℃ and Very High Oxide Bond Energy Compress Metal

Direct Bond Interconnect Cross-Section



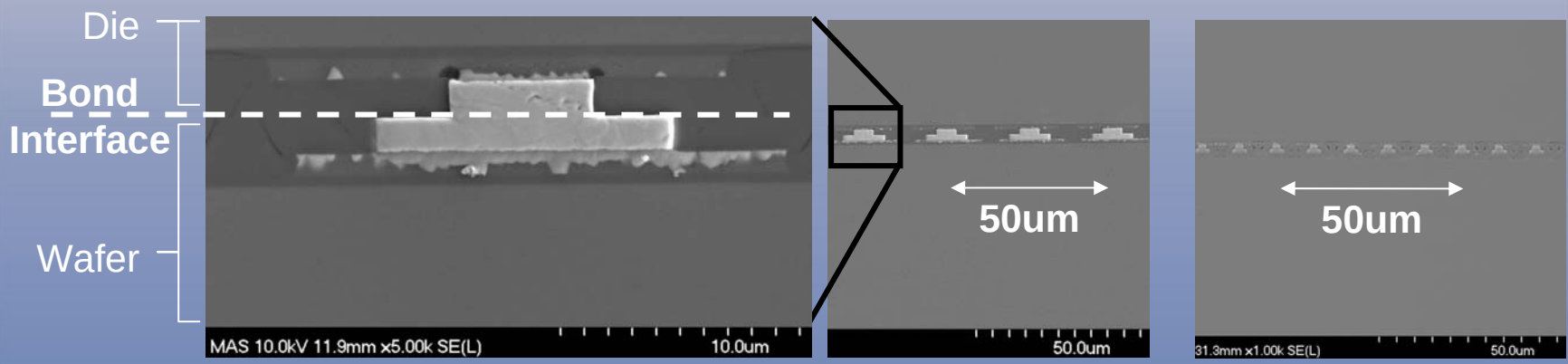
Scaleable to < 8 um Pitch

Direct Bond Interconnect Low Voltage Test



"Barrier-Free" at 1pA (<50fV> @ 50mΩ / Connection)

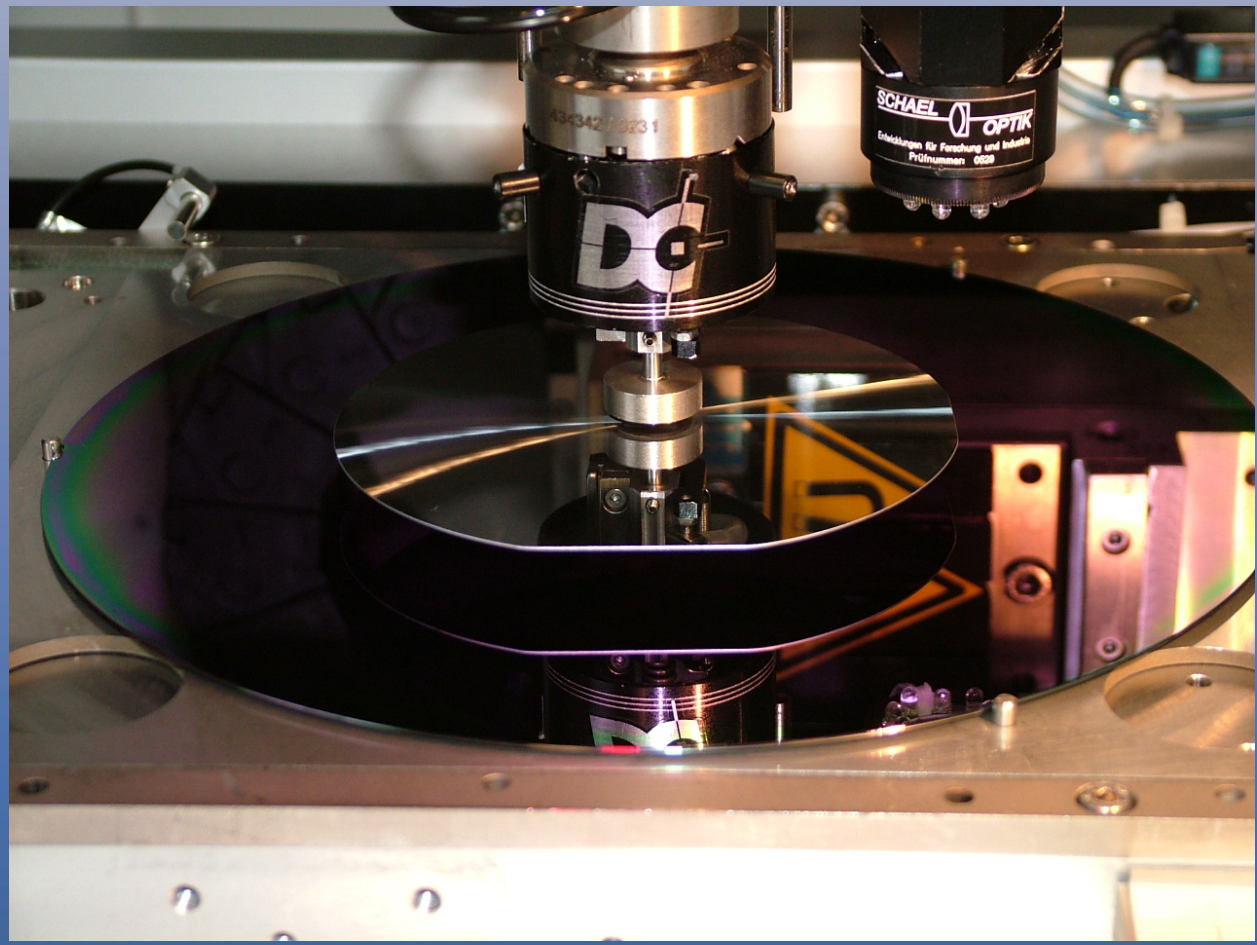
Direct Bond Interconnect Reliability



		50um Pitch	25um Pitch	10um Pitch
	Test Part	9,950 Serial Connections	72,500 Serial Connections	460,000 Serial Connections
	Typical <R>	<20 mΩ (<1.5 Ω/um²)	<50 mΩ (<0.5 Ω/um²)	<50 mΩ (<0.5 Ω/um²)
Bare Die Reliability	**T cycling** (-65C - 175C)	1,000 Cycles, 18/18 PASS 10,000 Cycles, 9/9 PASS	1,000 Cycles, 5/5 PASS 10,000 Cycles, 4/4 PASS	1,000 Cycles, 10/10 PASS
	HAST (130C, 85%RH, 33psi)	96 Hours 12/12 PASS	288 Hours 6/6 PASS	

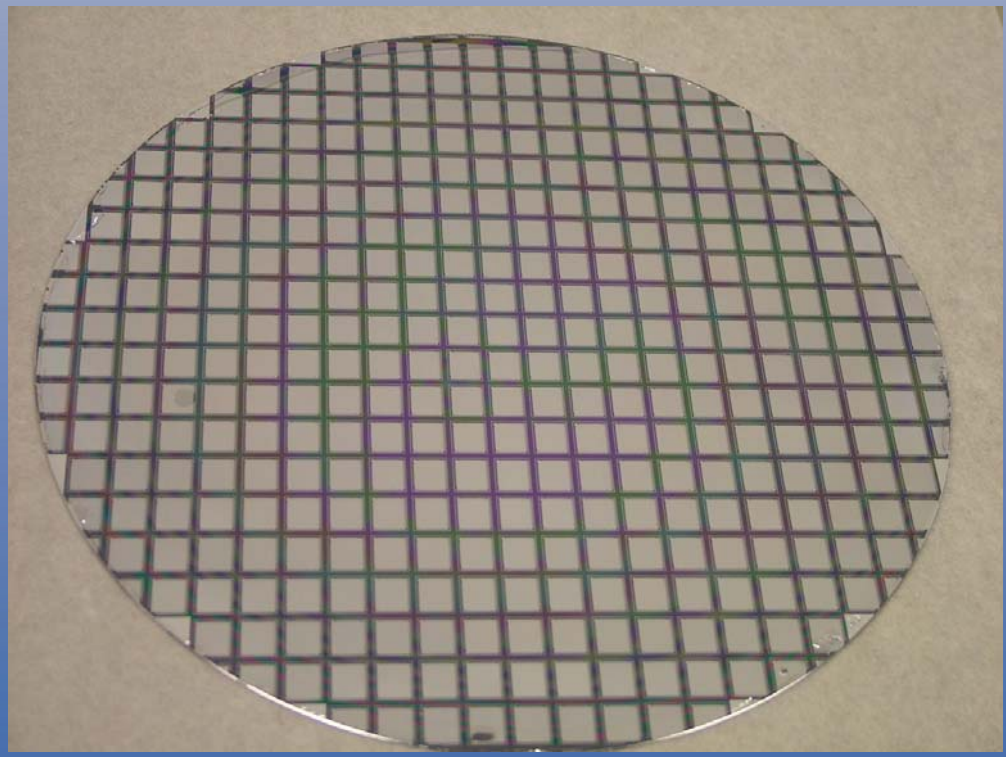
Reliable Technology

Wafer Align / Place



Alignment / Placement Compatible with Conventional Tools at Wafer Level with Low Cycle Time

Wafer Level Capability



Process Flow

1) DBI Wafer-Wafer Bond
2) Remove Silicon Substrate
3) Remove Field Oxide
4) Probe Daisy Chain Die

Results

> 300 Die / Wafer
> 450,000 Connections / Die
10 um Pitch, 1 M / cm^2
< 1 um Bond Alignment
> 2/3 of Die Fully Functional
Dominant Failure Mode is Seed Metal Defects
Typical DBI Yield ~ 99.999%

Direct Bond Interconnect Scales to > 200mm

Manufacturing Implementation

Wafer Bumping

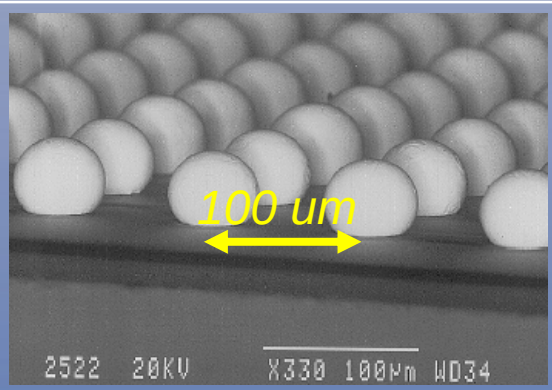
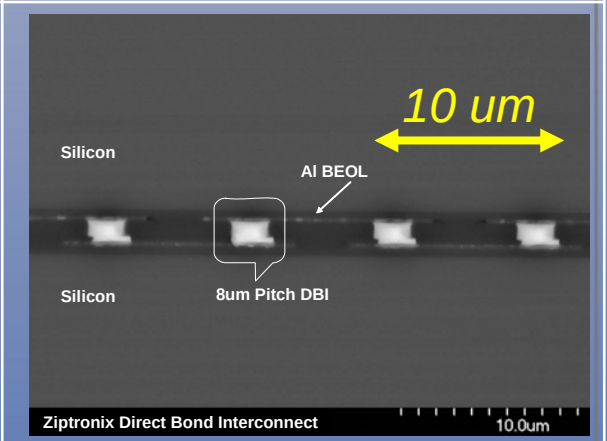
Foundry (Front End)		Packaging (Back End)
Front-End-of-Line Transistor Fab	Back-End-of-Line Interconnect Fab Planarization	→ Assembly Package Test 3D & Wafer Level CSP

Direct Bond Interconnect

Foundry (Front End)		Packaging (Back End)
Front-End-of-Line Transistor Fab	Back-End-of-Line Interconnect Fab Bond Planarization (Wafer) Placement / Bonding	→ Assembly Package Test (Die) Placement / Bonding

Planarization Synergistic with Front End
Silicon-like Production and Process Technology

Wafer Level CSP Criteria

Technology	Wafer Bumping / PCB	Direct Bond Interconnect / Silicon Substrate
	 *P.A. Magill, Unitive, 1998*	
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TCE Mismatch	Silicon vs. PCB	Silicon Substrate
Silicon Scaleable Pkg	NO	YES
Silicon-like Production	NO	YES

Direct Bond Interconnect and Silicon Substrate Technologies are Potential Solutions to ITRS Assembly & Packaging Challenges

Summary

- Exceptional Oxide Bond Energy Enables Interconnections
- Interconnection Density Capability Beyond ITRS Roadmap
- Die-to-Wafer or Wafer-to-Wafer Formats
- Solder (Alloy) -Free Reliability > 10x JEDEC Requirements
- Silicon-like CMP Production Technology
- Synergistic with Wafer-Level Silicon Substrate CSP