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Advanced Process Technology
Thin Films Technology
Spansion Inc.

Advanced Patterning Thin Films

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FLASH FORWARD

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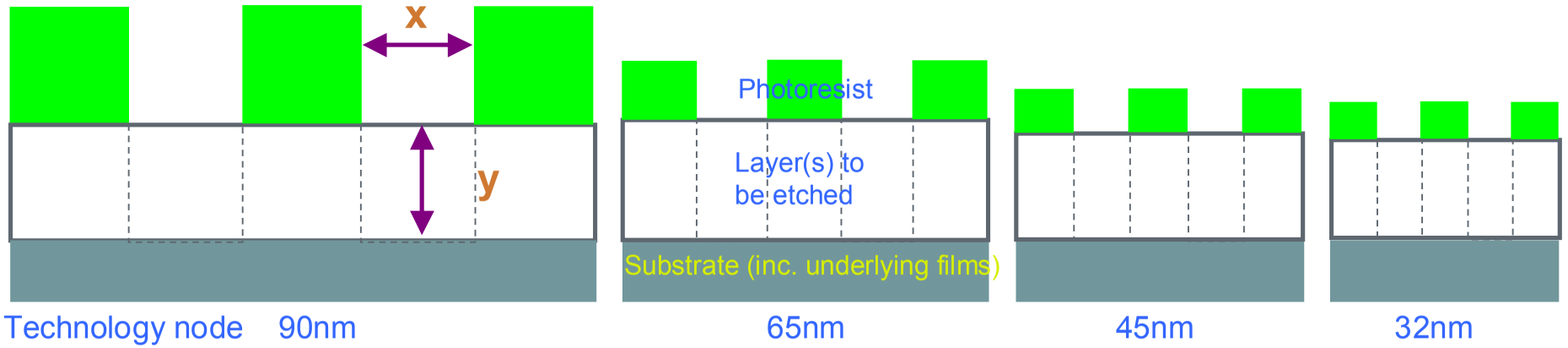
Outline

- ARC (Anti-Reflection Coating) & Hardmask module area overview
- ARC-Hardmask module development
- Films challenges associated with use of a-C
- Integration challenges associated with use of a-C.

ARC-Hard Mask overview

- Node-to-node migration to shorter λ to improve pattern definition.
- **Number of layers using amorphous carbon hard mask:**
  - **90nm: 0 layer → 65nm: 1 layer → 45nm: 3 layers → 32nm = 3+ layers?**
  - **Vendors for a-C or equivalent films:**
    - AMAT (APF),
    - NVLS (AHM),
    - ASM (NCP).
- **Use of SiON films as ARC layers continues with t/n/k optimization**

Why Hard Mask?



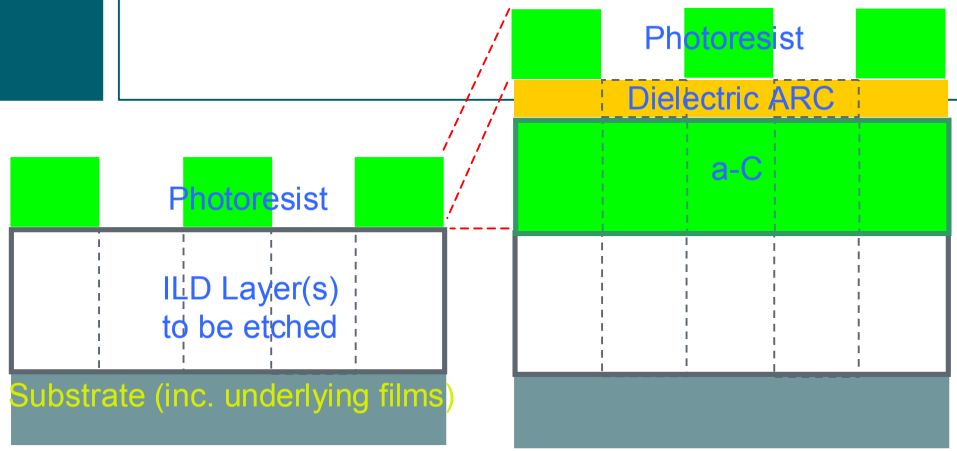
- **As technology (pitch) shrinks:**
  - **Lithography wavelength → shorter**
  - **DOF → smaller**
  - **Resist thickness → thinner**
  - **However, etch-layer thickness does not scale as fast**
  - **Insufficient resist margin.**

Masking Layer C	90nm	65nm	45nm	32nm
Wavelength	248nm	193nm	i-193nm	i-193nm
pitch (um)	1	0.74	0.49	0.39
Target DICD (arb. units)	1	0.69	0.39	0.31
Resist thickness (arb. units)	1	0.49	0.36	0.30
Etch layer thk (arb. units)	1	1.03	0.91	0.84
AR (relative)	1.0	1.5	2.3	2.7

AR = y / x

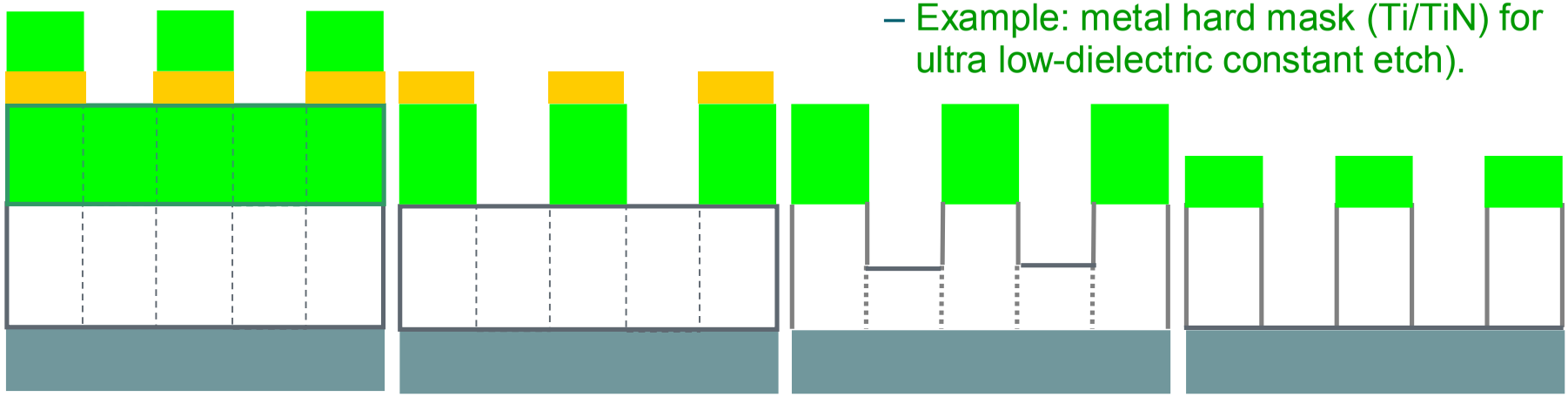
Why Hard Mask? (2)

- **Solution for insufficient resist margin:**
  - **To etch dielectric layer(s) with good etch selectivity to resist, use amorphous carbon**
    - organic film like resist: ashable
    - a.k.a. APF (AMAT), AHM (NVLS)
    - similar organic film is NCP (ASM)
  - **a-C used together with inorganic ARC film (eg. SiON) as hard mask.**
  - **Other solutions depend on integration need (material etched).**
    - Example: metal hard mask (Ti/TiN) for ultra low-dielectric constant etch).



65nm

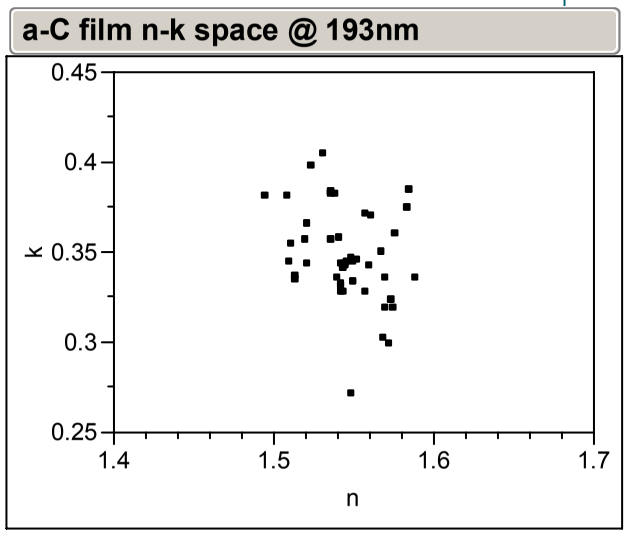
65nm w a-C/SiON

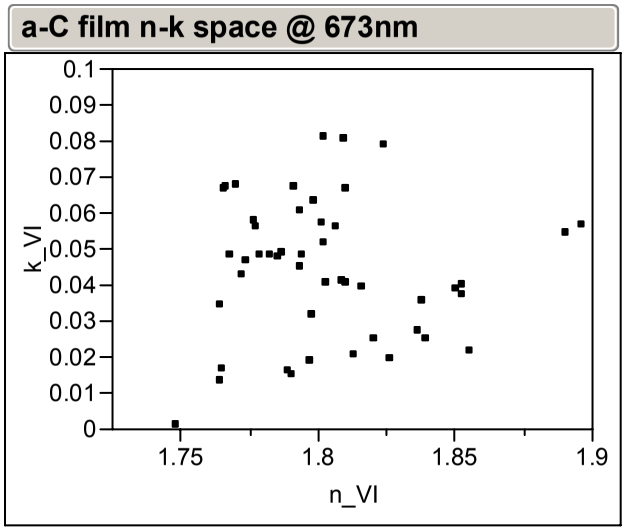


1. Etch dielectric ARC
2. Etch a-C (and remove PR)
3. Etch ILD and remove ARC. Here partial ILD etch is shown.
4. Remove remaining a-C

Requirements of films

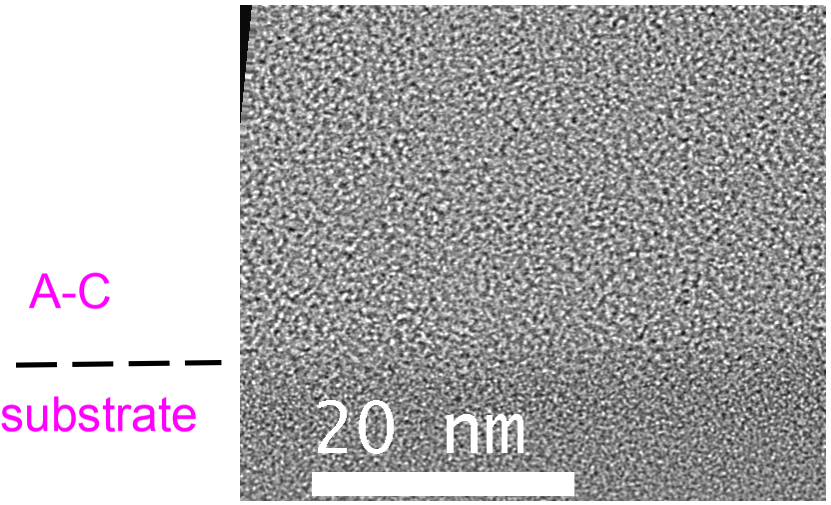
- **Lithography**:
  - **Low reflectance for combined film stack (ARC, a-C, films to be etched) (R < ~1%) at lithography wavelength.**
    - ARC & a-C thickness, refractive index, extinction coefficient need to be tuned for low reflectance based on available resist and to-be-etched film stack.
  - **A-C film transparent for stepper alignment.**
- **Etch**:
  - **ARC & a-C thickness tuned based on film stack and etch selectivities.**

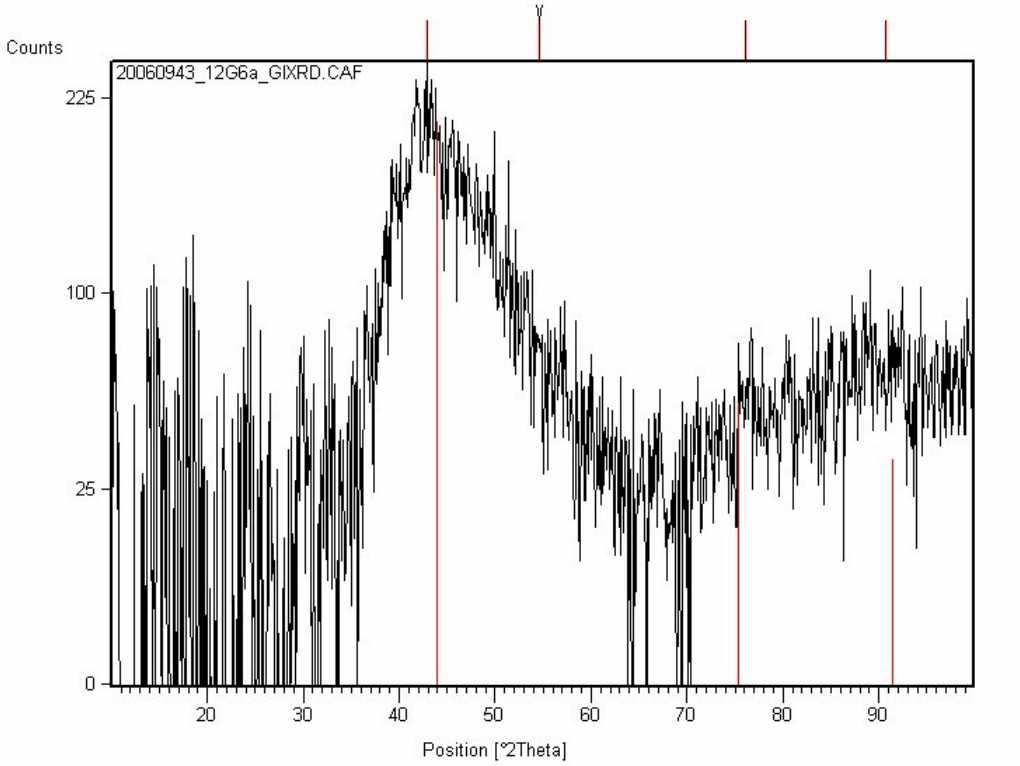




Is a-C really amorphous?

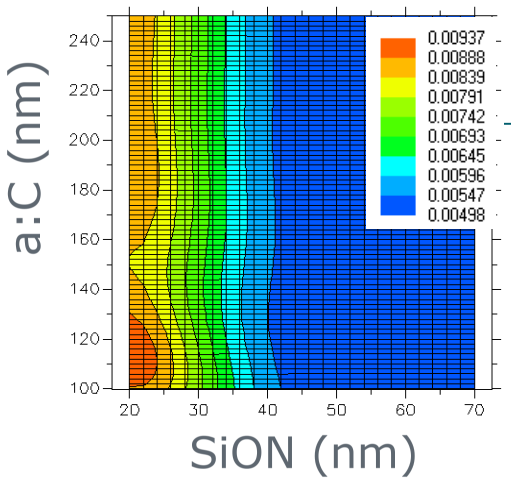
- **TEM, XRD → Carbon film is indeed amorphous**
  - **no peaks associated with diamond structure observed.**
  - **should not impact LER.**





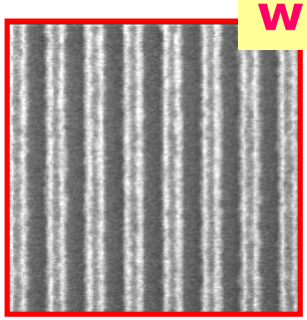
Example 1

F. Tsai

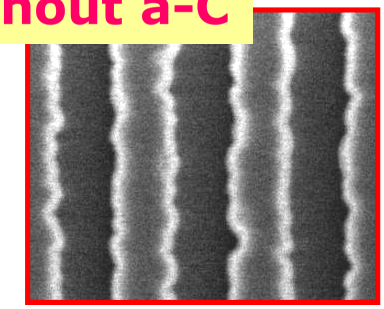


Reflectance < 1% with wide range of a-C thickness

without a-C

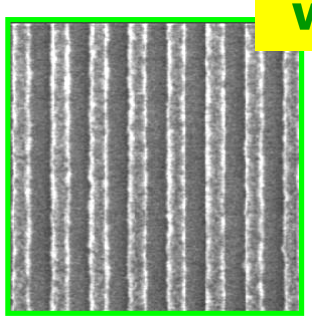


Fuzzy resist profile

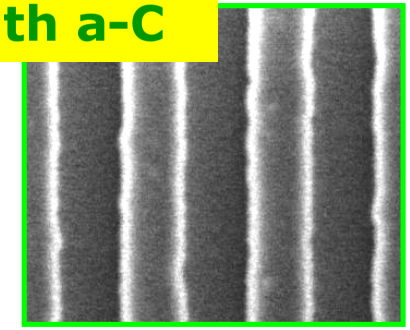


High LER after etch

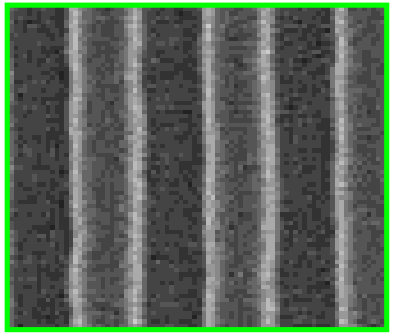
with a-C



Sharper resist profile



Lower LER after etch



Further LER improvement

- **A-C enhances pattern definition**

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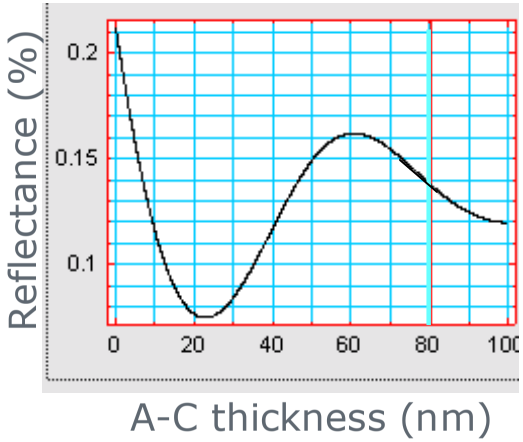
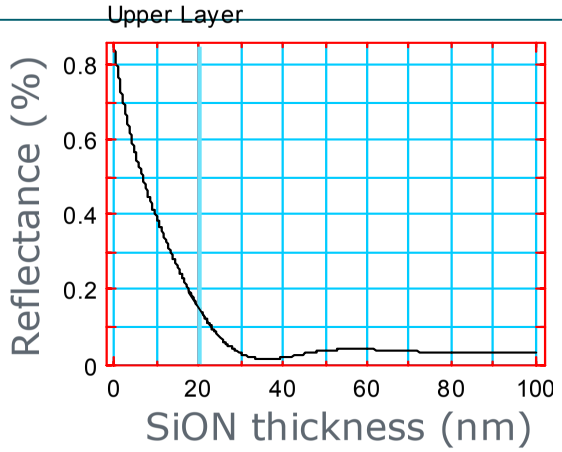
Example 2



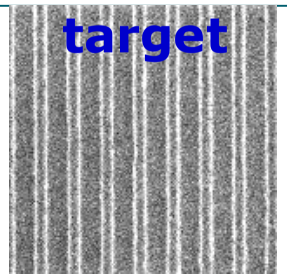


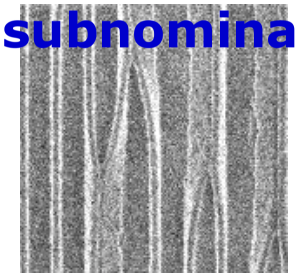
- **Reflectance < 1% for wide range of a-C & SiON thicknesses.**
- **Optical properties of a-C & SiON films:**

A-C:		
T(A)	**N**	**K**
200 – 1000	**~1.5**	**~0.4**

SiON:		
T(A)	**N**	**K**
200 – 1000	**~2**	**~1**

SEM by M. Takahashi



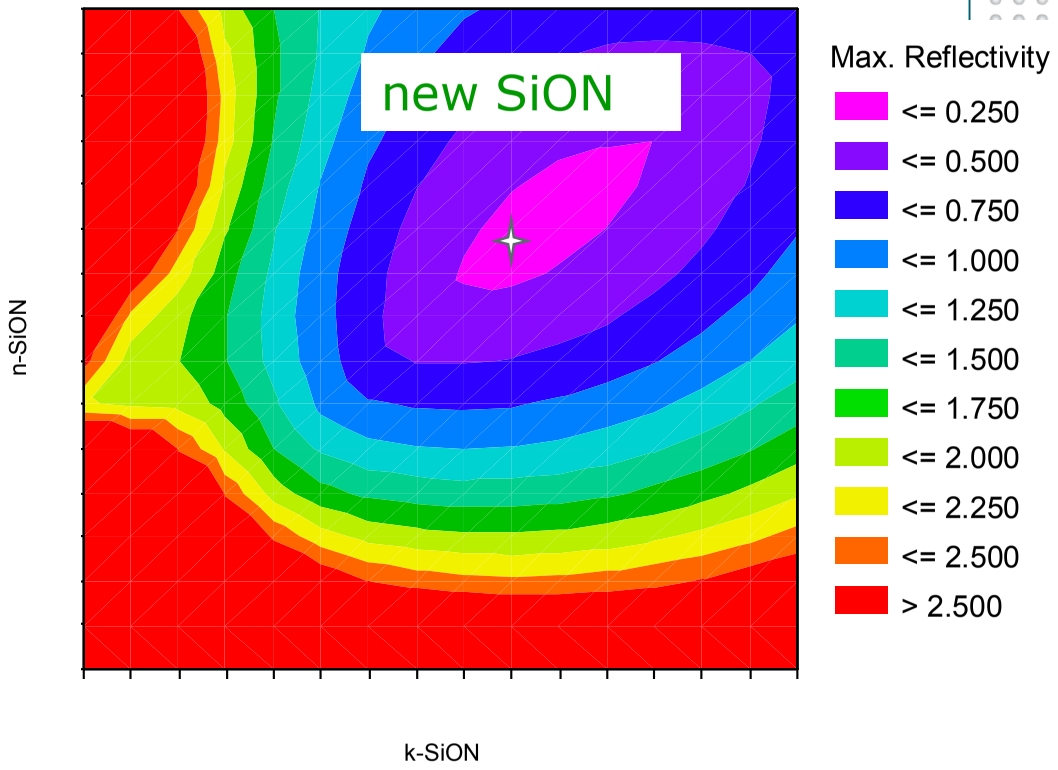


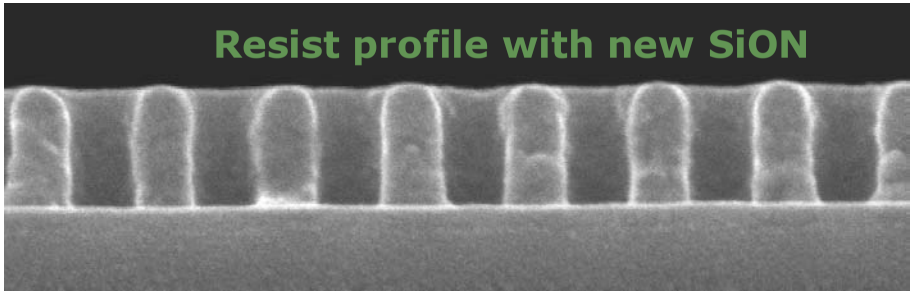
- **Nominal-feature DICD meets target; resist collapse at subnominal feature**
- **Advantage of a-C → can thin down PR**

Example 3

SiON:		
Thickness	N	K
~ 200 - 1000A	~2	~1

- New SiON with appropriate n/k targeted for baseline o-BARC.



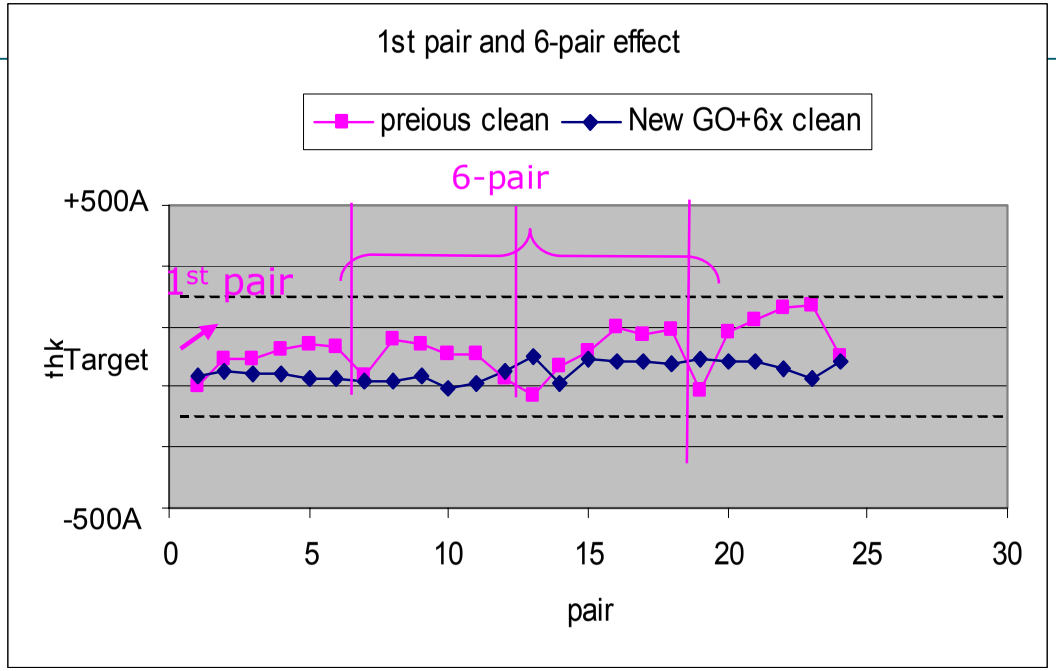


J. Reiss

Challenges of using a-C – Films module

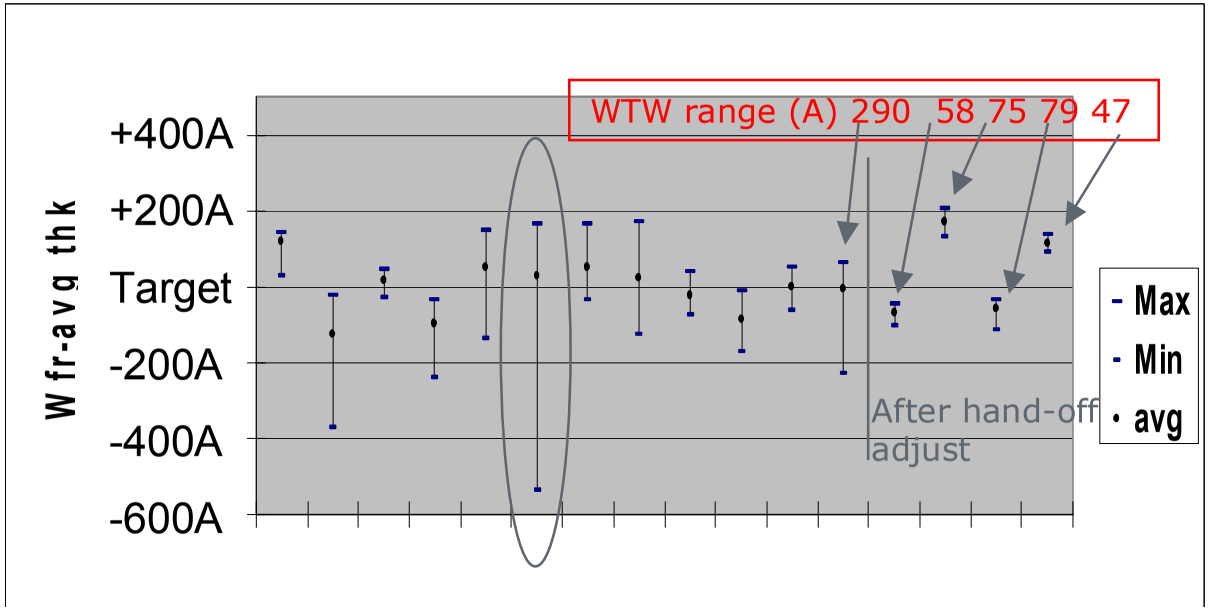
- Chamber conditioning
- Wafer placement
- Film aging
- Metrology of thin a-C

Chamber temperature instability → WTW variation

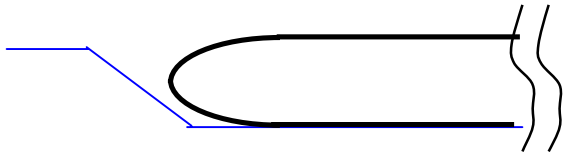


- Challenges:
  - Temperature instability → WTW variation (1st pair & 6-pair effects)
  → Can lead to FICD and line or contact resistance variation.
- Improvements:
  - New chamber seasoning
  - Eliminating chamber idle-time difference between wafers.

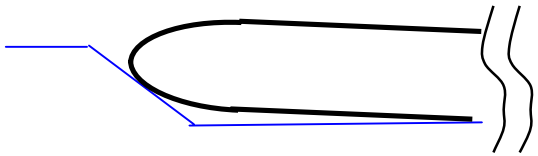
Wafer placement impact on WTWNU



Multiple-wafer runs



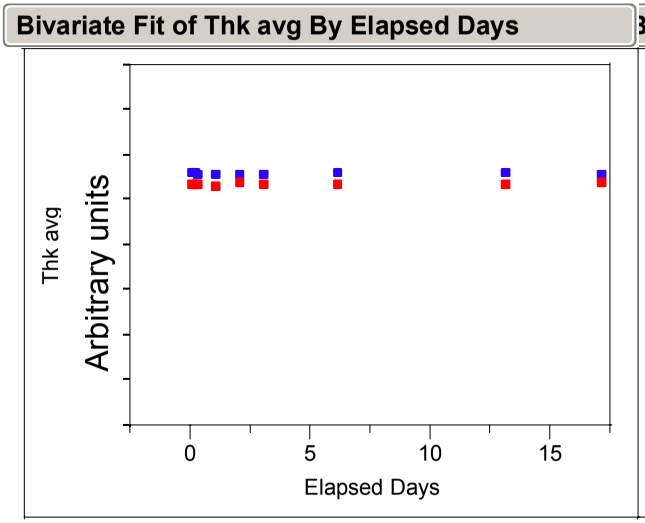
Good wafer placement

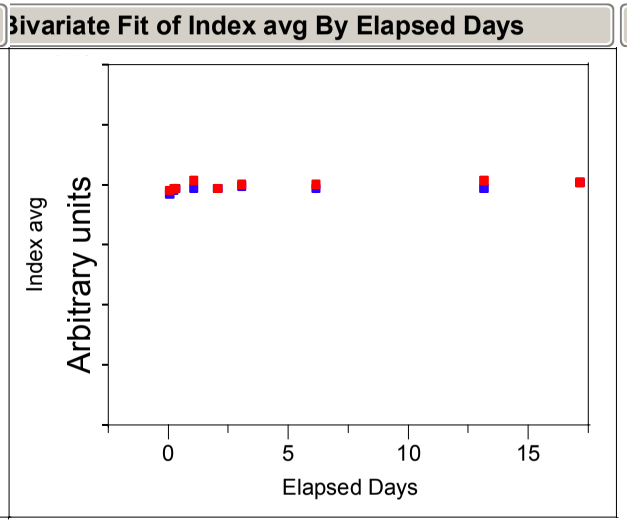


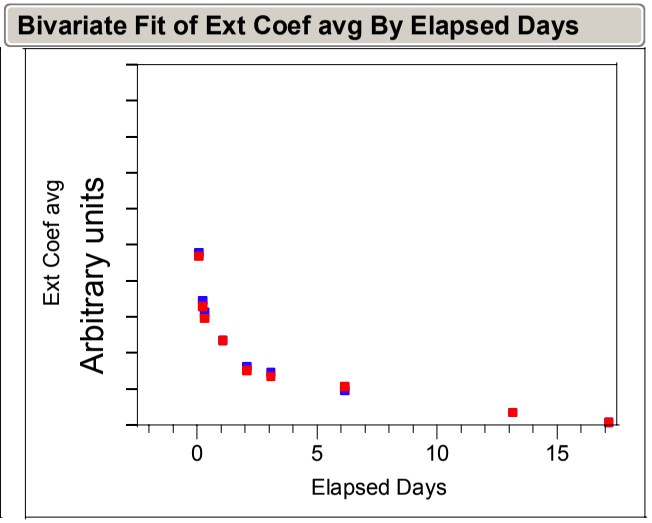
Poor wafer placement

- Wafer placement can impact dep rate → thickness variation → Can lead to FICD and line or contact resistance variation.

Film aging - time-dependence of k

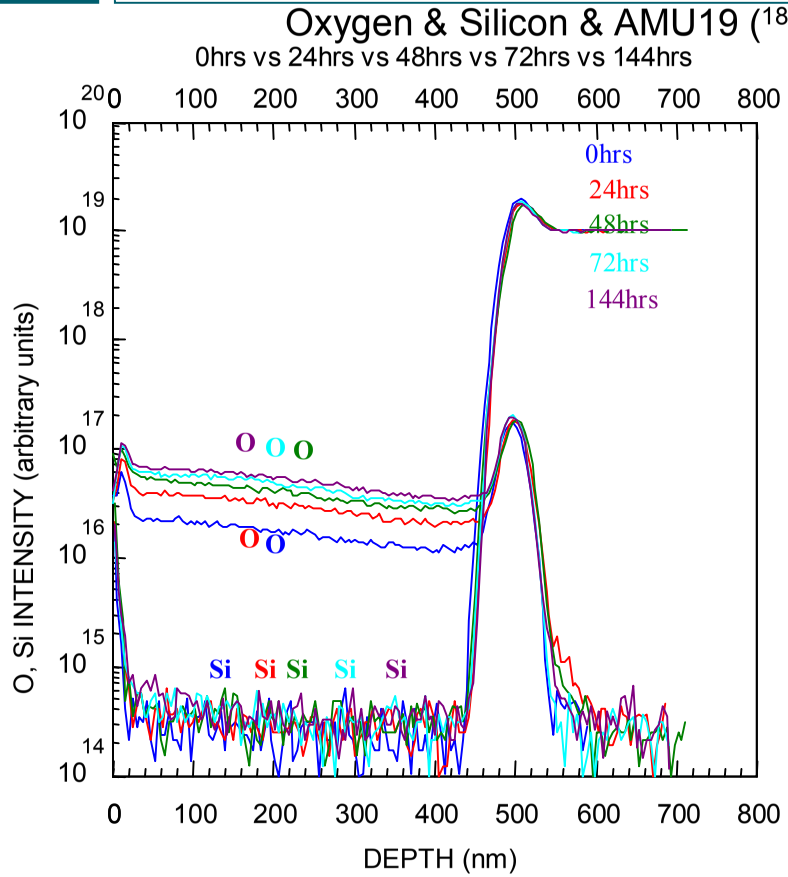


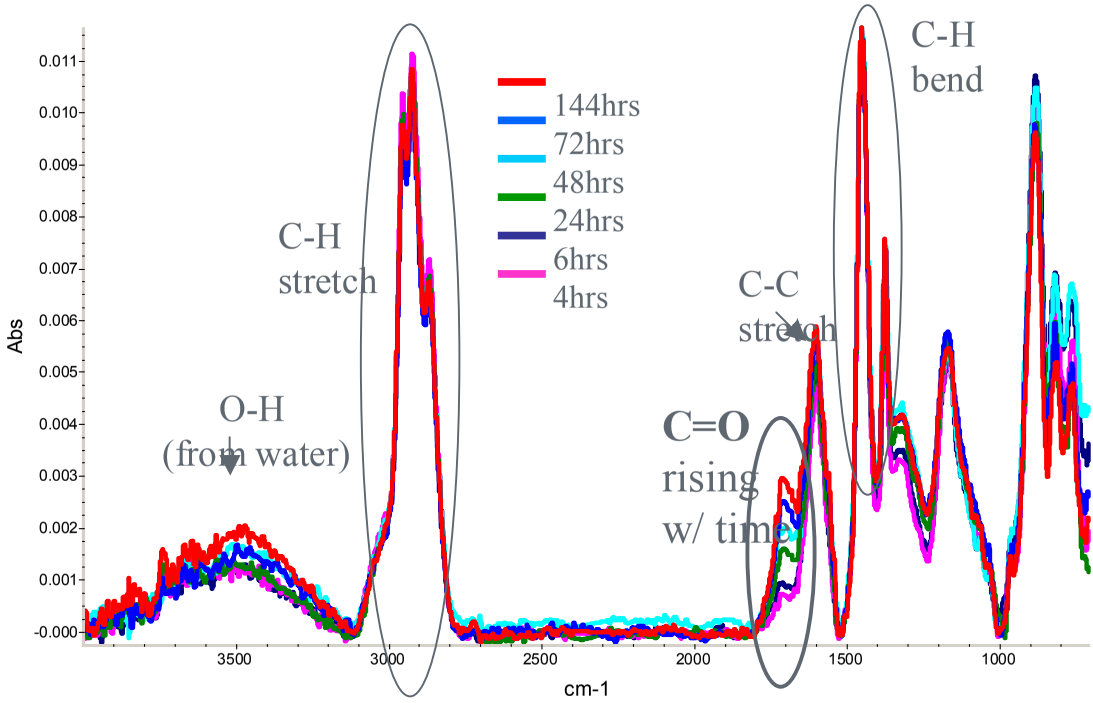




- Extinction coefficient decreases as function of time while index, thickness remain constant.

Film aging - SIMS & FTIR data





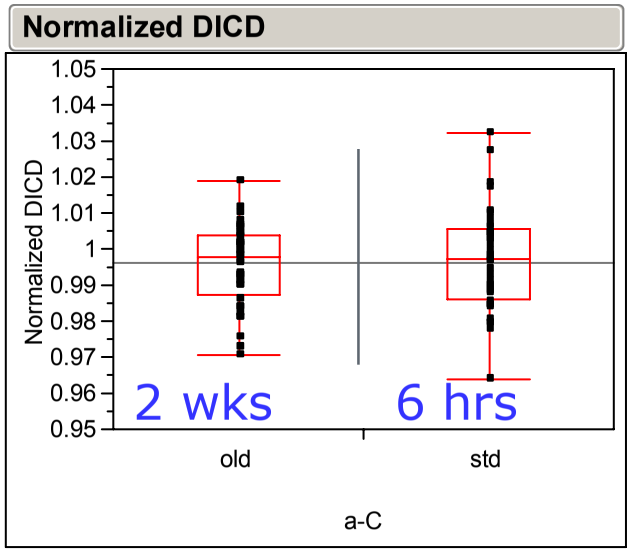
- SIMS: Oxygen increases over time; 3X the original level at 144 hrs.
- FTIR: C=O, O-H (water) contents increase with time

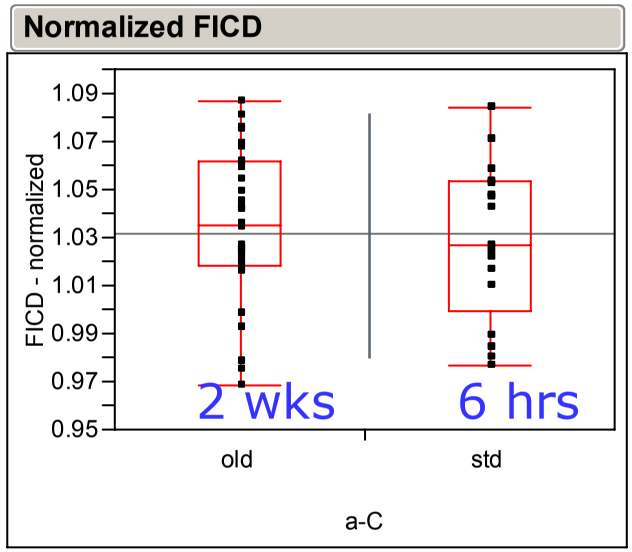
Film aging – Litho / Etch impact

after litho

after etch

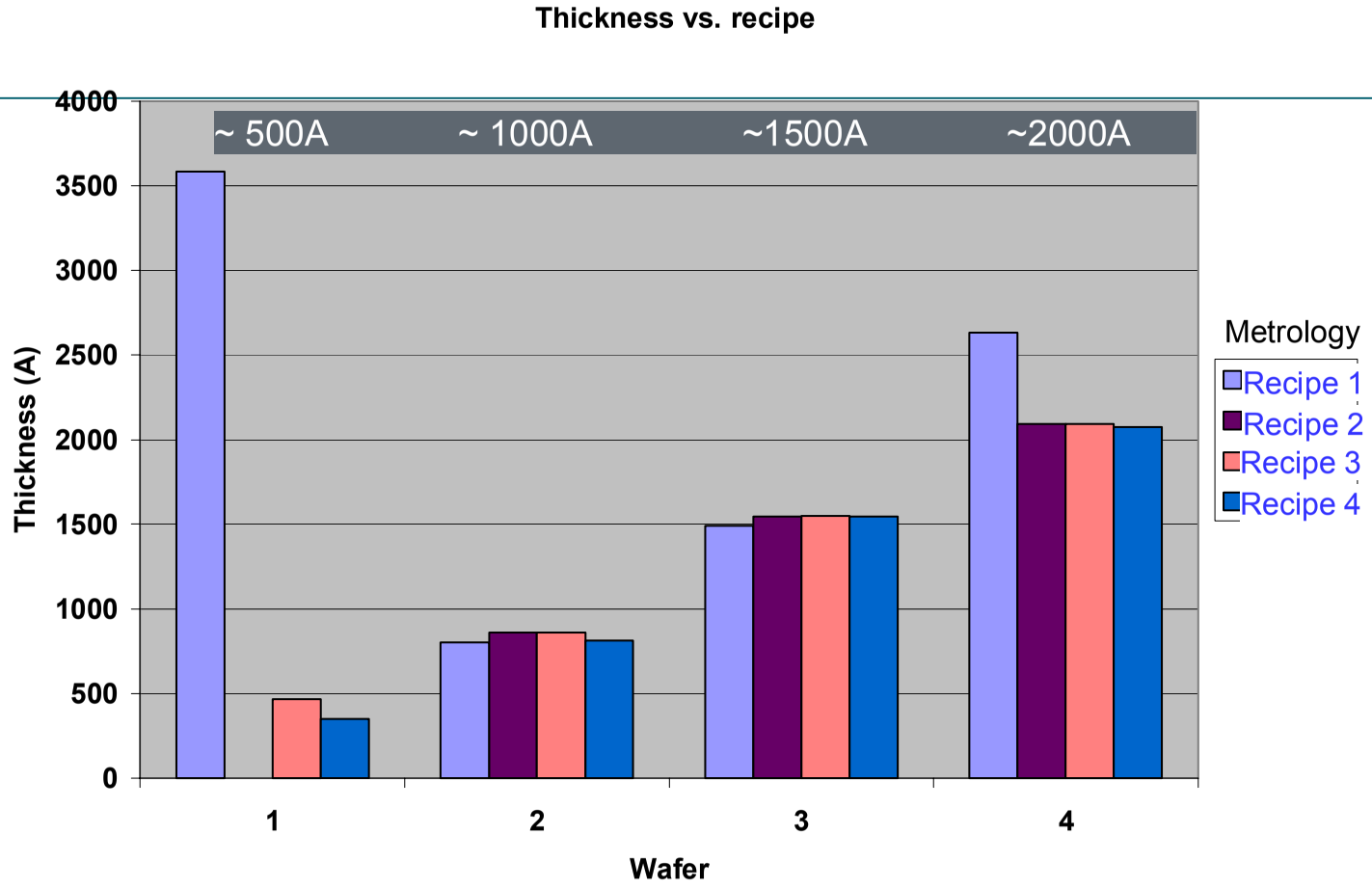
Time before SiON cap →





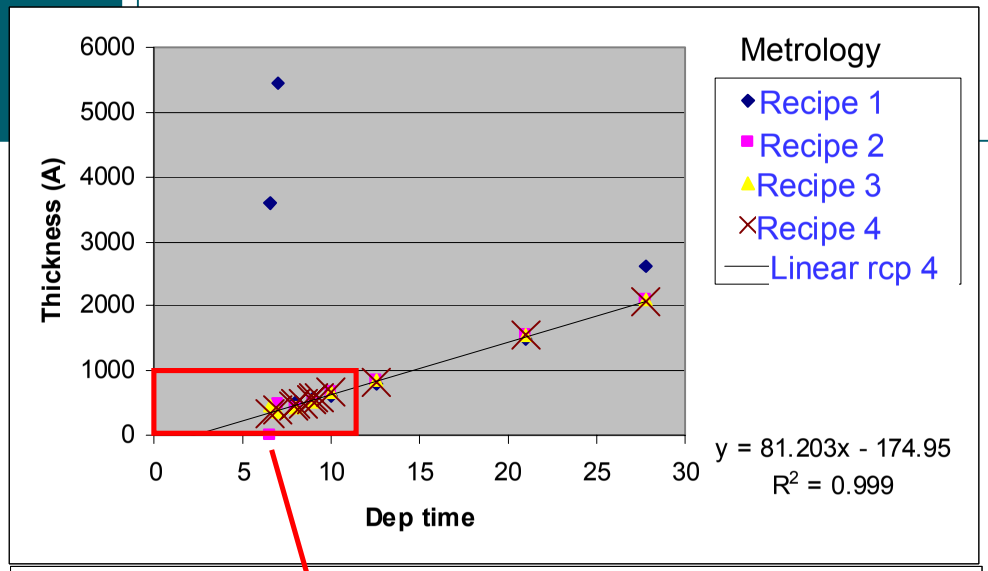
- No impact on litho, etch seen due to film aging (up to 2-week queue time).

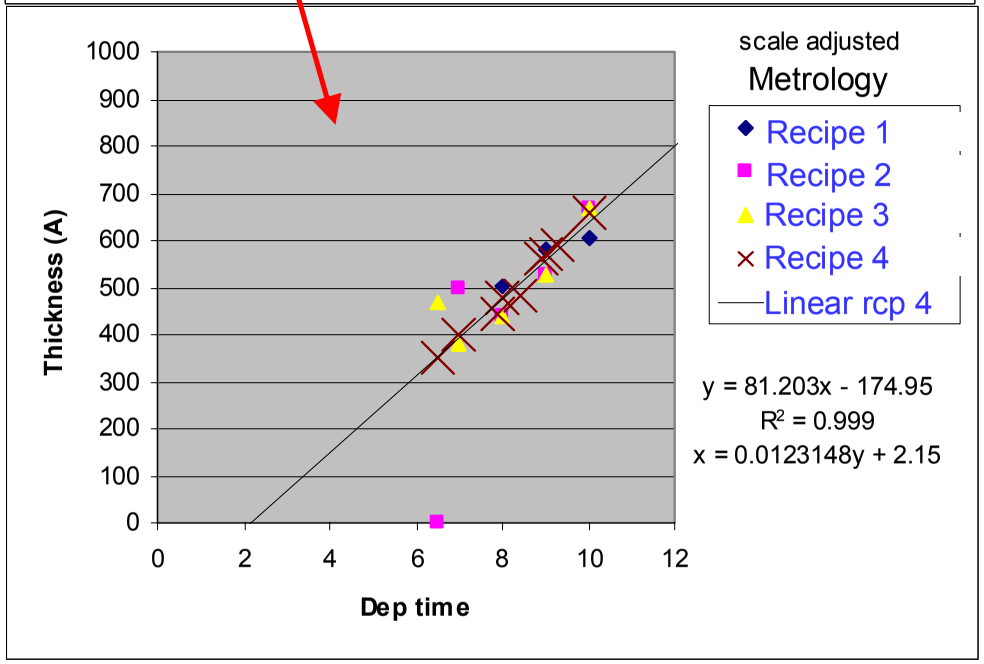
Thin a-C metrology (1)



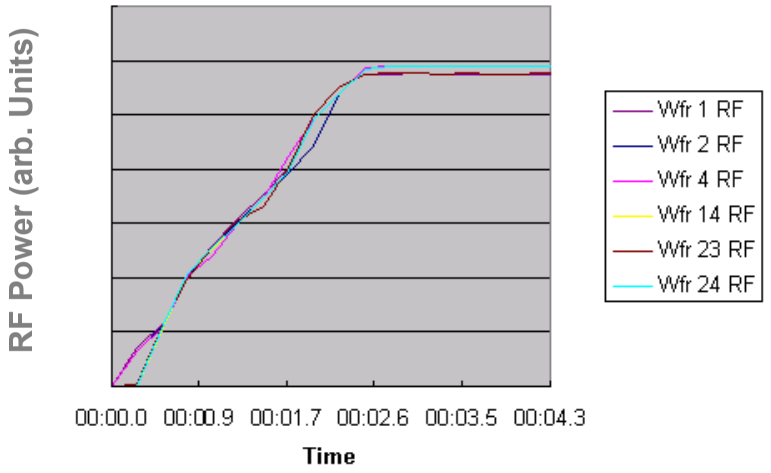
- Film thickness measured inline with optical thickness metrology tool.
- Standard metrology recipe 1 is unstable at low thickness, giving wrong result.
- Correct targeting requires more reliable recipe.

Thin a-C metrology (2)





- Recipe 4 tested, has good linearity.



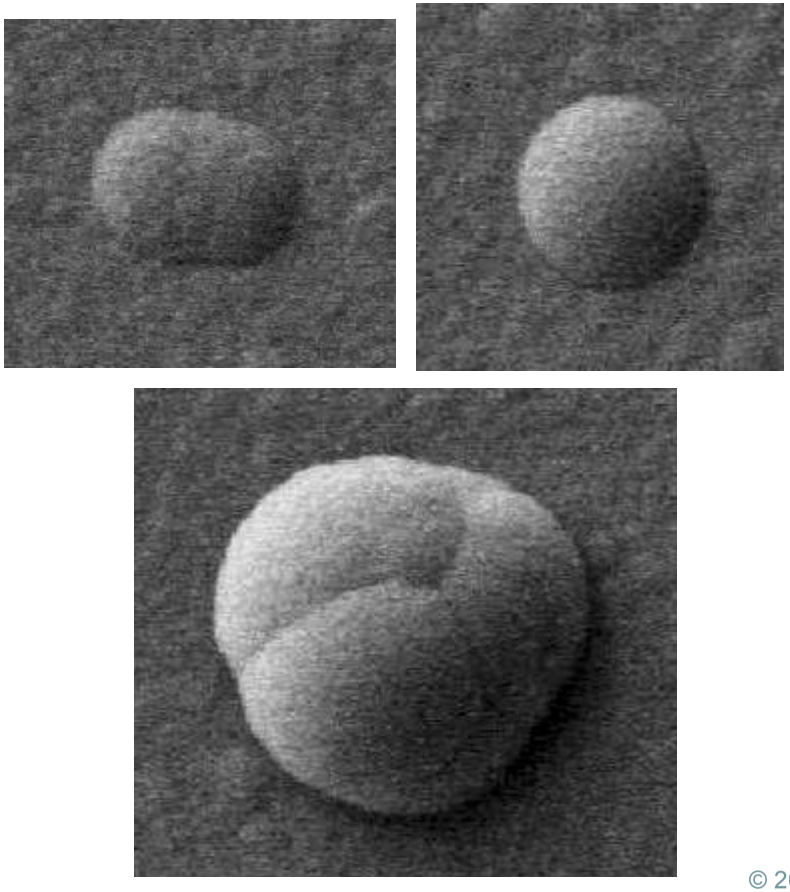
- Power ramping during first ~2 seconds to avoid arcing.

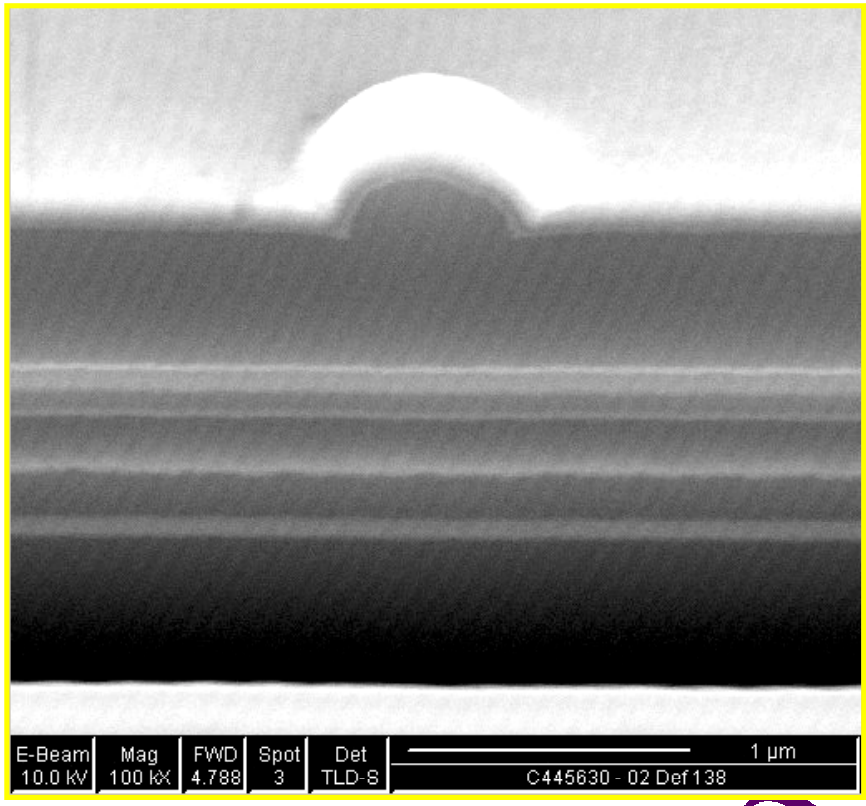
Challenges of using a-C – Integration concerns

- Bump defects
- Adhesion of SiON cap on a-C
- Rework concerns
- Rework sensitivity of SiON cap film

Bump defects - SEM

- Most bumps are 0.4-0.6um.
- XSEM → decoration defects

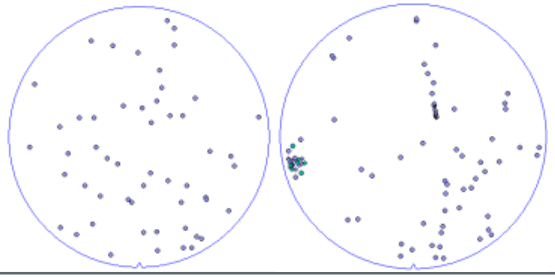
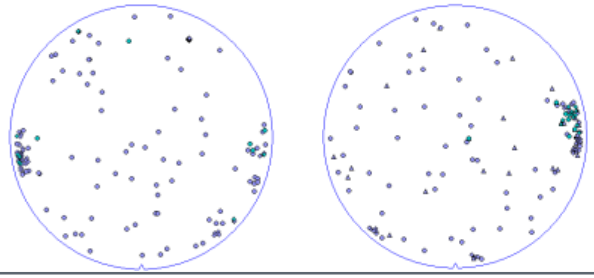
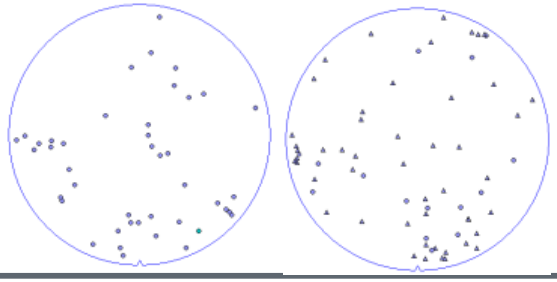
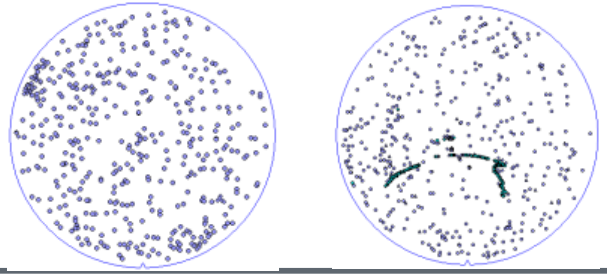


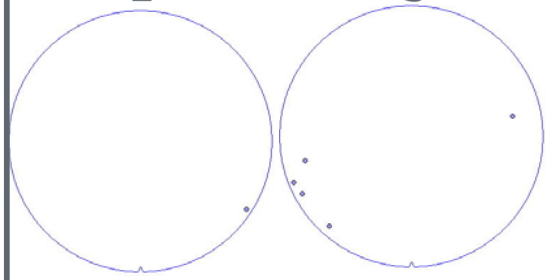
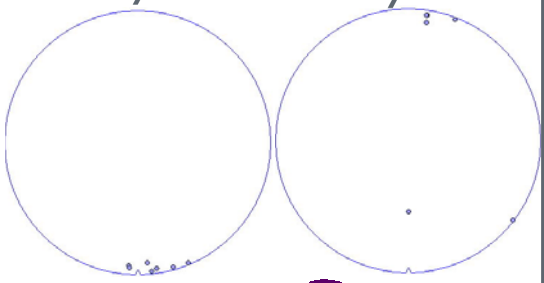


Bump defects – Impact of cleaning tool / recipe

- Backside clean comparable to no clean.
- Whole wafer clean (spray – SPM/APM) worse.
- Whole wafer clean (sink – SPM/APM) worst.

- Different tool set eliminates bumps

no clean	Spray clean
53 101 	211 118 
Backside clean	**Sink**
43 66 	453 438(no cluster) 

No clean	Backside clean
1 5 	7 7 

Challenges with integration of a-C HM – Adhesion (1)

- **Adhesion of a-C to substrates is strong.**
  - a-C film adheres well to various substrates.

Sample	Expected Fracture toughness Kapp M Pa $m^{1/2}$	Rank
AC 1 on Si	0.3 < Kic < 0.5	VERY GOOD
AC 2 on Si	0.3 < Kic < 0.5	VERY GOOD
AC 3 on Si	>=0.6	EXCELLENT
AC 1 on PECVD oxide	0.3 < Kic < 0.5	VERY GOOD
AC 1 on Poly	0.3 < Kic < 0.5	VERY GOOD
AC 1 on furnace nitride	0.3 < Kic < 0.5	VERY GOOD
AC 1 on furnace oxide	0.3 < Kic < 0.5	VERY GOOD
AC 1 on thermal oxide	0.3 < Kic < 0.5	VERY GOOD
AC 2 on furnace nitride	>0.35	VERY GOOD
AC 2 on PECVD nitride	>0.35	VERY GOOD

Adhesion data from mELT technique

Challenges with integration of a-C HM – Adhesion (2)

- **Adhesion of a-C to SiON cap depends on …**
  - **SiON film**

Sample	Expected Fracture toughness Kapp M Pa $m^{1/2}$	Rank
AC 1 + SION 3	0.09 < Kapp<0.15	POOR
AC 1 + SiON 6	0.09 < Kapp<0.15	POOR
AC 1 + SiON 2	0.2 < Kapp<0.3	GOOD

  - **A-C film**

Sample	Expected Fracture toughness Kapp M Pa $m^{1/2}$	Rank
AC 1 + SiON 2	0.2 < Kapp<0.3	GOOD
AC 3 + SION 2	~0.1	POOR
AC 4 + SION 2	>0.35	VERY GOOD

  - **queue time**

Sample	Expected Fracture toughness Kapp M Pa $m^{1/2}$	Rank
AC 1 + SiON 2	0.2 < Kapp<0.3	GOOD
AC 1 + SiON 2 (fresh)	> 0.3	VERY GOOD

- **Potential defectivity issue, critical for immersion lithography.**

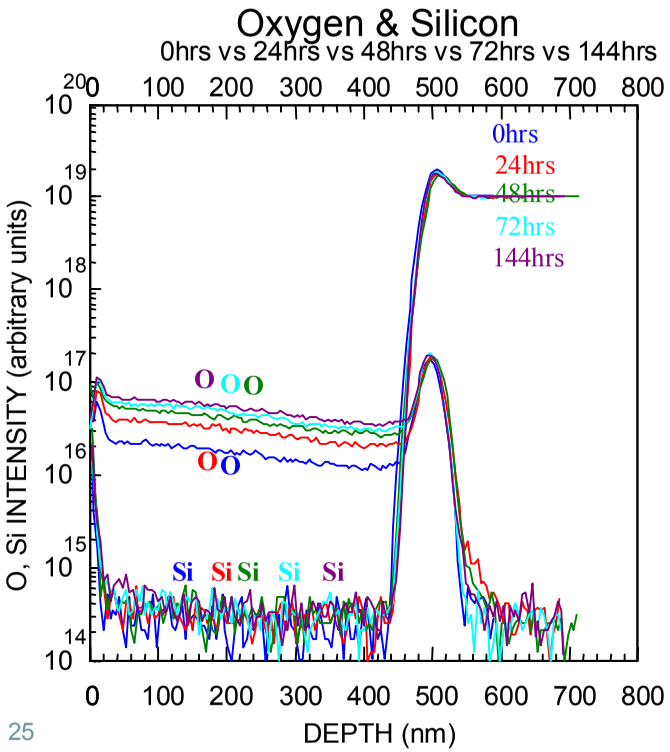
Challenges with integration of a-C HM – Adhesion (3)

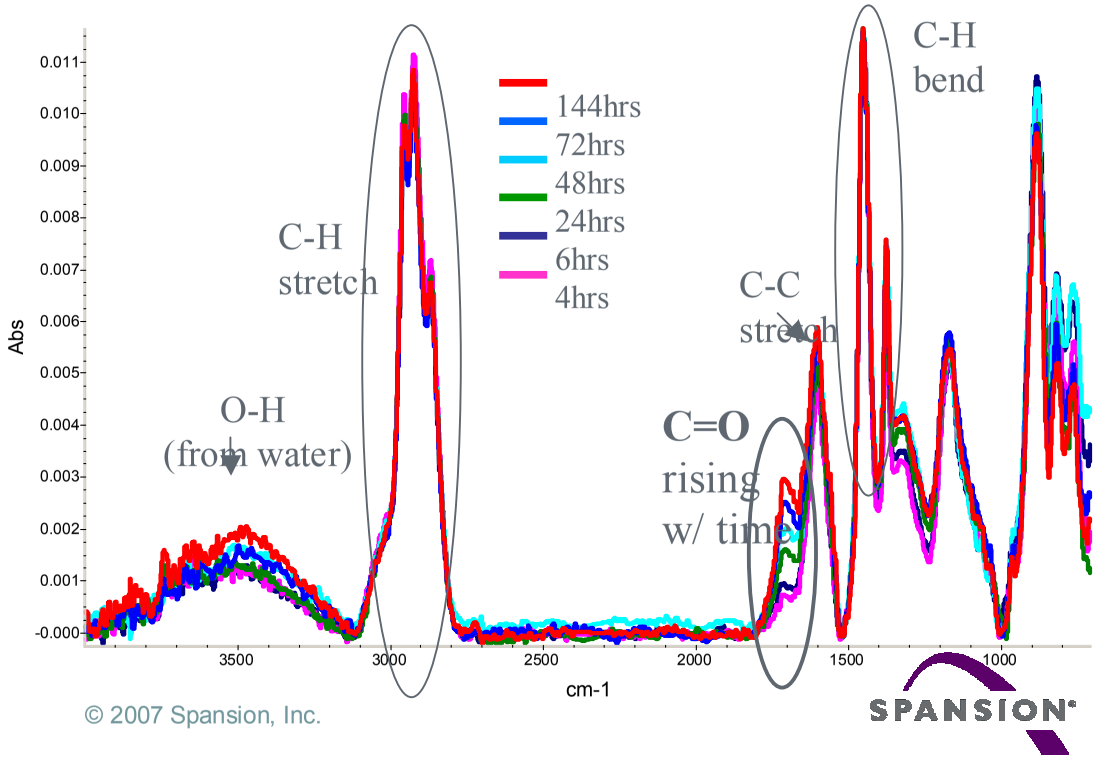
- **Adhesion of a-C to SiON cap depends on …**
  - **SiON deposition condition**

Sample	Expected Fracture Toughness Kapp (MPa $m^{1/2}$)	Rank
AC 1 + SiON 2	0.2 < Kapp<0.3	GOOD
AC 1 + SION 2.1	0.09 <Kapp<0.15	POOR
AC 1 + SION 2.2	0.09 <Kapp<0.15	POOR
AC 1 + SION 2.2	0.09 <Kapp<0.15	POOR
AC 1 + SiON 6	0.09 < Kapp<0.15	POOR
AC 1 + SION 6.1	0.09 <Kapp<0.15	POOR
AC 1 + SION 6.2	0.09 <Kapp<0.15	POOR
AC 1 + SION 6.3	0.09 <Kapp<0.15	POOR
AC 1 + SION 3	0.09 < Kapp<0.15	POOR
AC 1 + SION 3.1	0.09 <Kapp<0.15	POOR
AC 1 + SION 3.2	0.09 <Kapp<0.15	POOR
AC 1 + SION 3.3	0.09 <Kapp<0.15	POOR
AC 3 + SION 2	~0.1	POOR
AC 3 + SION 2.1	<0.09	VERY POOR
AC 3 + SION 2.2	0.1<Kic<0.35	GOOD
AC 3 + SION 2.3	>0.35	VERY GOOD

Challenges with integration of a-C HM (Adhesion 4)

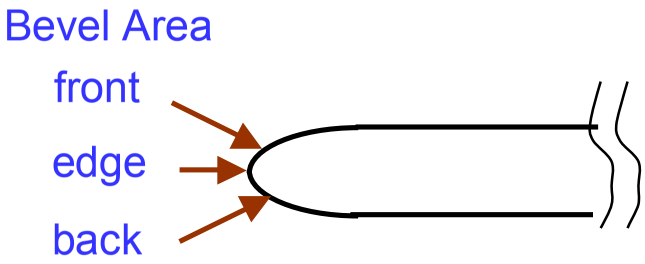
- **Adhesion of SiON to a-C due to queue time between a-C & SiON dep.**
  - **surface & film oxidized**
  - **→ Si-C bonding sites reduced → poorer adhesion**
  - **→ immersion litho concern.**

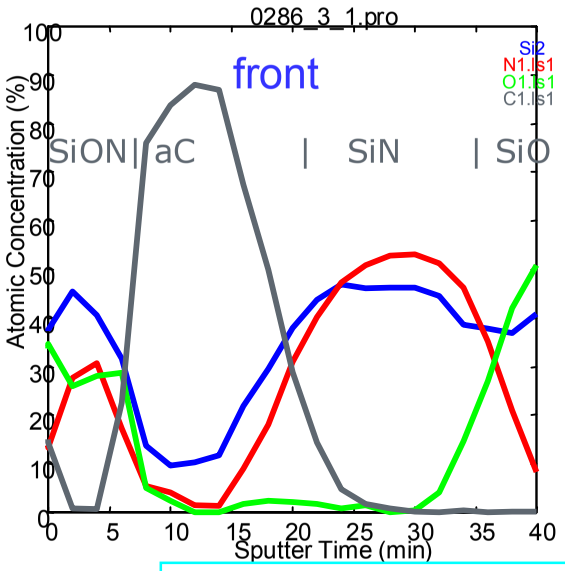


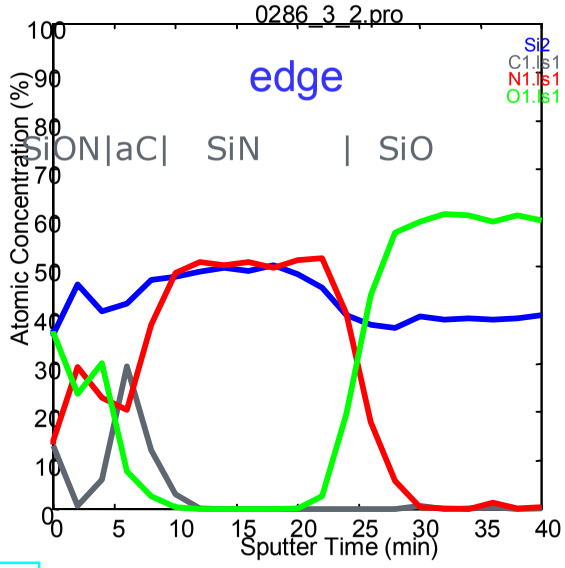


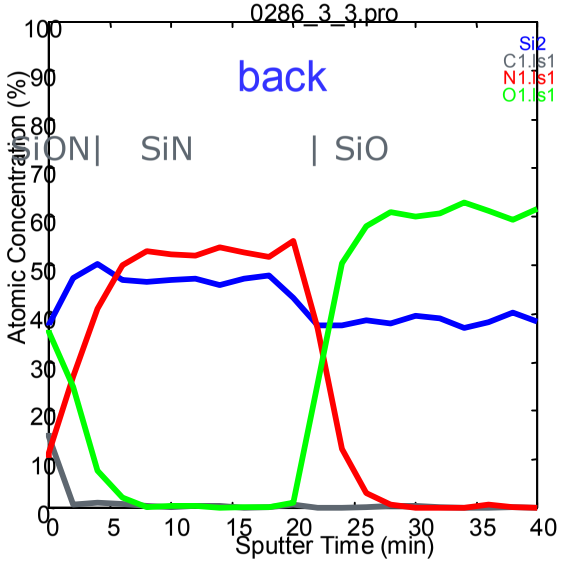
Challenges with integration of a-C HM - rework

- **A-C encapsulated by SiON on bevel.**
  - Concern: a-C will be removed/undercut during litho rework → defectivity from flaking of remaining SION.
  - **XSEM & AES verified good encapsulation of a-C by SiON.**







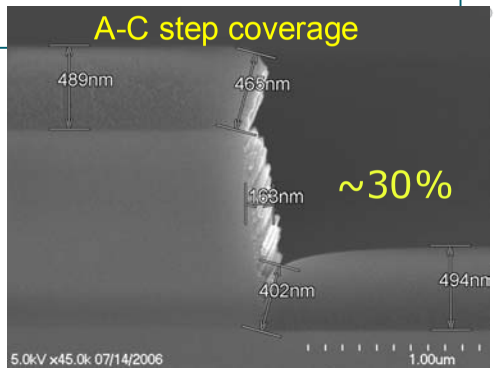


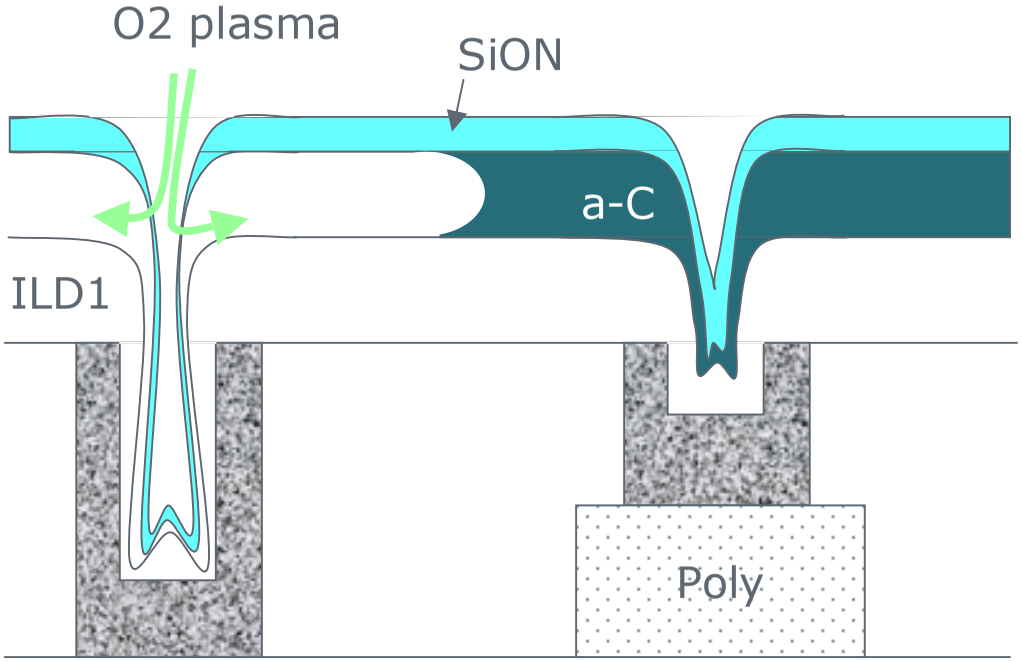
Nominal etch rate is 25A/minute.

150A SiON/300A a-C | 50A SiON/< 50A a-C | trace SiON / no a-C

Challenges with integration of a-C HM (rework 2)

- **Rework damage due to SiON pin holes or SiON/a-C step coverage**
  - If exist, SiON pin holes → a-C undercut during rework as a-C, like photoresist, is removed by rework process (O2 ash).
  - **Rework tests on blanket SiON on a-C has detected no such defects**
  - **If there is topography, intrinsically low step coverage of a-C and SiON film would lead to locally thin/cracked SiON and expose a-C to attack during rework process.**





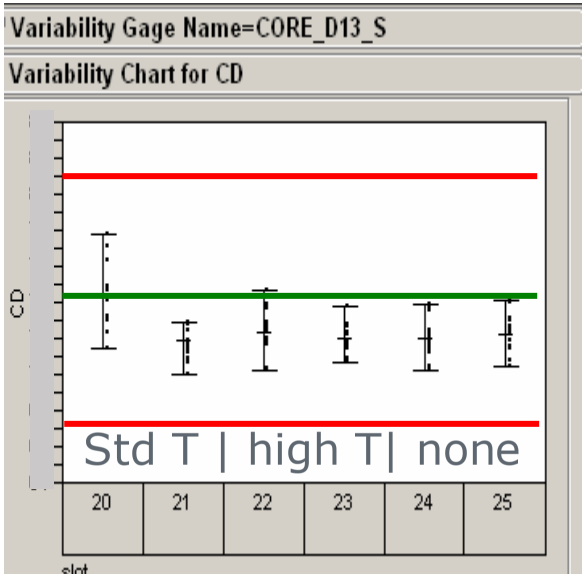
Challenges with integration of a-C HM (2)

Sensitivity of resist to SiON surface due to rework?

Layer	Rework	post- pre N	post-pre K
B	std	-0.001	0.000
B	long	-0.005	-0.004
C	std	0.000	0.000
C	long	0.000	0.000
D	std temp	-0.002	0.003
D	high temp	-0.001	0.003

XPS Surface Relative Atomic % Composition

Rework condition	C	N	O	Si
None (control)	16.3	16.1	35	32.6
Std	9.9	16.4	38.6	35.1
High Temp	13.5	14.9	37.5	34



Note: W20 processed on different day than the rest.

- **No significant change in n/k observed inline.**
- **Slight oxidation of SiON surface with rework.**
- **Rework tests showed same DICD before and after rework.**

Summary

- **Amorphous carbon hardmask improves pattern definition required for advanced patterning (eg. at 65nm, 45nm, 32nm, etc.).**
- **Some challenges with a-C:**
  - **Module: hardware set up, process control, metrology, film aging**
  - **Integration:**
    - Defects (decoration defects)
    - Potential issues: adhesion (→ defects), rework, film encapsulation.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