Feature scale modeling of a gate etch process used to study SRAM bit cell pattern transfer into a gate stack

Phillip Stout
Applied Materials
Santa Clara, CA

Thin Film User Group (TFUG)
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OVERVIEW

- etch correction strategies
- gate etch model
  - overview
  - coupling to lithography model
- steps in gate etch process
- gate etch modeling of sram bit cell

**ETCH CORRECTION: RULE BASED**

- Experimentally determined “etch function”

- Determine “etch function” : cd etch loss (d) for a given ADI spacing (s)

\[
ADI - ACI = f(S)
\]

\[
2d = f(S)
\]

- Determine undersizing (\(\Delta\)) required for a given spacing, target ACI, target ADI, and “etch function”

\[
2\Delta + f(s + 2\Delta) = T_{ADI} - T_{ACI}
\]

\[
2(\Delta + \delta) = T_{ADI} - T_{ACI}
\]

\[
2\Delta + 2\delta = T_{ADI} - T_{ACI}
\]

\(\delta\) – predicted etch loss

\(\Delta\) – undersize correction
EXTERNAL USE

ETCH CORRECTION: CELL SPECIFIC

- computation (full physics) & experiment determines “etch function”

- light intensity simulation and test structure calibration

- full physics etch simulation calibration

- hand adjust

- opc

- target

- corrected

- aerial image
ETCH CORRECTION: WHOLE MASK

- Computation (quick transform) & experiment determines “etch function”

- Light intensity simulation and test structure calibration

- Compare with target

- Adjust corrections

- “Quick” etch simulation (2D geometry transform) calibration

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Corrected aerial image

External Use
Multi-scale reactor/sheath/lithography/feature/atomistic models calibrated with experimental data (EM fields, SEMs, TEMs, growth/etch rates, ...)

Feature

Lithography

TEMs

Atomistic

Sheath

External Use

Reactor
A statistical method

- Feature surface represented by unoccupied/occupied interface in a "material" mesh

- Particle number incident on surface proportional to incident flux rate

- Lagrangian particle tracking includes shadowing by surface

- 2D/3D, packing (sc,fcc,bcc), multi-material, multi-specie

- Includes specie transport, adsorption, surface diffusion, reflection (diffusive, specular), energy loss, etch, sputter, and deposition

- Surface properties (tac, sticking coefficient, sputter yield, etch rates, and reflection) are functions of angle, energy, specie, and material
PAPAYA COUPLED TO LITHOGRAPHY MODELS

- Papaya uses initial photo resist mask calculated by lithography models
  - Extruded aerial image or developed 3D photo resist (PR) profile used
  - Allows study of mask pattern transfer and gate profile during gate etch

Mask data

Resist profile

Extruded aerial image

Aerial image

Photoresist development

ST-LITH 3D Resist Profile, 10% of resist thickness
GATE ETCH STEPS MODELED: SRAM BIT CELL

- steps modeled in gate etch model
- He/O2/HBr/Cl2/CF4/Ar/N2/CHF3 chemistries
- PR/hard mask/ARC/Si stack
GATE ETCH PARTITION FOR P & N-TYPE POLYSILICON

- Profiles sensitive to previous profiles
- Faceting at hard mask etch indicates PR budget exceeded
- Sloping ARC profile translates into poly silicon profile
- Poly silicon trapezoidal after main etch
- P- (hourglass, undercut) and n-type (coke bottle, trapezoidal) characteristic profiles become apparent at soft landing (much more neutral driven etch) and over etch.
developed photo resist (ADI) shows bridging at line ends
SRAM BIT CELL: TRIM

- Angled line ends at ADI lead to large line end pull back at etch.
Exceeding the PR budget at hard mask etch exacerbates line end pull back.
SRAM BIT CELL : TRIM ETCH TIME

- increased trim time increases side wall slope and pull back
- wider line ends with their larger cds also have a larger height
SRAM BIT CELL : LINE END PULL BACK

- Line end pull back is of concern at gate etch for SRAM bit cell.
- Too much pull back can violate layout rules, or decrease layout density.
HIGHER PR ION ETCH YIELD

- slice of bit cell showing effect of increased etch rate
- hard mask etch overlayed with final clean
- bit cell with higher PR ion yield increases line end pull back as PR slopes at line ends and becomes a less effective etch mask
Allowing passivant to contribute to sidewall polymer growth straightens profile at over-etch.

As the polymerization rate is decreased during the process, hour-glassing can become more prevalent.
SUMMARY

- A reactor/feature/lithography/atomistic modeling suite is being applied to gate etch.

- Coupling to lithography models allows study of pattern transfer as well as poly silicon profile.

- Studying the cumulative effect of the gate etch processes required to transfer the pattern through the gate stack helps understand the impact one step can have on subsequent steps:
  - Less etch resistant resist leads to more line end pull back.
  - Polymer deposition at main etch “sets up” the profile type seen subsequently at soft landing and over etch.

- Model based etch correction strategies can take advantage of reactor/feature modeling suites.