Feature scale modeling of a gate etch process used to study SRAM bit cell pattern transfer into a gate stack

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think it. apply it.™

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Sunnyvale, California

OVERVIEW

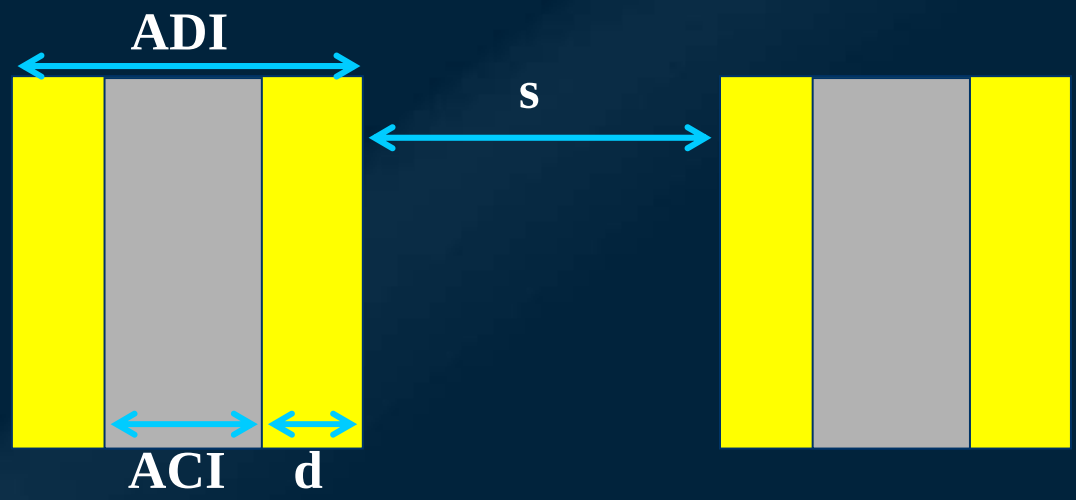
- etch correction strategies
- gate etch model
  - overview
  - coupling to lithography model
- steps in gate etch process
- gate etch modeling of sram bit cell

P. J. Stout, S. Rauf, R. D. Peters, and P. L. G. Ventzek, “A gate etch process model for SRAM bit cell and FinFET construction”, J. Vac. Sci. Technol. B 24(4) pp. 1810-1817 (2006)

ETCH CORRECTION: RULE BASED

- experimentally determined “etch function”
- determine “etch function” : cd etch loss (d) for a given ADI spacing (s)

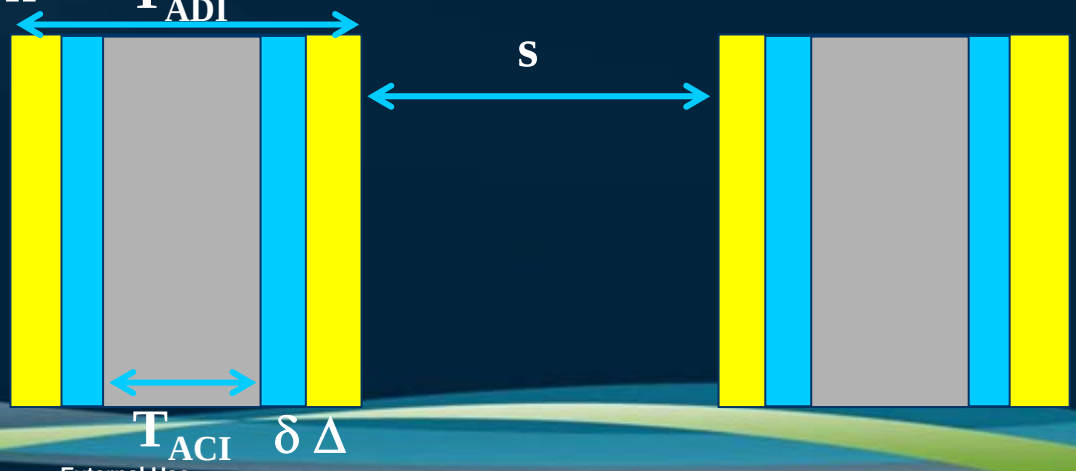
ADI – ACI = f(S)
2d = f(S)



- determine undersizing (Δ) required for a given spacing, target ACI, target ADI, and “etch function”

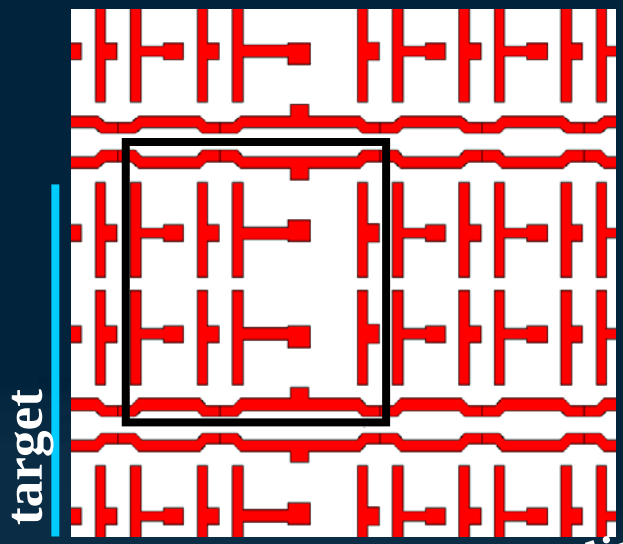
$$2\Delta + f(s + 2\Delta) = T_{ADI} - T_{ACI}$$

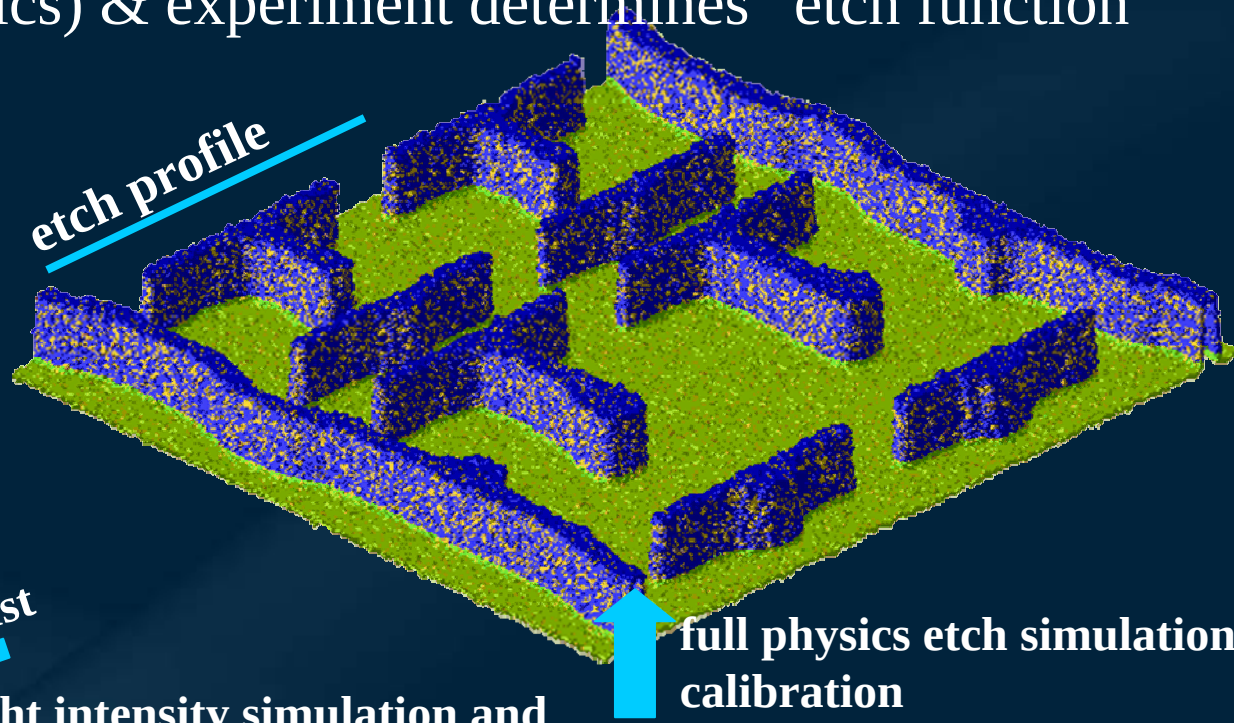
$2(\Delta + \delta) = T_{ADI} - T_{ACI}$
$2\Delta + 2\delta = T_{ADI} - T_{ACI}$
δ – predicted etch loss
Δ – undersize correction



ETCH CORRECTION: CELL SPECIFIC

- computation (full physics) & experiment determines "etch function"

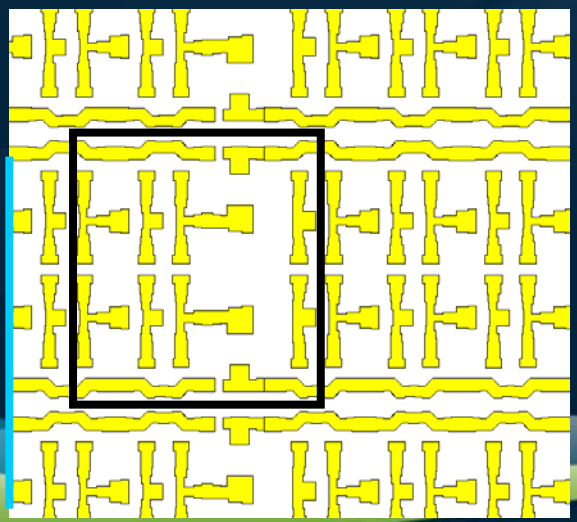


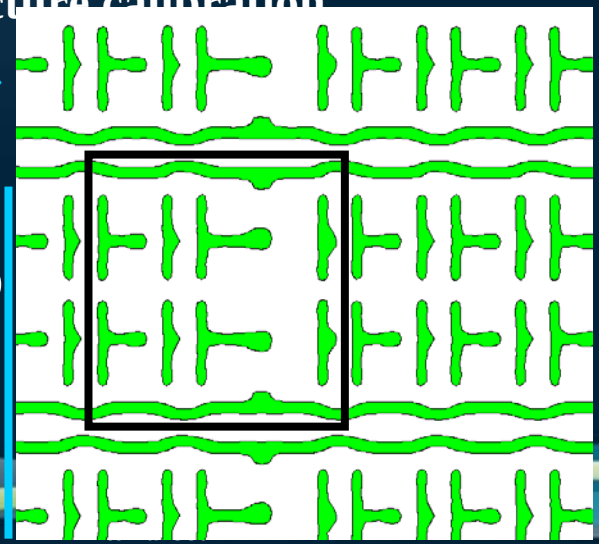


opc

hand adjust

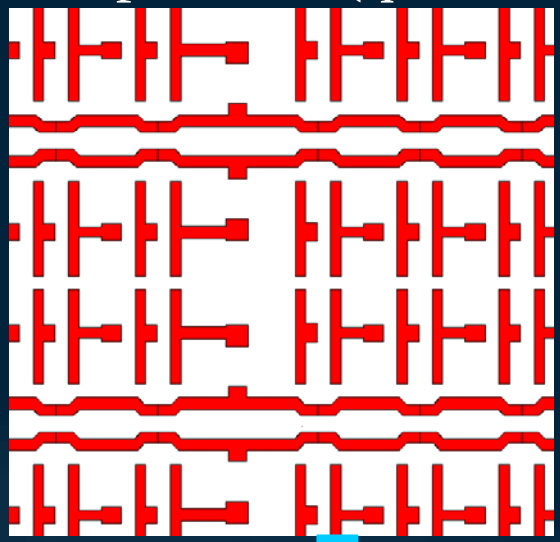
light intensity simulation and
test structure calibration





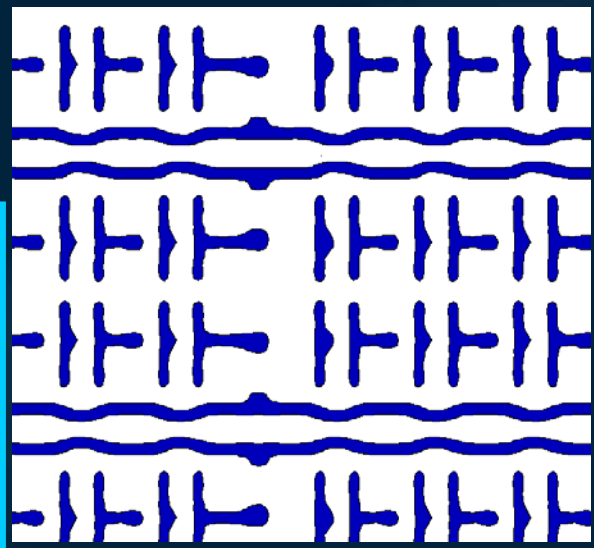
ETCH CORRECTION: WHOLE MASK

- computation (quick transform) & experiment determines "etch function"



target

compare with target



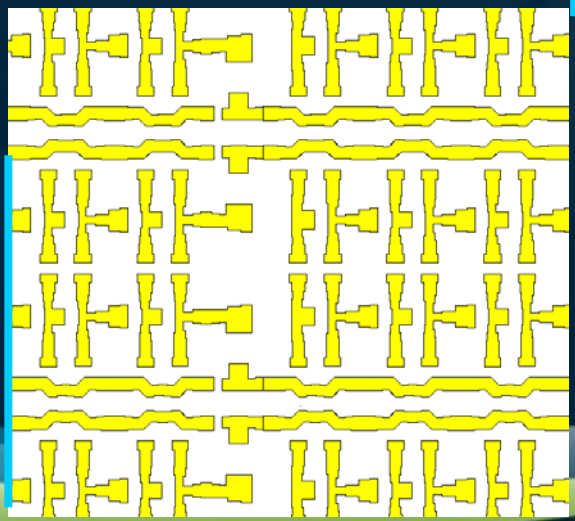
etch contours

adjust corrections

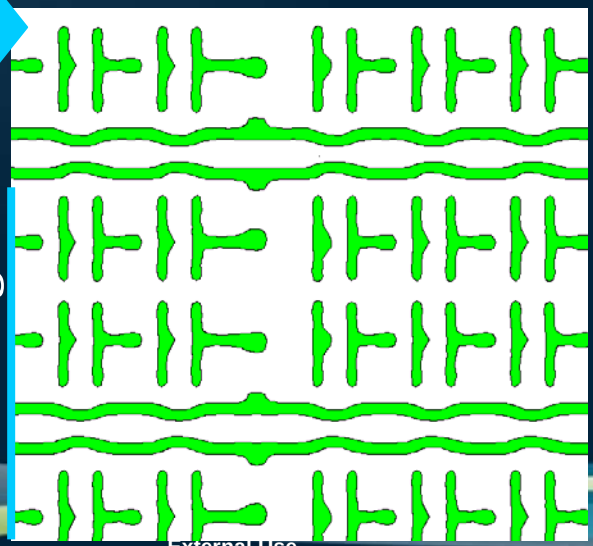
corrections

light intensity simulation and test structure calibration

"quick" etch simulation (2d geometry transform) calibration



corrected

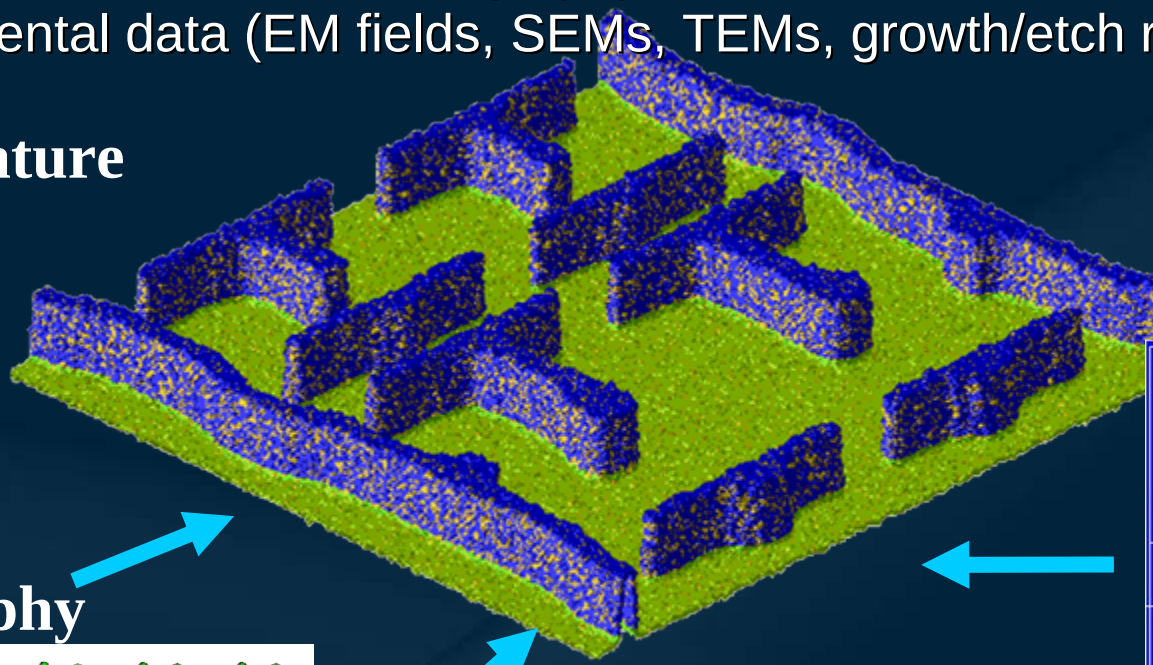


aerial image

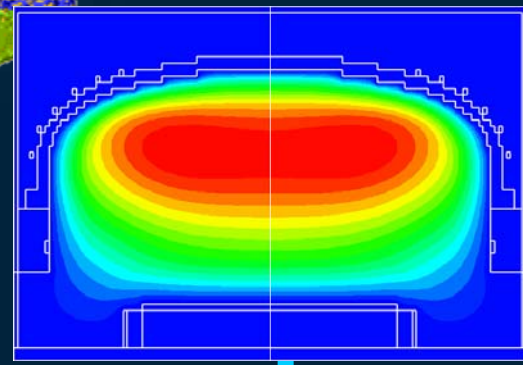
REACTOR/FEATURE ETCH MODEL

Multi-scale reactor/sheath/lithography/feature/atomistic models calibrated with experimental data (EM fields, SEMs, TEMs, growth/etch rates, ...)

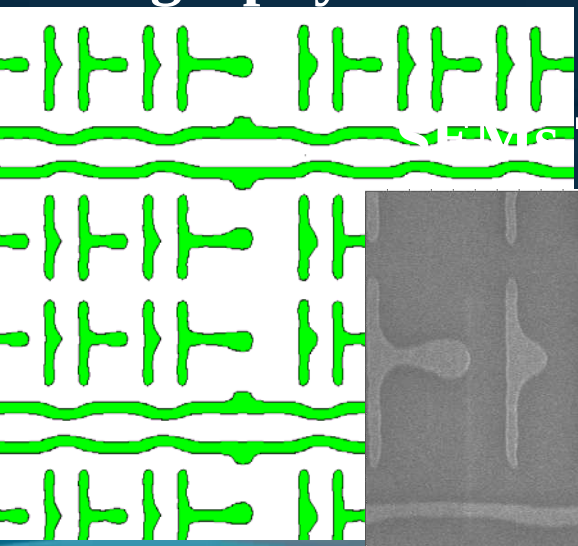
Feature



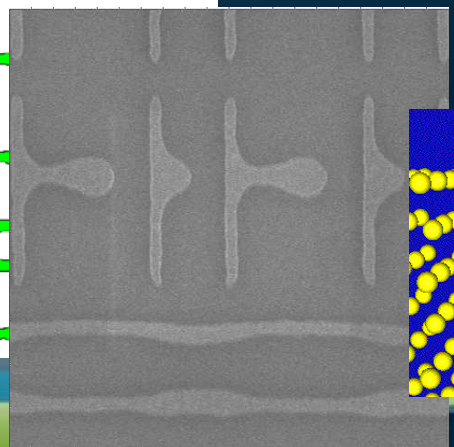
Reactor



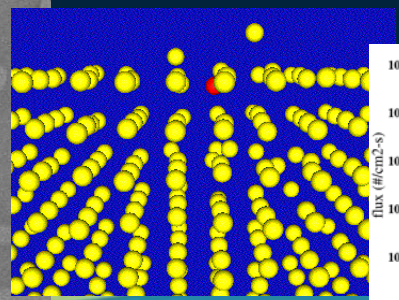
Lithography



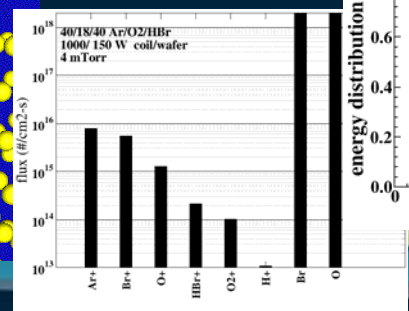
SEMs TEMs

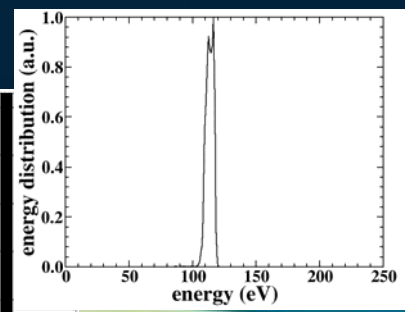


Atomistic



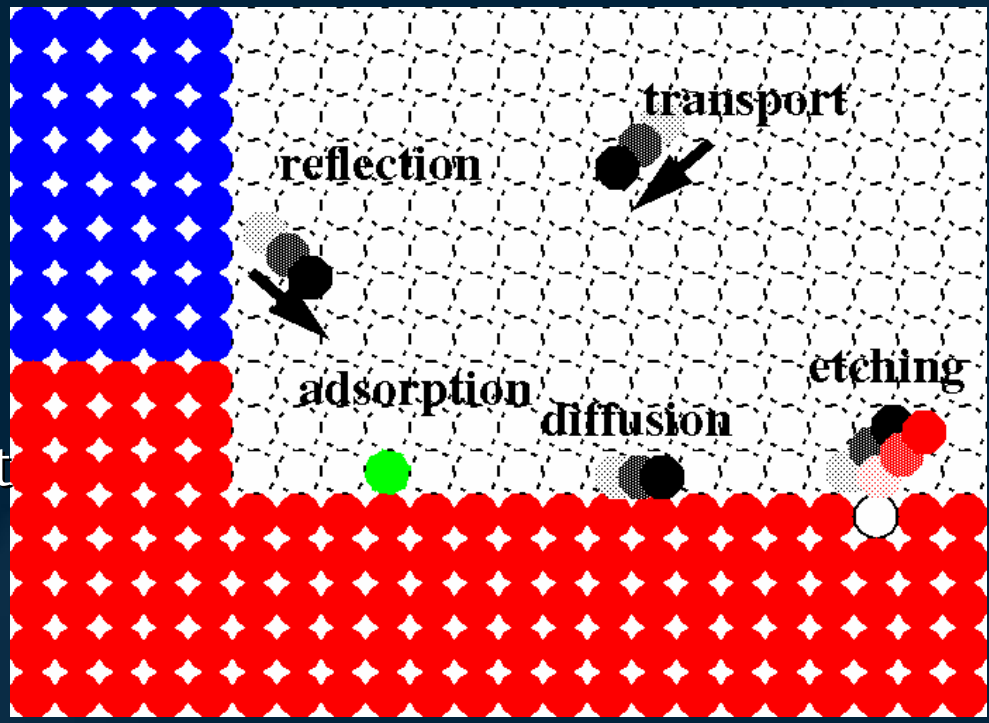
Sheath





MONTE CARLO FEATURE MODEL

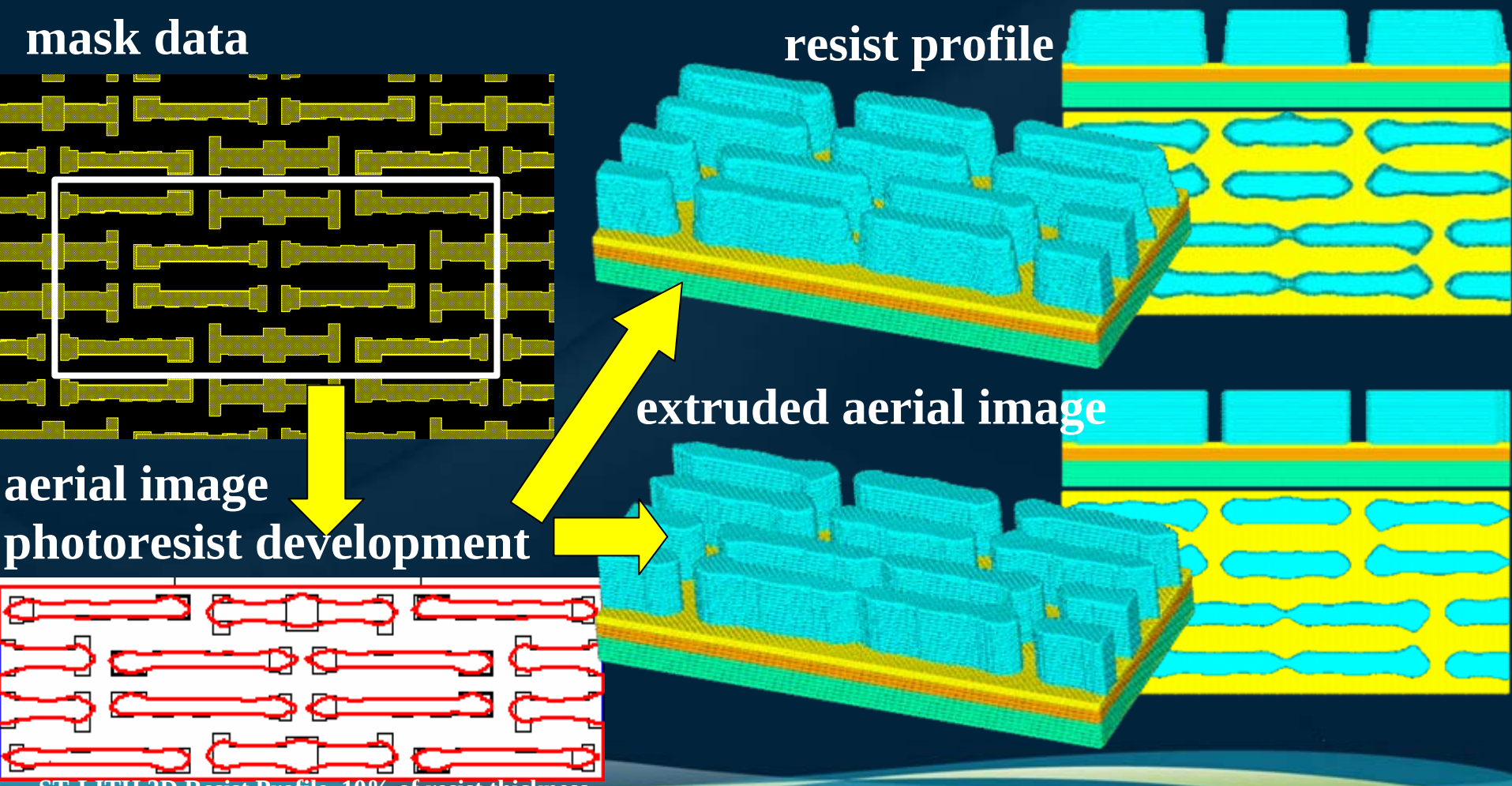
- A statistical method
- feature surface represented by unoccupied/occupied interface in a “material” mesh
- Particle number incident on surface proportional to incident flux rate
- Lagrangian particle tracking includes shadowing by surface



- 2D/3D, packing (sc,fcc,bcc), multi- material, multi-specie
- Includes specie transport, adsorption, surface diffusion, reflection (diffusive, specular), energy loss, etch, sputter, and deposition
- Surface properties (tac, sticking coefficient, sputter yield, etch rates, and reflection) are functions of angle, energy, specie, and material

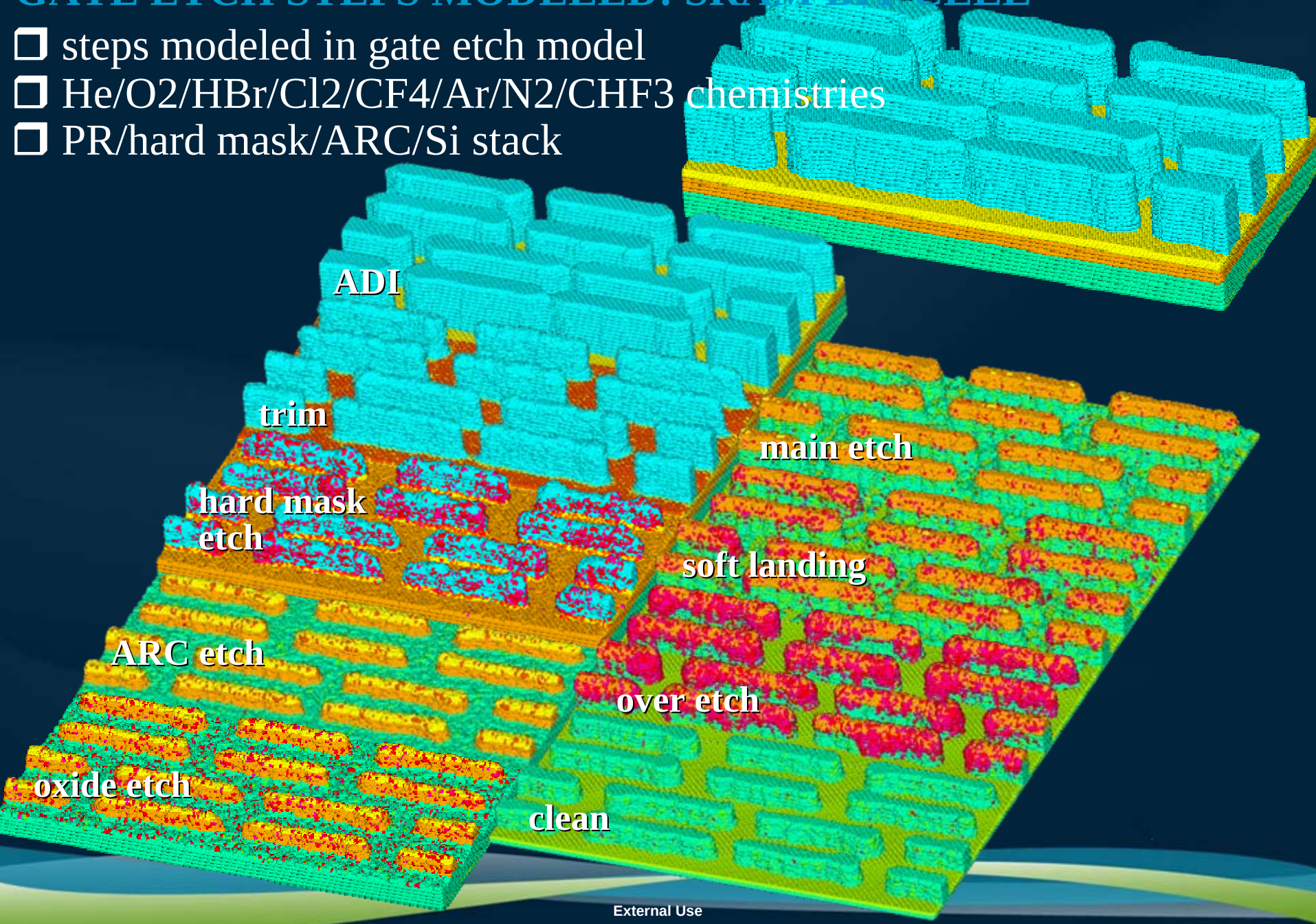
PAPAYA COUPLED TO LITHOGRAPHY MODELS

- papaya uses initial photo resist mask calculated by lithography models
  - extruded aerial image or developed 3D photo resist (PR) profile used
  - allows study of mask pattern transfer and gate profile during gate etch



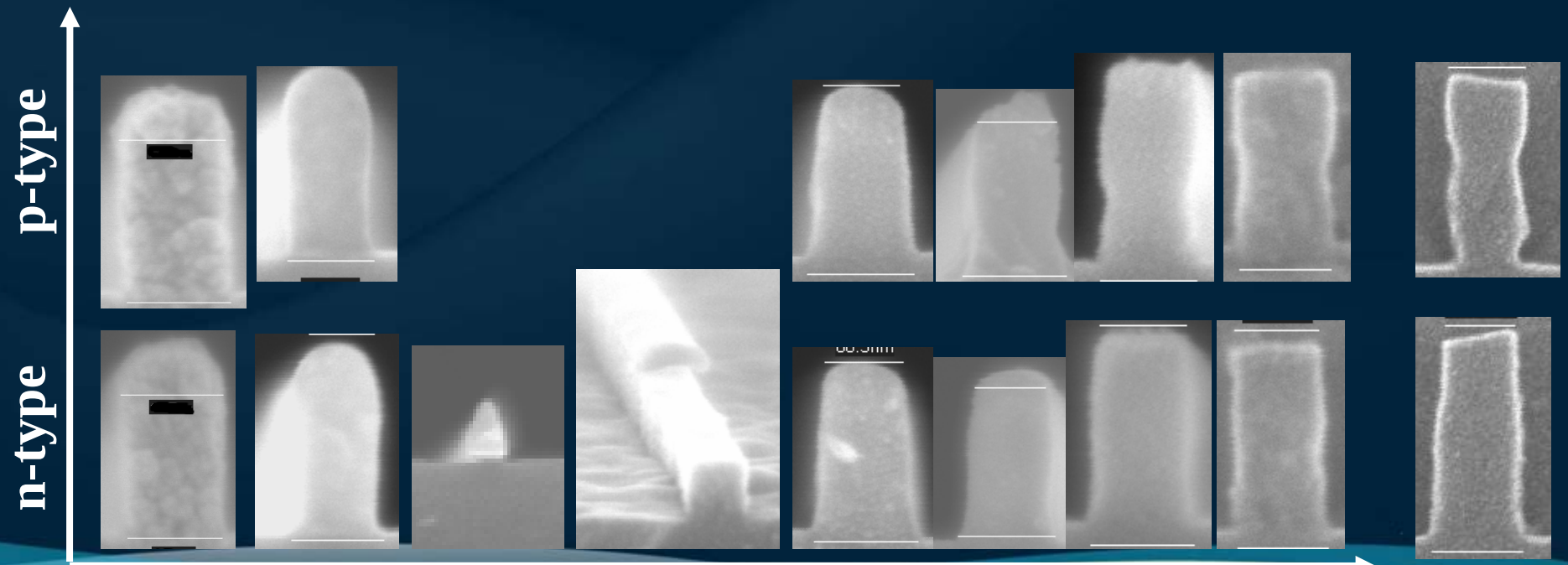
GATE ETCH STEPS MODELED: SRAM BIT CELL

- steps modeled in gate etch model
- He/O2/HBr/Cl2/CF4/Ar/N2/CHF3 chemistries
- PR/hard mask/ARC/Si stack



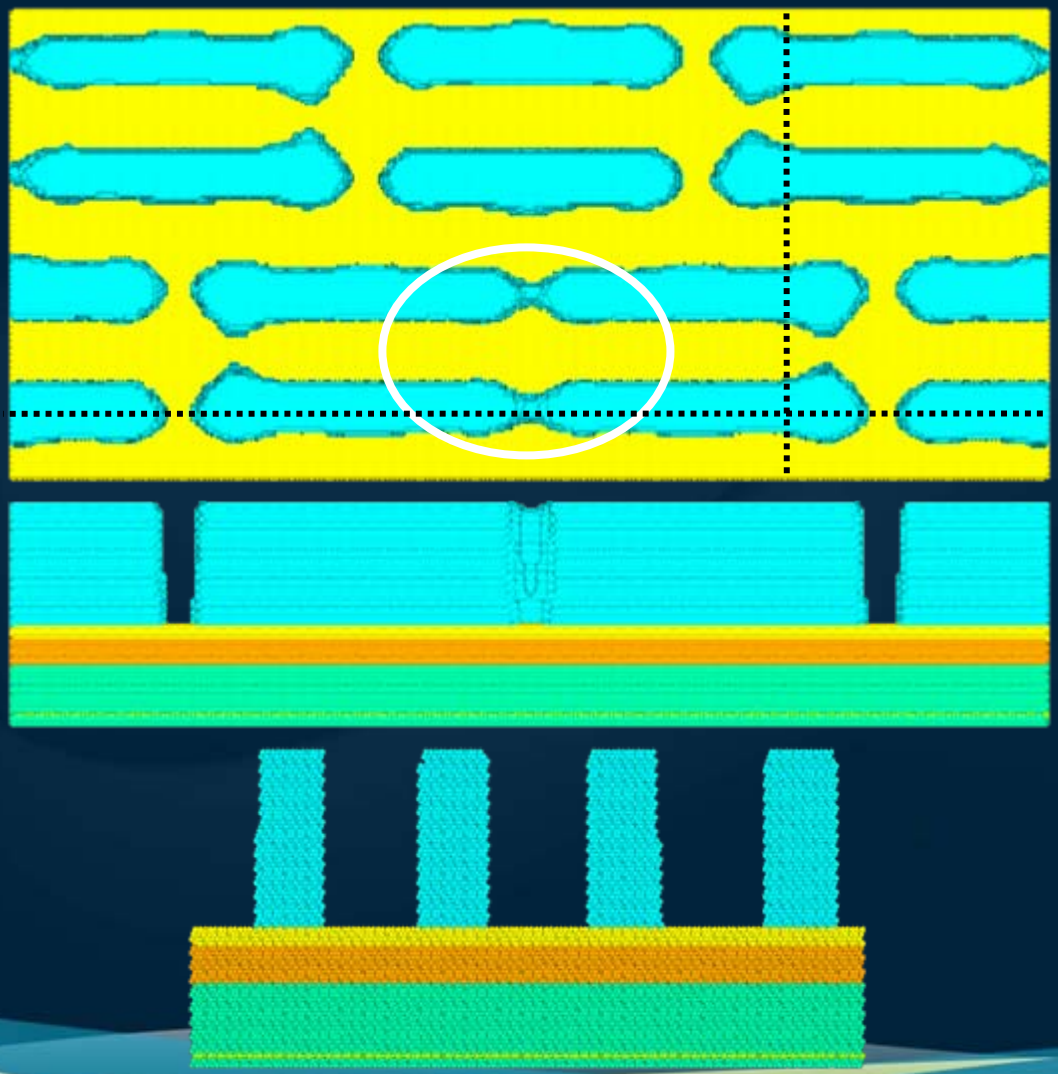
GATE ETCH PARTITION FOR P & N-TYPE POLYSILICON

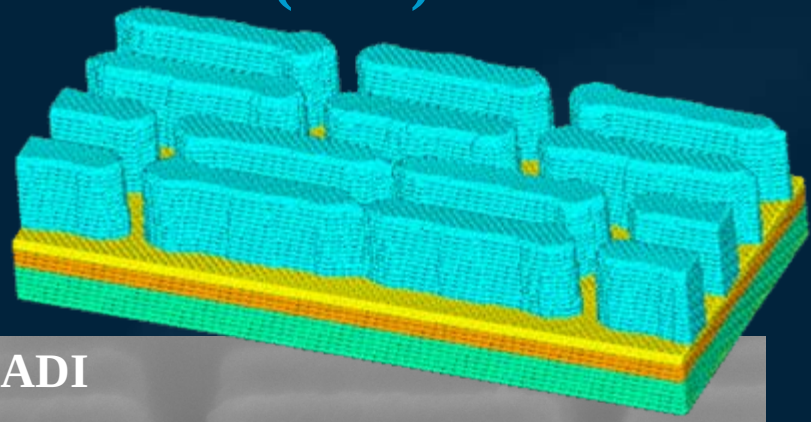
- profiles sensitive to previous profiles
- faceting at hard mask etch indicates PR budget exceeded
- sloping ARC profile translates into poly silicon profile
- poly silicon trapezoidal after main etch
- p- (hourglass, undercut) and n-type (coke bottle, trapezoidal) characteristic profiles become apparent at soft landing (much more neutral driven etch) and over etch.

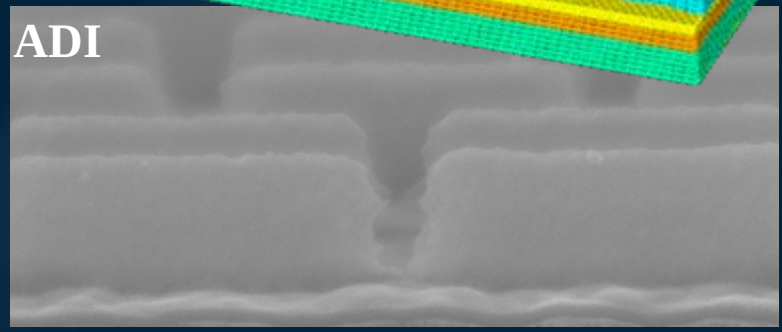


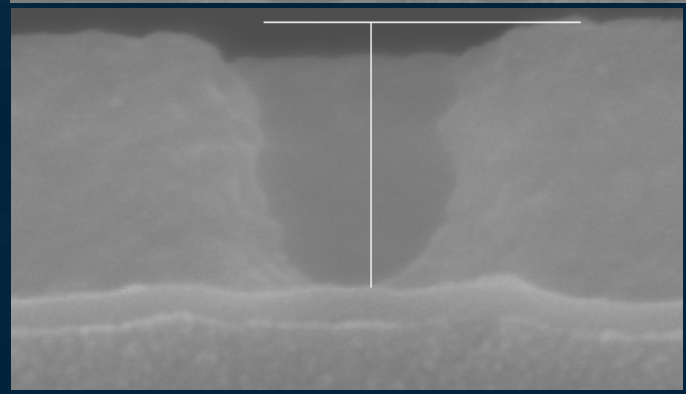
SRAM BIT CELL : AS DEVELOPED IMAGE (ADI)

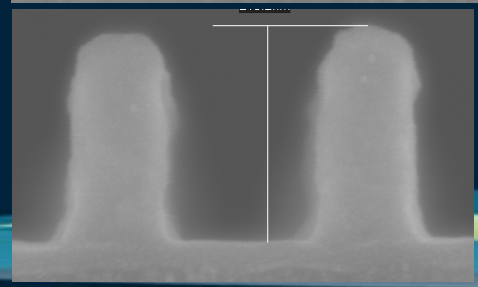
- developed photo resist (ADI) shows bridging at line ends





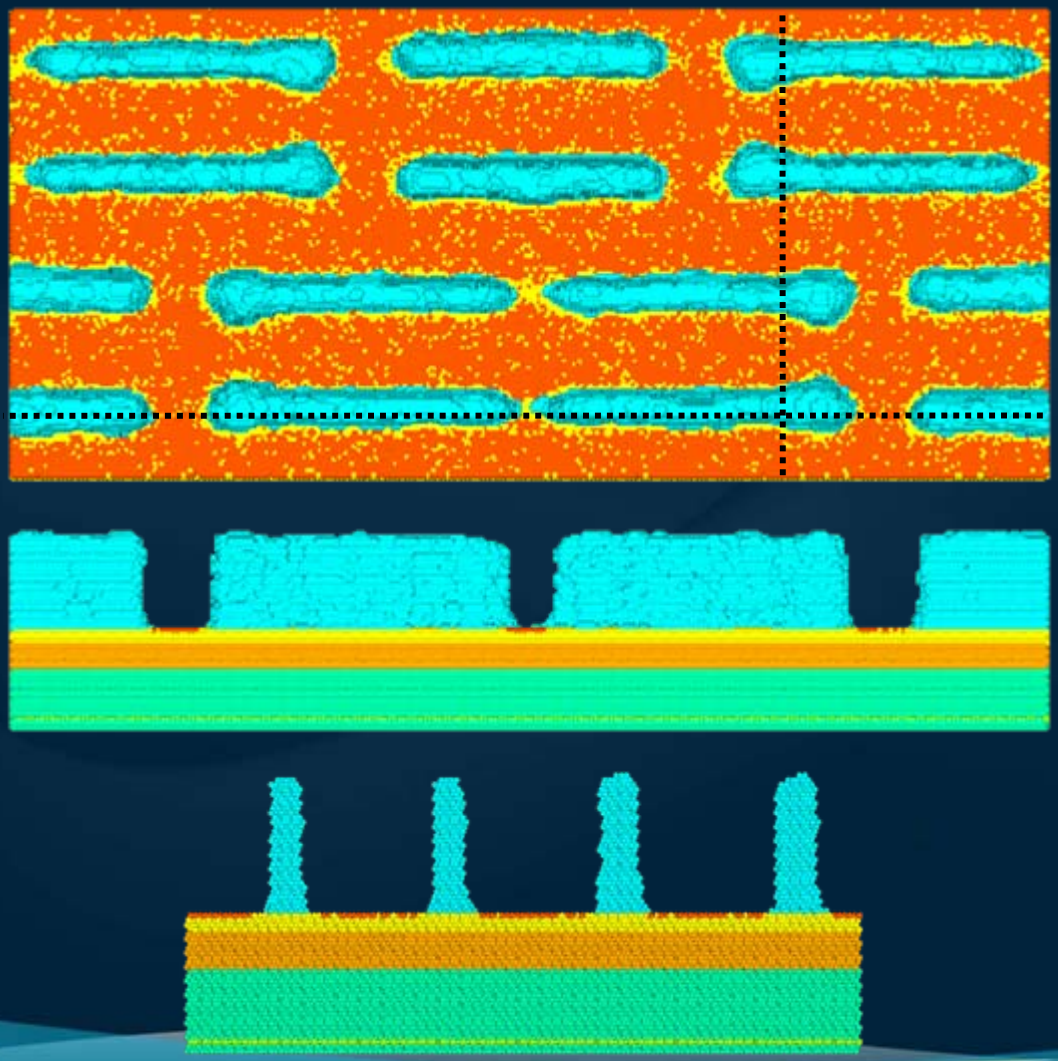


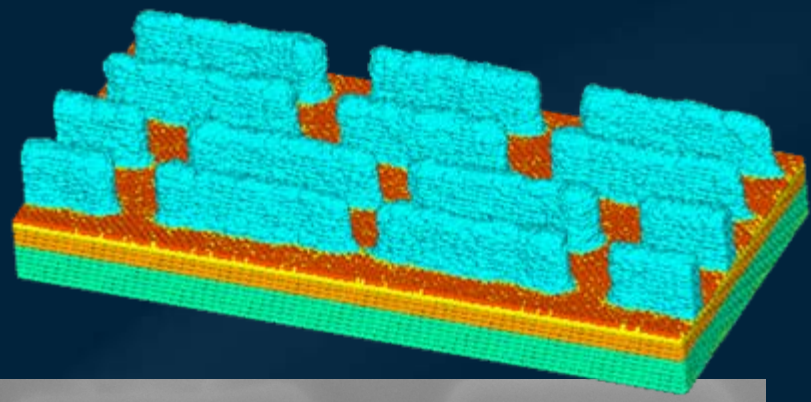


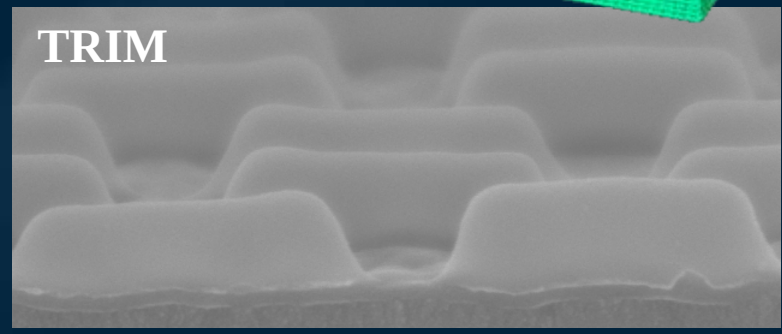


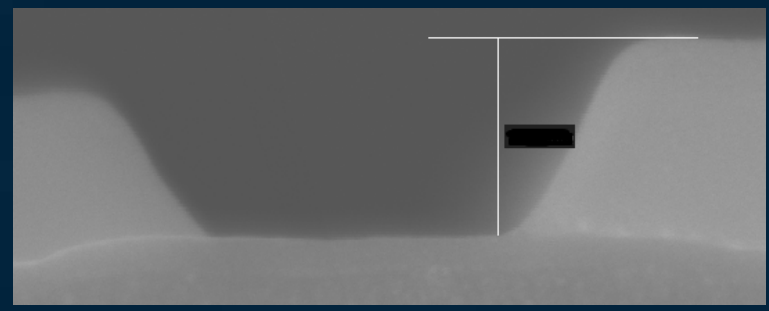
SRAM BIT CELL: TRIM

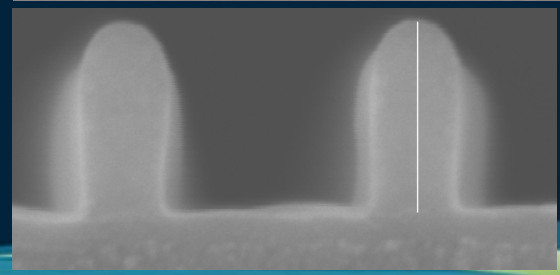
- Angled line ends at ADI lead to large line end pull back at etch.





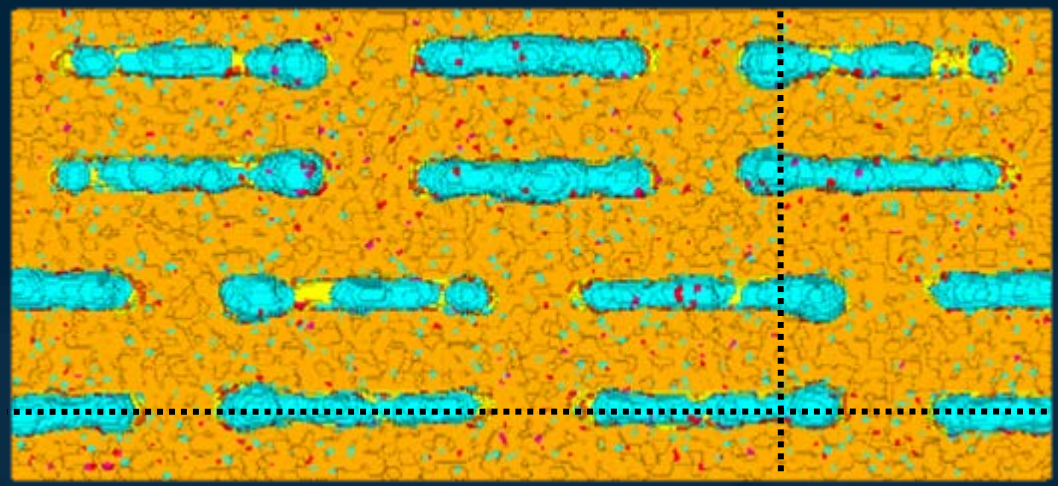


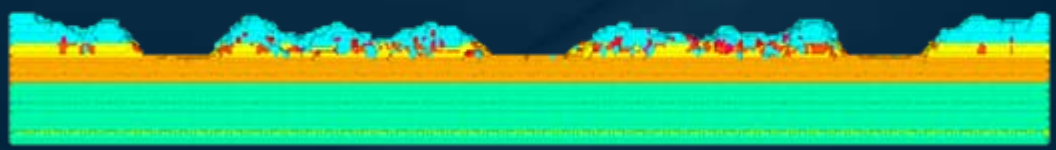


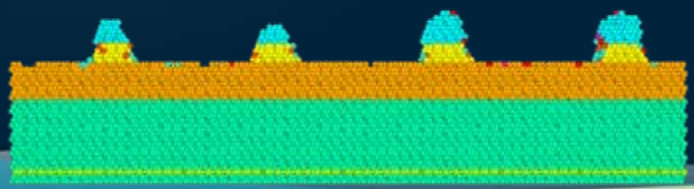


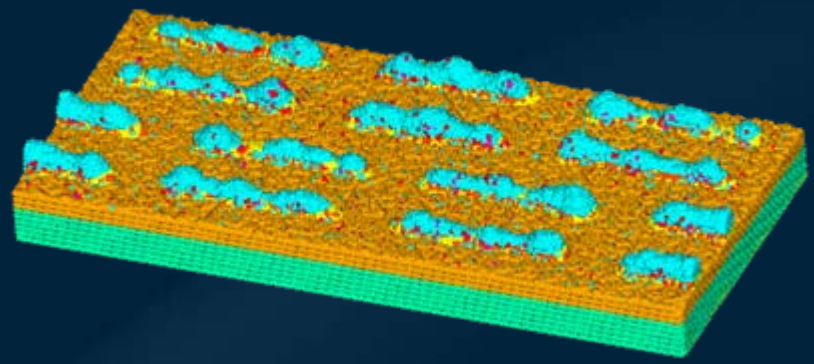
SRAM BIT CELL : HARD MASK

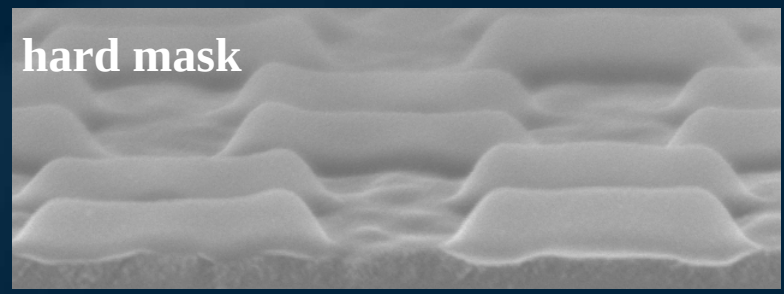
- Exceeding the PR budget at hard mask etch exacerbates line end pull back

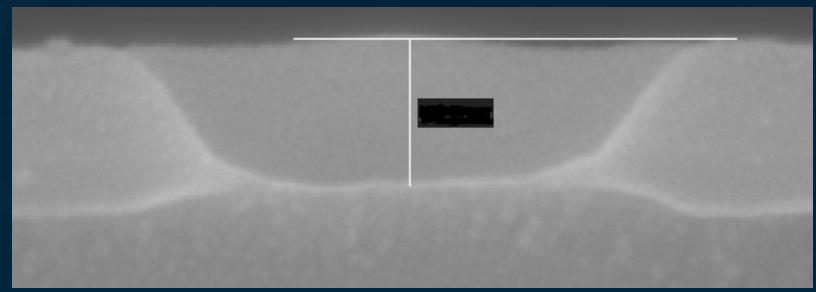


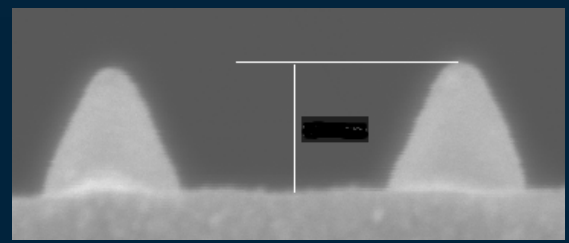






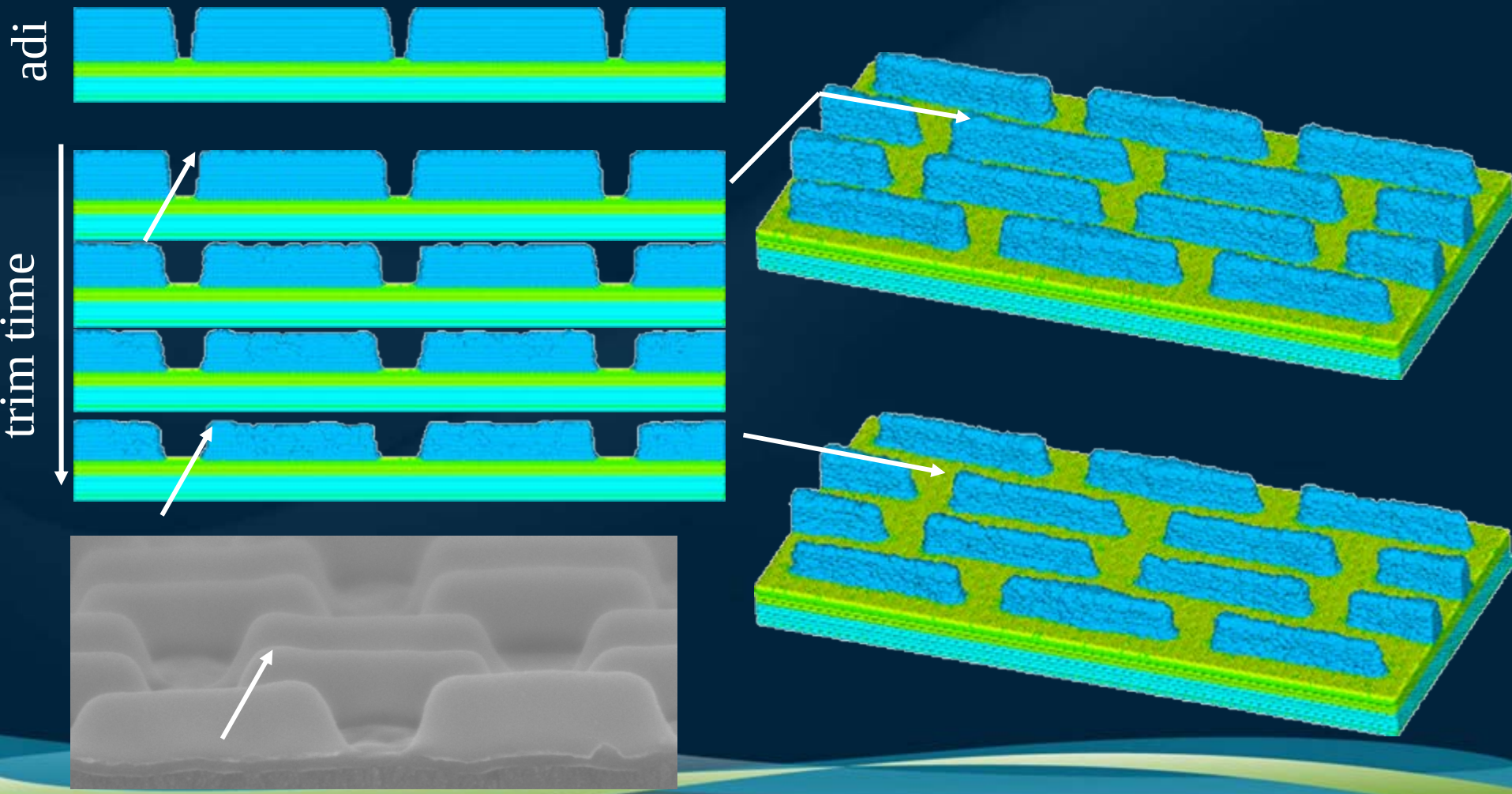






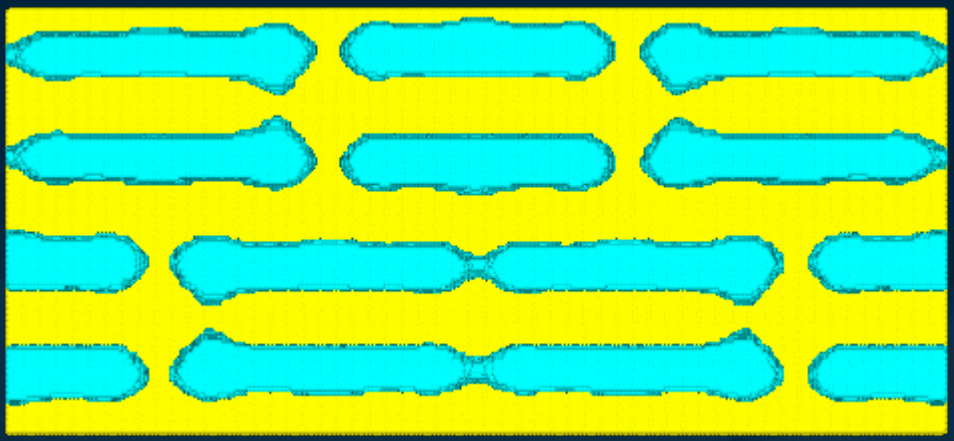
SRAM BIT CELL : TRIM ETCH TIME

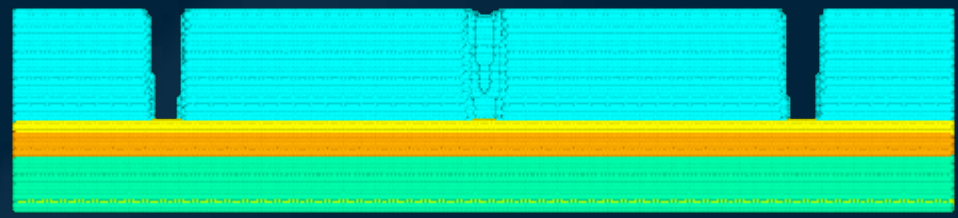
- increased trim time increases side wall slope and pull back
- wider line ends with their larger cds also have a larger height

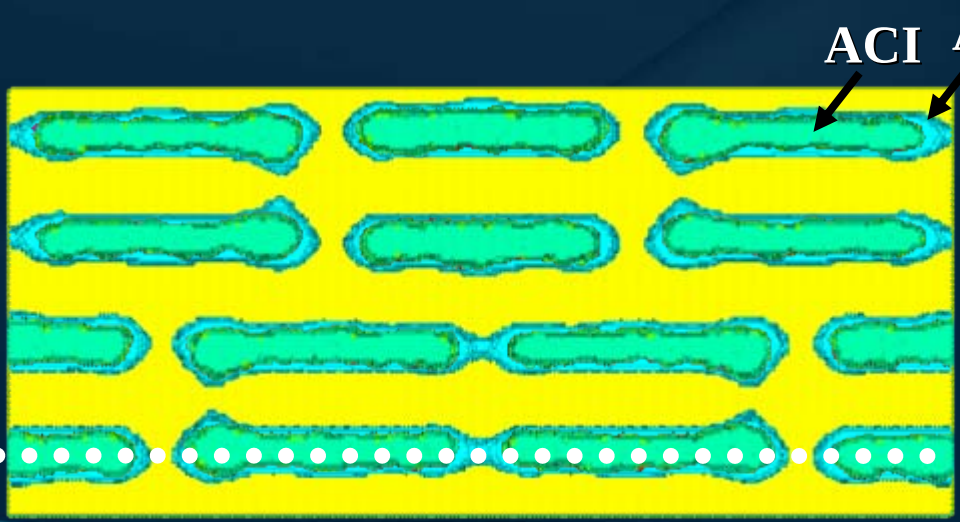


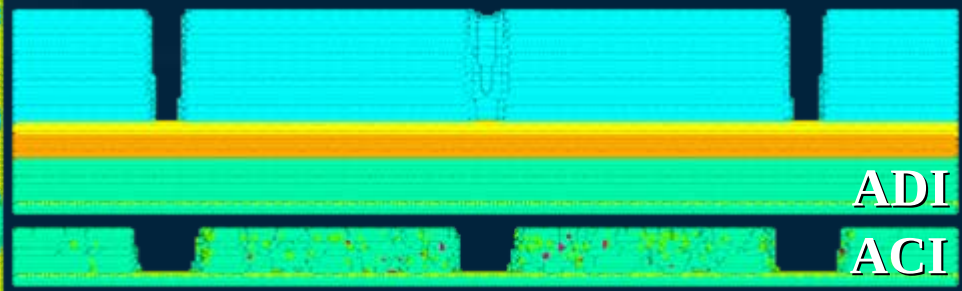
SRAM BIT CELL : LINE END PULL BACK

- line end pull back is of concern at gate etch for sram bit cell
- too much pull back can violate layout rules, or decrease layout density



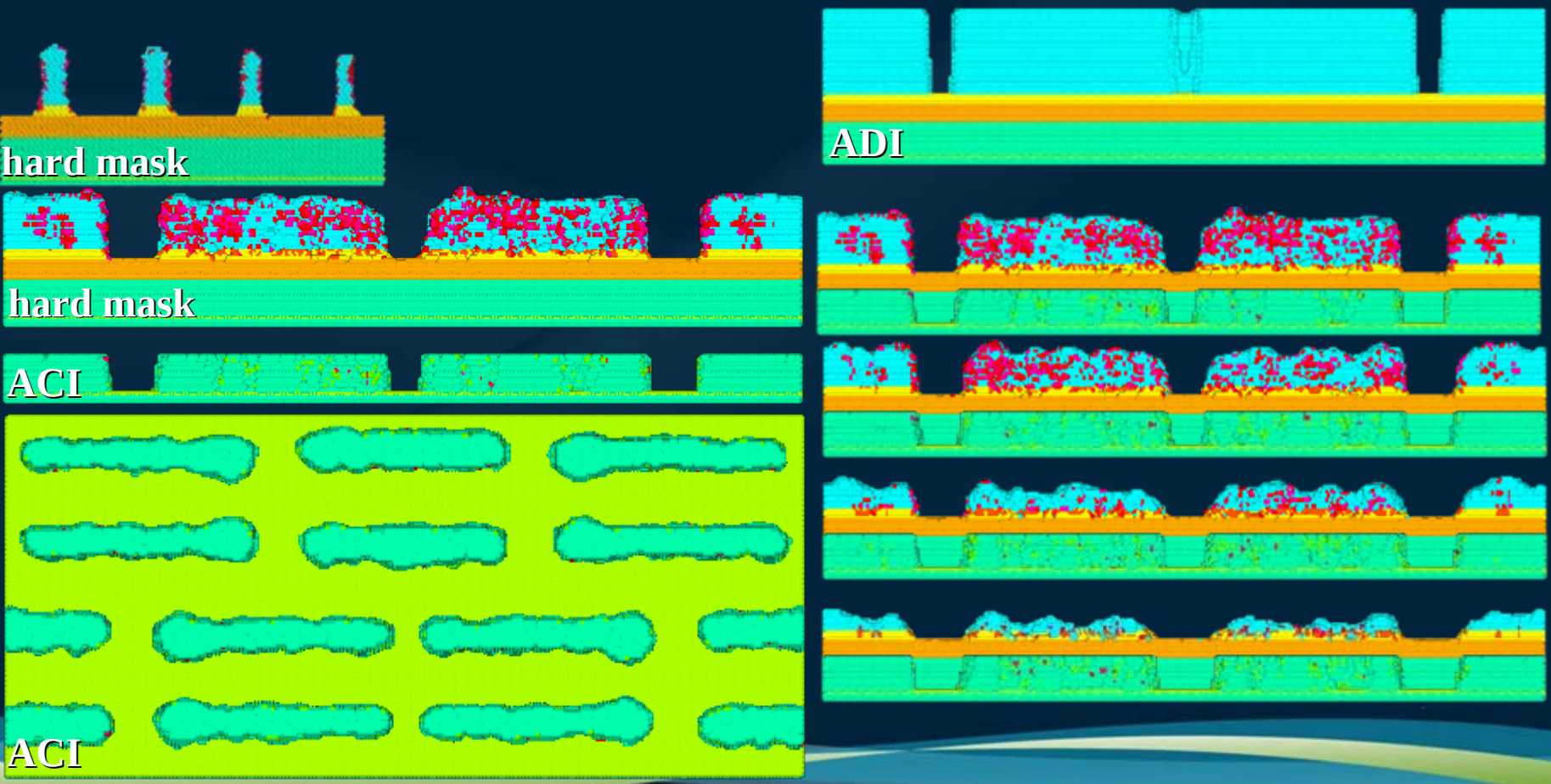






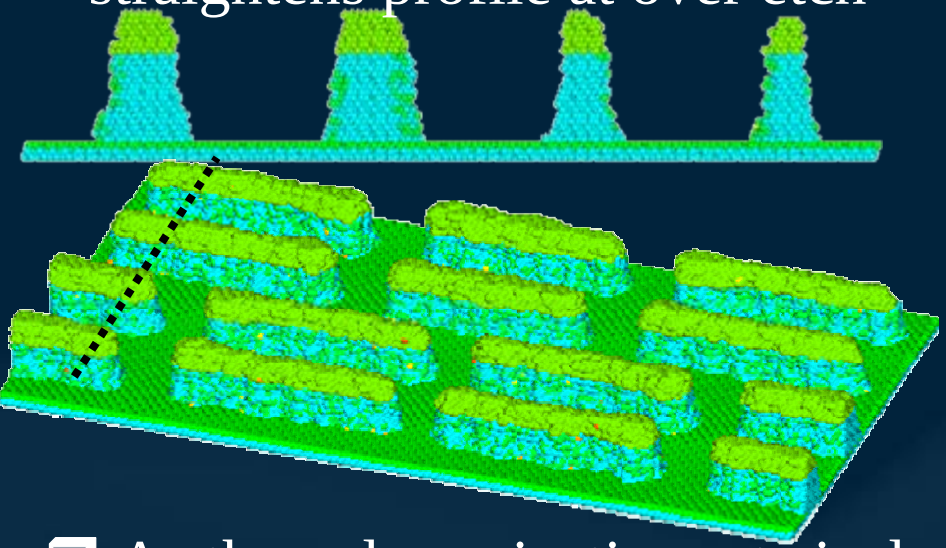
HIGHER PR ION ETCH YIELD

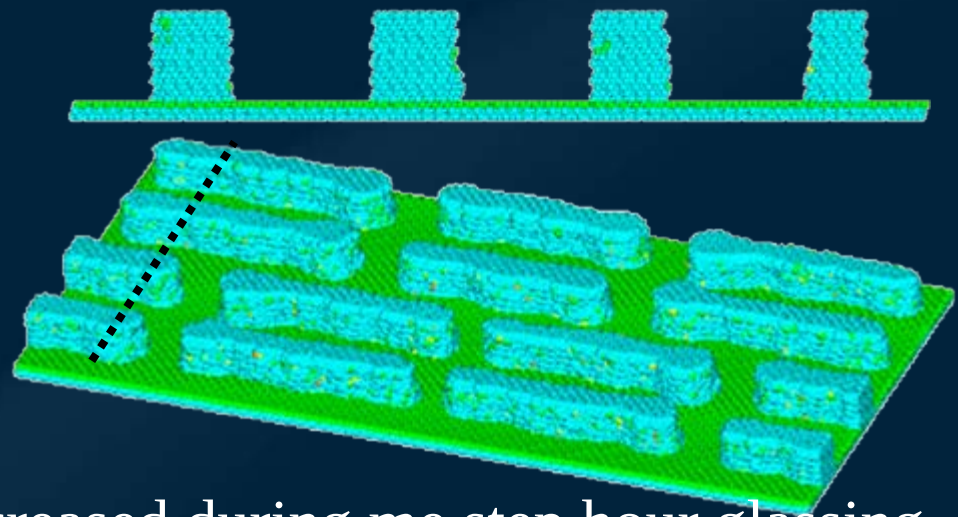
- slice of bit cell showing effect of increased etch rate
- hard mask etch overlayed with final clean
- bit cell with higher PR ion yield increases line end pull back as PR slopes at line ends and becomes a less effective etch mask



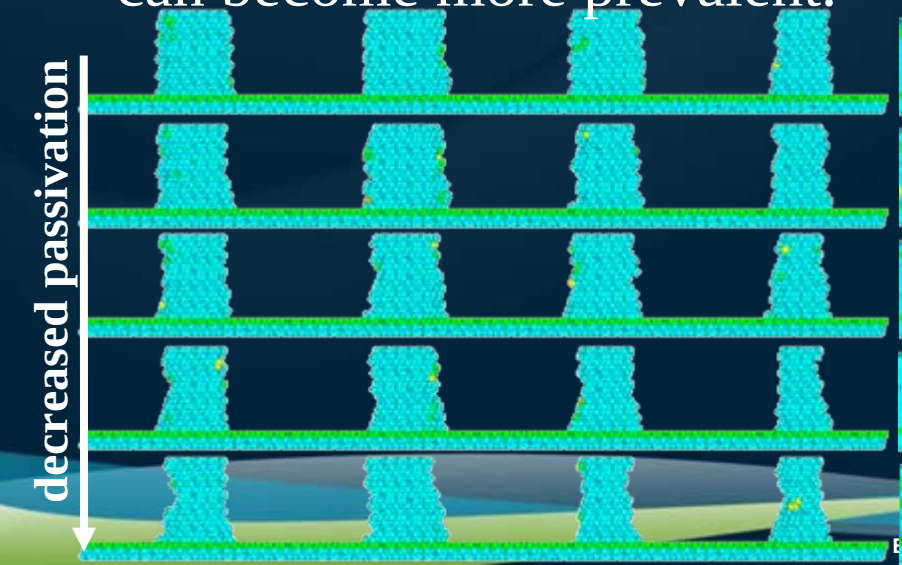
STRAIGHTENED SIDEWALLS, HOURGLASSING

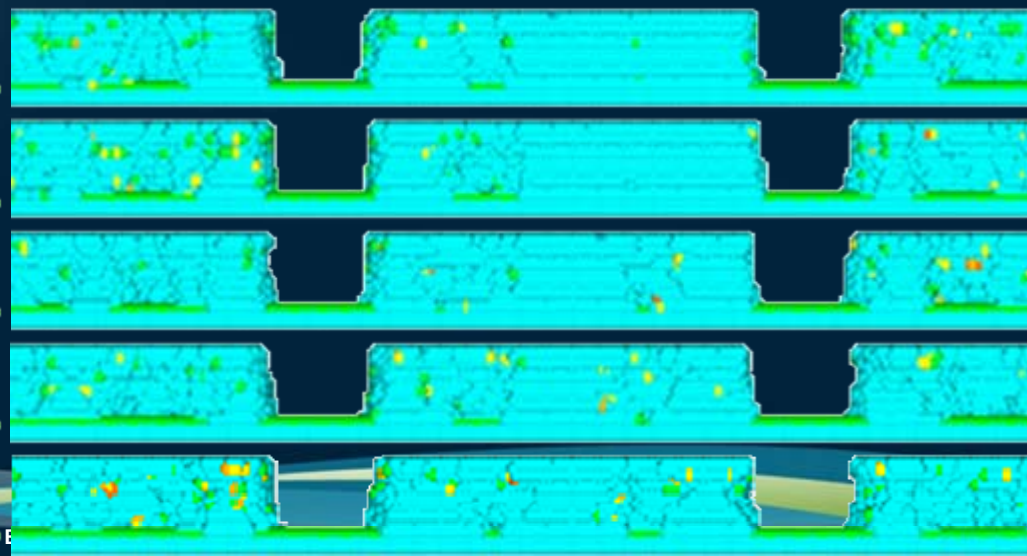
- Allowing passivant to contribute to sidewall polymer growth straightens profile at over etch





- As the polymerization rate is decreased during me step hour glassing can become more prevalent.





SUMMARY

- reactor/feature/lithography/atomistic modeling suite is being applied to gate etch
- coupling to lithography models allows study of pattern transfer as well as poly silicon profile
- studying the cumulative effect of the gate etch processes required to transfer the pattern through the gate stack helps understand the impact one step can have on subsequent steps
  - less etch resistant resist leads to more line end pull back
  - polymer deposition at main etch “sets up” the profile type seen subsequently at soft landing and over etch
- model based etch correction strategies can take advantadge of reactor/feature modeling suites