

**Engineering Document** 

# Resistive switching for next generation Flash technology Christie Marrian, Spansion

10/24/07

**Spansion Confidential** 

### **Cautionary Statement**

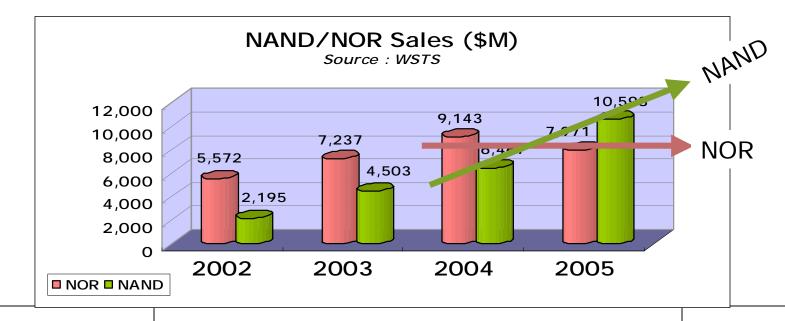


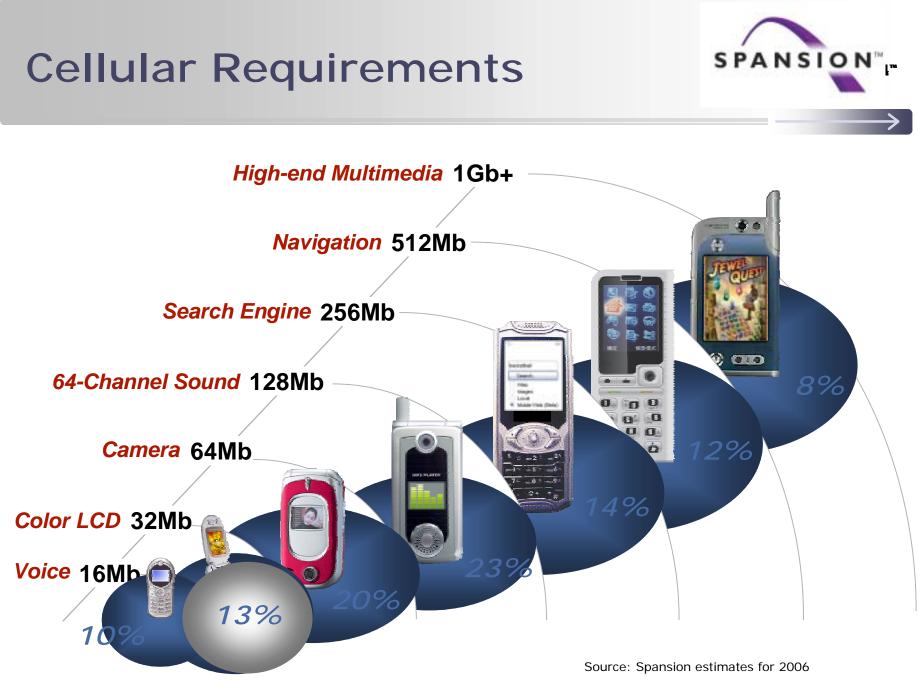
This presentation and comments made pursuant thereto may contain forward-looking statements that are made pursuant to the safe harbor provisions of the Private Securities Litigation Reform Act of 1995, including statements regarding future deployment of MirrorBit<sup>TM</sup> technology, the company's ability to capitalize on its product and technology leadership and its operational efficiency. Investors are cautioned that the forward-looking statements in this presentation involve risks and uncertainties that could cause actual results to differ materially from the company's current expectations, including the possibility that demand for the company's Flash memory products will be lower than currently expected; that customer acceptance of MirrorBit choose NAND-based Flash memory products over NOR- and MirrorBit ORNAND architecture-based Flash memory products for their applications; that there will be a lack of customer acceptance of MirrorBit ORNAND architecture-based Flash memory products; that the company will not achieve its current product and technology introduction or implementation schedules; that the company will not be able to meet customer demand during cyclical industry or economic downturns; that competitors will introduce new memory technologies that render the company s Flash memory products uncompetitive or obsolete. The company urges investors to review in detail the risks and uncertainties in the company's Securities and Exchange Commission filings, including but not limited to the company's Annual Report on Form 10-K for the year ended December 25, 2005.

#### Introduction



- NAND market
  - Almost 100% data storage.
  - Memories are mostly for memory cards or memory products.
- NOR market
  - Mainly for code storage.
  - Memories are embedded in systems.
- NOR flash memory technology
  - Only for NOR market? No.



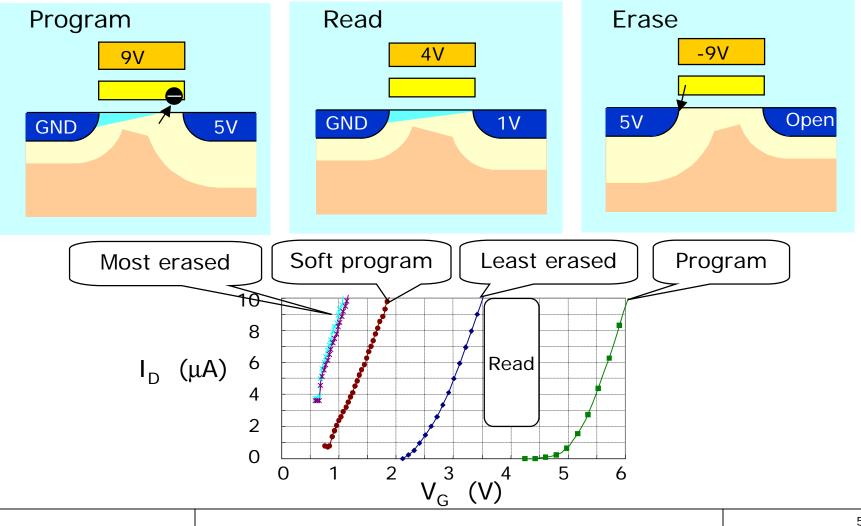


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#### Floating Gate Cell Basic Operations



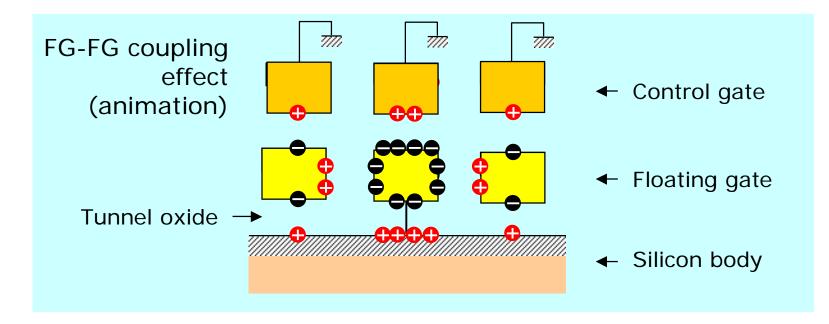
• Initial cell  $V_T$  is low (Data 1).



#### Floating Gate Scaling Barrier

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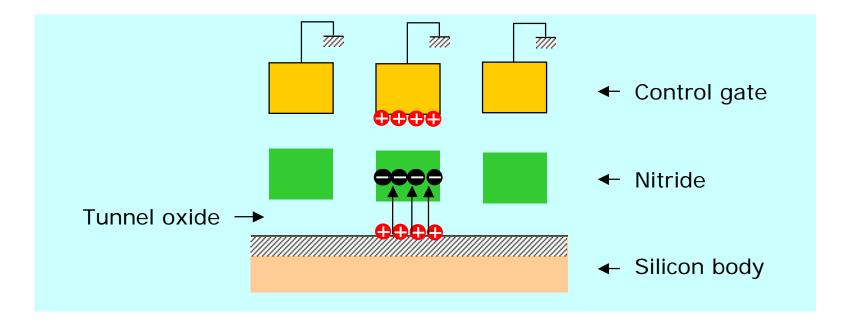
- Floating gate electro-static interaction
  - Narrow floating-gate spacing
  - Tall floating gate



#### Nitride Storage



- The favorite NVM technology
  - Charge does not move around the storage electrode
  - Less floating gate electro-static interaction results in denser memories.

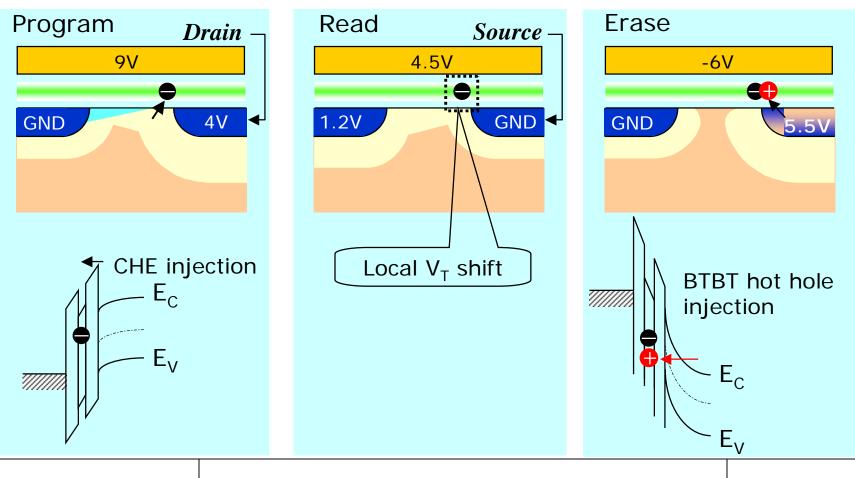


#### **MirrorBit Basic Operations**



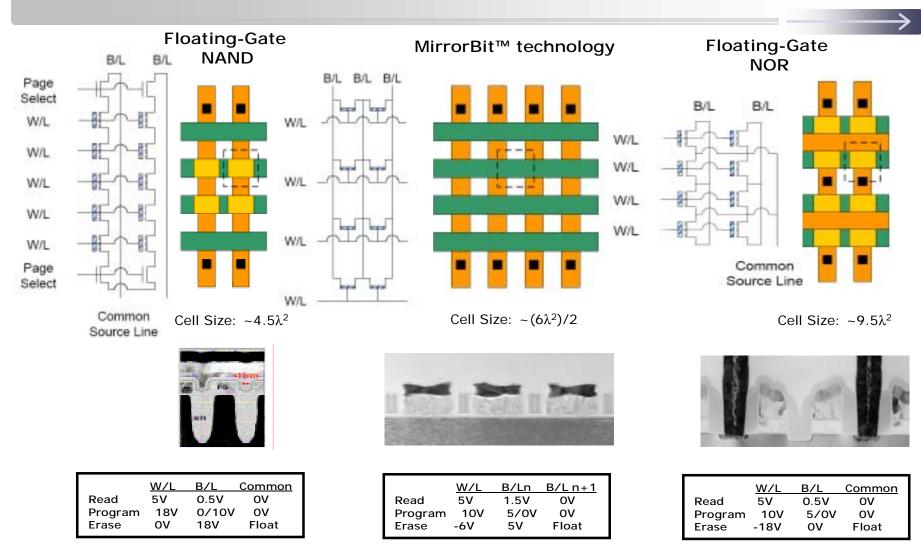
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- Channel hot electron (CHE) programming
- Transpose source and drain for reading the data
- Band to band (BTBT) hot hole injection erasing



## **Cell Operation**



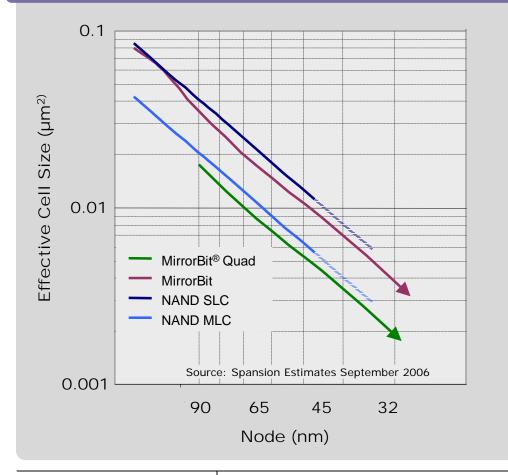


MirrorBit<sup>®</sup> Quad: Technology of the Future—Today



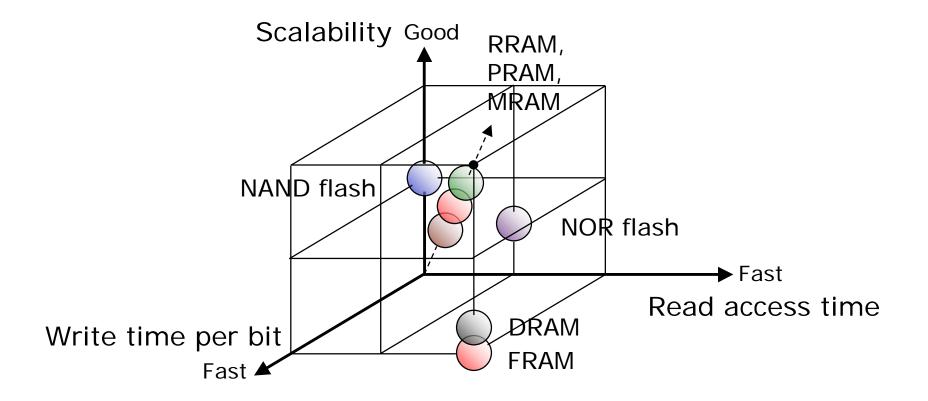
#### Scaling to 32nm and Beyond

**Goal – One Node Per Year** 



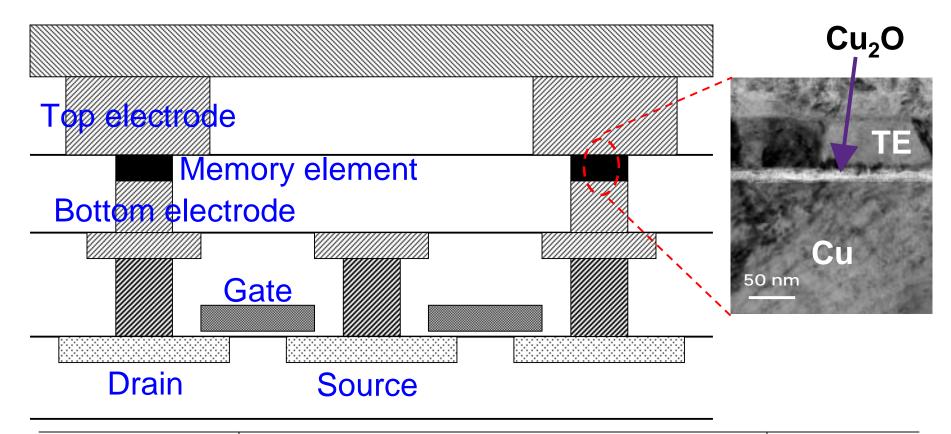
110nm	-	_	_	-
90nm		-		_
65nm			-	-
45nm				-
	2005	2006	2007	2008
	Production			

# **Emerging Memory Technologies**



# **Memory Cell Structure**

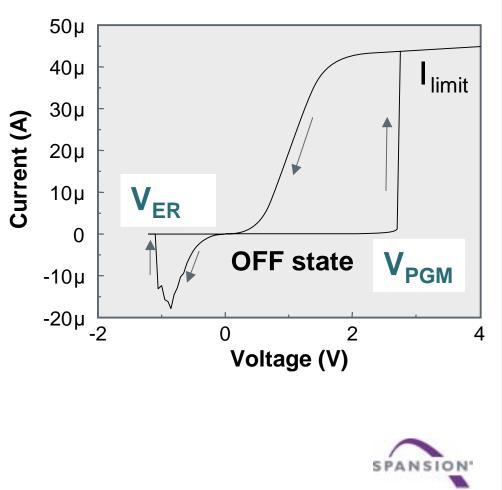
- > MIM memory element built on a via
- > Memory element connected with a select transistor
- Fully compatible with standard CMOS process



#### **Background – Trapping Model\***

- OFF state mainly by space-charge-limitedconduction (SCLC) and Frenkel-Poole (FP)
- OFF → ON switch at trap-filled-limit voltage (VTFL)
  - \* Chen *et. al* "Non-volatile resistive switching for advanced memory applications," *Electron Devices Meeting, 2005. IEDM Technical Digest. IEEE International*, vol., no.pp. 746- 749, 5-7 Dec. 2005

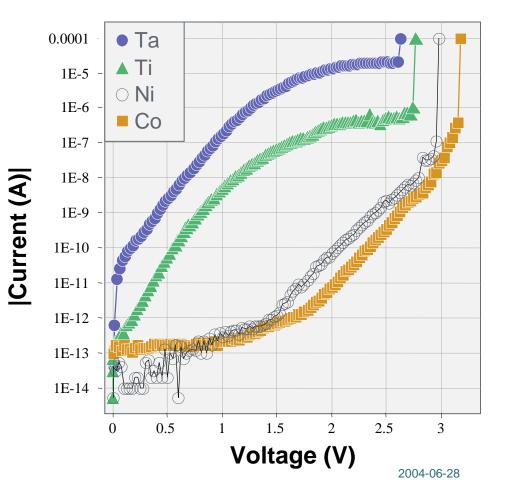
#### **Cu2O MIM Memory Cell**



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#### **Electrode Effect**

# OFF-state current leakage increases with reactivity between top electrode and $Cu_2O$ (Ni/Co<Ti<Ta).



# Free energy of formation

Мох	∆G₀ <u>(kcal/mole)</u>
CoO	-51
NiO	-51.7
TiO <sub>2</sub>	-212
<b>Ta</b> 2 <b>O</b> 5	-457



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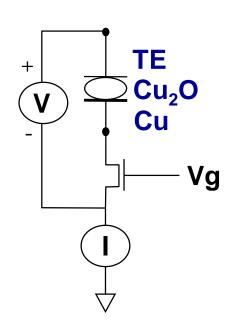
#### Switching Characteristics: Ni vs. Ti TE

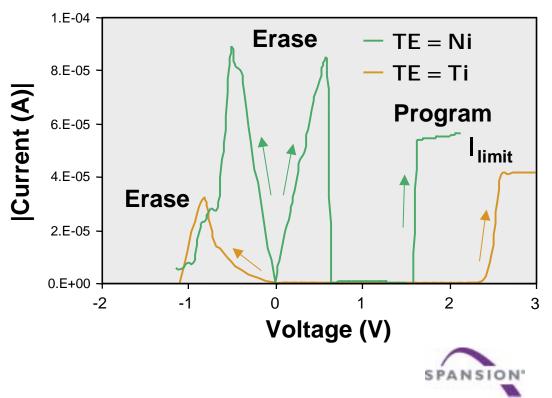
#### Cells with Ni top electrode

- Erase with both polarity
- Higher erase current

# Cells with Ti top electrode

- Reverse polarity field
- Low erase current

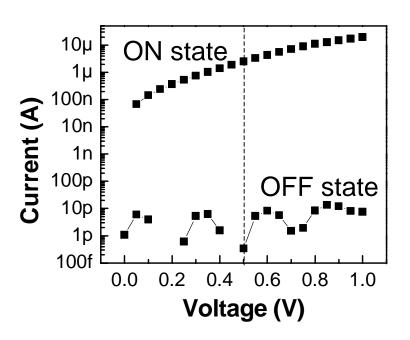


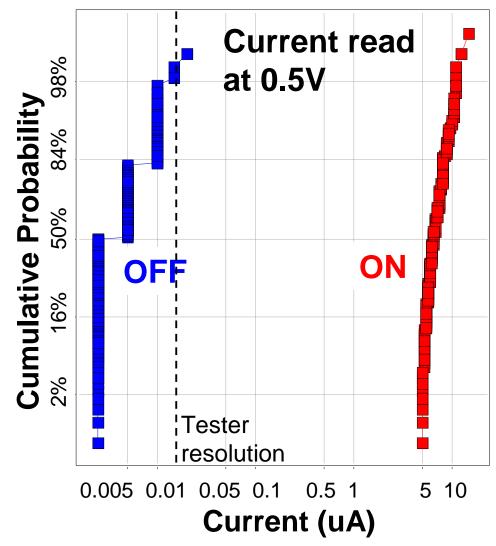


# **ON/OFF** Window

 Model predicts high ON/OFF ratio with deep-trap materials
 ON/OFF ratio of

**10<sup>5</sup> – 10<sup>6</sup> observed** 





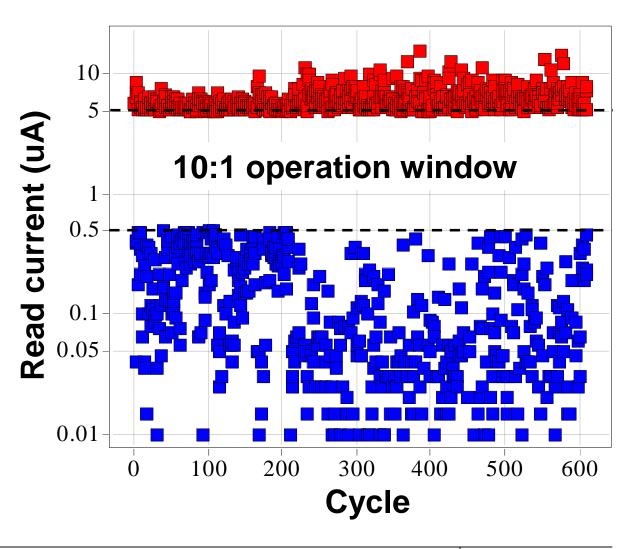
# Retention

Long retention predicted 25°C 50 hrs retention with deep-trap materials Color by Binned Switching current (uA): Cumulative Probability 16% 50% 84% 98% Retention related to 0-0.1 0.1-0.5 program current 0.5-1 1-5 5 - 10 10-31.25 90°C 30 hrs retention 10<sup>-5</sup> Current (A) THERSTAL RELEASE TIMES FROM TRAFS AT ROOM TEMPERATURE  $\tau_{\pm} = 10^{-11} \exp[(E_{\pm} - E_{0})/hT], hT = (1/40) \text{ eV}$  $E_* - E_1$ τ., 1.6 (1.61) 1 86\* 3.92 10 days day 2 min 2% 10 .... 10-1 ai (0.52) 10<sup>-4</sup> mm 10,400 10<sup>-4</sup> sec  $= 3 \times 10^{9}$  yr  $\approx$  the age of the earth 10 0.2 0.6 0.8 0.4 1.2  $10^{3}$ 10<sup>5</sup> 0 10<sup>1</sup>  $10^{2}$  $10^{4}$ Current(50hr) / Current(0hr) Time (min) M.A. Lampert et al, "Current injection in solids", Academic Press, 1970.

10/26/2007

# Cycling

 Program with 100 ns pulses
 0.5uA – 5uA window for cycling



#### **Electrical Characteristics Summary**

Characteristics		Values	
Programming	V/I	(2-5 V) / (~ 50 uA)	
	Speed	≤ 100 ns	
Erasing	V	1-2 V	
	Speed	≤ 100 ns	
Retention		30 hours at 90°C tested	
Cycling		> 600 cycles tested	
Read disturb		Zero up to 25 hours at V < 0.5V	
Cell size		0.18 um	

A. Chen et. Al, IEDM 2005



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#### **BEOL** Thin Film Challenges for RCM

- Thin ~100A metal oxide films
- Hard to etch (process) metal films
  - Interfaces in metal-oxide-metal cell
- Highly planar CMP
  - Maintain electric field uniformity across cell
- Phase Change RCM
  - Ternary materials plus dopant
  - Encapsulation





T-N Fang, S. Kaza, S. Haddad,
A. Chen, Y-C Wu, Z. Lan,
S. Avanzino, D. Liao,
C. Gopalan, S. Choi, S. Mahdavi,
M. Buynoski, Y. Lin, C. Marrian,
C. Bill, M. VanBuskirk,
and M. Taguchi

Erase Mechanism for Copper Oxide Resistive Switching Memory Cells with Nickel Electrode



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