Resistive switching for next generation Flash technology

Christie Marrian, Spansion

10/24/07
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Introduction

- NAND market
  - Almost 100% data storage.
  - Memories are mostly for memory cards or memory products.
- NOR market
  - Mainly for code storage.
  - Memories are embedded in systems.
- NOR flash memory technology
  - Only for NOR market? No.

![NAND/NOR Sales ($M)](chart)

*Source: WSTS*
Cellular Requirements

Source: Spansion estimates for 2006

- **Camera** 64Mb
- **64-Channel Sound** 128Mb
- **Search Engine** 256Mb
- **Navigation** 512Mb
- **High-end Multimedia** 1Gb+
- **Color LCD** 32Mb
- **Voice** 16Mb
- **10%**
- **13%**
- **20%**
- **23%**
- **14%**
- **12%**
- **8%**

Source: Spansion estimates for 2006
Floating Gate Cell Basic Operations

- Initial cell $V_T$ is low (Data 1).

![Diagram showing program, read, and erase operations](image)
Floating Gate Scaling Barrier

- Floating gate electro-static interaction
  - Narrow floating-gate spacing
  - Tall floating gate

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FG-FG coupling effect (animation)

Control gate
Floating gate
Silicon body
Tunnel oxide
Nitride Storage

• The favorite NVM technology
  – Charge does not move around the storage electrode
  – Less floating gate electro-static interaction results in denser memories.
MirrorBit Basic Operations

- Channel hot electron (CHE) programming
- Transpose source and drain for reading the data
- Band to band (BTBT) hot hole injection erasing

**Program**
- **Drain**
  - 9V
  - GND
  - 4V
- CHE injection $E_C$
- $E_V$

**Read**
- **Source**
  - 4.5V
  - 1.2V
  - GND
- Local $V_T$ shift

**Erase**
- **Drain**
  - -6V
  - GND
  - 5.5V
- BTBT hot hole injection
- $E_C$
- $E_V$
## Cell Operation

### Floating-Gate NAND

- **Cell Size:** $\sim 4.5\lambda^2$

<table>
<thead>
<tr>
<th>W/L</th>
<th>B/L</th>
<th>Common</th>
</tr>
</thead>
<tbody>
<tr>
<td>Read</td>
<td>5V</td>
<td>0.5V</td>
</tr>
<tr>
<td>Program</td>
<td>18V</td>
<td>0/10V</td>
</tr>
<tr>
<td>Erase</td>
<td>0V</td>
<td>18V</td>
</tr>
</tbody>
</table>

### MirrorBit™ technology

- **Cell Size:** $\sim (6\lambda^2)/2$

<table>
<thead>
<tr>
<th>W/L</th>
<th>B/Ln</th>
<th>B/L n+1</th>
</tr>
</thead>
<tbody>
<tr>
<td>Read</td>
<td>5V</td>
<td>1.5V</td>
</tr>
<tr>
<td>Program</td>
<td>10V</td>
<td>5/0V</td>
</tr>
<tr>
<td>Erase</td>
<td>-6V</td>
<td>5V</td>
</tr>
</tbody>
</table>

### Floating-Gate NOR

- **Cell Size:** $\sim 9.5\lambda^2$

<table>
<thead>
<tr>
<th>W/L</th>
<th>B/L</th>
<th>Common</th>
</tr>
</thead>
<tbody>
<tr>
<td>Read</td>
<td>5V</td>
<td>0.5V</td>
</tr>
<tr>
<td>Program</td>
<td>10V</td>
<td>5/0V</td>
</tr>
<tr>
<td>Erase</td>
<td>-18V</td>
<td>0V</td>
</tr>
</tbody>
</table>
MirrorBit® Quad: Technology of the Future—Today

Scaling to 32nm and Beyond

Goal – One Node Per Year

Source: Spansion Estimates September 2006
Emerging Memory Technologies

- Write time per bit:
  - NAND flash: Fast
  - NOR flash: Fast
  - RRAM, PRAM, MRAM: Good
  - DRAM, FRAM

- Read access time:
  - NAND flash
  - NOR flash
  - RRAM, PRAM, MRAM
  - DRAM, FRAM

- Scalability: Good
Memory Cell Structure

- MIM memory element built on a via
- Memory element connected with a select transistor
- Fully compatible with standard CMOS process

![Diagram of Memory Cell Structure]

Cu

Cu₂O

MIM memory element built on a via
Memory element connected with a select transistor
Fully compatible with standard CMOS process

Top electrode
Bottom electrode
Memory element
Gate
Drain
Source
Background – Trapping Model*

- OFF state mainly by space-charge-limited-conduction (SCLC) and Frenkel-Poole (FP)
- OFF → ON switch at trap-filled-limit voltage (VTFL)

Electrode Effect

OFF-state current leakage increases with reactivity between top electrode and Cu$_2$O (Ni /Co<Ti<Ta).

Free energy of formation

<table>
<thead>
<tr>
<th>Mo$_x$</th>
<th>$\Delta G_0$ (kcal/mole)</th>
</tr>
</thead>
<tbody>
<tr>
<td>CoO</td>
<td>-51</td>
</tr>
<tr>
<td>NiO</td>
<td>-51.7</td>
</tr>
<tr>
<td>TiO$_2$</td>
<td>-212</td>
</tr>
<tr>
<td>Ta$_2$O$_5$</td>
<td>-457</td>
</tr>
</tbody>
</table>
Switching Characteristics: Ni vs. Ti TE

Cells with Ni top electrode
- Erase with both polarity
- Higher erase current

Cells with Ti top electrode
- Reverse polarity field
- Low erase current

\[ V \]

\[ \text{Cu}_2\text{O} \]

\[ \text{Cu} \]

\[ V_g \]

\[ I \]

\[ \text{TE} \]

\begin{align*}
\text{Voltage (V)} & \quad -2 \quad -1 \quad 0 \quad 1 \quad 2 \quad 3 \\
\text{Current (A)} & \quad 2.0 \times 10^{-5} \quad 4.0 \times 10^{-5} \quad 6.0 \times 10^{-5} \quad 8.0 \times 10^{-5} \quad 1.0 \times 10^{-4} \quad 0.0 \times 10^{00}
\end{align*}

Erase
- \( \text{TE} = \text{Ni} \)
- \( \text{TE} = \text{Ti} \)

Program
- \( I_{\text{limit}} \)
ON/OFF Window

- Model predicts high ON/OFF ratio with deep-trap materials
- ON/OFF ratio of $10^5 - 10^6$ observed

![Graph of Current vs. Voltage](image)

**Cumulative Probability**

- 2% OFF
- 16% OFF
- 50% OFF
- 84% OFF
- 98% OFF

**Current read at 0.5V**

**Current (µA)**

- 0.005
- 0.01
- 0.05
- 0.1
- 0.5
- 1
- 5
- 10

**Tester resolution**
Retention

- Long retention predicted with deep-trap materials
- Retention related to program current

90°C 30 hrs retention

25°C 50 hrs retention

Cycling

- Program with 100 ns pulses
- 0.5uA – 5uA window for cycling

10:1 operation window

Read current (uA)

Cycle
## Electrical Characteristics Summary

<table>
<thead>
<tr>
<th>Characteristics</th>
<th>Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>Programming V/I</td>
<td>(2-5 V) / (~ 50 uA)</td>
</tr>
<tr>
<td>Speed</td>
<td>( \leq 100 \text{ ns} )</td>
</tr>
<tr>
<td>Erasing V</td>
<td>1-2 V</td>
</tr>
<tr>
<td>Speed</td>
<td>( \leq 100 \text{ ns} )</td>
</tr>
<tr>
<td>Retention</td>
<td>30 hours at 90°C tested</td>
</tr>
<tr>
<td>Cycling</td>
<td>&gt; 600 cycles tested</td>
</tr>
<tr>
<td>Read disturb</td>
<td>Zero up to 25 hours at ( V &lt; 0.5 \text{V} )</td>
</tr>
<tr>
<td>Cell size</td>
<td>0.18 um</td>
</tr>
</tbody>
</table>

A. Chen et. Al, *IEDM 2005*
BEOL Thin Film Challenges for RCM

- Thin ~100A metal oxide films
- Hard to etch (process) metal films
  - Interfaces in metal-oxide-metal cell
- Highly planar CMP
  - Maintain electric field uniformity across cell

- Phase Change RCM
  - Ternary materials plus dopant
  - Encapsulation
Erase Mechanism for Copper Oxide Resistive Switching Memory Cells with Nickel Electrode

Advanced Memory Group
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