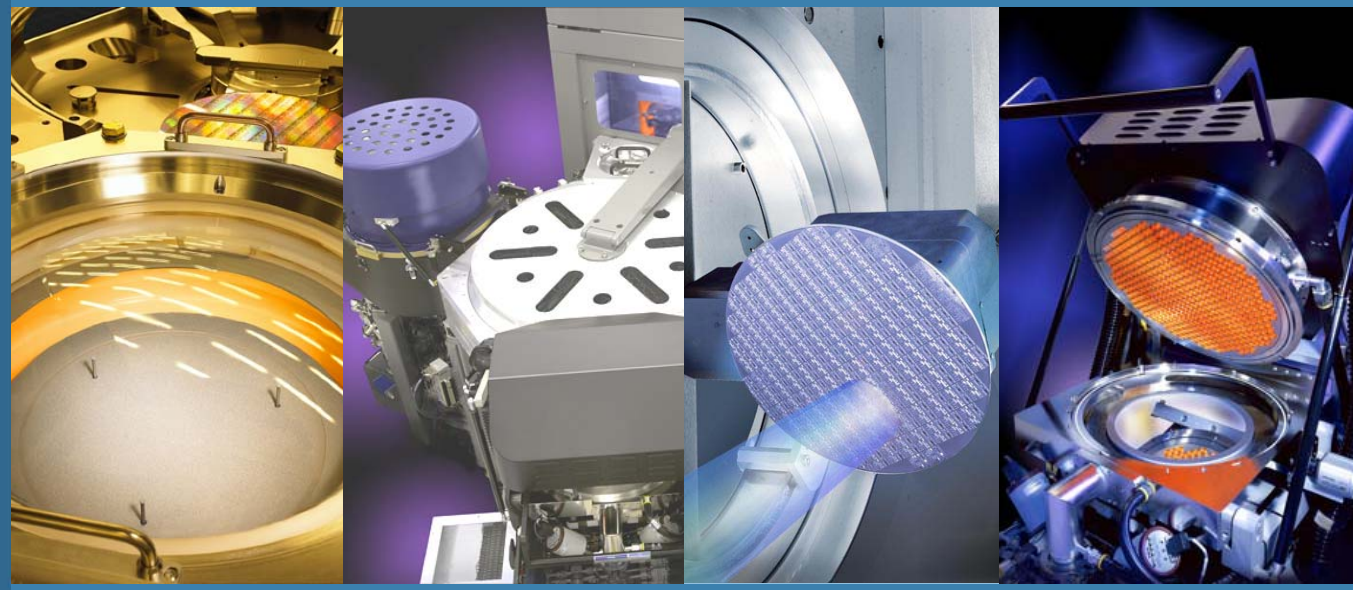


Gate Stack Scaling, Challenges and Approaches in Meeting Technology Requirements

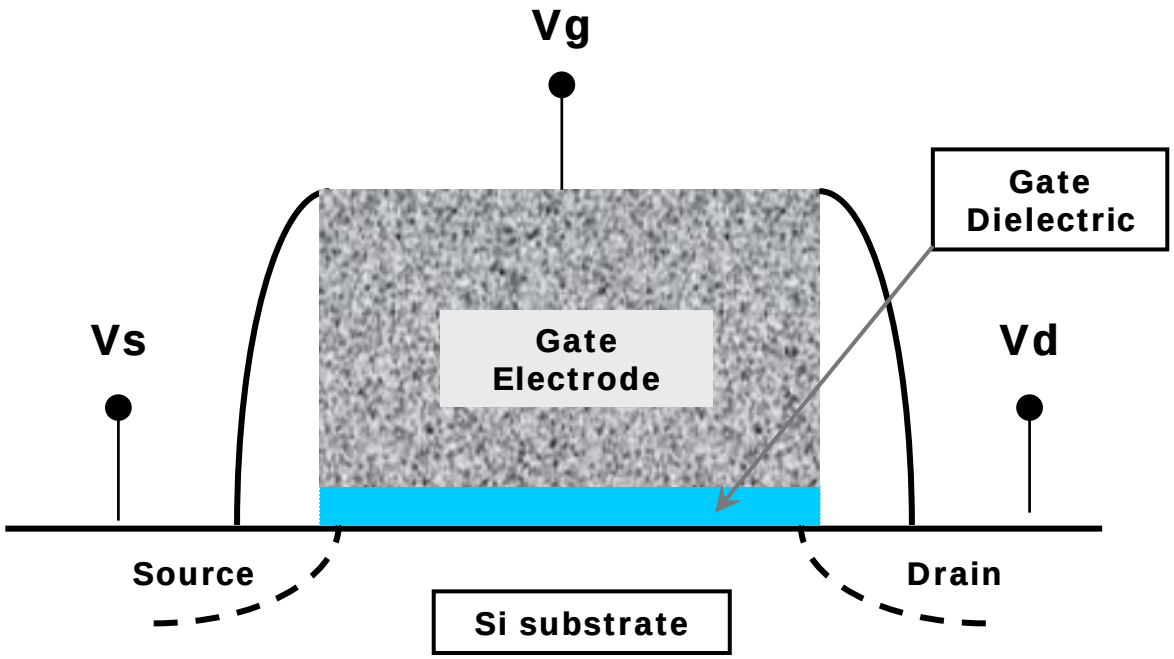
Yi Ma
Applied Materials
Santa Clara
Apr. 26th, 06

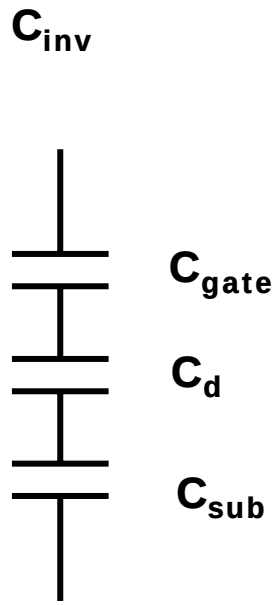
TFUG Seminar

Outline

- Introduction
- Oxynitride
- Hi-K gate dielectric material and processing
- Hi-K gate dielectric electrical performance issues
- Poly depletion reduction
- Metal gate approaches
- Summary

Gate stack scaling





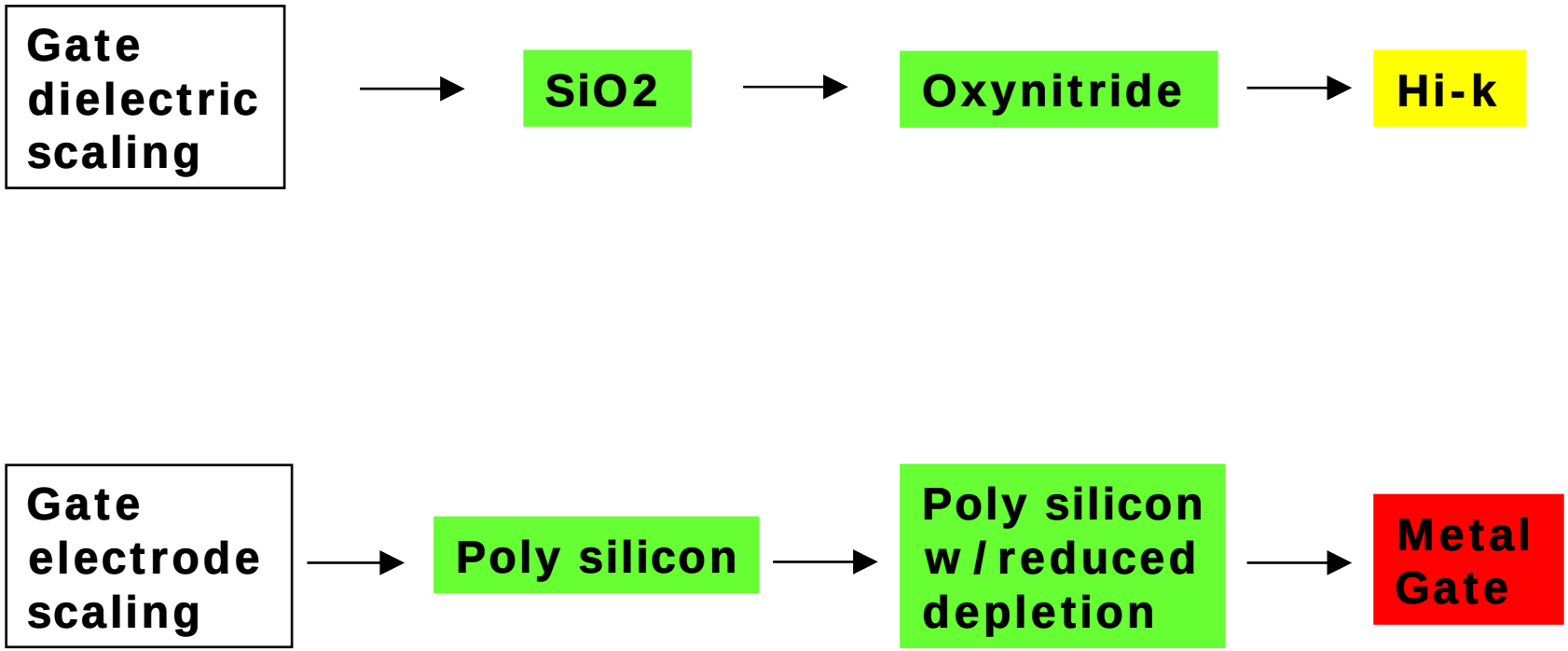
Gate stack scaling includes both dielectric scaling and electrode scaling

ITRS Roadmap for High Performance Devices

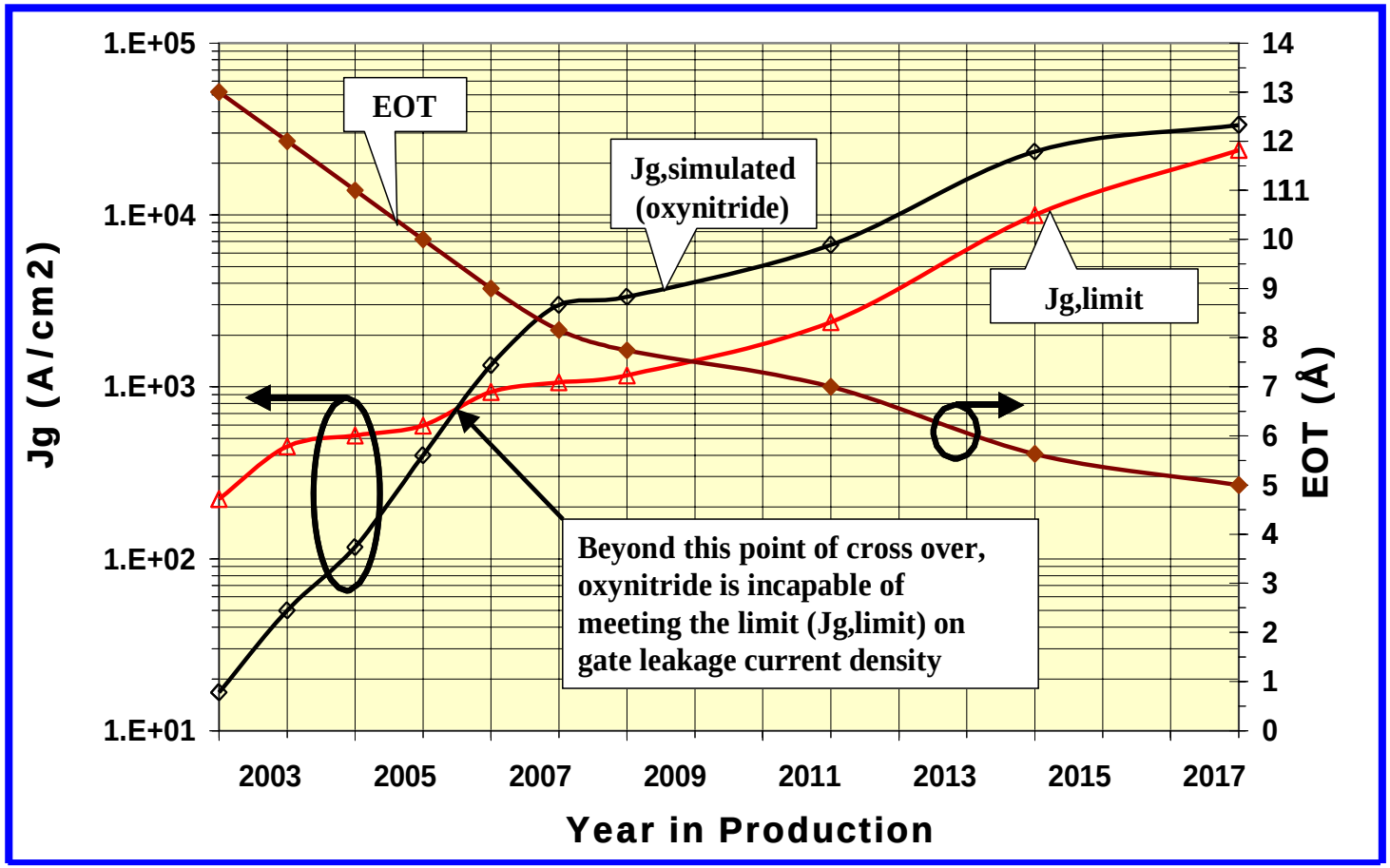
ITRS Roadmap	130 nm	90 nm	65 nm	45 nm
Tox,inv (Å)	23	21	17	12
EOT (Å)	15	13	10	8
Poly depletion + QM (Å)	**8**	**8**	**7**	**4**
Gate Leakage (A/cm2)	15	100	300	2000
Nominal power supply voltage (V)	1.2	1.2	1.1	1
Physical Thickness Control (% 3σ)	<4	<4	<4	<4

Due to the aggressive technology evolution, down scaling gate dielectric only is not enough to meet device performance

Gate Stack Scaling Paths

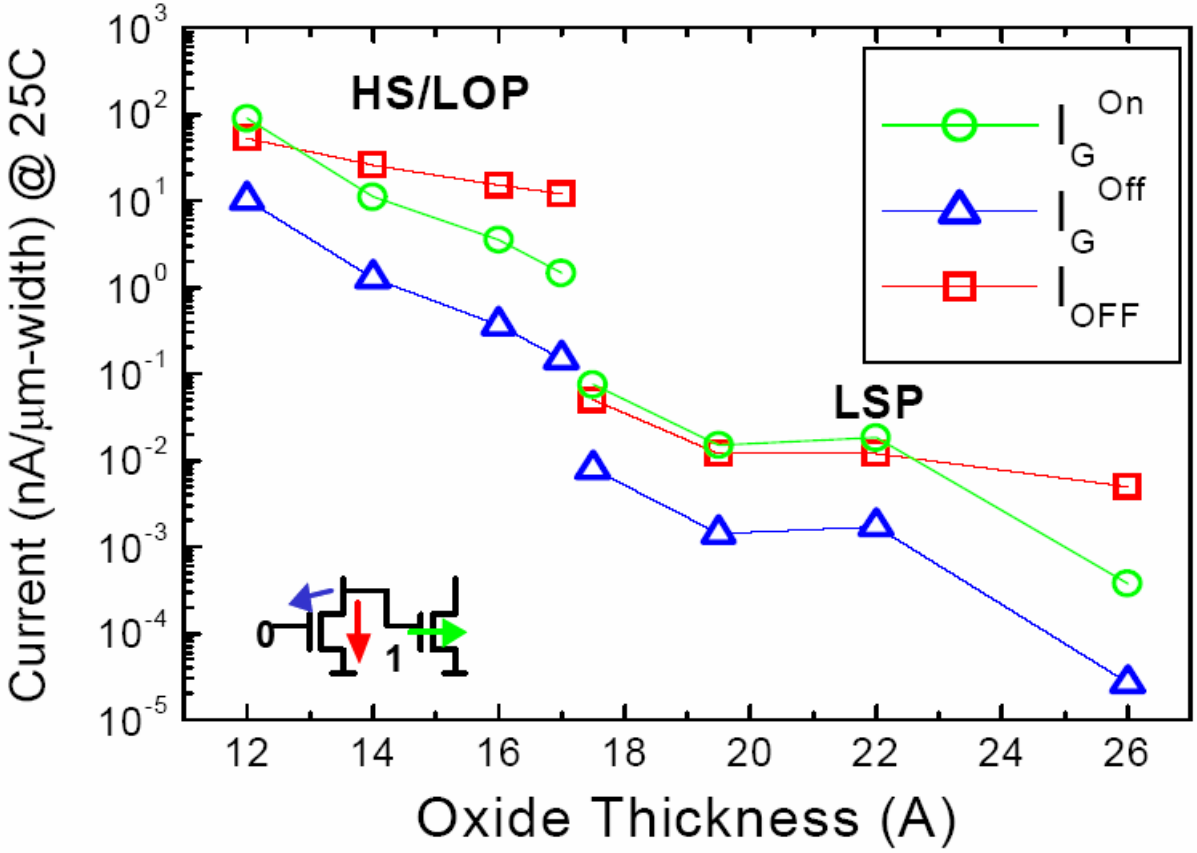


What happens when gate dielectric is scaled



Gate leakage has become too high due to aggressive gate dielectric thickness scaling

Major Leakage Components



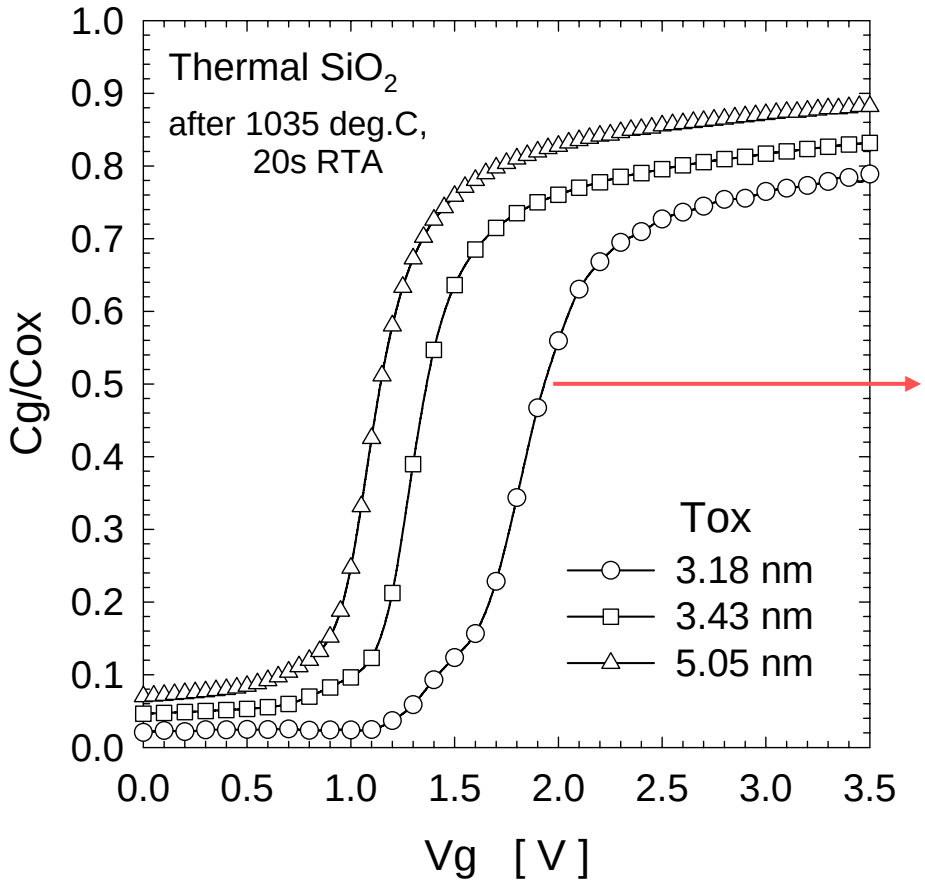
There is significant Leakage even while devices are off

C. Diaz, IEDM 2003

Consequences of the leakages

- **Larger power consumption $P_{leak} = Vdd * I_{leak}$**
  - Cost money
  - Shorter battery life for mobile products
- **Accelerated device degradation**
  - Interfacial defect formation
  - Charge trapping
  - Leakage increases
  - Vt shift
  - Lower drive current (Lower carrier mobility)
  - Shorter device lifetime

Another problem with thinner SiO2



V_{FB} shift due to B penetration

Boron penetration

Data courtesy of Toshiba

Thicker dielectric for gate leakage reduction

$$J_G = b \bullet \exp(-a \bullet f \bullet T_d^{ph})$$

$$T_d^{ph} \uparrow \Rightarrow J_G \downarrow$$

Thinner Dielectric for Performance Enhancement

$$C_d = \frac{\delta Q}{\delta V} = \frac{A}{T_d^{ph}} \times \varepsilon_d \varepsilon_o$$

$$T_d^{ph} \uparrow \Rightarrow C_d \downarrow \qquad \varepsilon_d \uparrow \Rightarrow C_d \uparrow$$

$$\frac{\varepsilon_{hi-k}}{T_{hi-k}^{ph}} >> \frac{3.9}{T_{SiO2}^{ph}}$$

The goal of scaling is to find a material that behaves physically thicker and electrically thinner

Dielectric constant of typical materials

- The dielectric constant is the ratio of the permittivity of a substance to the permittivity of free space. It is an expression of the extent to which a material concentrates electric flux.
- Dielectric constant of a few typical materials:

Air: 1

SiO_2: 3.9

Si_3N_4: 7.8

Al_2O_3: 10

HfO_2: 25

HfSiON: 10-20

ZrO_2: 25

Ta_2O_5: 26

Oxynitride

How to stop boron and reduce gate leakage

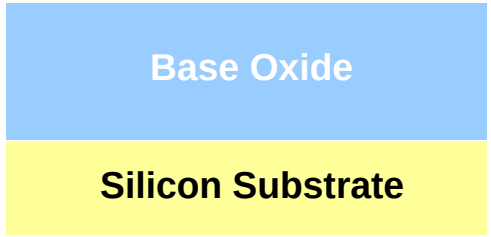
- Nitrogen incorporation

Two major techniques

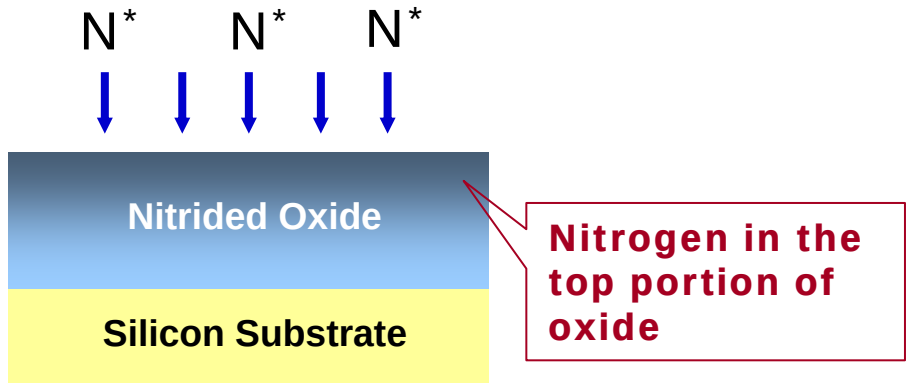
- Plasma Nitridation
  - Expose thermally grown oxide to nitrogen plasma.
- Conventional thermal nitridation
  - Anneal oxide in NO, N2O or NH3.
  - Grow oxide in NO, N2O or mixture of NO, N2O, NH3 with O2.

Nitrogen Incorporation Processes – Plasma Nitridation

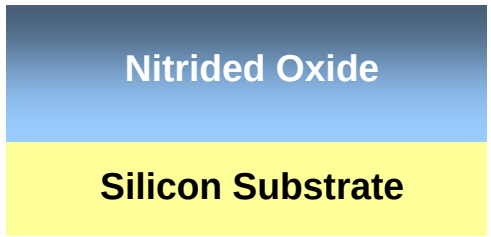
1. Base oxide growth with ISSG or RTO



2. Plasma nitridation (DPN), leaving nitrogen in the top portion of base oxide

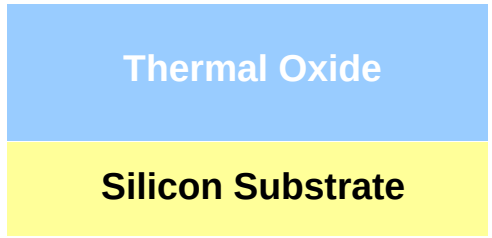


3. Post nitridation anneal (PNA) for interfacial and bulk oxide improvement

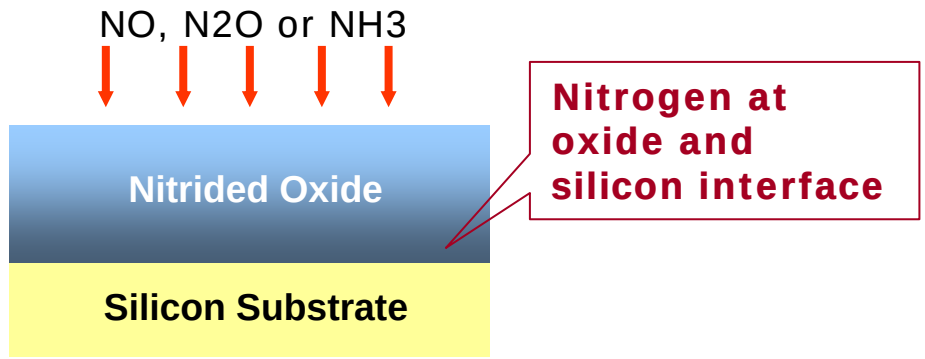


Nitrogen Incorporation Processes – Thermal Nitridation

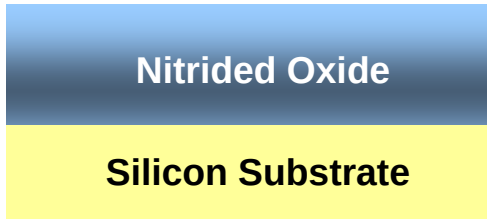
1. Thermal oxide growth



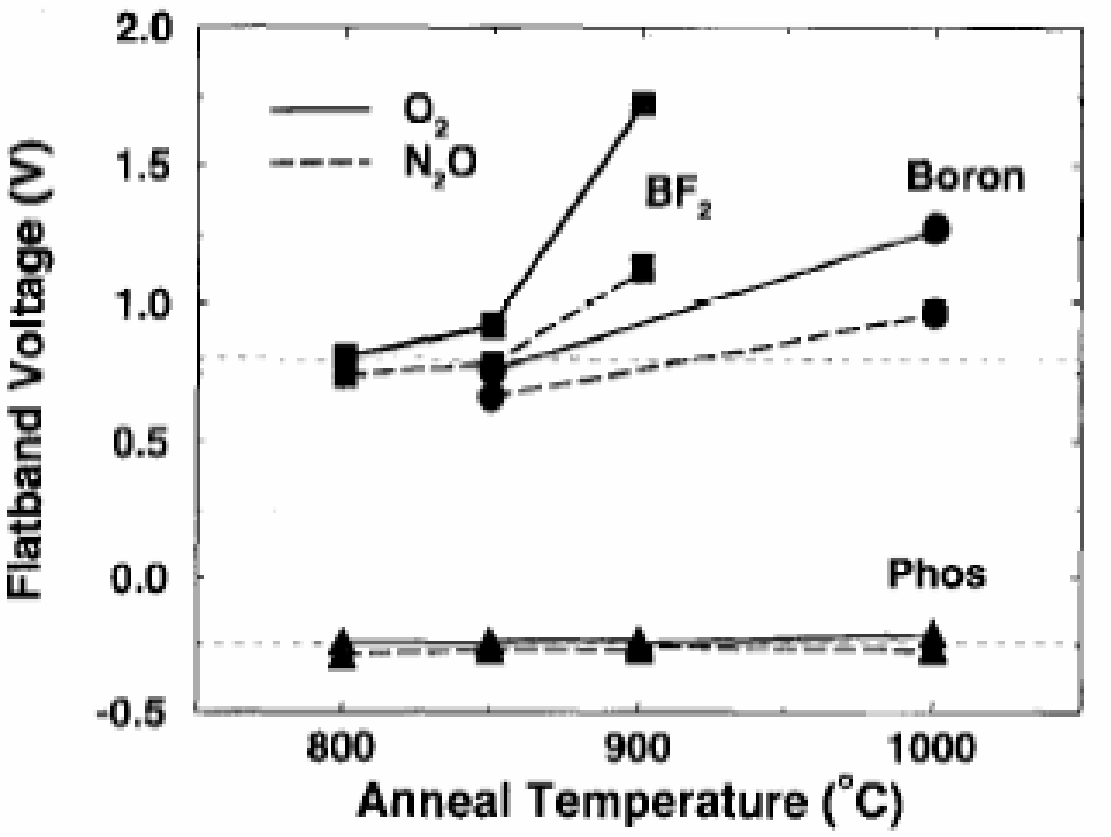
2. Anneal in NO, N2O or NH3 gas, leaving nitrogen at near oxide and silicon interface



3. Re-oxidation to move nitrogen away from oxide-silicon interface



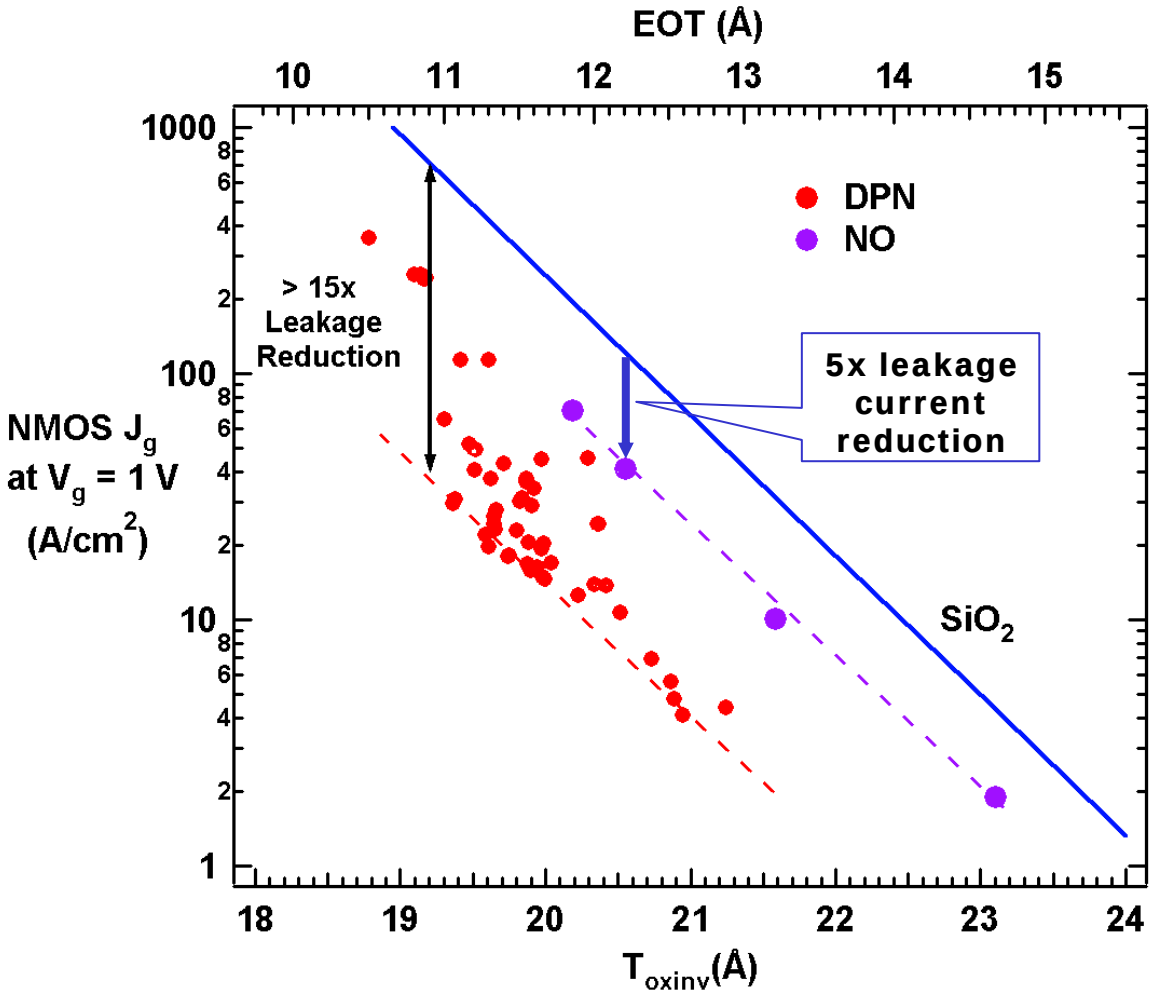
Boron penetration



Nitrogen incorporation in oxide can effectively suppress boron penetration

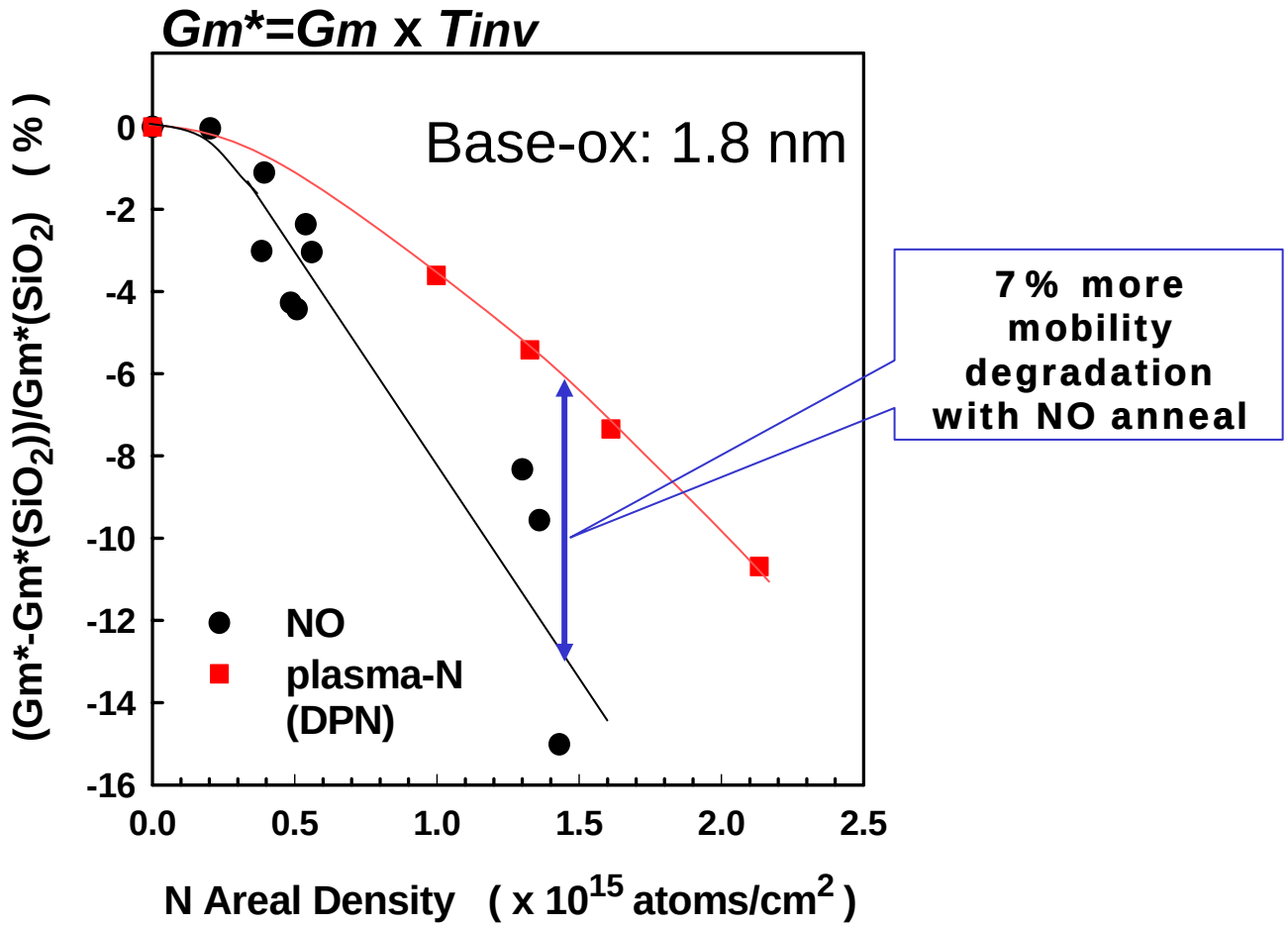
K.S.Krisch et al, Trans. ED-43, p982 (1996)

Gate Leakage Current Reduction



DPN process is more effective in leakage current reduction

Channel Mobility



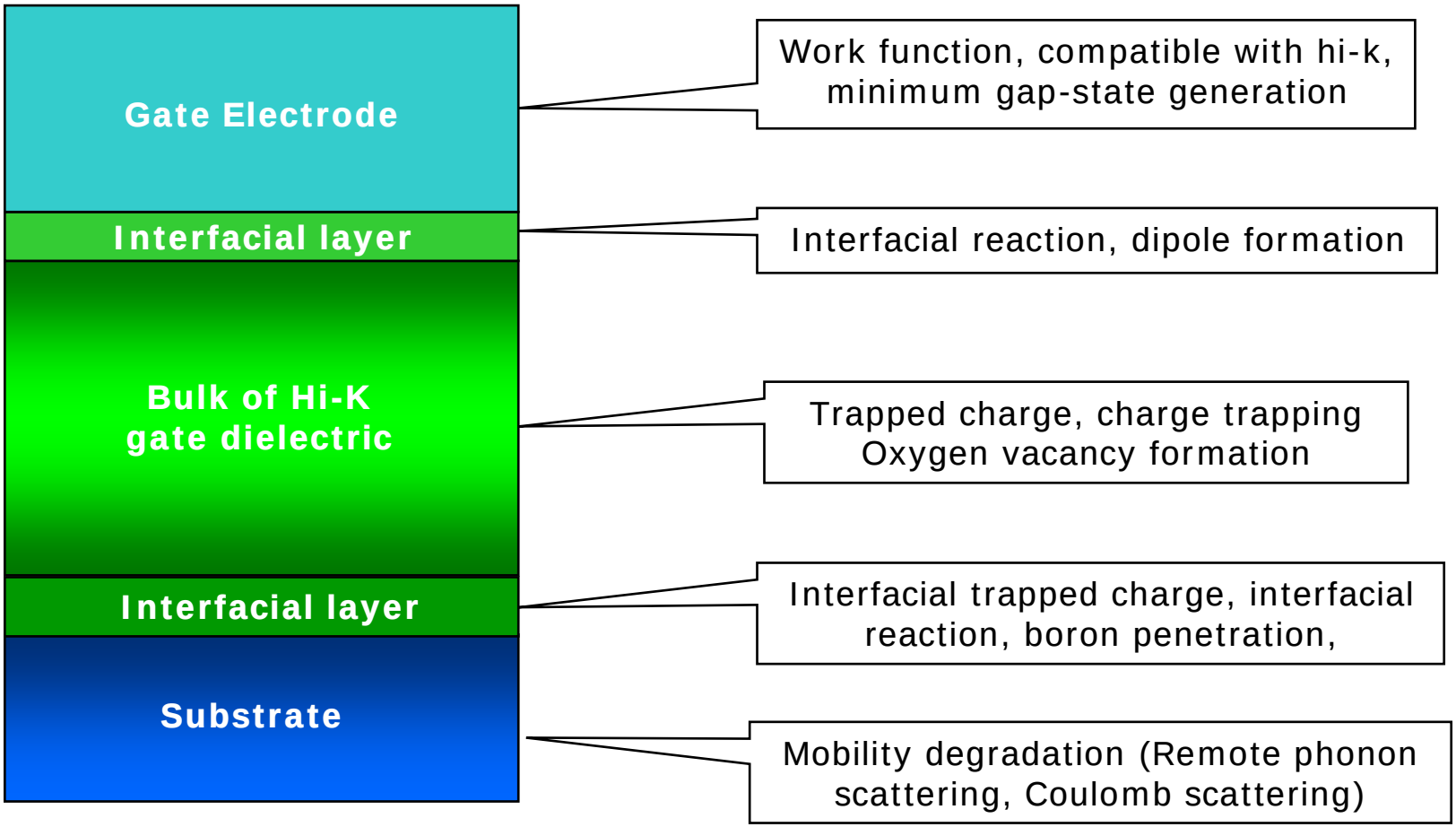
More channel mobility degradation was observed with NO anneal process due to nitrogen at oxide and silicon interface

Data courtesy of Toshiba

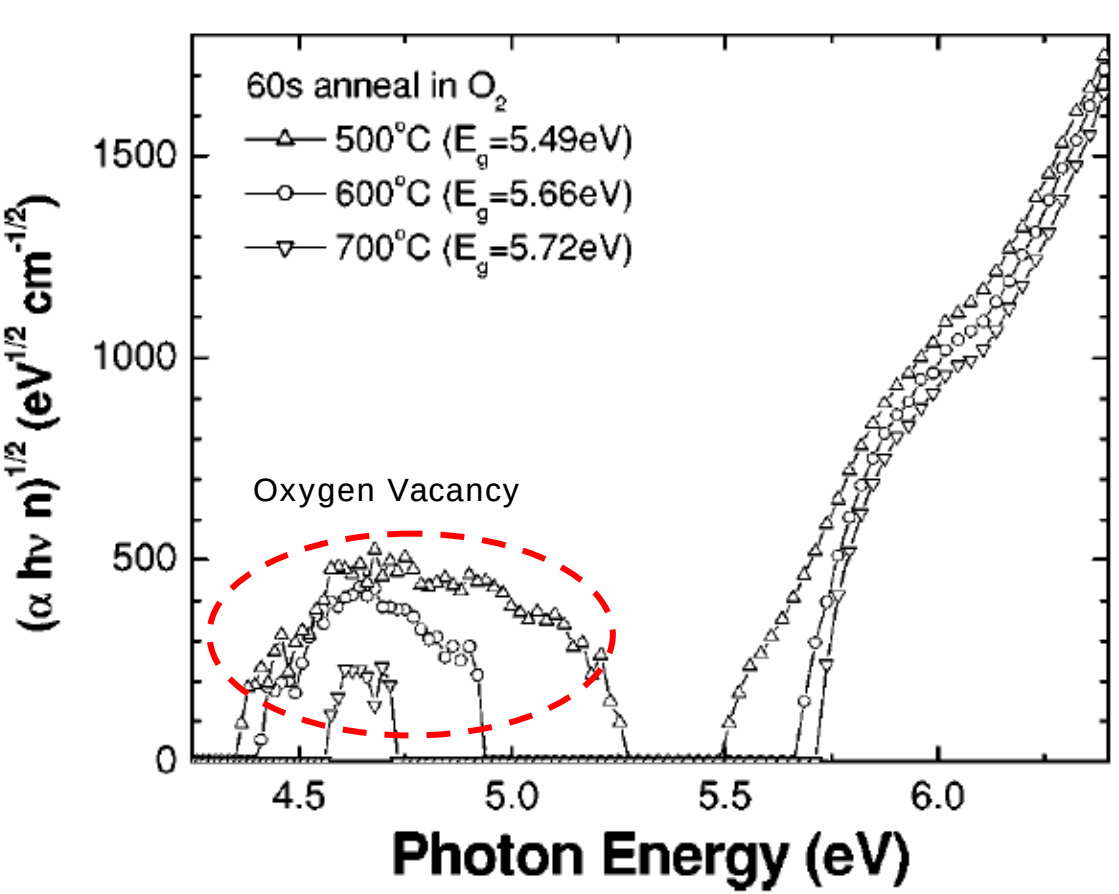
Hi-k Gate Dielectric Material and Processing

NCCAVS TFUG meeting Apr. 26, 2006

A detailed view of a completely new “M-I-S” system



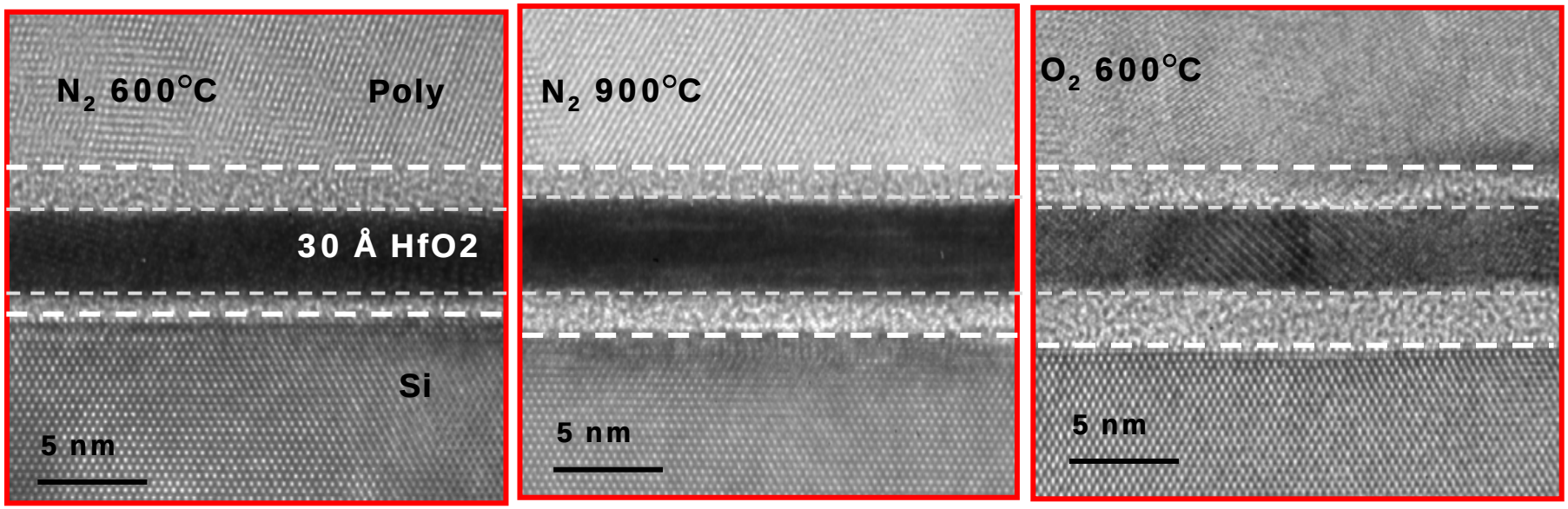
Oxygen Vacancy – Spectroscopic Ellipsometry



Post deposition anneal is needed for oxygen vacancy reduction

Takeuchi et al. JVST 2004

Interfacial reaction



Bottom IL 7Å
EOT 17.5Å

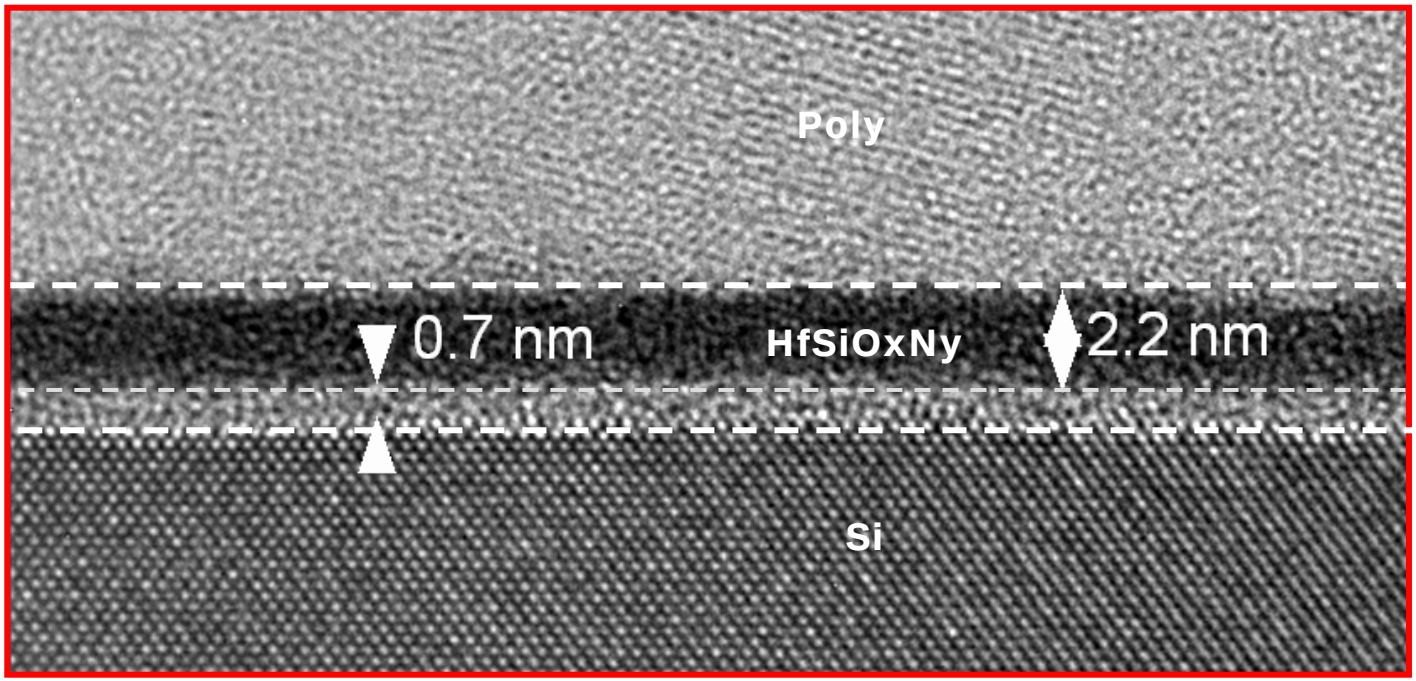
Bottom IL 11Å
EOT 21.5Å

Bottom IL 18Å
EOT 27.3Å

Interfacial layer growth is a potentially limiting factor to dielectric scaling

Interfacial reaction suppression

- Plasma Nitridation

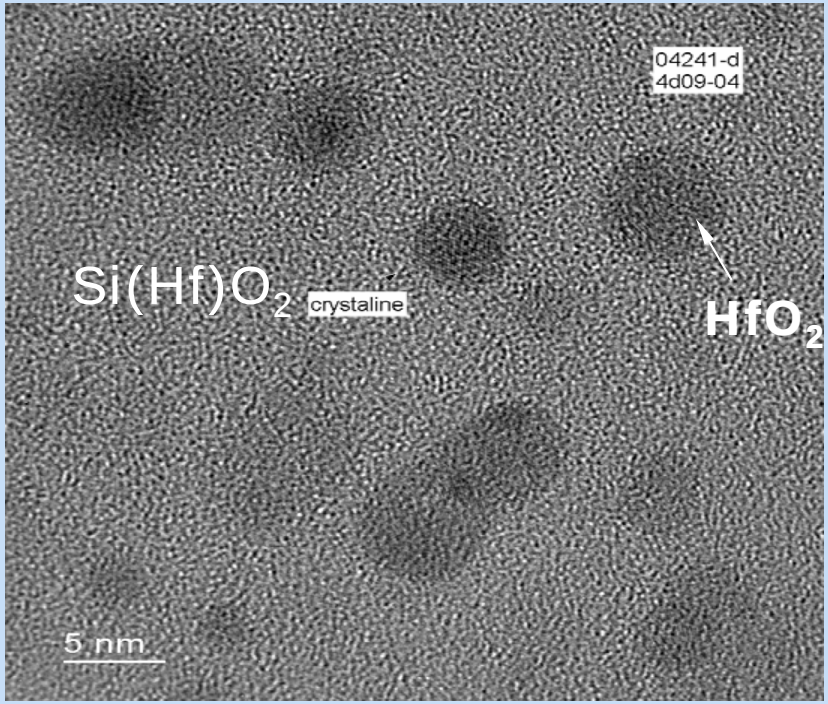


T = 650°C, EOT = 11Å
$t_{PHYS,TEM}$ IL = 7Å
$t_{PHYS,TEM}$ HfSiOxNy = 22Å

Plasma nitridation is an efficient approach to suppress interfacial layer growth

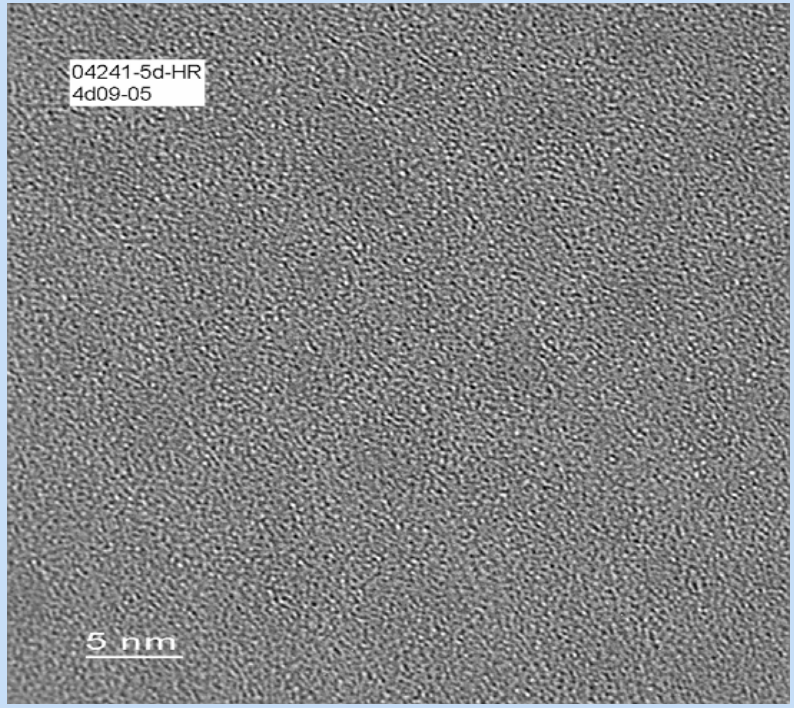
Thermal Stability of ALD HfSiOx at 1050°C

Without DPN Nitridation
HfSiOx after 1050°C, 15 sec RTA



Phase segregation occurs without DPN nitridation

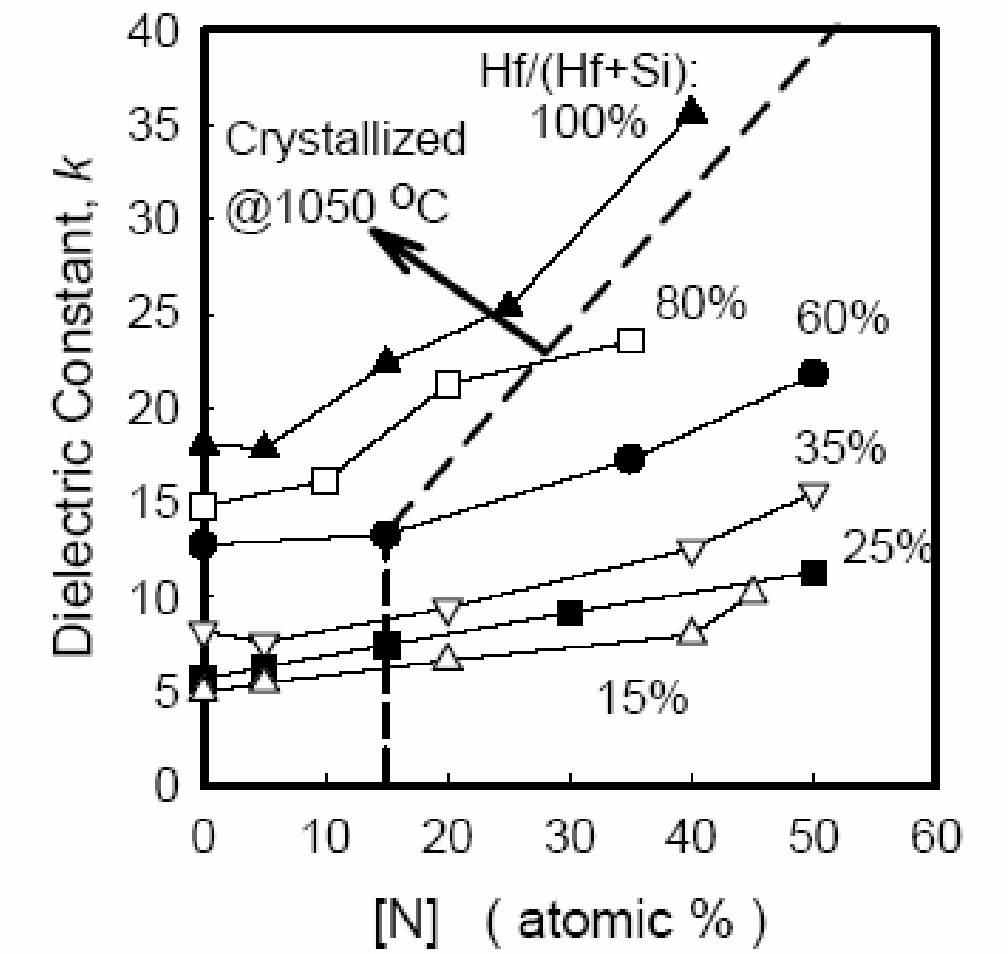
With DPN Nitridation
HfSiON after 1050°C, 30 sec RTA



Film stable up to 1050°C, 30 sec with DPN nitridation

Thermally stable ALD HfSiOx film can be formed by incorporating nitrogen with plasma nitridation technique

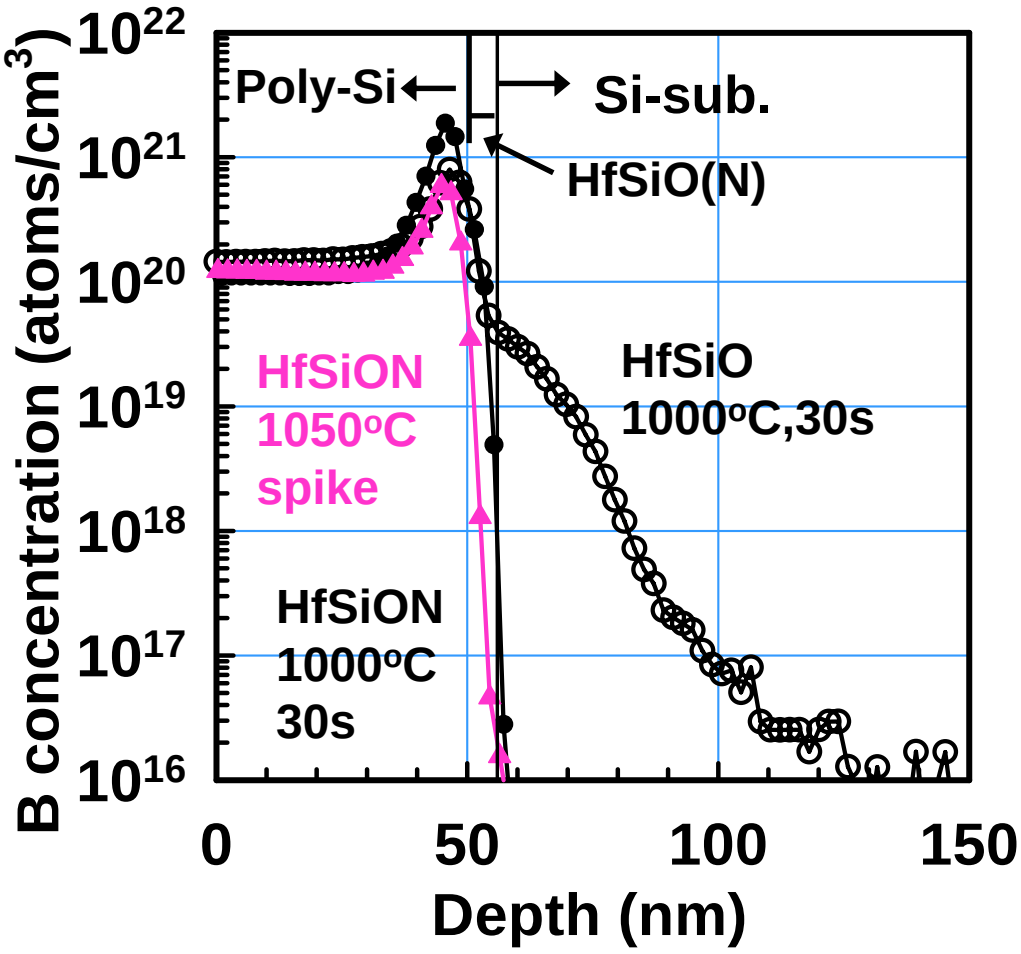
Dielectric constant and phase stability



K value and phase stability are dependent on Hf and nitrogen concentration

M.Takayagani et al, IEDM 2005

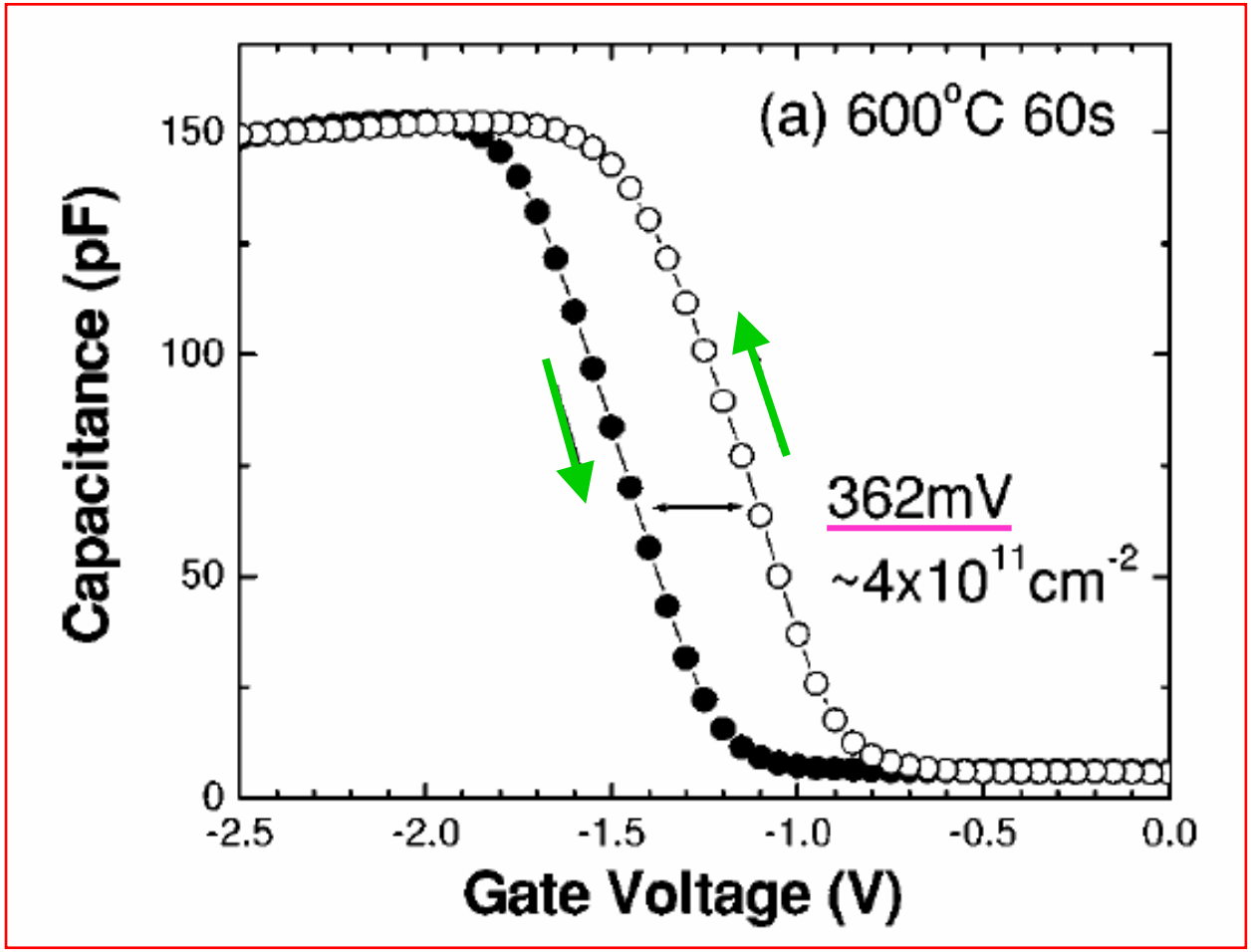
Boron penetration evaluation



Nitrogen is needed in high-k film for suppressing boron penetration

T. Watanabe et al. VLSI Symp. 2003

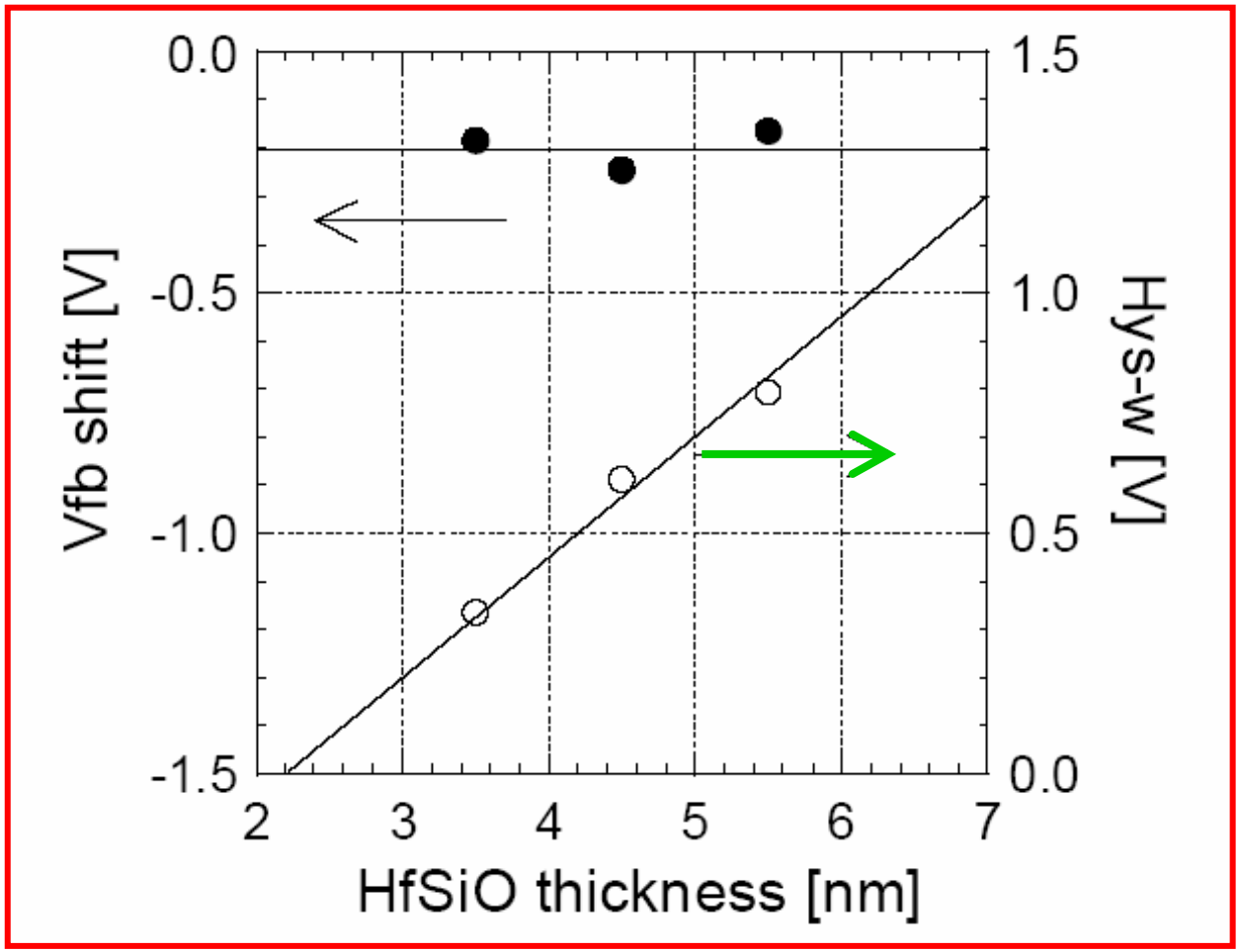
Trapped Charges in Hi-K films



High trapped charge density in hi-k film needs to be reduced with post deposition anneal

Takeuchi et al. JVST 2004

Trapped Charge - Thickness dependent



As a disadvantage of thicker dielectric film, more trapped charges

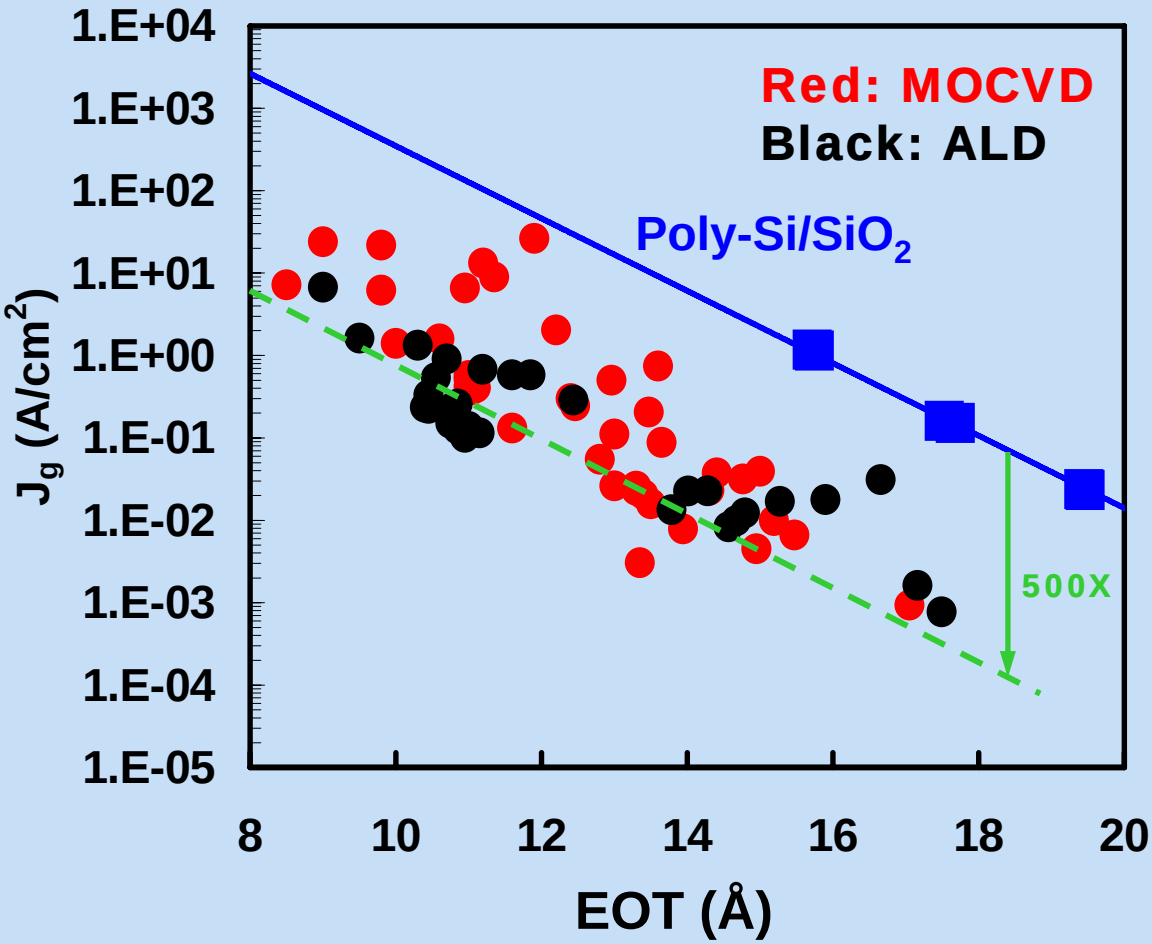
A. Morioka et al., VLSI 2003

Hi-k Gate Dielectric Electrical Performance

Requirements for High-k Gate Dielectrics

- More than 500x gate leakage reduction
- Compatibility to conventional CMOS process
  - material stable up to 1050°C – S/D activation temperature
  - interfacial properties with silicon channel and gate electrode
  - robustness to Boron penetration
  - V_{th} control
- Effective-mobility is larger than 90% of SiO_2
- Sufficient long-term reliability
  - Charge trapping (more severe for thicker film)
- Scalability

High-k $HfSiO_x$ with Polysilicon Gate

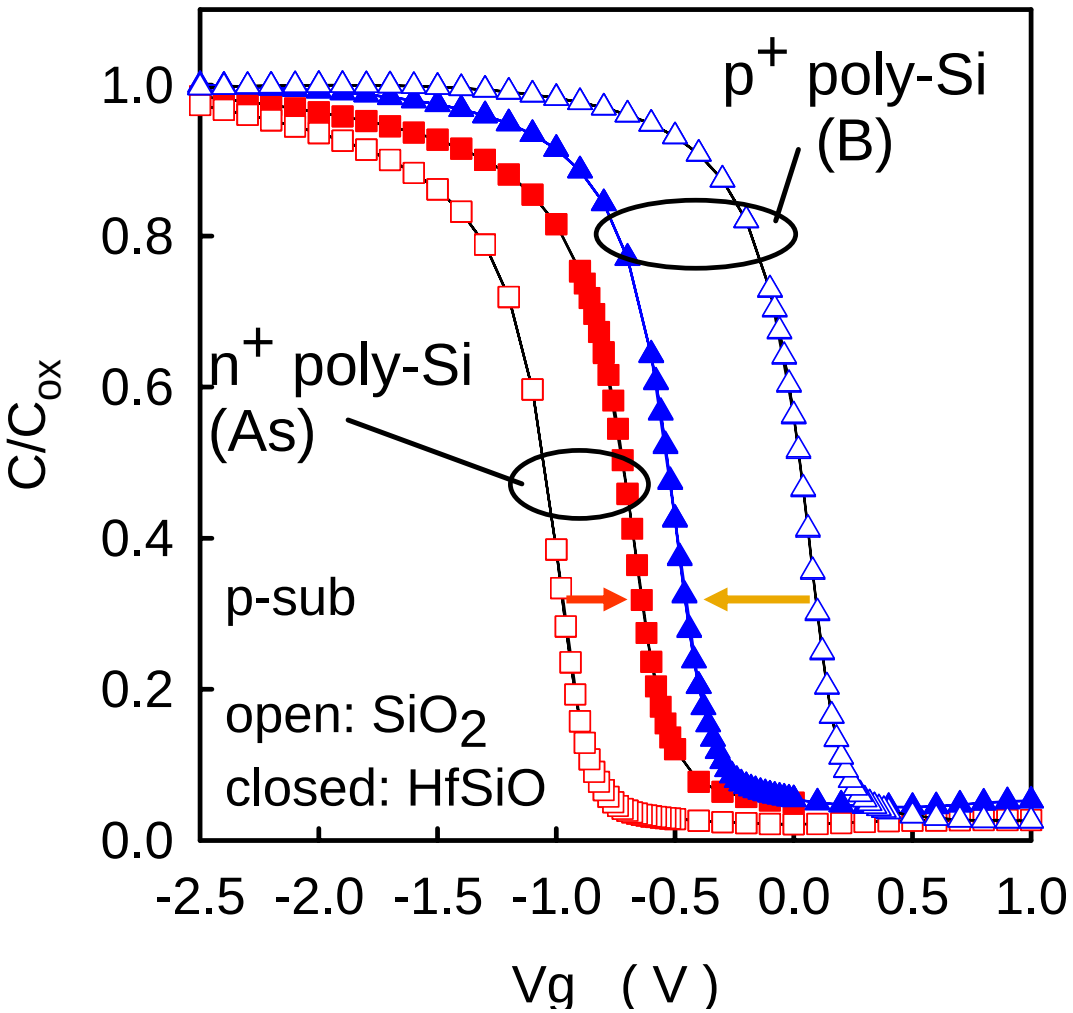


Electrical Results Highlight:

- <1.0nm EOT
- >500 times leakage reduction
- Stable film up to 1050°C, 30 sec RTA

Gate leakage reduction of >500x can be achieved with MOCVD and ALD technologies

High PMOS Flatband Voltage



- ΔV_{FB} of P-sub. MOS-CAP is

n$^+$ poly-Si: ~+200mV

p$^+$ poly-Si: ~-600mV

- Difficult to adopt to HP application without solving this problem.
- Channel implantation for V_{th} adjustment is very difficult.

A. Kaneko et al., SSDM 2003

Mobility Concerns

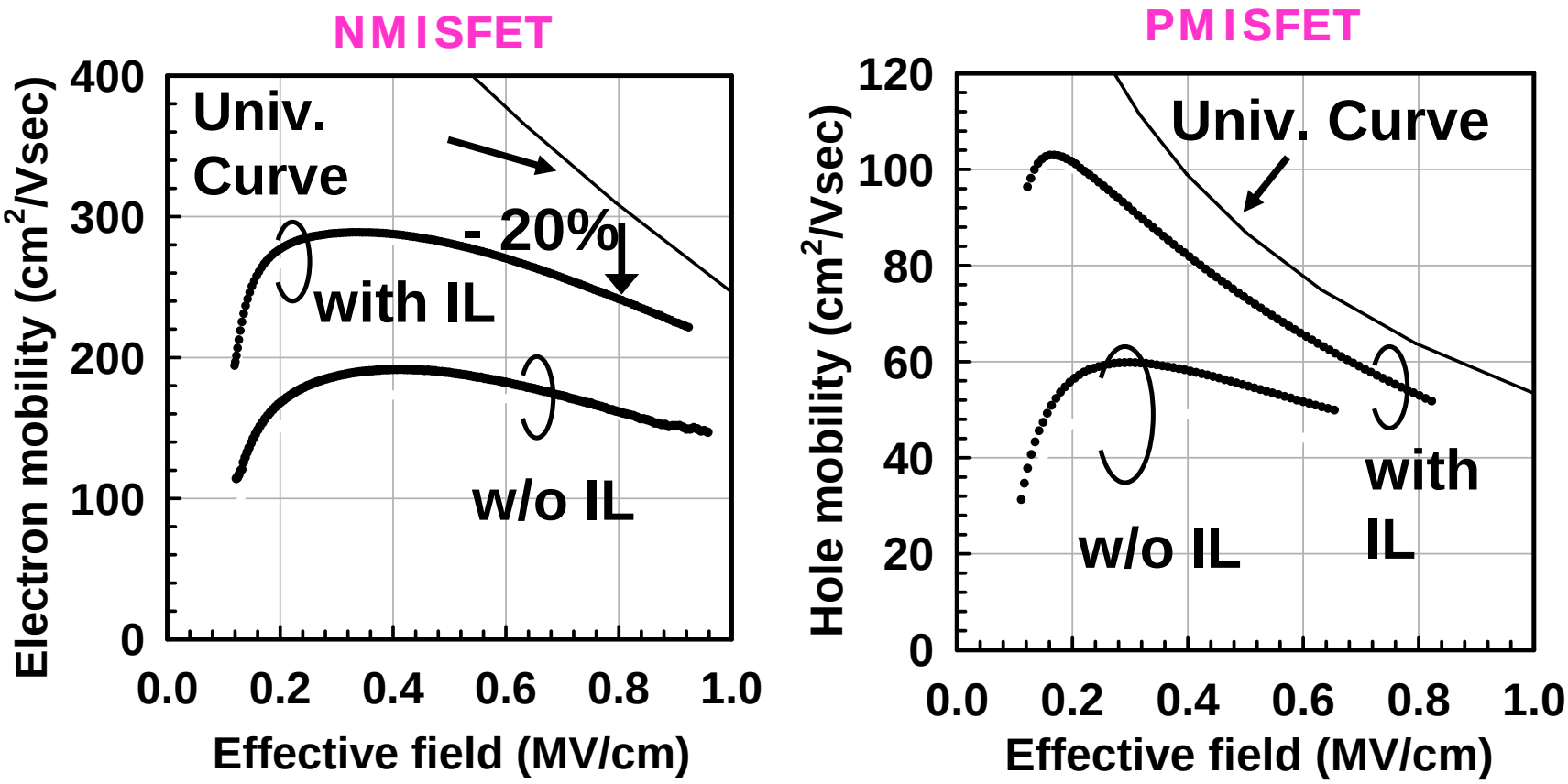
$$\frac{1}{\mu_{eff}} = \frac{1}{\mu_{coul}} + \frac{1}{\mu_{ph}} + \frac{1}{\mu_{sr}}$$

μ_{coul} : Coulomb scattering

μ_{ph} : Phonon scattering

μ_{sr} : Surface roughness

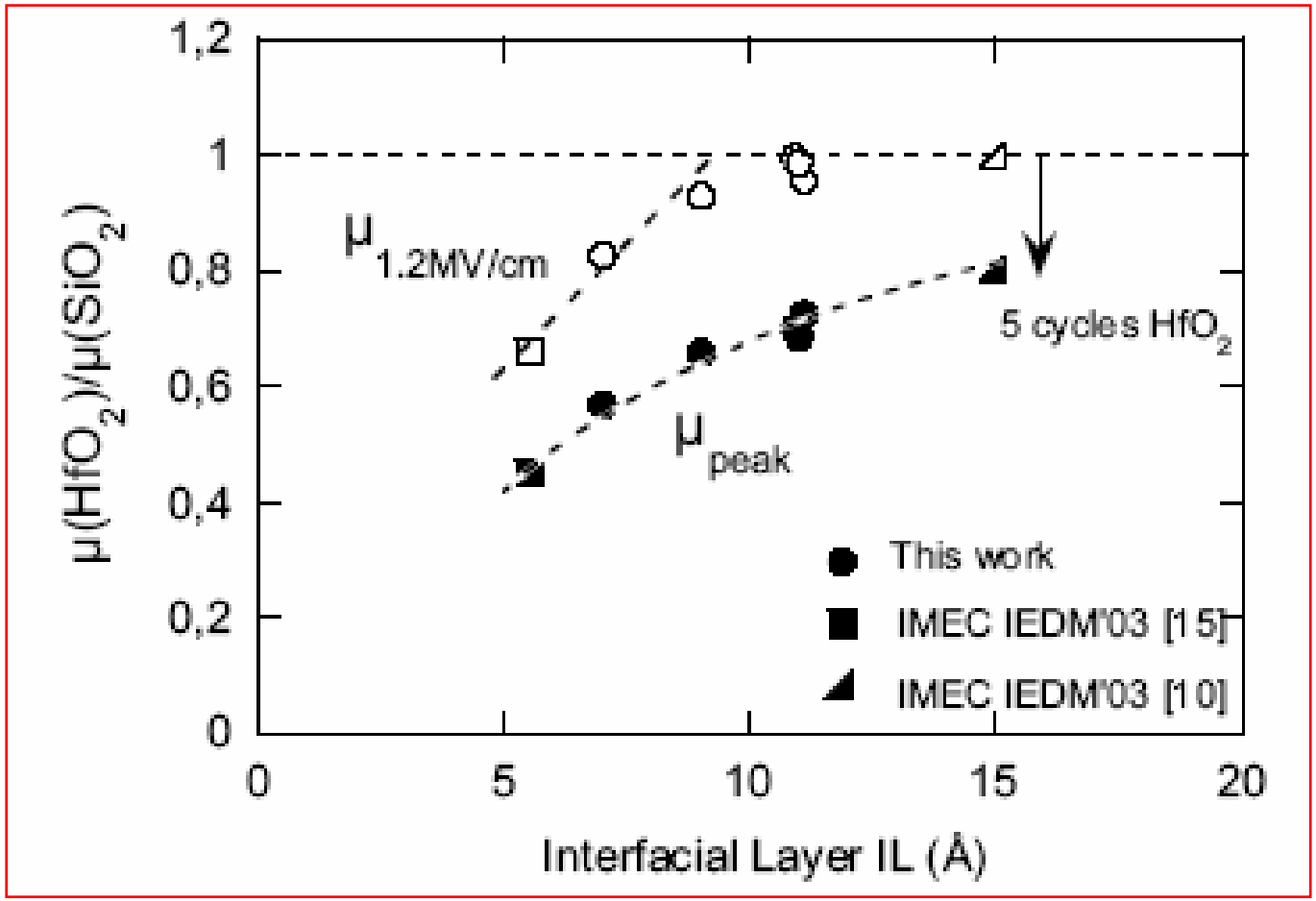
Mobility – Impact of Interfacial Layer



Mobility improvement with interfacial layer may be due to reduction of roughness and phonon scattering

T. Watanabe et al. VLSI Symp. 2003

Phonon Scattering Reduction

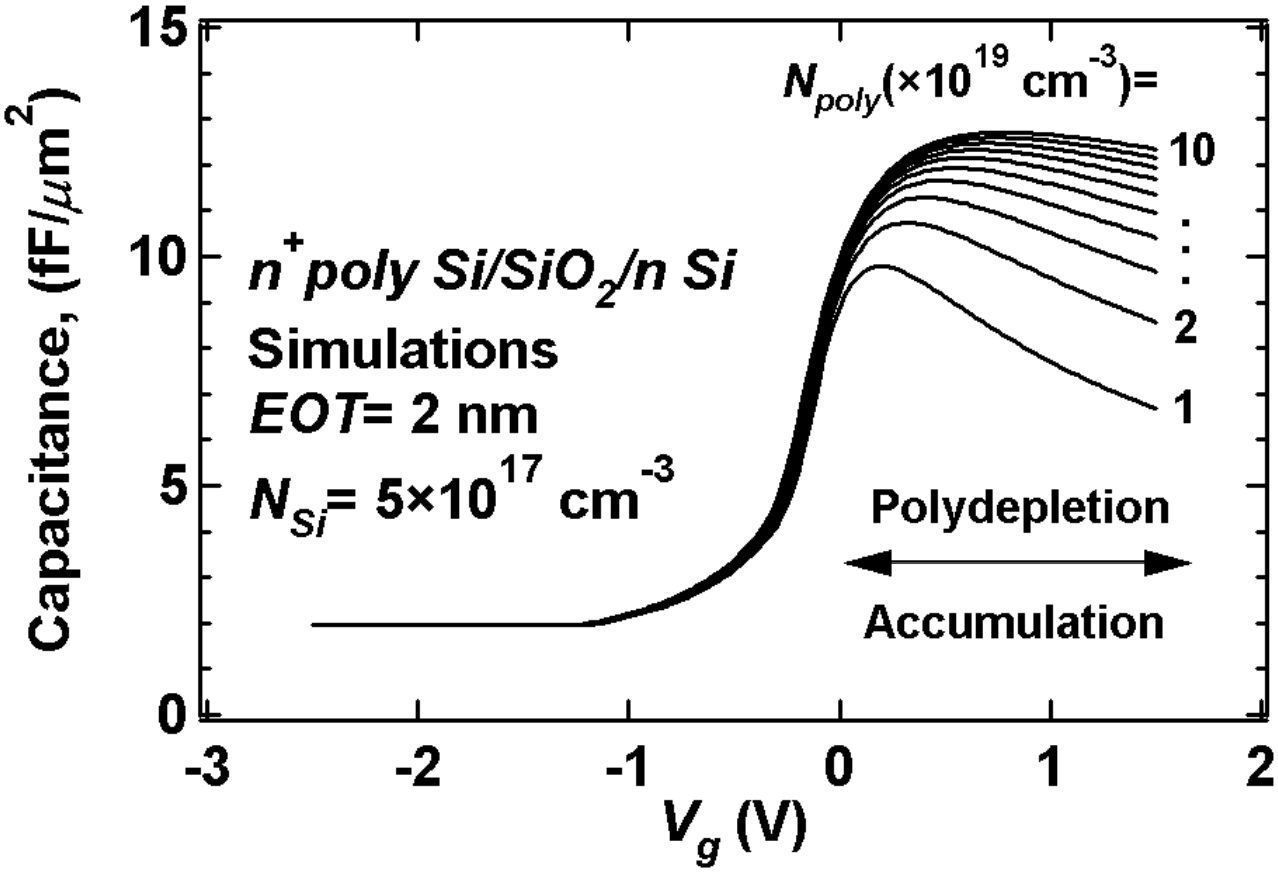


Mobility can be improved with thicker interfacial SiO2 layer. However, EOT scaling is compromised.

O. Webber et al., Proceeding of ESSDERC, Gronoble, France, 2005

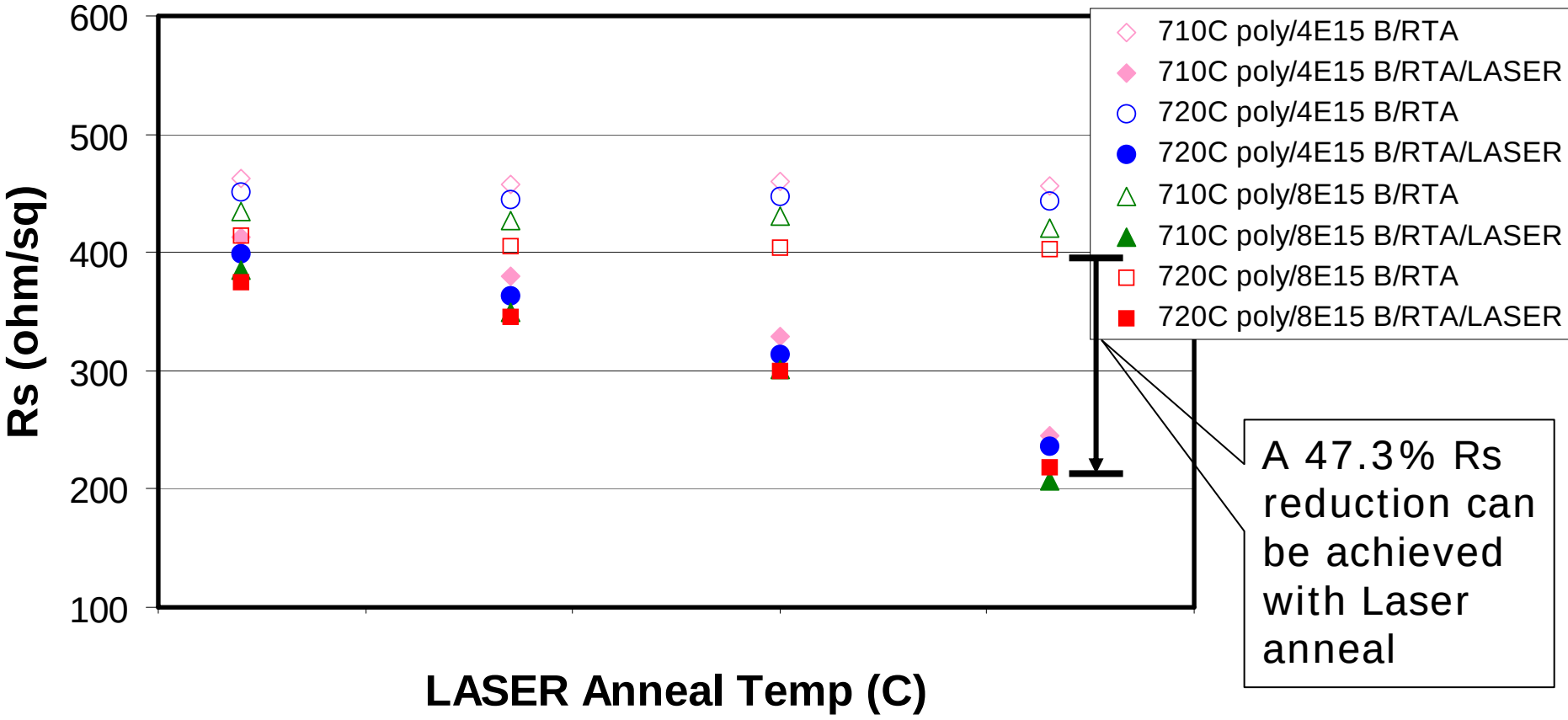
Poly Depletion Reduction

Poly depletion vs poly carrier concentration



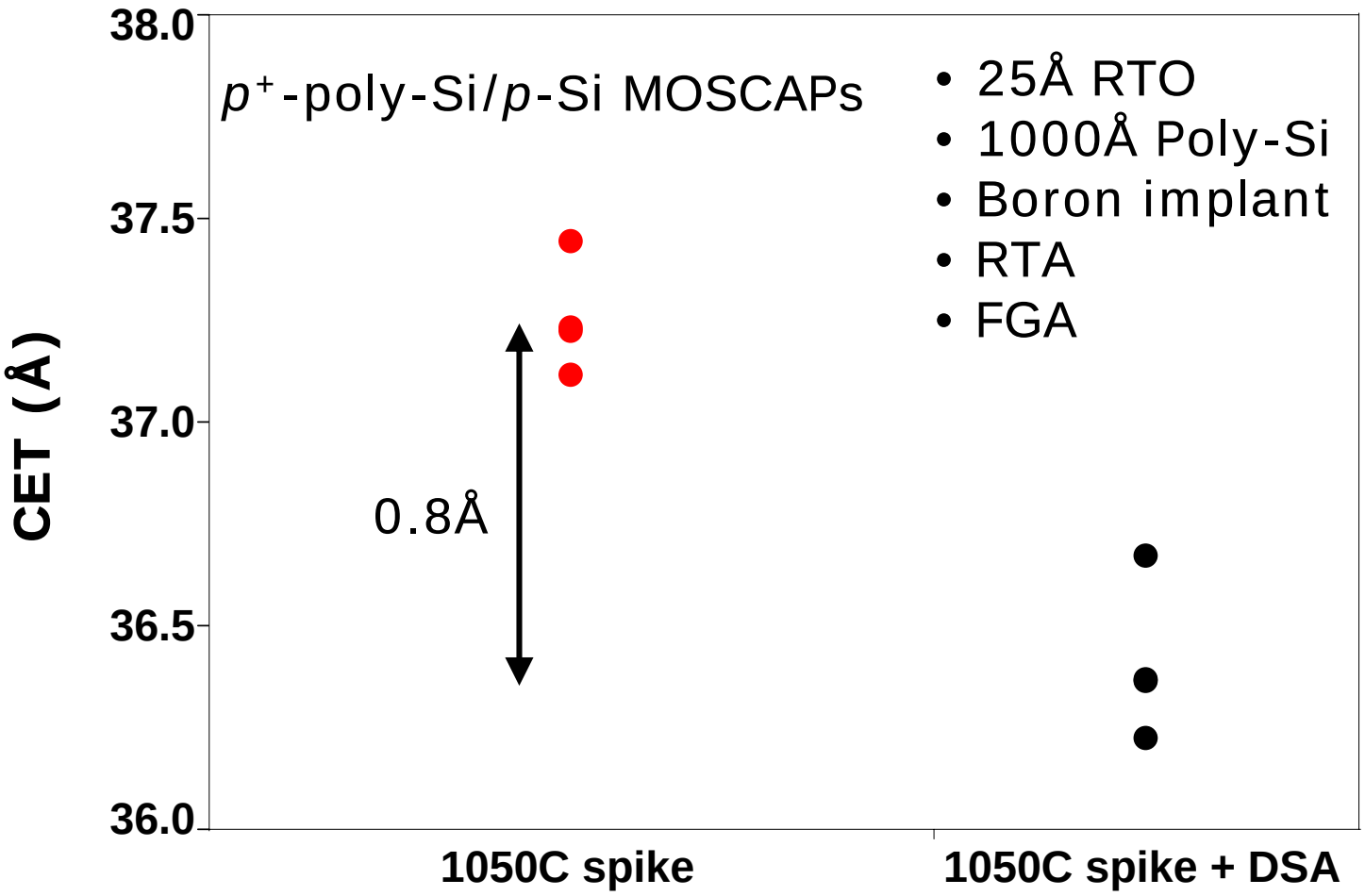
More poly depletion with lower carrier concentration

Laser Annealing for Higher Carrier Concentration



Laser anneal temperature has significant impact in Rs reduction

Improved Poly-Si Depletion with DSA



A poly depletion reduction of 0.8Å can be achieved with Laser annealing.

Metal Gate

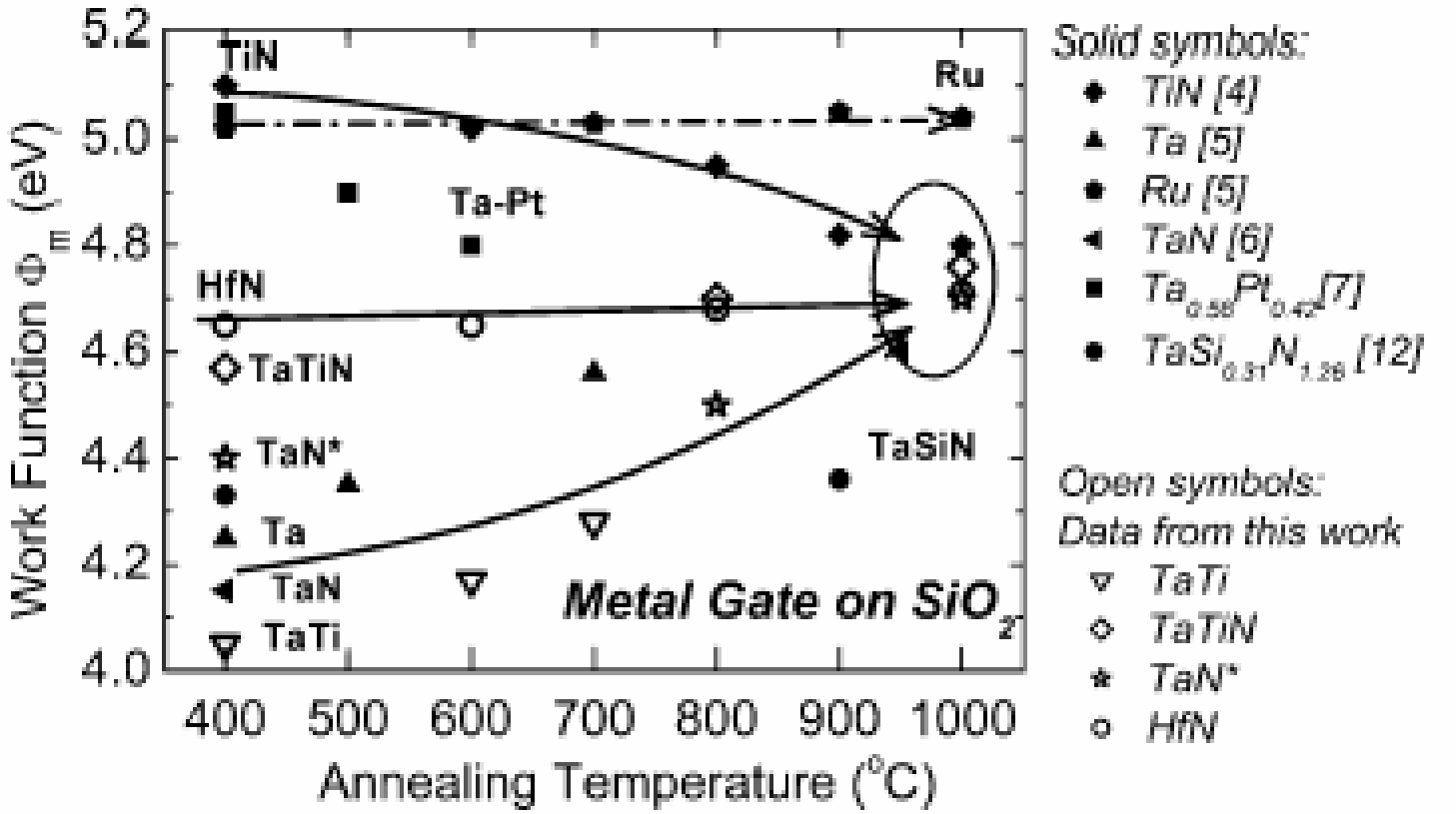
Basic Requirements

- Zero gate depletion
- Right workfunction
- Compatible with hi-k gate dielectric
- Compatible with CMOS technology
  - Thermally stable
  - No interface reaction
  - No workfunction change
- Electrically stable under operation

Key Approaches

- Metal
- FUSI
- Metal/Poly stack

Challenge in metal gate - Thermal stability



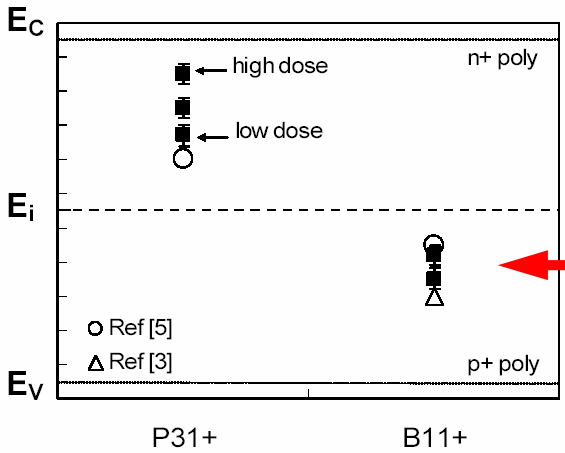
Metal gate workfunction changes toward mid-gap under high temperature anneal

H.Y.Yu et al, EDL V.25, p.337, 2004

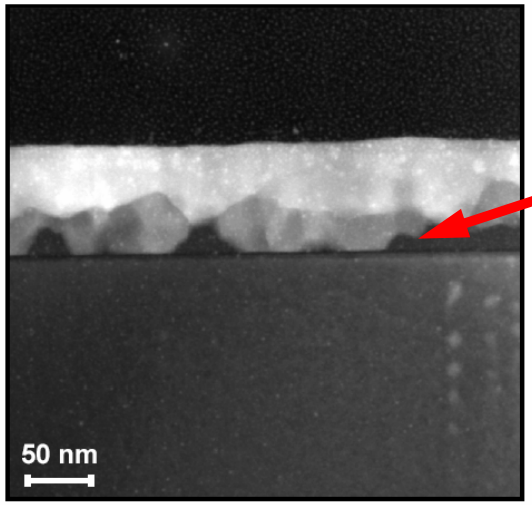
Fully Silicided Gate - FUSI

- Key processes
  - Poly deposition
  - Nickel or other metal deposition
  - Silicidation
- Benefits
  - Compatible with CMOS technology
  - No new material introduced – low cost/fast development cycle
  - Depletion reduction

Challenges in FUSI

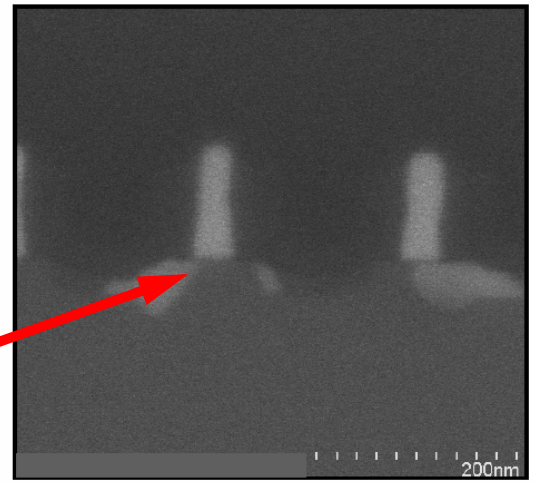


Workfunction is not enough



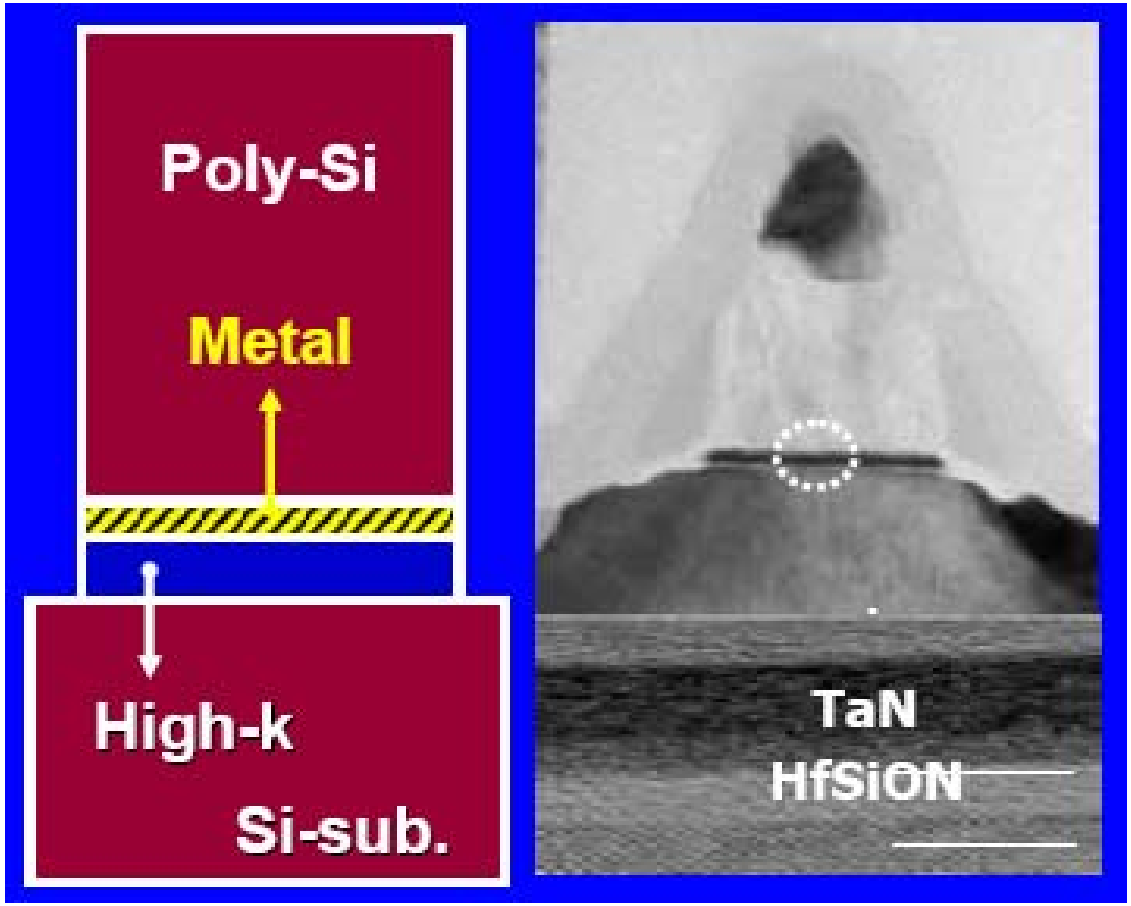
Incomplete silicidation

Ni diffusion through gate oxide



P. Ranade et al, IEDM 2005

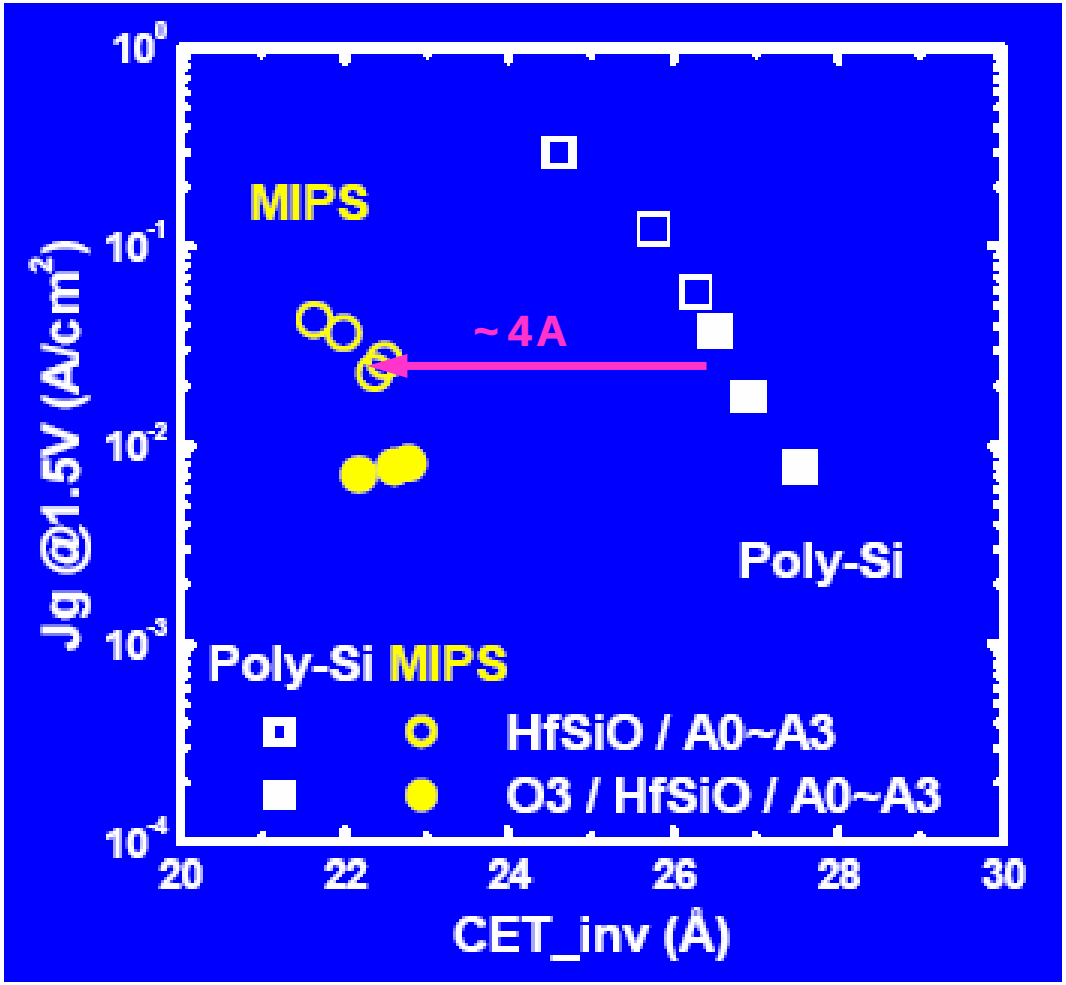
Short term approach - Metal / Poly Stack



Thin layer of metal for poly depletion reduction. Poly for workfunction control

H.S.Jung et al, VLSI 2005

Poly depletion eliminated



A thin layer of Al2O3 is needed for mitigate HfSiOx charges

H.S.Jung et al, VLSI 2005

Summary

- Nitrogen incorporation can effectively reduce leakage current and stop boron penetration.
- Hf based hi-k dielectric meets gate leakage current requirement
- Charge trapping and interfacial properties in the hi-k materials need to be controlled with well engineered processes
- Electrons and holes mobility degradation can be improved by interfacial layer engineering
- Poly depletion can be reduced with Laser annealing
- Metal/Poly stack might be a viable short term solution for eliminating poly depletion

Thank You :-)