Gate Stack Scaling, Challenges and Approaches in Meeting Technology Requirements

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Outline

- Introduction
- Oxynitride
- Hi-K gate dielectric material and processing
- Hi-K gate dielectric electrical performance issues
- Poly depletion reduction
- Metal gate approaches
- Summary
Gate stack scaling includes both dielectric scaling and electrode scaling.
Due to the aggressive technology evolution, down scaling gate dielectric only is not enough to meet device performance.

<table>
<thead>
<tr>
<th>ITRS Roadmap</th>
<th>130 nm</th>
<th>90 nm</th>
<th>65 nm</th>
<th>45 nm</th>
</tr>
</thead>
<tbody>
<tr>
<td>Tox,inv (Å)</td>
<td>23</td>
<td>21</td>
<td>17</td>
<td>12</td>
</tr>
<tr>
<td>EOT (Å)</td>
<td>15</td>
<td>13</td>
<td>10</td>
<td>8</td>
</tr>
<tr>
<td>Poly depletion + QM (Å)</td>
<td>8</td>
<td>8</td>
<td>7</td>
<td>4</td>
</tr>
<tr>
<td>Gate Leakage (A/cm2)</td>
<td>15</td>
<td>100</td>
<td>300</td>
<td>2000</td>
</tr>
<tr>
<td>Nominal power supply voltage (V)</td>
<td>1.2</td>
<td>1.2</td>
<td>1.1</td>
<td>1</td>
</tr>
<tr>
<td>Physical Thickness Control (% 3σ)</td>
<td>&lt;4</td>
<td>&lt;4</td>
<td>&lt;4</td>
<td>&lt;4</td>
</tr>
</tbody>
</table>
Gate Stack Scaling Paths

Gate dielectric scaling

Gate electrode scaling

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What happens when gate dielectric is scaled

Gate leakage has become too high due to aggressive gate dielectric thickness scaling

Beyond this point of cross over, oxynitride is incapable of meeting the limit (Jg,limit) on gate leakage current density

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ITRS Roadmap, 2004

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Major Leakage Components

There is significant Leakage even while devices are off

C. Diaz, IEDM 2003

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Consequences of the leakages

- Larger power consumption $P_{\text{leak}} = V_{dd} \times I_{\text{leak}}$
  - Cost money
  - Shorter battery life for mobile products

- Accelerated device degradation
  - Interfacial defect formation
  - Charge trapping
  - Leakage increases
  - $V_t$ shift
  - Lower drive current (Lower carrier mobility)
  - Shorter device lifetime
Another problem with thinner SiO2

Thermal SiO₂ after 1035 deg.C, 20s RTA

Vg [ V ]

Cg/Cox

Tox
- 3.18 nm
- 3.43 nm
- 5.05 nm

VFB shift due to B penetration

Boron penetration

Data courtesy of Toshiba

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Thicker dielectric for gate leakage reduction

\[ J_G = b \cdot \exp(-a \cdot f \cdot T_d^{ph}) \]

\[ T_d^{ph} \uparrow \implies J_G \downarrow \]
Thinner Dielectric for Performance Enhancement

\[ C_d = \frac{\delta Q}{\delta V} = \frac{A}{T_d^{ph}} \times \varepsilon_d \varepsilon_o \]

\[ T_d^{ph} \uparrow \implies C_d \downarrow \]

\[ \varepsilon_d \uparrow \implies C_d \uparrow \]

\[ \frac{\varepsilon_{hi-k}}{T_{hi-k}^{ph}} \gg \frac{3.9}{T_{SiO2}^{ph}} \]

The goal of scaling is to find a material that behaves physically thicker and electrically thinner.
Dielectric constant of typical materials

- The dielectric constant is the ratio of the permittivity of a substance to the permittivity of free space. It is an expression of the extent to which a material concentrates electric flux.

- Dielectric constant of a few typical materials:
  
  - Air: 1
  - SiO₂: 3.9
  - Si₃N₄: 7.8
  - Al₂O₃: 10
  - HfO₂: 25
  - HfSiON: 10-20
  - ZrO₂: 25
  - Ta₂O₅: 26
Oxynitride
How to stop boron and reduce gate leakage
- Nitrogen incorporation

Two major techniques

- Plasma Nitridation
  - Expose thermally grown oxide to nitrogen plasma.

- Conventional thermal nitridation
  - Anneal oxide in NO, N2O or NH3.
  - Grow oxide in NO, N2O or mixture of NO, N2O, NH3 with O2.
Nitrogen Incorporation Processes – Plasma Nitridation

1. Base oxide growth with ISSG or RTO

2. Plasma nitridation (DPN), leaving nitrogen in the top portion of base oxide

3. Post nitridation anneal (PNA) for interfacial and bulk oxide improvement
Nitrogen Incorporation Processes – Thermal Nitridation

1. Thermal oxide growth

2. Anneal in NO, N2O or NH3 gas, leaving nitrogen at near oxide and silicon interface

3. Re-oxidation to move nitrogen away from oxide-silicon interface
Boron penetration

Nitrogen incorporation in oxide can effectively suppress boron penetration

Gate Leakage Current Reduction

DPN process is more effective in leakage current reduction

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More channel mobility degradation was observed with NO anneal process due to nitrogen at oxide and silicon interface.
Hi-k Gate Dielectric Material and Processing
A detailed view of a completely new “M-I-S” system

- **Gate Electrode**
  - Work function, compatible with hi-k, minimum gap-state generation

- **Interfacial layer**
  - Interfacial reaction, dipole formation

- **Bulk of Hi-K gate dielectric**
  - Trapped charge, charge trapping, Oxygen vacancy formation

- **Interfacial layer**
  - Interfacial trapped charge, interfacial reaction, boron penetration,

- **Substrate**
  - Mobility degradation (Remote phonon scattering, Coulomb scattering)
Post deposition anneal is needed for oxygen vacancy reduction

Takeuchi et al. JVST 2004  
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Interfacial reaction

Interfacial layer growth is a potentially limiting factor to dielectric scaling
Interfacial reaction suppression
- Plasma Nitridation

Plasma nitridation is an efficient approach to suppress interfacial layer growth

\[ T = 650^\circ C, \text{ EOT} = 11\text{Å} \]
\[ t_{\text{PHYS,TEM}} \text{ IL} = 7\text{Å} \]
\[ t_{\text{PHYS,TEM}} \text{ HfSiOxNy} = 22\text{Å} \]
Thermal Stability of ALD HfSiOx at 1050°C

**Without DPN Nitridation**
HfSiOx after 1050°C, 15 sec RTA

Phase segregation occurs without DPN nitridation

**With DPN Nitridation**
HfSiON after 1050°C, 30 sec RTA

Film stable up to 1050°C, 30 sec with DPN nitridation

Thermally stable ALD HfSiOx film can be formed by incorporating nitrogen with plasma nitridation technique

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Dielectric constant and phase stability

K value and phase stability are dependent on Hf and nitrogen concentration

M. Takayagani et al, IEDM 2005
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Boron penetration evaluation

Nitrogen is needed in high-k film for suppressing boron penetration

T. Watanabe et al. VLSI Symp. 2003

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Trapped Charges in Hi-K films

High trapped charge density in hi-k film needs to be reduced with post deposition anneal

Takeuchi et al. JVST 2004

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Trapped Charge - Thickness dependent

As a disadvantage of thicker dielectric film, more trapped charges

A. Morioka et al., VLSI 2003
Hi-k Gate Dielectric Electrical Performance
Requirements for High-k Gate Dielectrics

- More than 500x gate leakage reduction
- Compatibility to conventional CMOS process
  - material stable up to 1050°C – S/D activation temperature
  - interfacial properties with silicon channel and gate electrode
  - robustness to Boron penetration
  - $V_{th}$ control
- Effective-mobility is larger than 90% of SiO$_2$
- Sufficient long-term reliability
  - Charge trapping (more severe for thicker film)
- Scalability
High-k HfSiO\textsubscript{x} with Polysilicon Gate

Electrical Results Highlight:

- <1.0nm EOT
- >500 times leakage reduction
- Stable film up to 1050°C, 30 sec RTA

Gate leakage reduction of >500x can be achieved with MOCVD and ALD technologies

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High PMOS Flatband Voltage

• $\Delta V_{\text{FB}}$ of P-sub. MOS-CAP is
  \[ n^+ \text{poly-Si}: \sim +200 \text{mV} \]
  \[ p^+ \text{poly-Si}: \sim -600 \text{mV} \]

• Difficult to adopt to HP application without solving this problem.

• Channel implantation for $V_{\text{th}}$ adjustment is very difficult.

A. Kaneko et al., SSDM 2003
Mobility Concerns

\[
\frac{1}{\mu_{\text{eff}}} = \frac{1}{\mu_{\text{coul}}} + \frac{1}{\mu_{\text{ph}}} + \frac{1}{\mu_{\text{sr}}}
\]

\(\mu_{\text{coul}}\) : Coulomb scattering

\(\mu_{\text{ph}}\) : Phonon scattering

\(\mu_{\text{sr}}\) : Surface roughness

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Mobility improvement with interfacial layer may be due to reduction of roughness and phonon scattering
Phonon Scattering Reduction

Mobility can be improved with thicker interfacial SiO2 layer. However, EOT scaling is compromised.
Poly depletion vs poly carrier concentration

$n^+\text{poly Si/SiO}_2/n \text{Si}$

Simulations

$EOT = 2 \text{ nm}$

$N_Si = 5 \times 10^{17} \text{ cm}^{-3}$

$N_{poly} (\times 10^{19} \text{ cm}^{-3}) = 10$

$N_{poly} (\times 10^{19} \text{ cm}^{-3}) = 2$

$N_{poly} (\times 10^{19} \text{ cm}^{-3}) = 1$

More poly depletion with lower carrier concentration

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Laser Annealing for Higher Carrier Concentration

A 47.3% Rs reduction can be achieved with Laser anneal

Laser anneal temperature has significant impact in Rs reduction

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Improved Poly-Si Depletion with DSA

\[ p^+ \text{-poly-Si}/p\text{-Si MOSCAPs} \]

- 25Å RTO
- 1000Å Poly-Si
- Boron implant
- RTA
- FGA

A poly depletion reduction of 0.8Å can be achieved with Laser annealing.

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Basic Requirements

- Zero gate depletion
- Right workfunction
- Compatible with hi-k gate dielectric
- Compatible with CMOS technology
  - Thermally stable
  - No interface reaction
  - No workfunction change
- Electrically stable under operation
Key Approaches

- Metal
- FUSI
- Metal/Poly stack
Challenge in metal gate - Thermal stability

Metal gate workfunction changes toward mid-gap under high temperature anneal

H.Y. Yu et al, EDL V.25, p.337, 2004

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Fully Silicided Gate - FUSI

- Key processes
  - Poly deposition
  - Nickel or other metal deposition
  - Silicidation

- Benefits
  - Compatible with CMOS technology
  - No new material introduced – low cost/fast development cycle
  - Depletion reduction
Challenges in FUSI

Workfunction is not enough

Incomplete silicidation

Ni diffusion through gate oxide
Short term approach - Metal/Poly Stack

Thin layer of metal for poly depletion reduction. Poly for workfunction control
Poly depletion eliminated

A thin layer of Al2O3 is needed for mitigate HfSiOx charges
Summary

- Nitrogen incorporation can effectively reduce leakage current and stop boron penetration.
- Hf based hi-k dielectric meets gate leakage current requirement.
- Charge trapping and interfacial properties in the hi-k materials need to be controlled with well engineered processes.
- Electrons and holes mobility degradation can be improved by interfacial layer engineering.
- Poly depletion can be reduced with Laser annealing.
- Metal/Poly stack might be a viable short term solution for eliminating poly depletion.
Thank You :-}