Device and Technology Challenges for Nanoscale CMOS

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Acknowledgments

- **Former IBM colleagues**
- **Stanford collaborators**
- **Many leaders in the device and technology areas around the world**
- **Financial support**

Outline

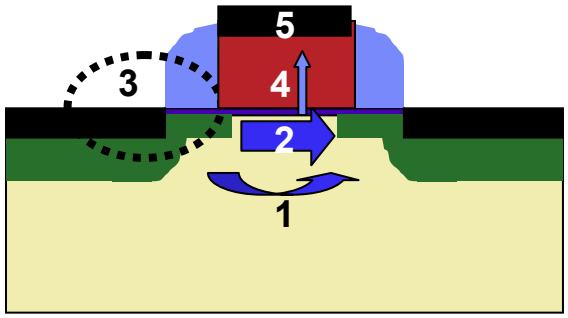
- **Device options**
  - Transport enhanced devices
  - Multi-gate devices
  - 1D nanomaterials
- **Technology options**
  - Device fabrication by self-assembly
  - Device footprint
- **The future**

Key Challenges

- **Power / performance improvement and optimization**
- **Variability**
- **Integration**
  - Device, circuit, system

New Structures and Materials

CURRENT BULK MOSFET



Problem 1: Poor Electrostatics ⇒ increased I_{off}
Solution: Double Gate
- Retain gate control over channel
- Minimize OFF-state drain-source leakage

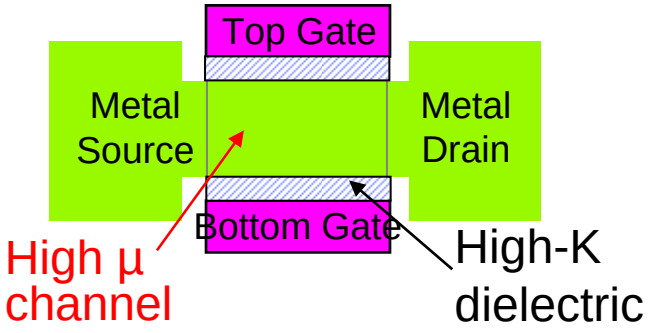
Problem 2: Poor Channel Transport ⇒ decreased I_{on}
Solution - High Mobility Channel
- High mobility/injection velocity
- High drive current and low intrinsic delay

Problem 3: S/D Parasitic resistance ⇒ decreased I_{on}
Solution - Metal Schottky S/D
- Reduced extrinsic resistance

Problem 4. Gate leakage increased
Solution - High-K dielectrics
- Reduced gate leakage

Problem 5. Gate depletion ⇒ increased EOT
Solution - Metal gate
- High drive current

FUTURE MOSFET



Source: K. Saraswat (Stanford)

Transport Enhancement

- **Drive current continues to improve until transport is completely ballistic** $\delta I_D / I_D = (\delta\mu / \mu) \times (1 - B)$
  - B ~ 0.5 at L_{gate} ~ 45 nm
- **Improving mobility increases drive current**

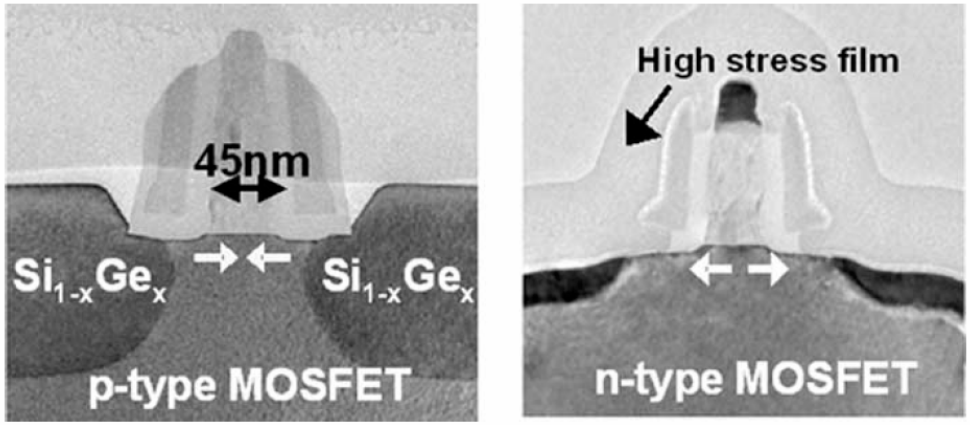
$$I_D / W = C_{ox}(V_G - V_T) v_T \left(\frac{1-r}{1+r}\right) \rightarrow v_{inj} = \frac{\mu\mathcal{E}}{1 + \mu\mathcal{E} / v_T}$$

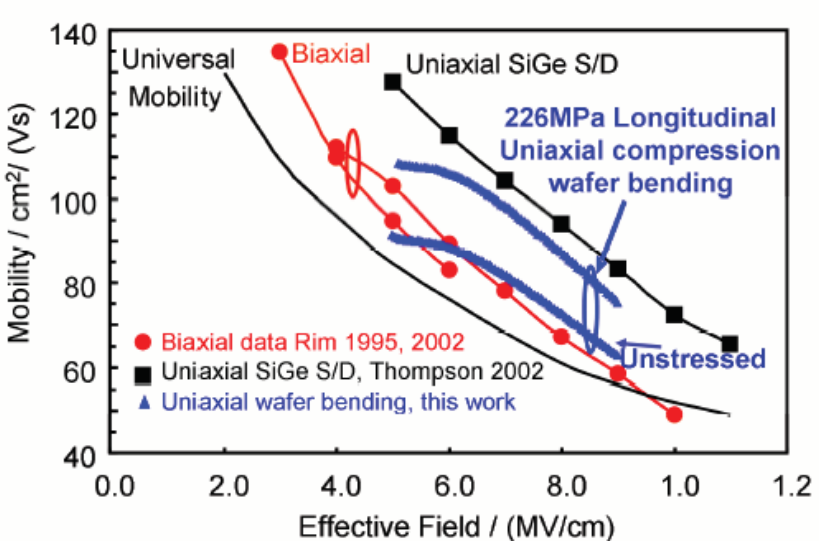
$$\frac{C_{gate} V_{DD}}{I_D} = \frac{L_{gate} \times V_{DD}}{(V_{DD} - V_T) \times v_{inj}}$$

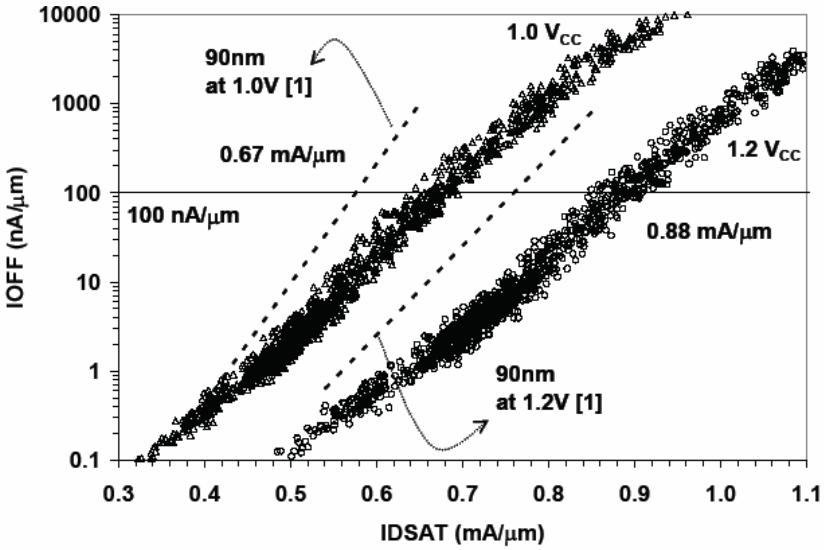
- **Band structure, effective mass engineering**
  - Strain, SiGe, Ge, III-V, …

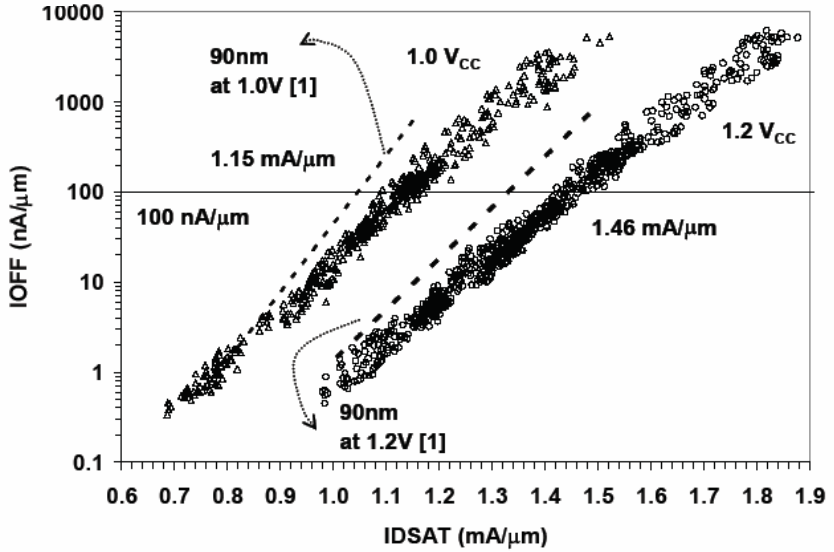
M. Lundstrom," On the Mobility Versus Drain Current Relation for a Nanoscale MOSFET," *IEEE Electron Device Letters*, p. 293 (2001).

Strained Si – Uniaxial Strain





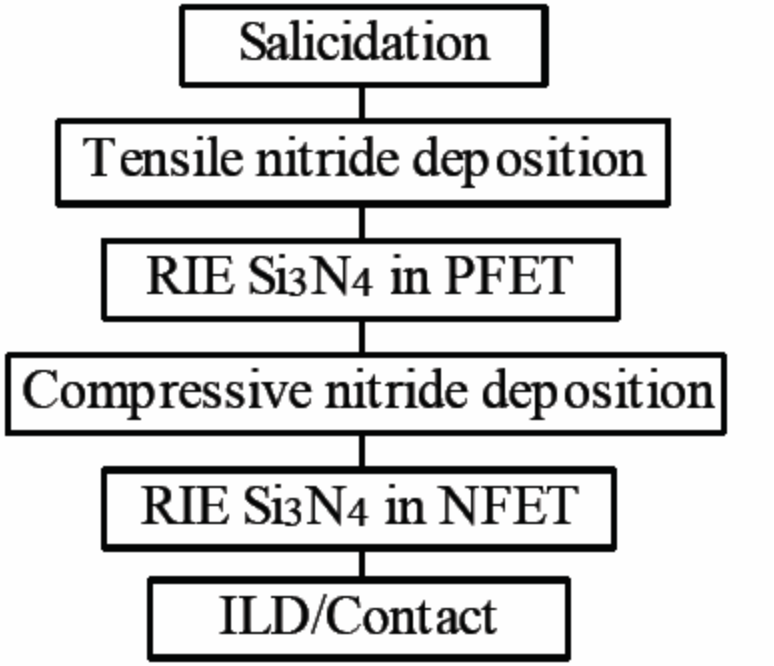


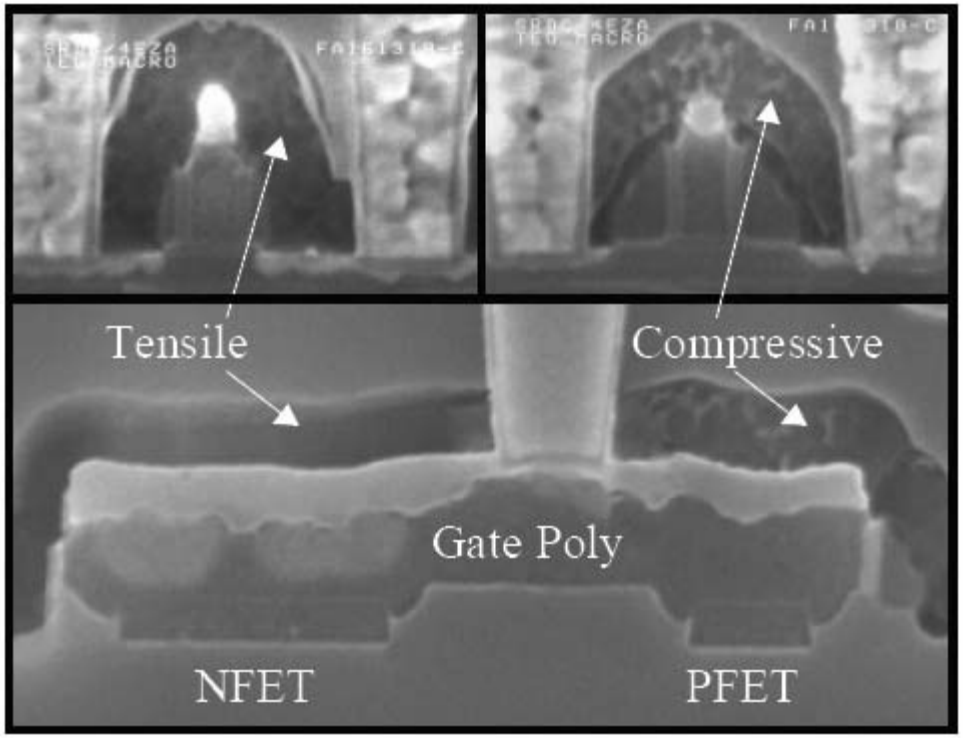


S. E. Thompson et al., "A logic nanotechnology featuring strained-silicon," *IEEE Electron Device Lett.,* Vol. 25, pp. 191 - 193, April 2004.

P. Bai et al., "A 65nm logic technology featuring 35nm gate lengths, enhanced channel strain, 8 Cu interconnect layers, low-k ILD and 0.57 μm2 SRAM Cell," *IEDM Tech. Dig.*, pp. 657 - 660, December 2004.

Uniaxial Strain – Stressor Films and Liners





H. S. Yang et al., "Dual stress liner for high performance sub-45nm gate length SOI CMOS manufacturing," *IEDM Tech. Dig.*, pp. 1075 - 1078, December 2004.

Strain – How Far Does It Go?

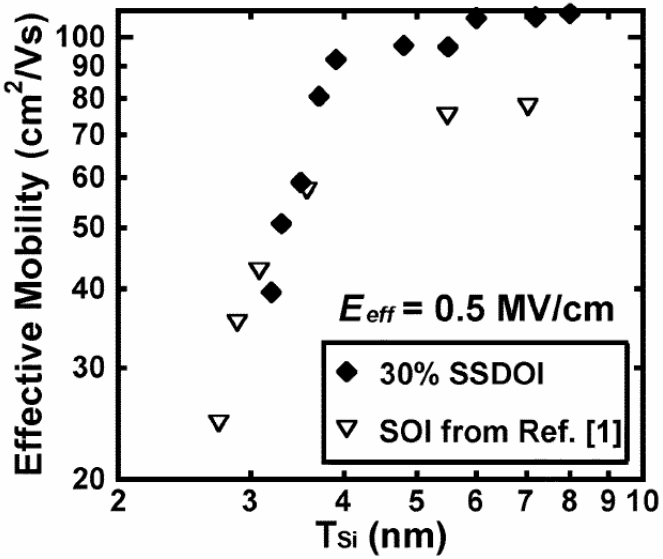


Fig. 3. Hole mobility for 30% SSDOI (this letter, solid symbols) and SOI (from [1], open symbols) at a vertical effective field of 0.5 MV/cm. At this field, the low dose channel implant in the SSDOI has limited influence on mobility [14]. Mobility for strained-Si decreases rapidly below $T_{Si} = 3.9$ nm, possibly due to thickness-fluctuation-induced scattering, as observed for ultrathin unstrained SOI in [1] and [4].

I. Aberg, J. Hoyt, "Hole Transport in UTB MOSFETs in Strained-Si Directly on Insulator With Strained-Si Thickness Less Than 5 nm," *IEEE EDL*, p. 661, Sept. 2005.

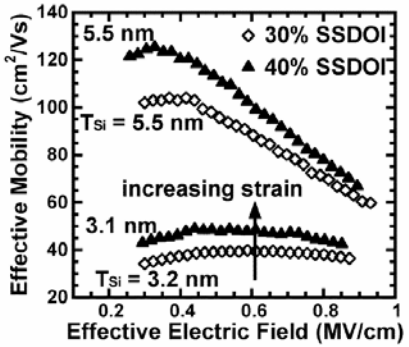


Fig. 4. Hole mobility versus effective electric field for 30% SSDOI (open symbols) and 40% SSDOI (solid symbols). Even for $T_{Si} = 3.1$ nm, mobility increases as the strain in the Si is increased. Locally thinned MOSFETs were used for this comparison.

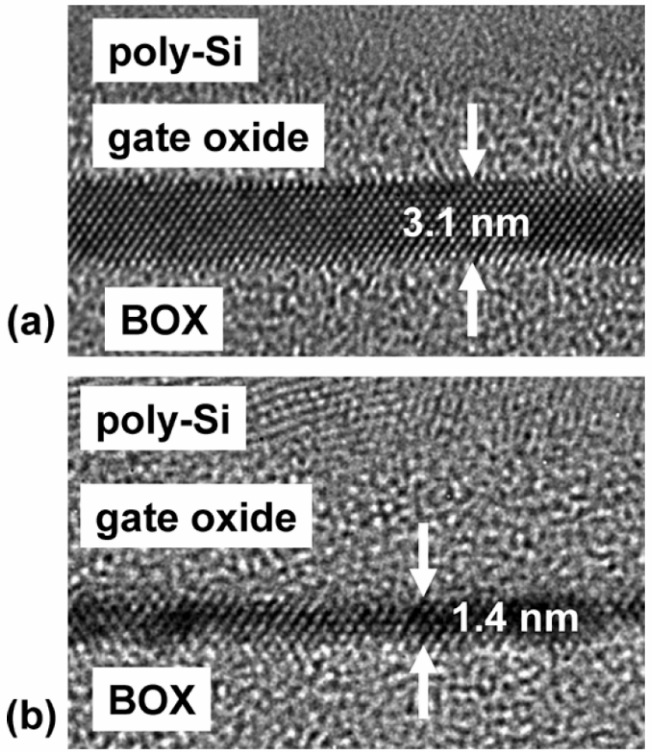
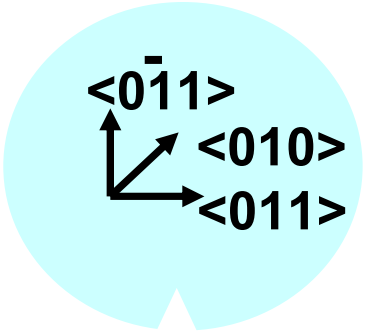
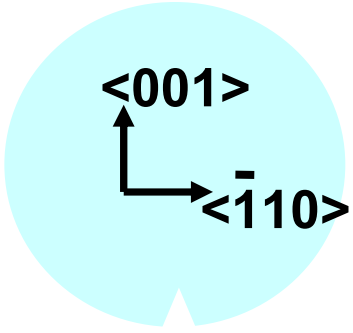


Fig. 1. XTEMs of (a) 3.1-nm-thick 40% SSDOI, and (b) 1.4-nm-thick 30% SSDOI. *C–V* measurements confirmed the continuity of the film.

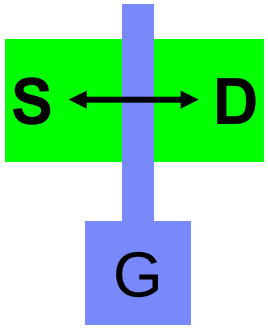
Surface Orientation & Current Flow Direction

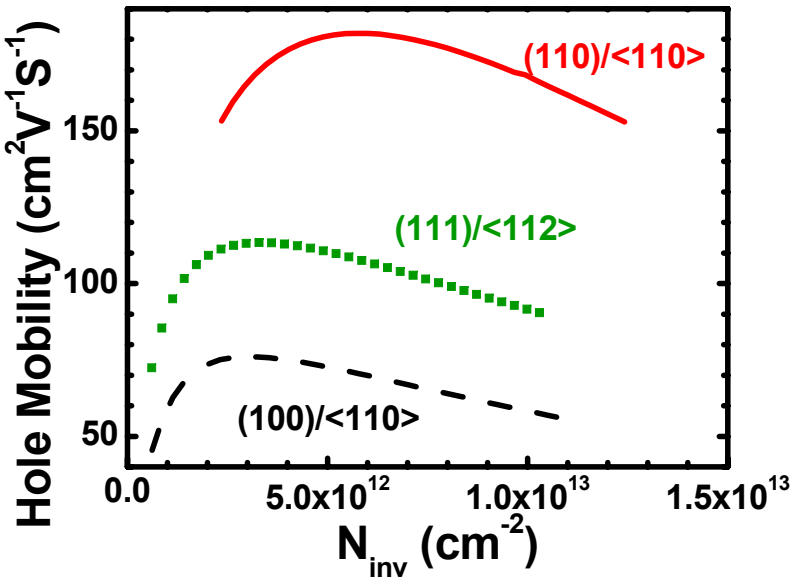


(100) surface

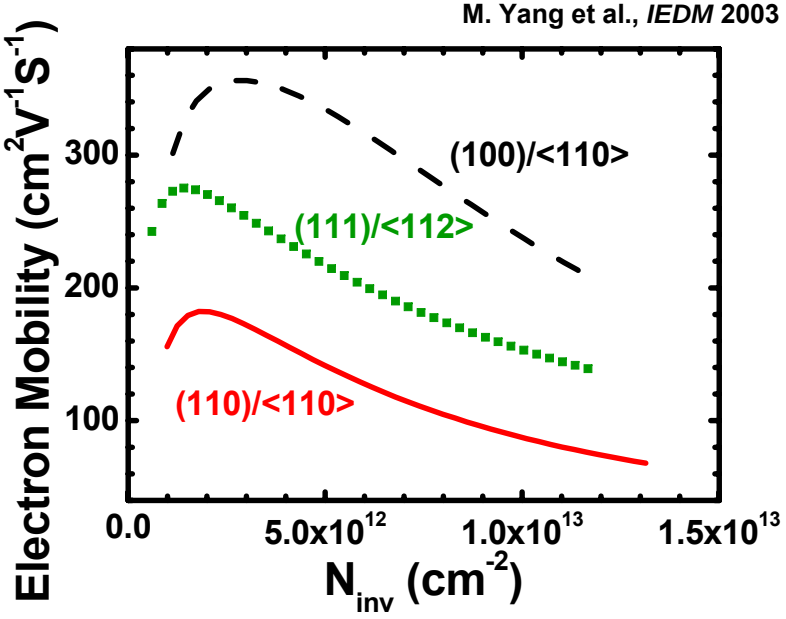


(110) surface



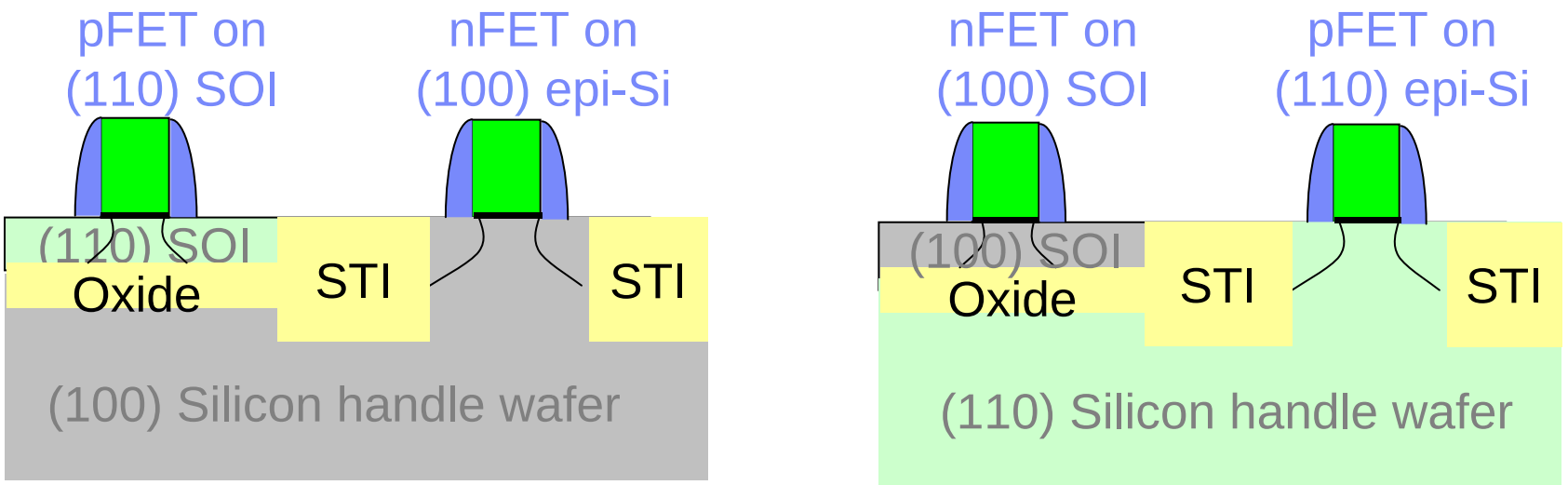


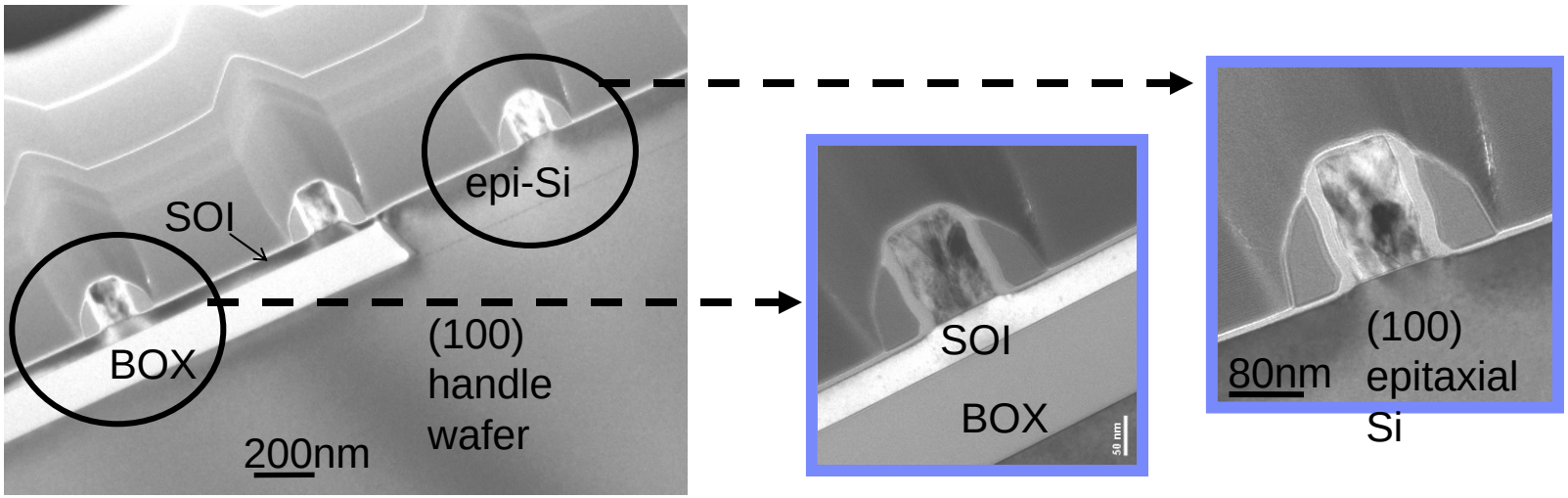
M. Yang et al., *IEDM* 2003



M. Yang et al., *IEDM* 2003

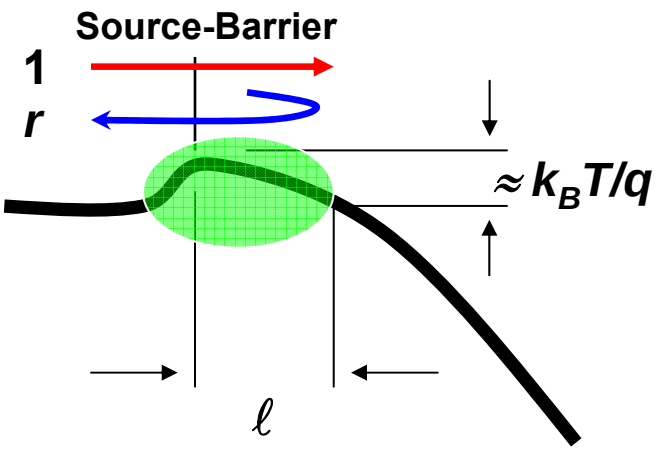
Hybrid Orientation Technology (HOT)





Enhanced Transport with Lower m_{eff}*

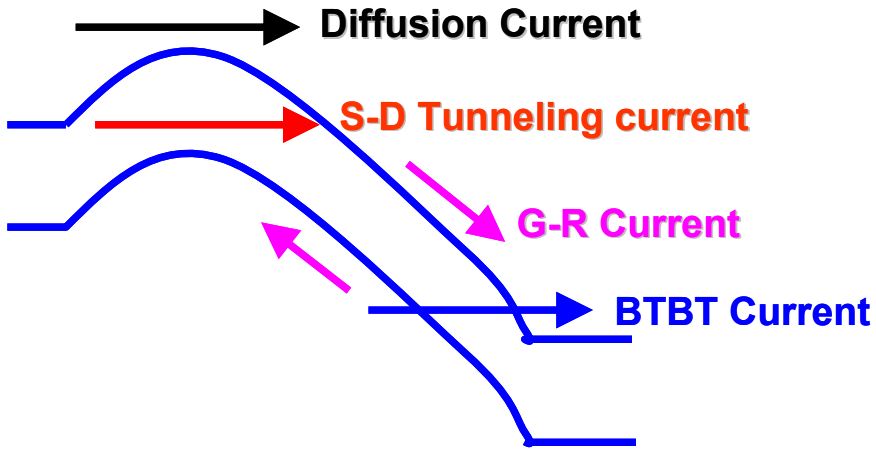
ADVANTAGES



$$I_{sat} = qN_S^{Source} v_{inj} \times \left(\frac{1-r}{1+r} \right)$$

Low $m^*_{transport}$ ⟶ High ν_{inj}, μ

DISADVANTAGES



Low E_g ⟶ High leakage currents
High κ_s ⟶ Worse SCE
Low m^* ⟶ High tunneling leakage

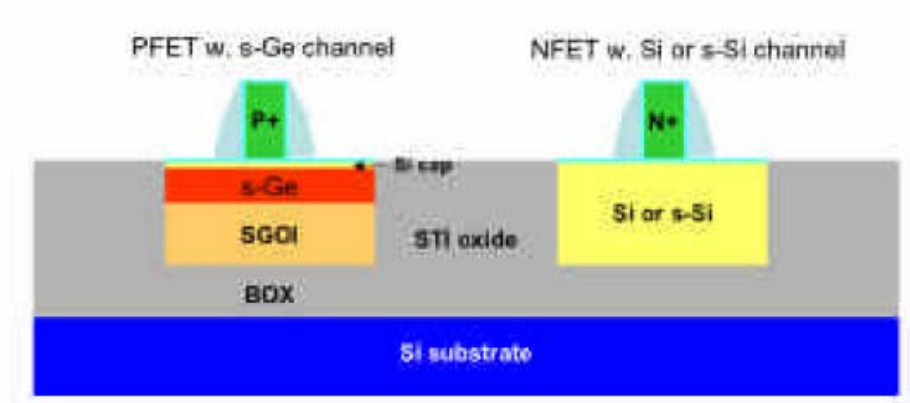
Higher injection velocity → Higher current

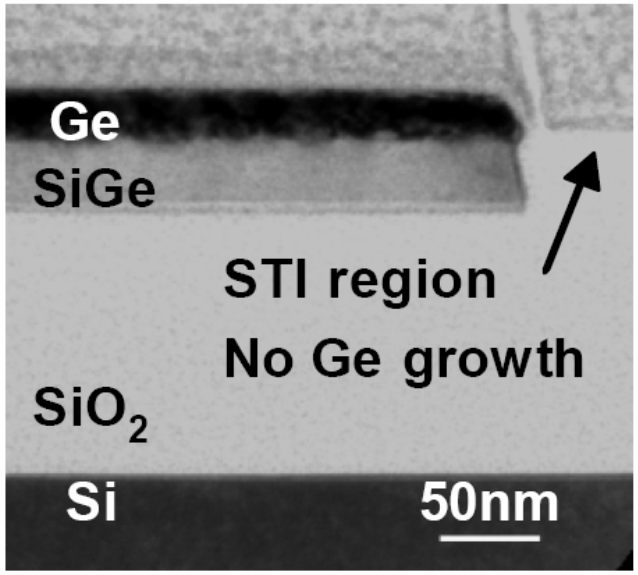
Leakage currents may hinder scalability

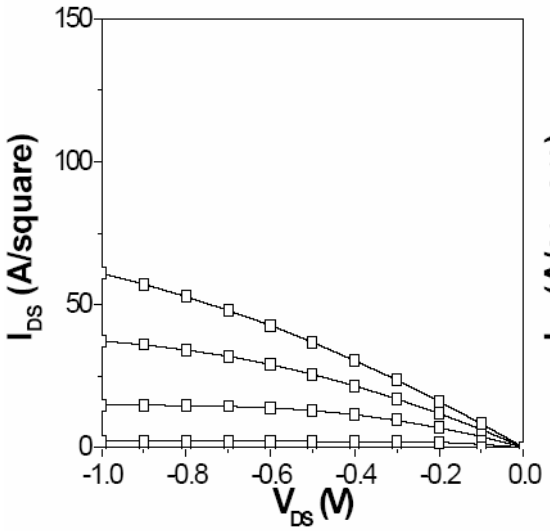
A. Pethe…K. Saraswat, *IEDM*, paper 26.3 (2005).

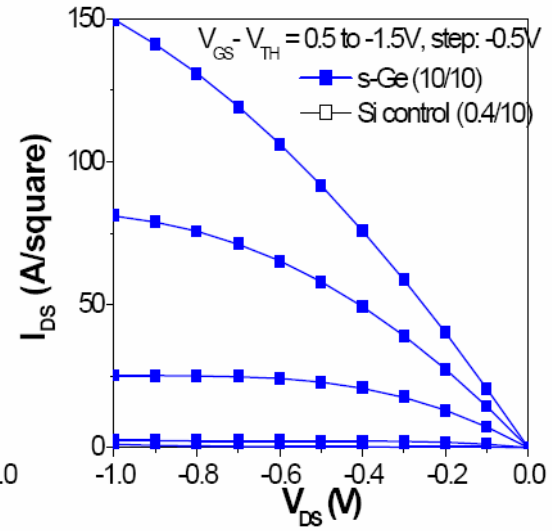
Strained Ge pFET with HfO_2

- **Integrated strained Ge on insulator with bulk Si**
  - 67% Ge by Ge condensation
  - Selective UHVCVD Ge on Si
- **3X drive current improvement**









H. Shang, J. O. Chu, S. Bedell, E. P. Gusev, P. Jamison, Y. Zhang, J. A. Ott, M. Copel, D. Sadana, K. W. Guarini, and M. Ieong, "Selectively formed high mobility strained Ge PMOSFETs for high performance CMOS," *IEDM Tech. Dig.*, pp. 157 - 160, December 2004.

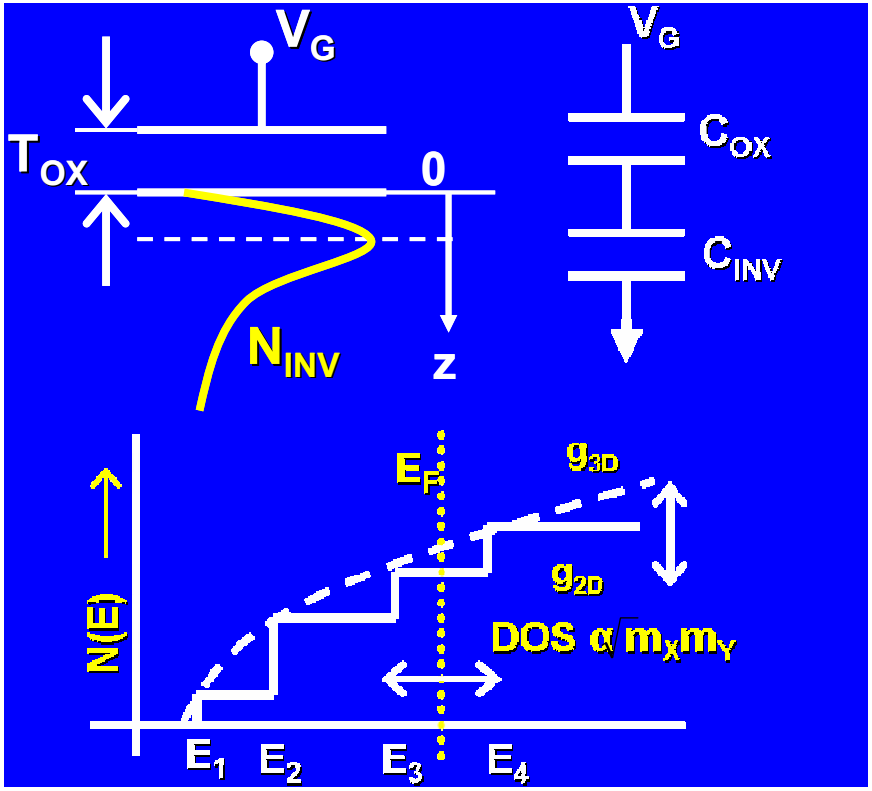
Which Low m_{eff}* Material?

Properties of Semiconductor materials

Material/Property	Si	Ge	GaAs	InAs	InSb
m_{eff}*	0.19	0.08	0.067	***0.023***	***0.014***
μ_n (cm^2/Vs)	1600	3900	9200	***40,000***	***77,000***
E_G (eV)	1.12	0.66	1.42	***0.36***	***0.17***
ε_r	11.8	16	12.4	14.8	***17.7***

- Low E_G – higher leakage
- High ε_r – worse SCE
  - SS ↑ - V_T ↑ Reduced overdrive for fixed I_{OFF}
  - DIBL ↑ - variation

Effect of reduced DOS



- C_{EFF} ↓
  - N_{INV} ↓ for same V_G
  - C_{LOAD} reduced for next stage

A. Pethe…K. Saraswat, *IEDM*, paper 26.3 (2005).

Best Performance

- **Low m_x (v_{inj} ↑)**
- **High m_y (DOS ↑)**
- **Low m_z (v_{inj} ↑)**
- **Population of sub-bands is an important consideration**
  - At high carrier density, carriers may populate sub-bands with different effective mass
  - Quantum confinement (high field, ultra-thin channel) and strain may cause carriers to populate sub-bands with different effective mass

Transport Enhanced Devices

- **Wafer-scale strained Si**
  - Strained Si on relaxed SiGe buffer on bulk Si
  - Strained Si on relaxed SiGe buffer on insulator
  - Strained Si directly on insulator
- **Local strain**
  - Dielectric films
  - Isolation (STI), device size dependent structures
  - SiGe in recessed source/drain
- **Crystal orientation and current flow direction**
- **Other materials**
  - Bulk Ge
  - Ge on insulator
  - Strained Ge
  - **III-V on Ge on insulator on Si !**

Not for 45 nm / 32 nm node

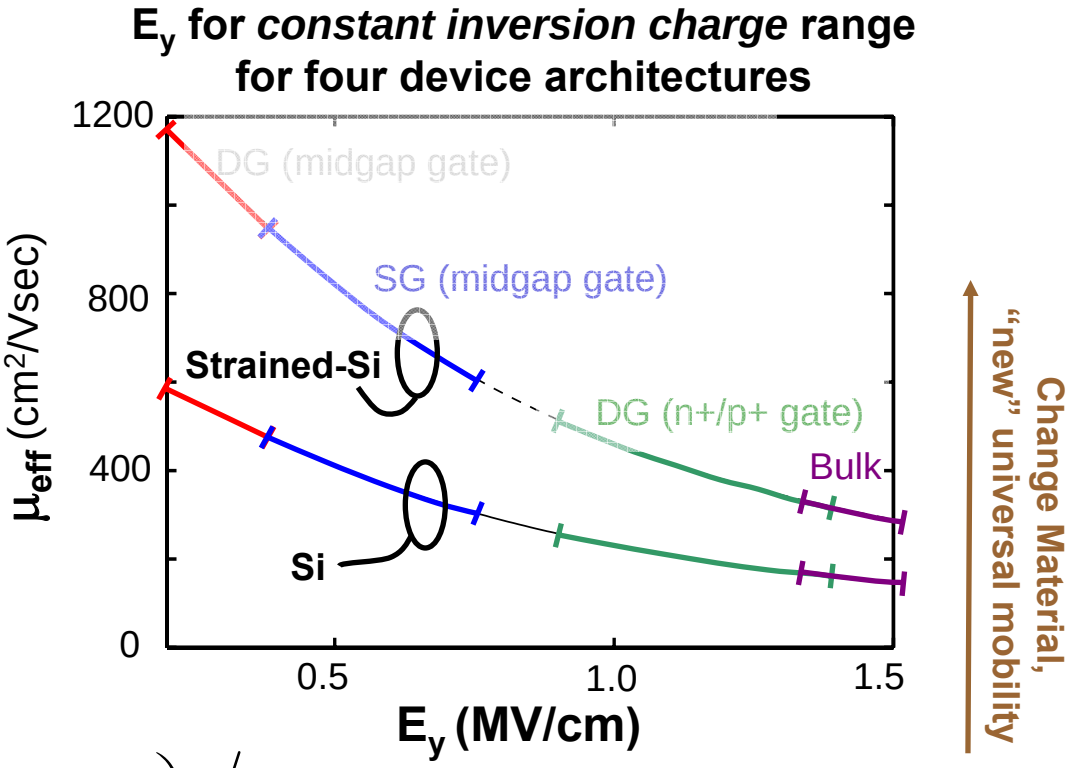
!

Enables:

- Fast III-V nFET
- If Ge works, fast pFET also
- Integrated optoelectronics

However, only small number of these devices allowed due to power dissipation

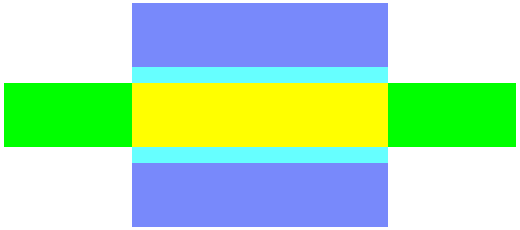
Device Design Considering Universal Mobility



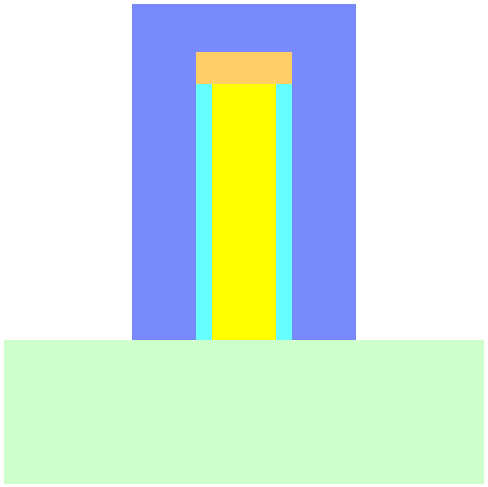
$$E_Y = \left(Q_B + \frac{1}{\eta} Q_{inv} \right) \Big/ \varepsilon$$

Source: D. Antoniadis (MIT)

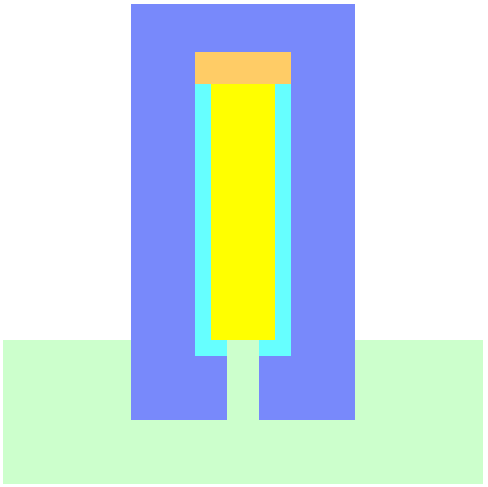
Multi-Gate Transistors



$T_{Si} \sim 1/2 – 2/3\ L_g$

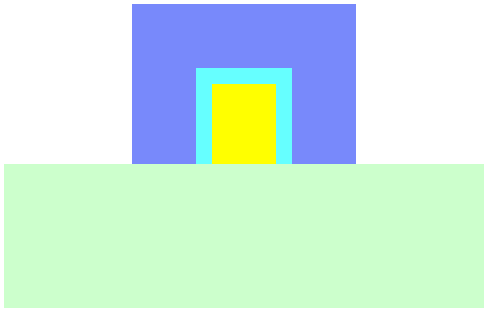


$T_{Si} \sim 1/2 – 2/3\ L_g$

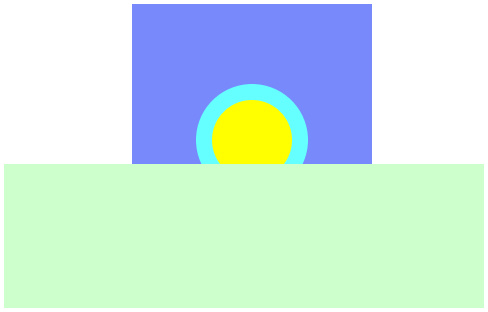


$T_{Si} \sim 1/2 – 2/3\ L_g$

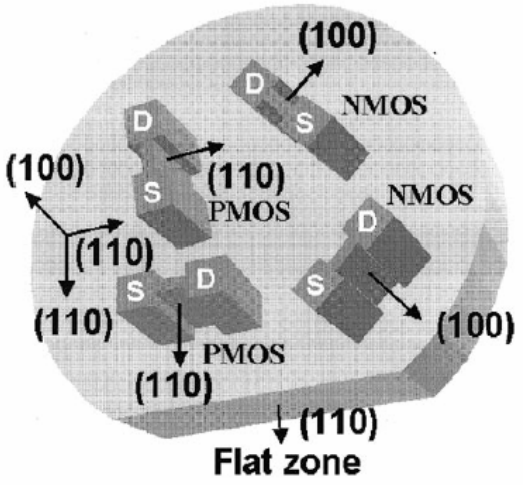
UTB SOI: $T_{Si} \sim 1/4 – 1/3\ L_g$



$T_{Si} \sim L_g$



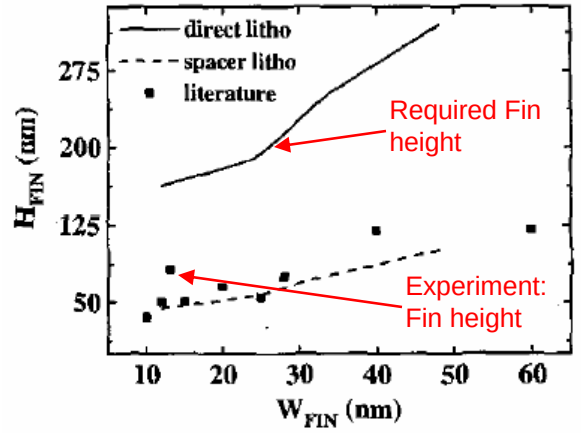
$T_{Si} \sim L_g$

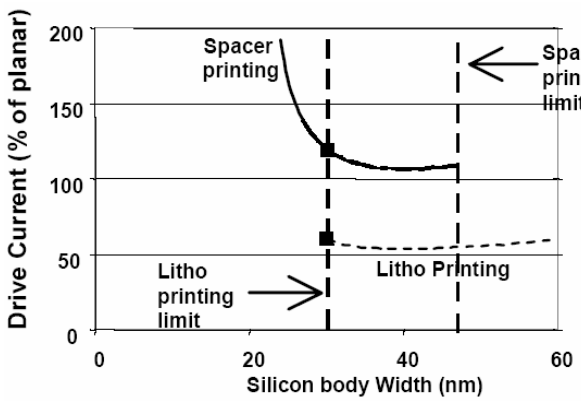


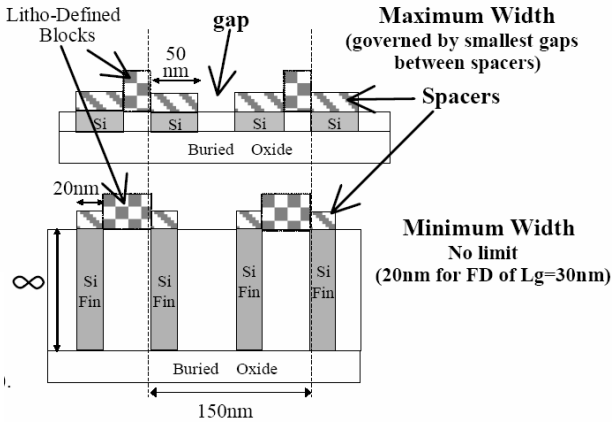
L. Chang et al., “Extremely scaled Silicon nano-CMOS Devices," *IEEE Proceedings*, pp. 1860 – 1873 (2003).

Device Density, Fin Height Considerations

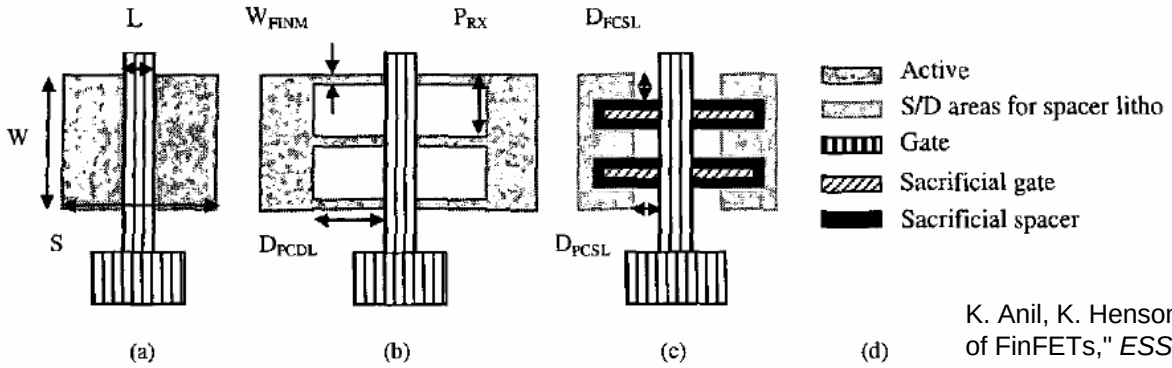
- **Spacer lithography required to achieve device density comparable to planar devices**
- **Active region in the gate length direction slightly longer than planar devices**





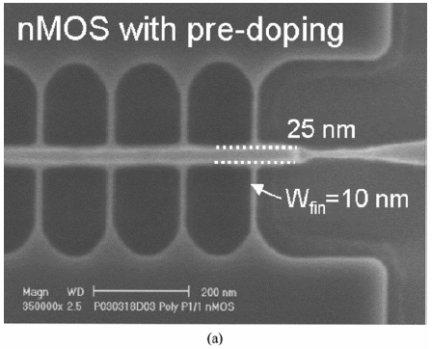


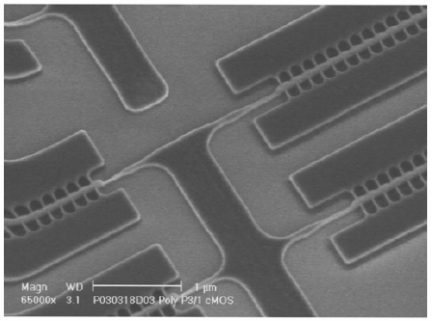
B. Doyle …R. Chau, "Tri-Gate Fully-Depleted CMOS Transistors," *Symp. VLSI Technology*, pp. 133 – 134, June 2003.



K. Anil, K. Henson, S. Biesemans, N. Collaert, "Layout density analysis of FinFETs," *ESSDERC,* pp. 139 – 142 (2003).

FinFET Circuits – Ring Oscillator & SRAM



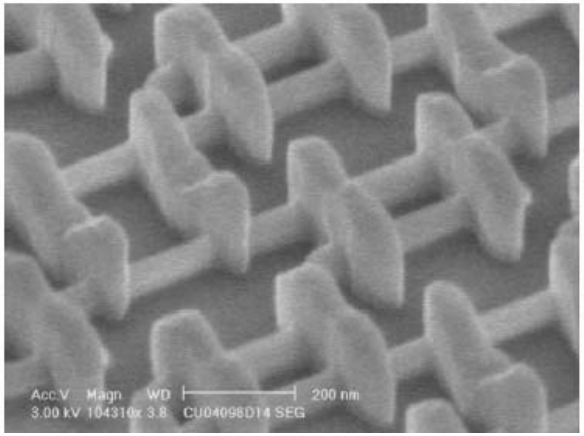


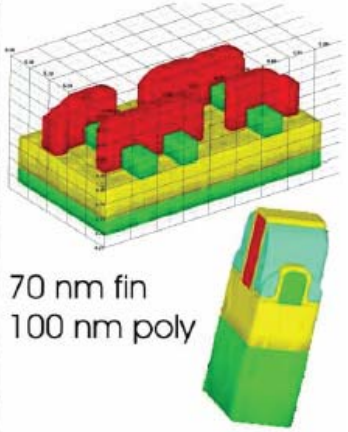
Ring oscillator:

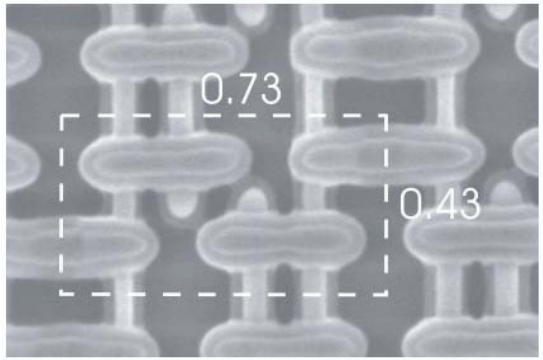
- **H_2 anneal to smooth fin**
- **Fin pre-doping (phos., nFET) to set V_T**

SRAM:

- **Implant shadowing by multiple fins (fin height)**
- **Double contact hole print/etch for fin topography**





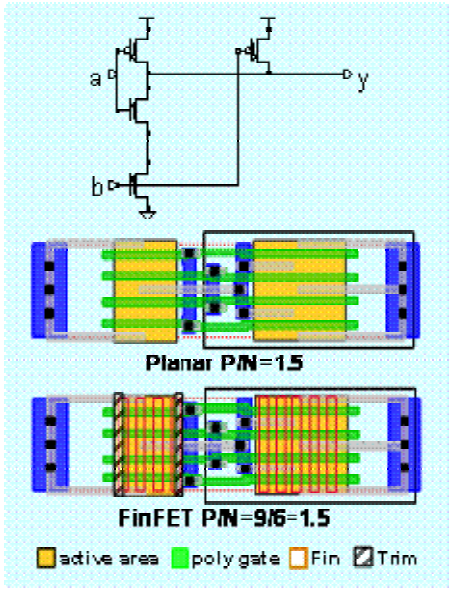


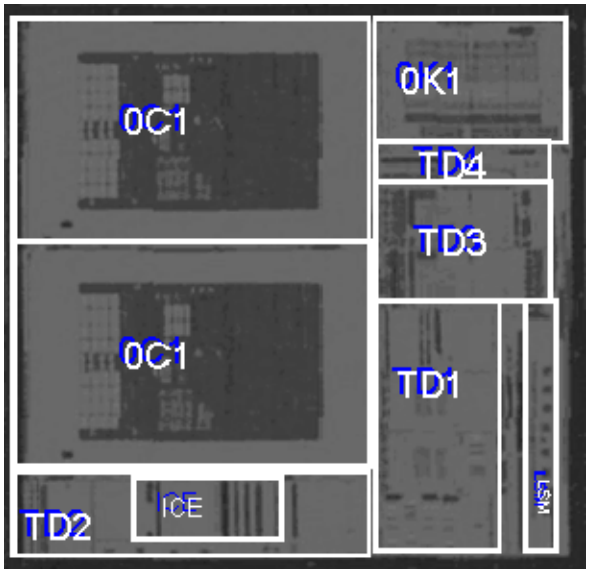
A. Nackaerts, … and S. Biesemans, "A 0.314μm2 6T-SRAM cell build with tall triple-gate devices for 45nm node applications using 0.75NA 193nm lithography," *IEDM Tech. Dig.*, pp. 269 - 272, December 2004.

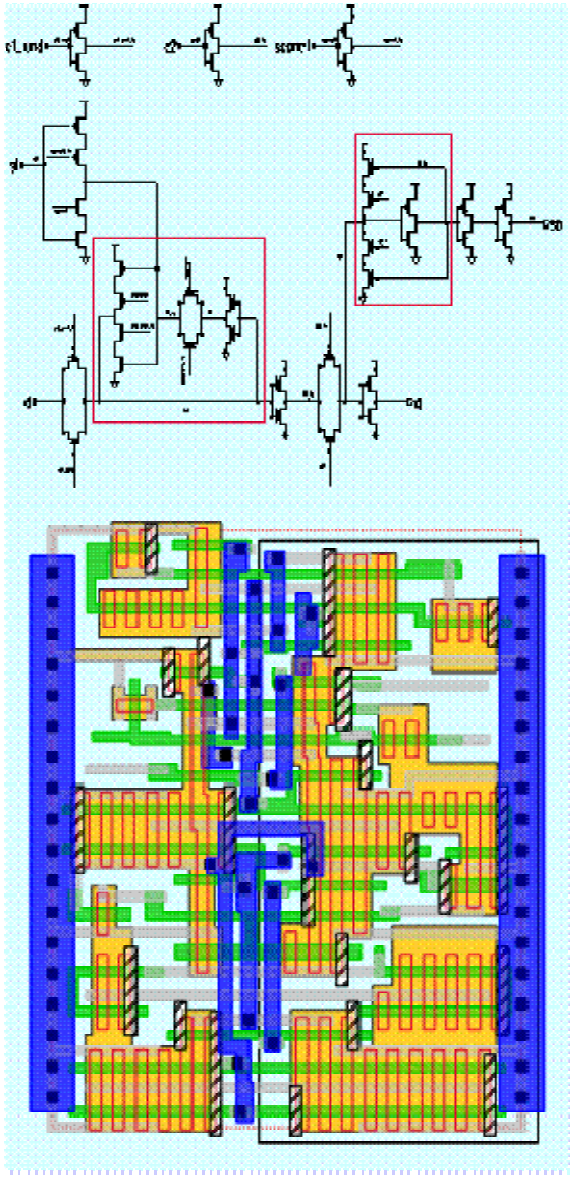
N. Collaert, … and S. Biesemans, "A functional 41-stage ring oscillator using scaled FinFET devices with 25-nm gate lengths and 10-nm fin widths applicable for the 45-nm CMOS node," *IEEE Electron Device Lett.,* Vol. 25, pp. 568 - 570, August 2004.

FinFET Microprocessor

- **Map planar SOI design to FinFET**
- **Automatic layout conversion (~ 90%)**
  - Device width tuning
  - EDS devices

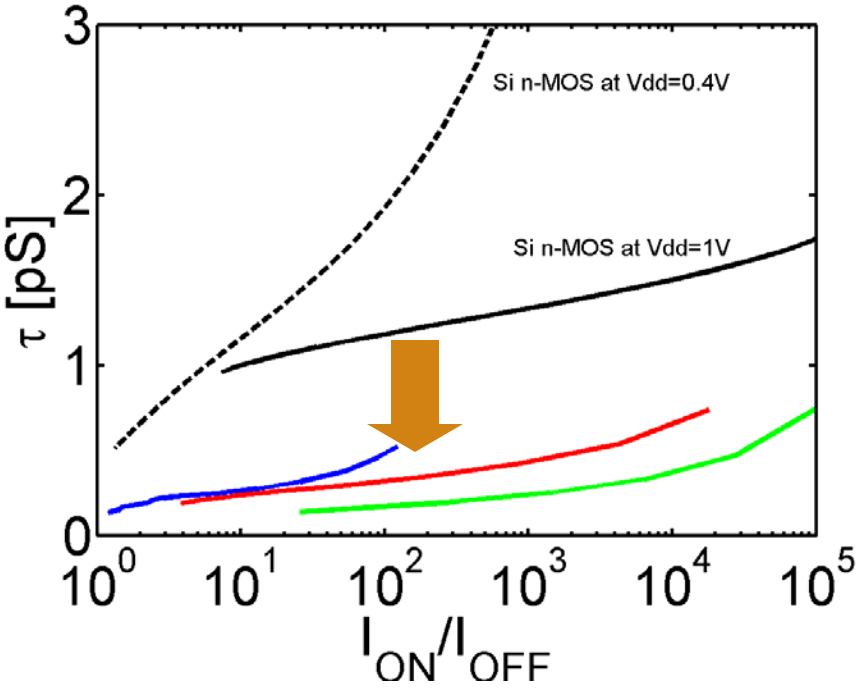






T. Ludwig, I. Aller, V. Gernhoefer, J. Keinert, E. Nowak, R.V. Joshi, A. Mueller, S. Tomaschko, "FinFET technology for future microprocessors," *IEEE SOI Conf.*, pp. 33 – 34 (2003).

Carbon Nanotube FET vs. Si MOSFET



CNTFETs (V_{DD} = 0.4V)

p-CNT MSDFET (Javey)

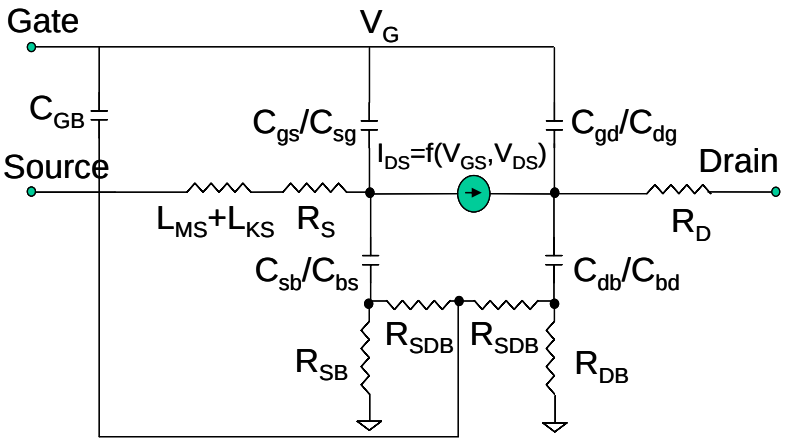
p-CNT MSDFET (projected)

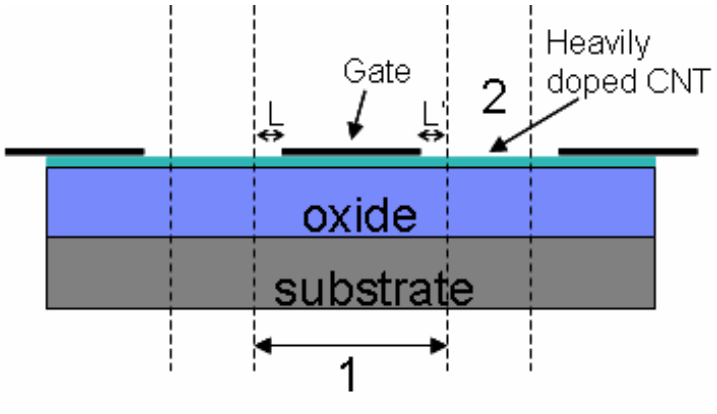
CNT MOSFET (projected)

J. Guo, A. Javey, H. Dai, M. Lunddstrom, "Performance analysis and design optimization of near ballistic carbon nanotube field-effect transistors," IEDM, p. 703 (2004).

Si n-MOS data is 70 nm L_G from 130 nm technology from Antoniadis and Nayfeh, MIT

CNFET Circuit-Level Performance Estimation





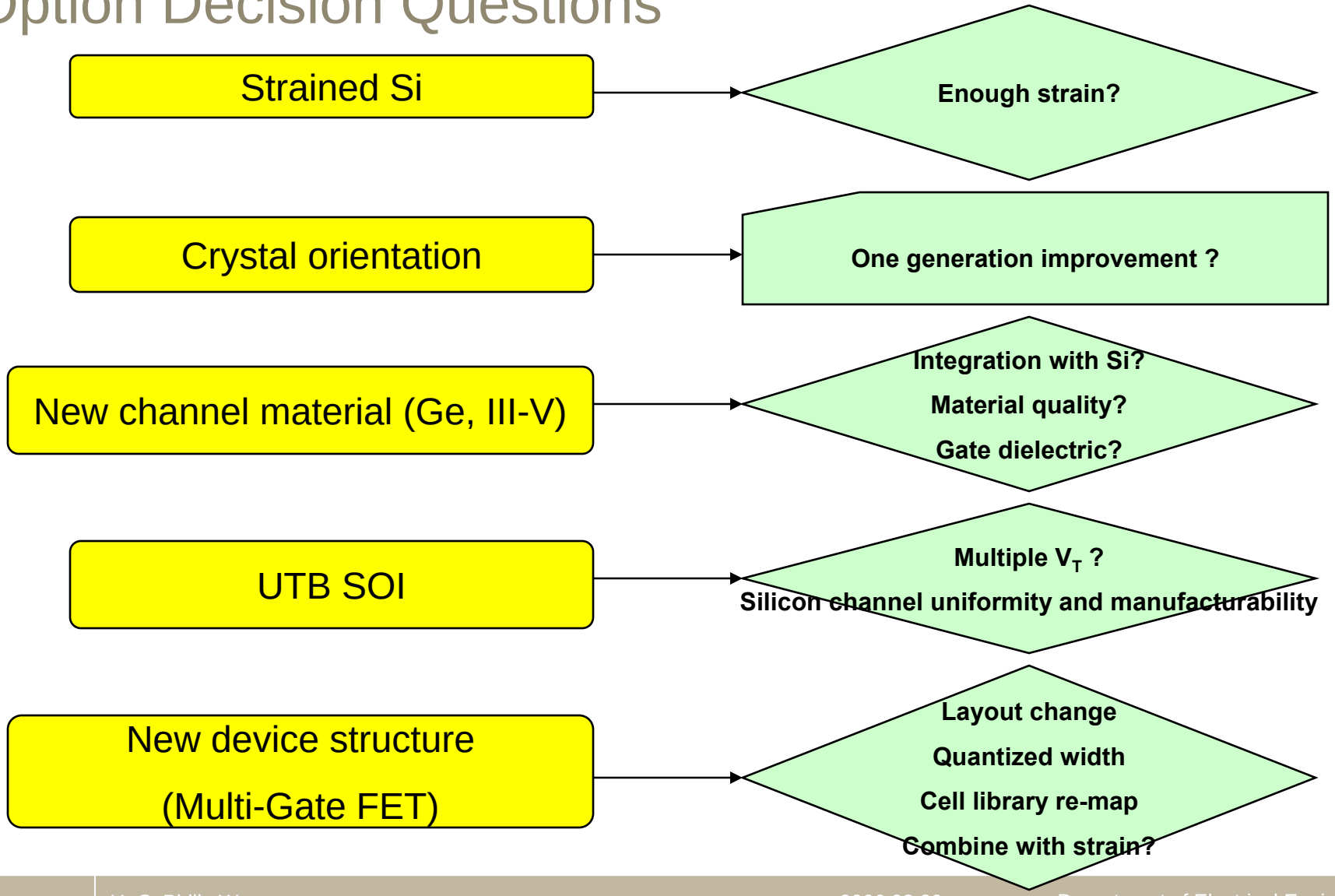

```
XNFET Drain Gate Source Sub  NFET  Lch=L_channel  Lss=L_sd  Ldd=L_sd  Wgate=sub_pitch
+                                  Rch=Rcnt  Rex=Rcnt  m=19  n=0  Mul=1

XPFET Drain Gate Source Sub  PFET  Lch=L_channel  Lss=L_sd  Ldd=L_sd  Wgate=sub_pitch
+                                  Rch=Rcnt  Rex=Rcnt  m=19  n=0  Mul=1
```

Nanotube chirality

Number of nanotubes

J. Deng, H.-S. P. Wong, *IEEE SISPAD (submitted)*, 2006.

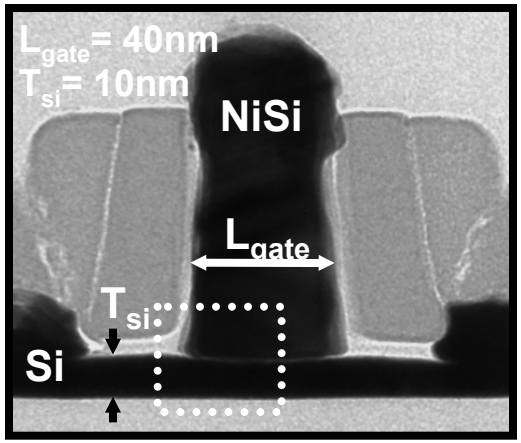
Option Decision Questions



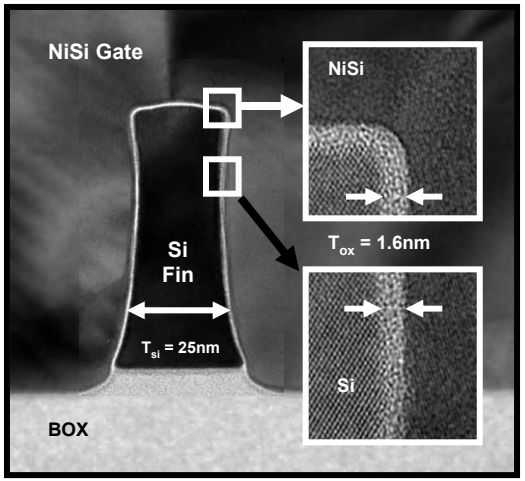
Technology Features Should be Additive

- **New materials and new device structures**
  - (a) Ultra-thin body FET
  - (b) Double- (or Multi-) gate FET
  - (c) Strained Si (bulk, on insulator)
  - (d) Ge (bulk, on insulator)
  - (e) High-k gate dielectrics
  - (f) Metal gates
  - (g) Crystal orientation

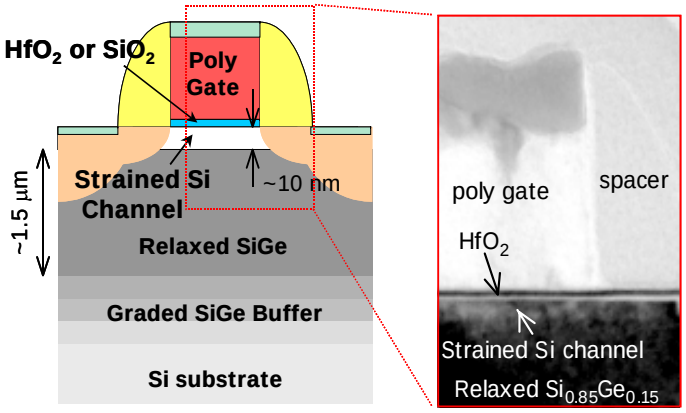
Demonstrated:
(a)+(c), (a)+(d), (a)+(e), (a)+(f)
(b)+(a) (b)+(f), (b)+(g),
(c)+(d), (c)+(e)
(d)+(e), (d)+(f), (d)+(e)+(f)
(e)+(f)
(g)+(e)



J. Kedzierski et al., *IEDM*, paper 18.4, 2003.



J. Kedzierski et al., *IEDM*, p. 247, 2002.



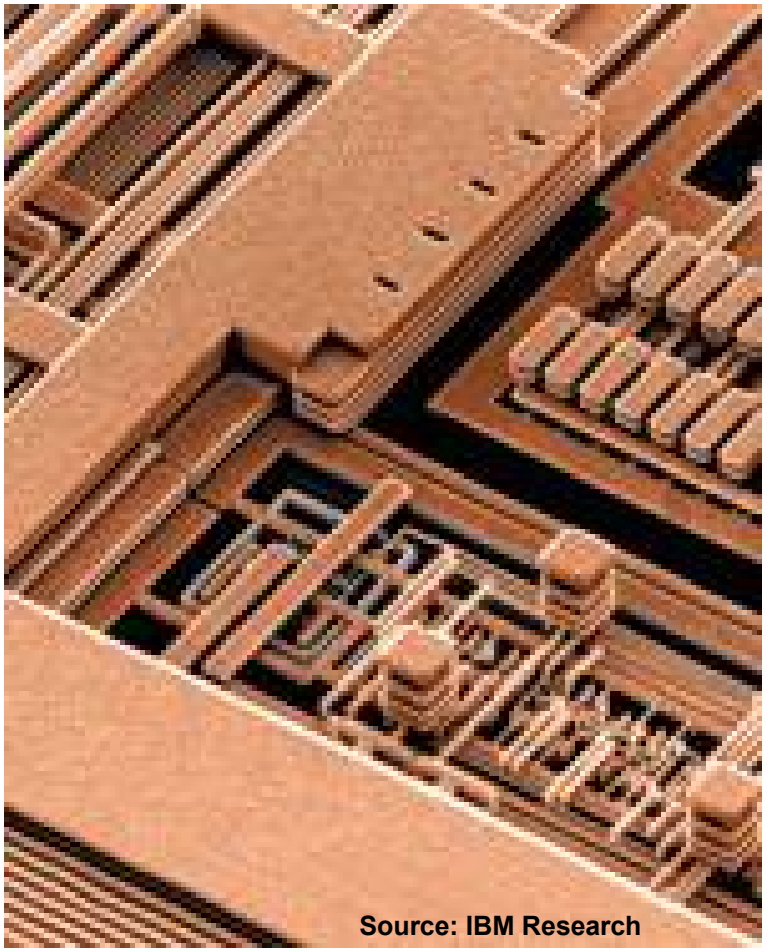
K. Rim et al., *Symp. VLSI Tech.*, p. 12, 2002.

Key Challenges

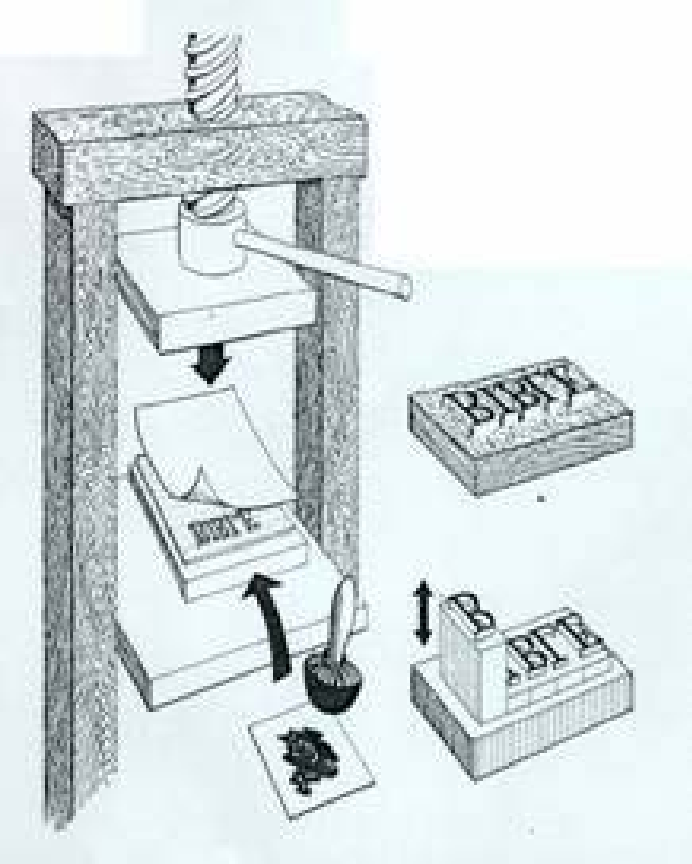
- **Power / performance improvement and optimization**
- **Variability**
- **Integration**
  - Device, circuit, system

Don’t forget these considerations

Today's Chip – Many Complex Shapes



Learn From The Past – The Printing Press



中國語言用大約3000 個常用的字。

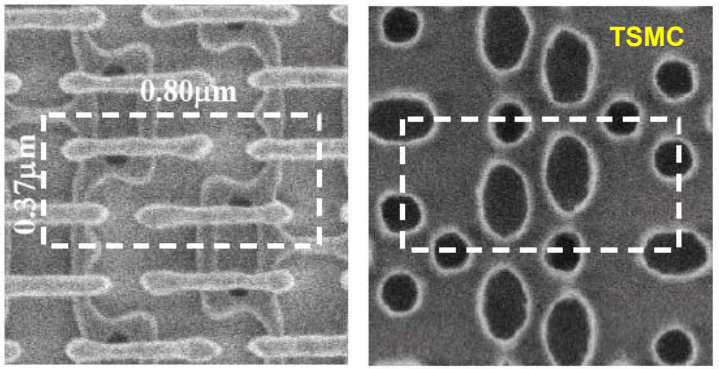
The Chinese language uses about 3000 common characters.

IT'S A LOT EASIER TO TYPE USING THE ENGLISH ALPHABET !

SRAM Cell Evolution

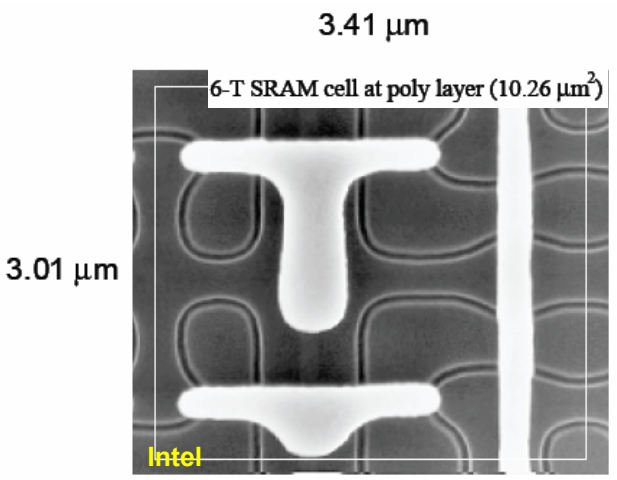
- **Cell layout evolved from arbitrary shapes to predominantly straight lines and holes**

45 nm CMOS



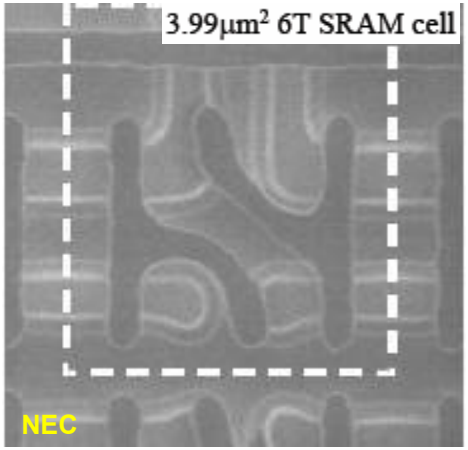
F.L. Yang et al., "45nm Node Planar-SOI Technology with 0.296μm2 6T-SRAM Cell" *Symp. VLSI Tech.*, pp. 8-9 (2004).

250 nm CMOS



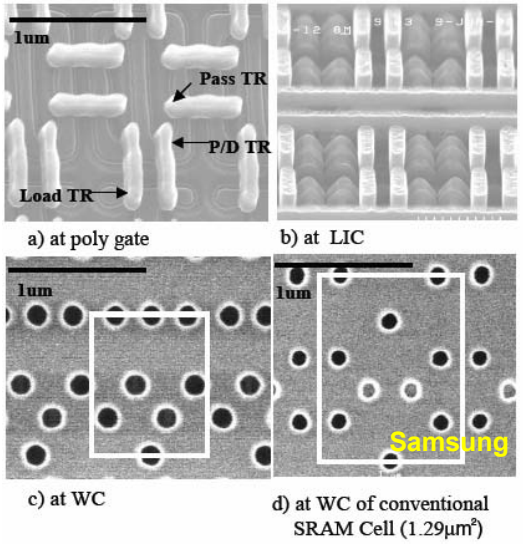
M. Bohr et al., "A high performance 0.25μm logic technology optimized for 1.8V operation," *IEDM Tech. Dig.*, pp. 847 - 850, December 1996.

130 nm CMOS



K. Imai et al., "A 0.13-μm CMOS technology integrating high-speed and low-power/High-density devices with two different well/Channel structures," *IEDM Tech. Dig.*, pp. 667 - 670, December 1999.

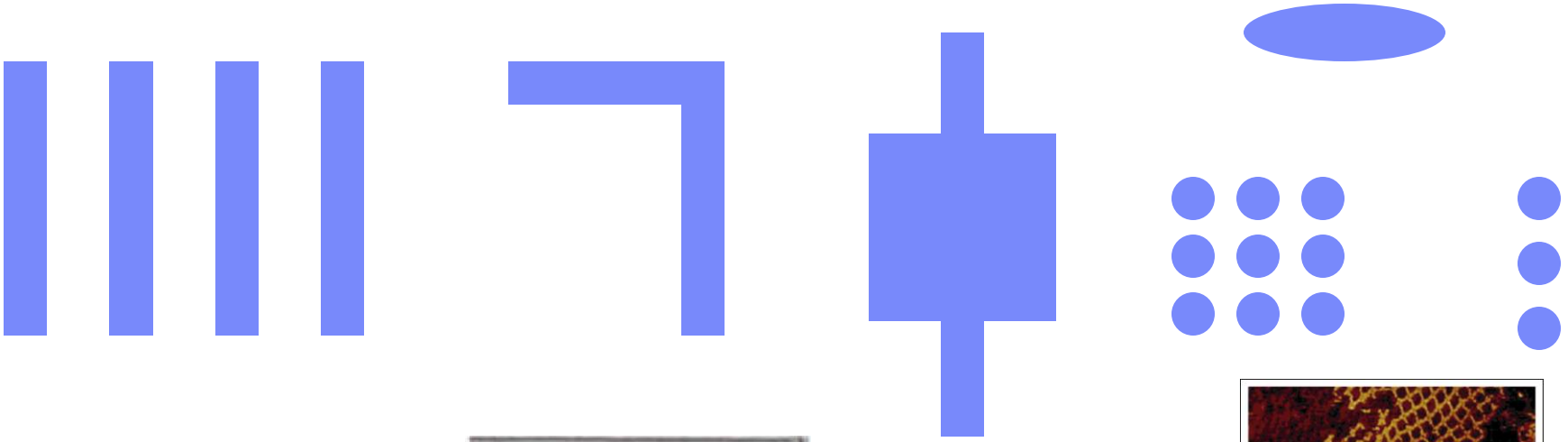
90 nm CMOS

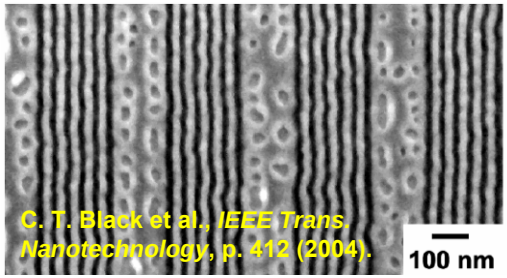


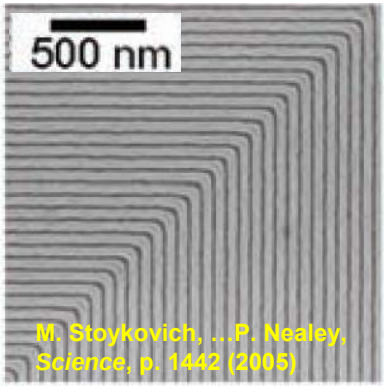
S.M. Jung et al., "A novel 0.79μm2 SRAM cell by KrF lithography and high performance 90nm CMOS technology for ultra high speed SRAM" *IEDM*, pp. 419 – 422 (2002).

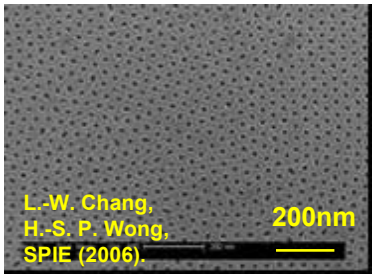
The Future of Physical Layout - Canonical Shapes

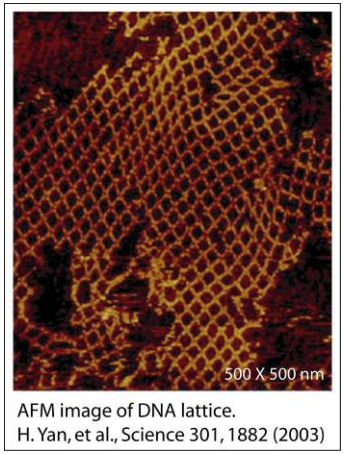
- **Freelance layout → litho re-design with assist features → regular fabric → strictly rely on canonical shapes**











Device Scaling Today

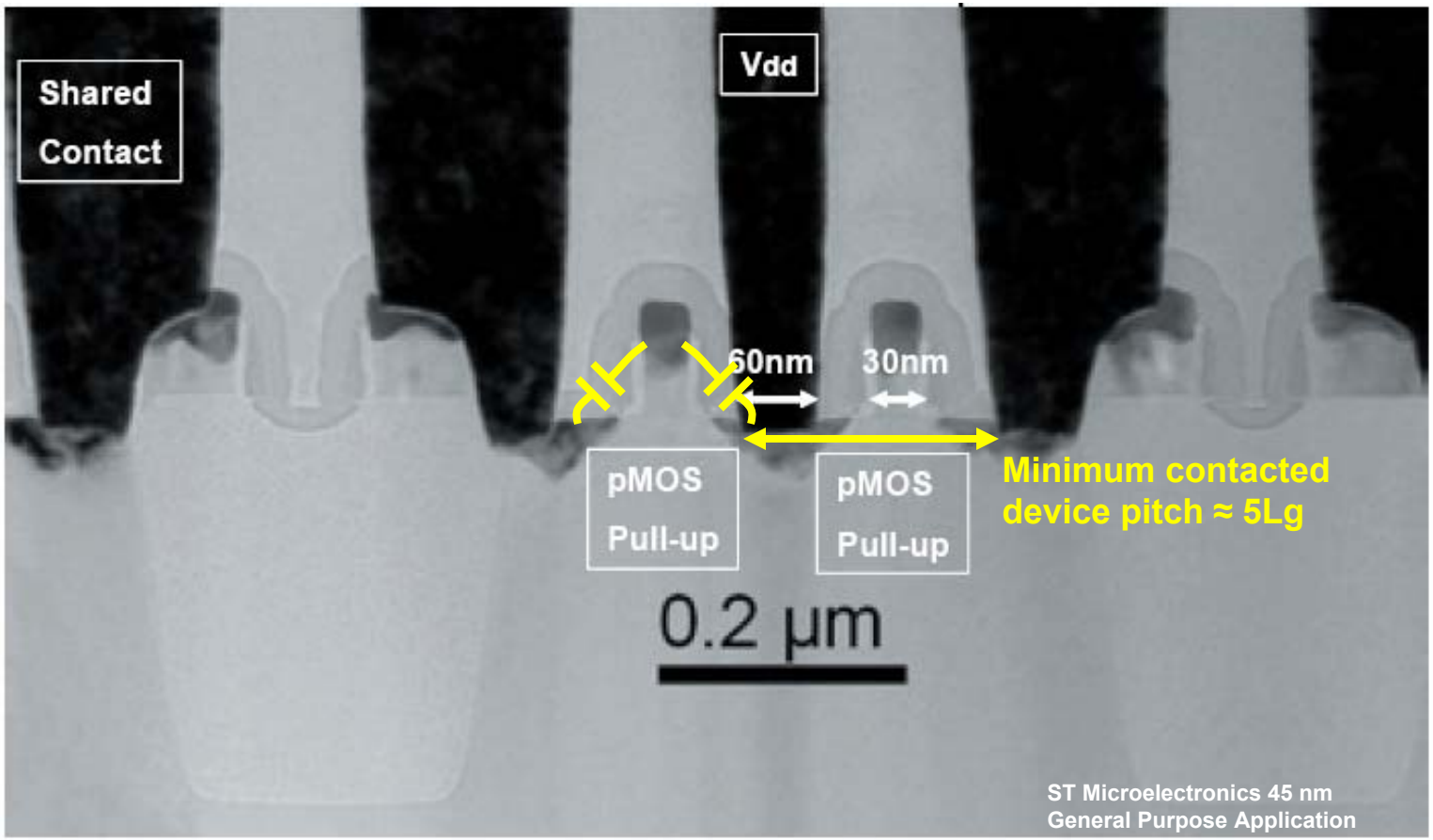


Fig. 12 : TEM cross section inside a 0.334µm² 6T-SRAM bit-cell

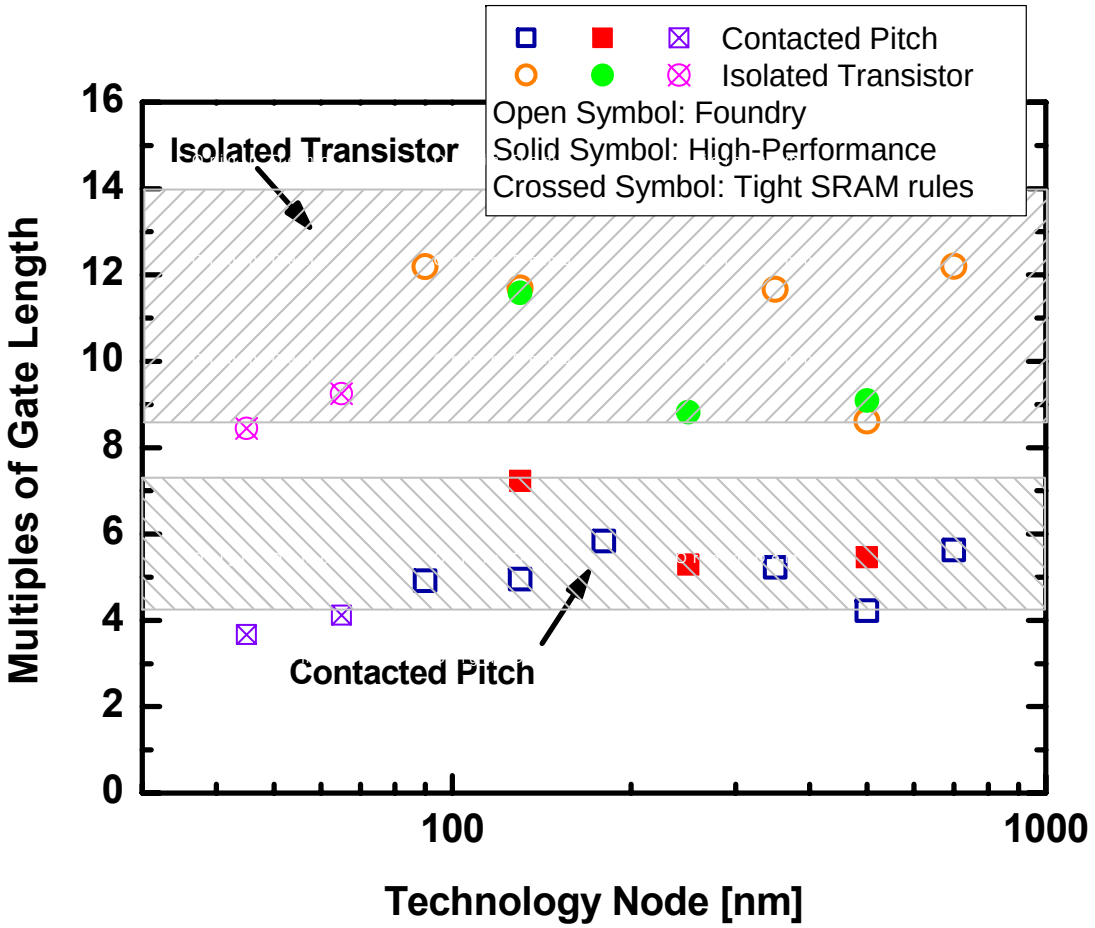
F. Boeuf…T. Skotnicki., *Symp. VLSI Tech.*, p. 130 (2005).

Future Of Device Scaling

- **Gate length scaling reaching diminishing return, due to**
  - Increasing leakage
  - Gate capacitance increasingly dominated by parasitic capacitance
    - Parasitics do not contribute to charge in the channel but load down the circuits
- **Smaller device footprint (high device density) still wins because wiring load will be reduced**
- **Net: reduce device footprint without scaling gate length**

FET Device Footprint

- **Device footprint scales with technology (historical data)**
- **This means:**
  - (a) scaling works (we all know that!)
  - (b) there is room for further innovation to reduce footprint



Isolated transistor: $16F^2$

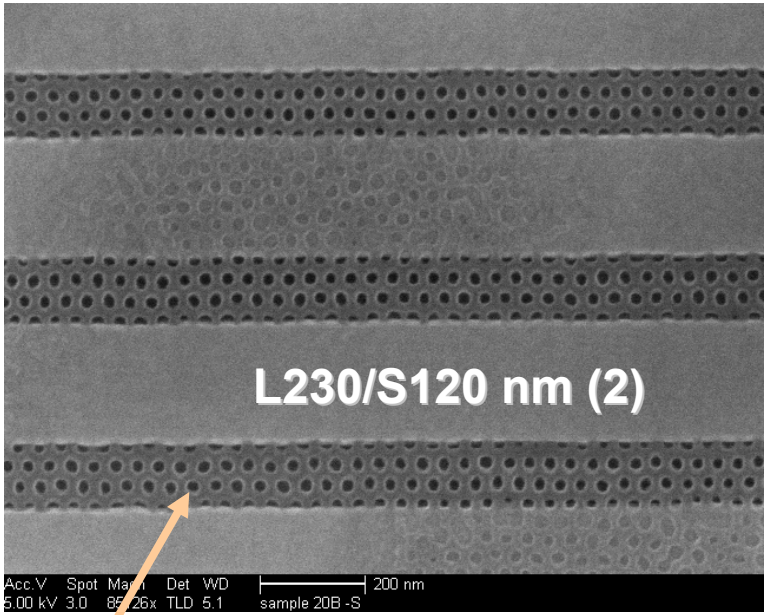
Contacted pitch transistor: $8F^2$

Including wiring, larger transistor sizes (W/L > 1): 25 - 64 F^2

Adapted from: H.-S. P. Wong, G. Ditlow, P. Solomon, X. Wang, *Intl. Conf. Solid State Devices and Materials (SSDM)*, p. 802, 2003.

Opportunities for Higher Device Density

- **Sublithographic device fabrication**
  - Regularized designs (no SRAF)
  - Sub-litho locally, conventional litho globally
  - Modular features based on canonical shapes
- **Novel process modules:**
  - Local metal strap
  - Low-k isolation
  - Low-k spacer



Self-aligned nanoscale contact holes using diblock copolymer self-assembly

L.-W. Chang, H.-S. P. Wong, *SPIE 31st International Symposium on Microlithography*, Feb 19 – 24, 2006.

Qualifying A Technology

Today:

- **Transistor and wiring level**
  - Process details (and errors) are hidden and quantified as "device behavior" (corners, ACLV…)
- **Design manual (SPICE model, layout rules)**
  - Performance is guaranteed at the transistor and interconnect level

Problem:

- **Device variation makes technology qualification difficult**
- **Performance (broadly defined as density, speed, power etc.) is left on the table**

Opportunity:

- **Future devices may not partition as devices/wires**
- **Logic and communication means may be intimately coupled**

Qualifying A Technology In The Future

- **Functional level**
  - Device details (and errors) are hidden and quantified as “circuit behavior” (timing, fan-out strength…)
  - Functional unit with local logic computation with global drive built-in
- **Design manual**
  - Performance is guaranteed at the functional level
- **Qualify a macro**
  - NAND gate, multiplier, register, storage cell, communication channel
- **Key need: define a canonical set of macros/system functions**

The Future

CMOS will be here to stay…till 10 nm gate

Smaller device footprint is goodness

- **Knobs (L_{gate}, μ, EOT) have been turned almost to the end**
- **New innovations offer opportunities to shrink contact size, overlay, isolation**
- **Don't only think lithography, think how to make features of a device**

Lithograpy:

- **Lithography features will be highly constrained**
- **Directed-assembly of canonical shapes at desired locations will assist lithography**

The industry will:

- **Define and develop a set of canonical circuit functions at the circuit macro level for**
  - Performance benchmarking
  - Hiding device details, improving fault tolerance
  - Technology qualification