The Case For High Aspect Ratio (HAR) Interconnects

Uri Cohen

UC Consulting

4147 Dake Avenue Palo Alto, CA 94306

Tel/Fax: (650)494-0268

uricohen@pacbell.net

Benefits of High Aspect Ratio (HAR) Interconnect

- ☺ Reduced RC-delays
- ☺ Reduced line resistance
- ☺ Reduced power consumption
- ☺ Reduced capacitance between adjacent metallization levels
- ☺ Reduced signal degradation & cross-talk
- ☺ Reduced heating, thermal stress, and stress-induced-voids (SIV) and electromigration (EM)
- ☺ SIV proportional to $1/(h)^{2.7}$ (h is line height)[1]; increased AR by 4X should reduce SIV by 40X!
- ☺ Reduced number of metallization levels
- ☺ Simplified CMP control (wider thinning window)

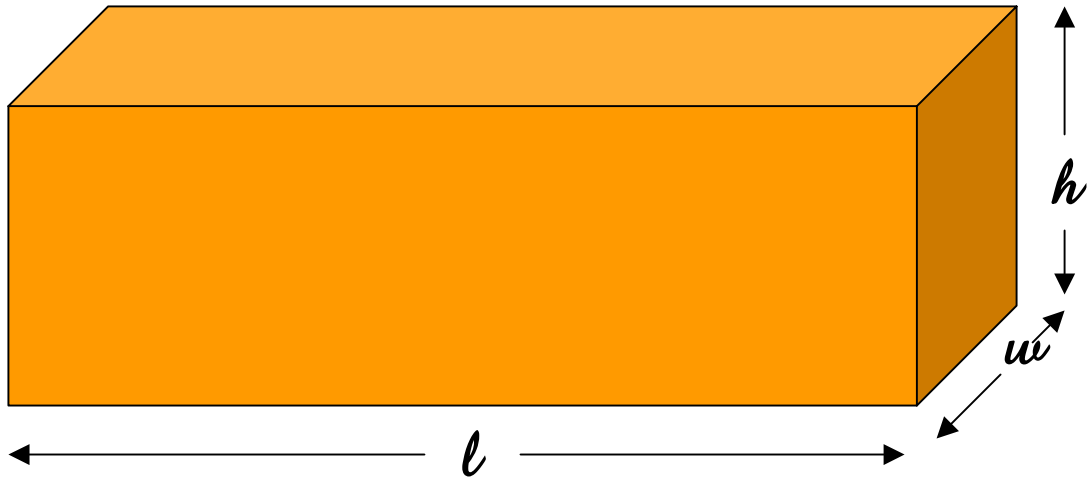
However, ITRS retains low-AR (LAR) of only 1.7:1 – 2.3:1

- **This implies shrinking the heights of vias and lines by the same scale factor used for the width**
- **As a result, line cross-section decreases as the square of the scale factor, and vias get shorter, which cause:**
  - ☹ Rapid increase of RC-delays
  - ☹ Rapid Increase of line resistance
  - ☹ Increased capacitance between adjacent metallization levels
  - ☹ Increased signal degradation & cross-talk
  - ☹ Increased heating, thermal stress, and related stress-induced-voids (SIV) and electromigration (EM)
  - ☹ Requires more metallization levels
  - ☹ Harder CMP control (tighter allowed variability or thinning)

Simulations: Higher AR Decreases RC-Delays

- **Due to surface scattering, line resistivity is proportional to the ratio A/V between the line's surface area (A) and volume (V)**
- **Inter-level capacitance is inversely proportional to via height (d) and to line height (h)[2]**
- **Doubling AR can reduce RC-delay by 30-50%, which is more than ultra low-k can accomplish**

Surface/Volume Ratio Decreases With Increasing Line Height



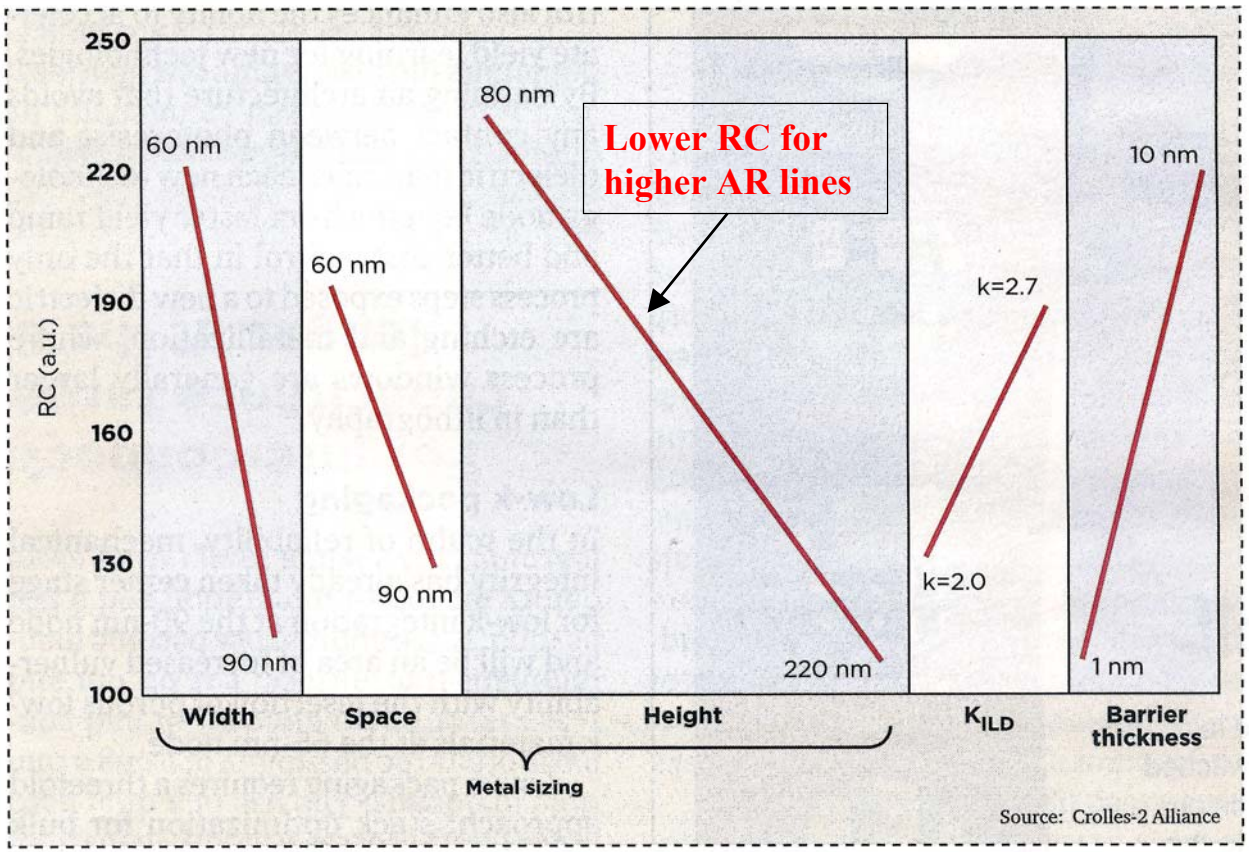
$$A/V = 2(lw + lh + wh)/lwh \approx 2(w + h)/wh$$

Assume: $h_1 = w$ (AR = 1:1); ⇨ $A_1/V_1 \approx 4.0/w$

Assume: $h_2 = 4w$ (AR = 4:1); ⇨ $A_2/V_2 \approx 2.5/w$

$$(A_2/V_2)/(A_1/V_1) \approx 2.5/4.0 = 0.63 \quad (37\% \text{ lower!})$$

RC Reduction by Thicker Lines



A single parameter variation influences modeled interconnect RC performance. Metal sizing and barrier thickness have a paramount effect on RC due to the exponential increase in copper resistivity.

O. Hinsinger et al., "Trade tips for scaling interconnects", EE Times, June 21, 2004[3]

RC Reduction by Thicker Lines

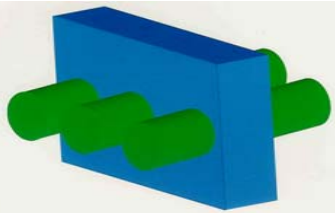


Figure 1: A 3D view of the cylindrical - shaped copper-low-κ interconnects.

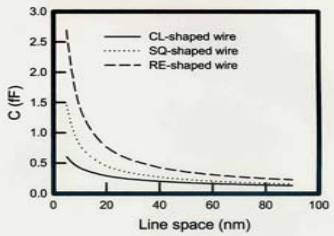


Figure 4: The calculated parasitic capacitance for the three interconnects with different line space.

← Lower C for CL shape

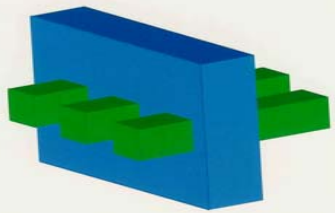


Figure 2: A 3D view of the square - shaped copper-low-κ interconnects.

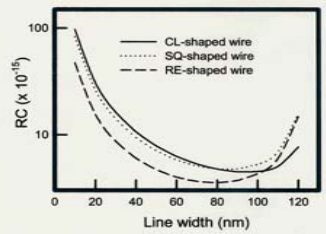


Figure 5: The RC time delay calculated for the three interconnects with different line width.

← Lower RC for RE shape

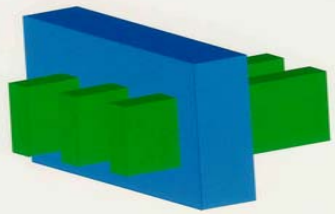


Figure 3: A 3D view of the rectangular - shaped copper-low-κ interconnects.

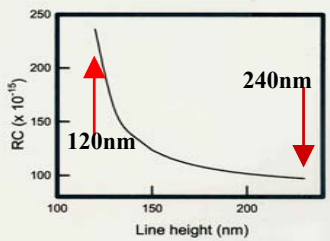


Figure 6: RC time delay of the RE-shaped interconnects with different line height.

← Lower RC for thicker (higher AR) RE lines

Yiming Li et al., Int. Workshop on Computational Electronics (IWCE-10), Oct. 2004[4]

Low-AR (LAR) Double-Whammy

- **Vias: Capacitance is inversely proportional to the dielectric thickness (d): C = kA/d**
  - Low-AR (LAR) shallow vias increase capacitive (noise) coupling between adjacent metallization levels!
- **Lines: Low-AR shallow trenches impair lines resistance: R = ρl/wh**
  - For line width **w** < 0.10μm, line resistivity **ρ** increases exponentially due to *surface and grain boundaries scatterings* (longer anneals reduce grain boundaries)
  - RC delays increase with shrinking **w** and/or **h**
  - Excessive power dissipation and heating ⇨ EM↑ & SIV↑
  - Signal/noise (integrity) degradation (due to IR-drop)
- ***Only reason for not using high-AR (HAR) is inability of PVD seed layer to provide full sidewalls coverage***

Ideal Seed Layers (SL)

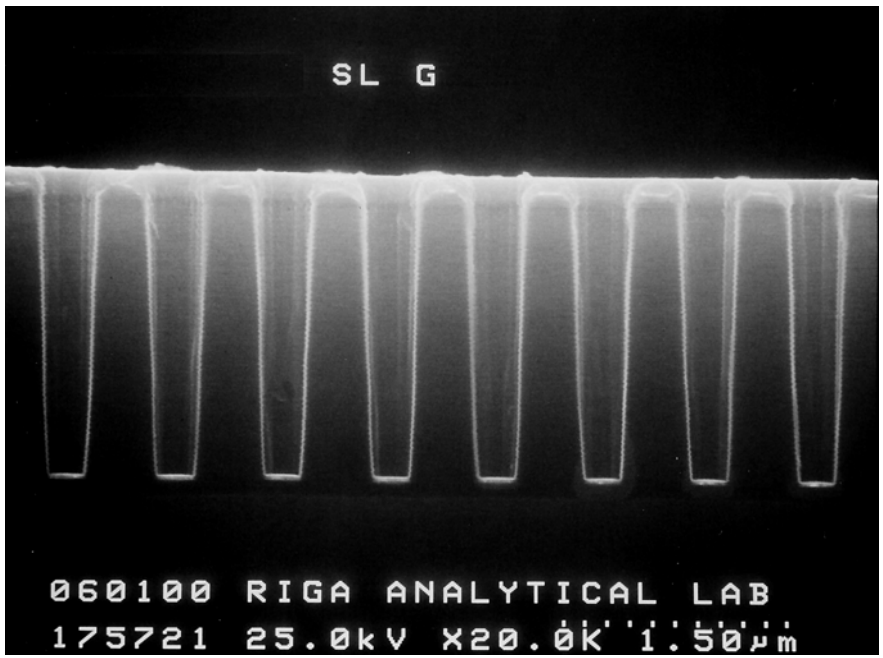
- Fully continuous sidewalls and bottom coverage of HAR openings, even with negative slopes, yet thin enough inside openings to avoid their pinching-off
- Sufficient thickness on the field for adequate surface conduction (minimize "Terminal Effect") for void-free electrofilling and good plating uniformity
- Minimal or no top corners overhangs
- SL should not be less noble than Cu in electrolyte
- SL should not develop oxide film in the electrolyte
- Excellent adhesion to the barrier, without any poor-adhesion spots, such as on negative slopes
- Consistent, robust, and highly reliable process
- High throughput deposition equipment

Combined Conformal and Non-Conformal Seed Layers[5-10]

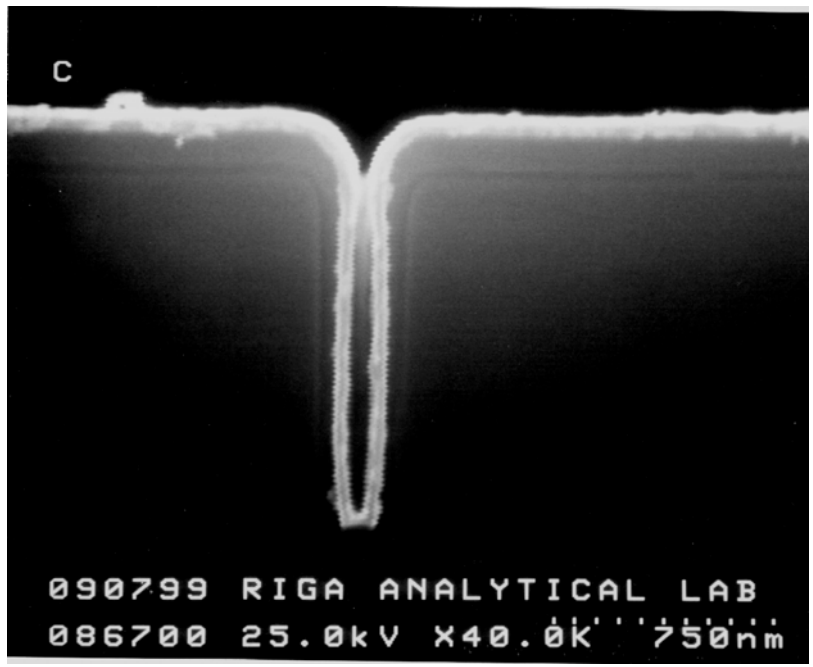
- Independent sidewalls and field coverages
- Fully continuous, thin coverage of bottom and sidewalls (including negative slopes)
- Adequate field thickness for void-free filling and plating uniformity
- Negligible overhangs when PVD SL is not required to provide fully continuous sidewalls coverage
- Excellent adhesion to barrier and plated Cu
- Robust and consistent process with high yields and reliability
- High deposition throughput: ~70 WPH

Conventional Seed Layers

(a)



(b)



Conventional Cu seed layers. (a) PVD seed layer; combined (Cu plus barrier): ~2,000Å on field and < 100Å on lower sidewalls; vias: ~0.25µm wide; 1.90µm deep; AR ~ 7.6:1. (b) CVD seed layer; combined (Cu plus barrier): ~450Å on field and sidewalls; trenches: ~0.13µm wide; 1.4µm deep; AR ~ 10.8:1

Problems with PVD Cu Seed Layers

ELECTRONIC ENGINEERING

EE TIMES

Issue 1233 www.eet.com The industry newspaper for engineers and technical management Monday August 26, 2002

Telcos' future: automation up, staffing down

By Craig Matsumoto

SAN JOSE, CALIF. – Telecom carriers must make severe changes–wholesale job cuts among them–for optical networking to fulfill its promise, speakers told the Opticon conference last week.

'The telecom vendors are just now learning how to live in a cyclical industry.'

A traditional, labor-intensive network is too expensive to maintain, these speakers insisted, so carriers must instead go to an automated, point-and-click operation.

Staggering through telecom's first down cycle after decades of steady if unspectacular growth, optical networking executives and engineers gathered here to assess the state of their battered industry. Understandably, the plunge was compared to the chip world's rhythmic ups and downs.

Via failures plague copper interconnect at 130 nm, forcing changes in design practice

Next-gen processes stare into the void

By Ron Wilson

SAN MATEO, CALIF. – Yield and reliability issues threaten the touted dual-damascene copper interconnect structures of leading 130-nanometer processes, having caused both poor yields at wafer sort and unacceptable failure rates over the life of apparently good chips, according to a wide range of industry sources.

Some of the mechanisms leading to those problems can be controlled by an unprecedented level of attention to processing steps, and leading foundries have demonstrated such devotion to detail in recent months. But other problems are inherent in the structure of the new interconnect stacks and can be addressed only by design rule changes and by changes in design practice, some reaching clear back to the architectural levels of design.

Thus, what first appeared in mid-2001 to be a detailed process issue has become an architectural consideration for chip connect stack. The failures are specific to dual-damascene copper metal stacks, and the issues involved appear to affect all current processes, though foundry response to the problems has reportedly varied by vendor.

Early in the progress of 130-nm production, it was observed that some vias–even though they appeared to be correctly imaged and formed–were not connected or presented such a high resistance that they had a major electrical impact on the circuit. Later, it was discovered that those effects could appear during accelerated engineers–infant mortality.

"In some cases we were still seeing new failures after 300 hours of stress testing," reported one insider at a fabless vendor.

It was necessary to identify the failure modes and correct the problem before declaring 130-nm processes fully production-ready. Yet the lack of surface defects–the usual cause of circuit failures in ICs–or of visible surface abnormalities concerned process integration engineers.

The problem turned out to be a confluence of several failure mechanisms, according to Bob Havemann, vice president of technology, process integration and applications at Novellus Systems Inc. (San Jose, Calif.). "It's ironic that copper was ballyhooed for its superior reliability in IC interconnect," Havemann observed. "It can in fact be highly reliable, and it's not as subject to some of aluminum's problems,

CONTINUED ON PAGE 98

A slew of detailed process problems can lead to via failures.

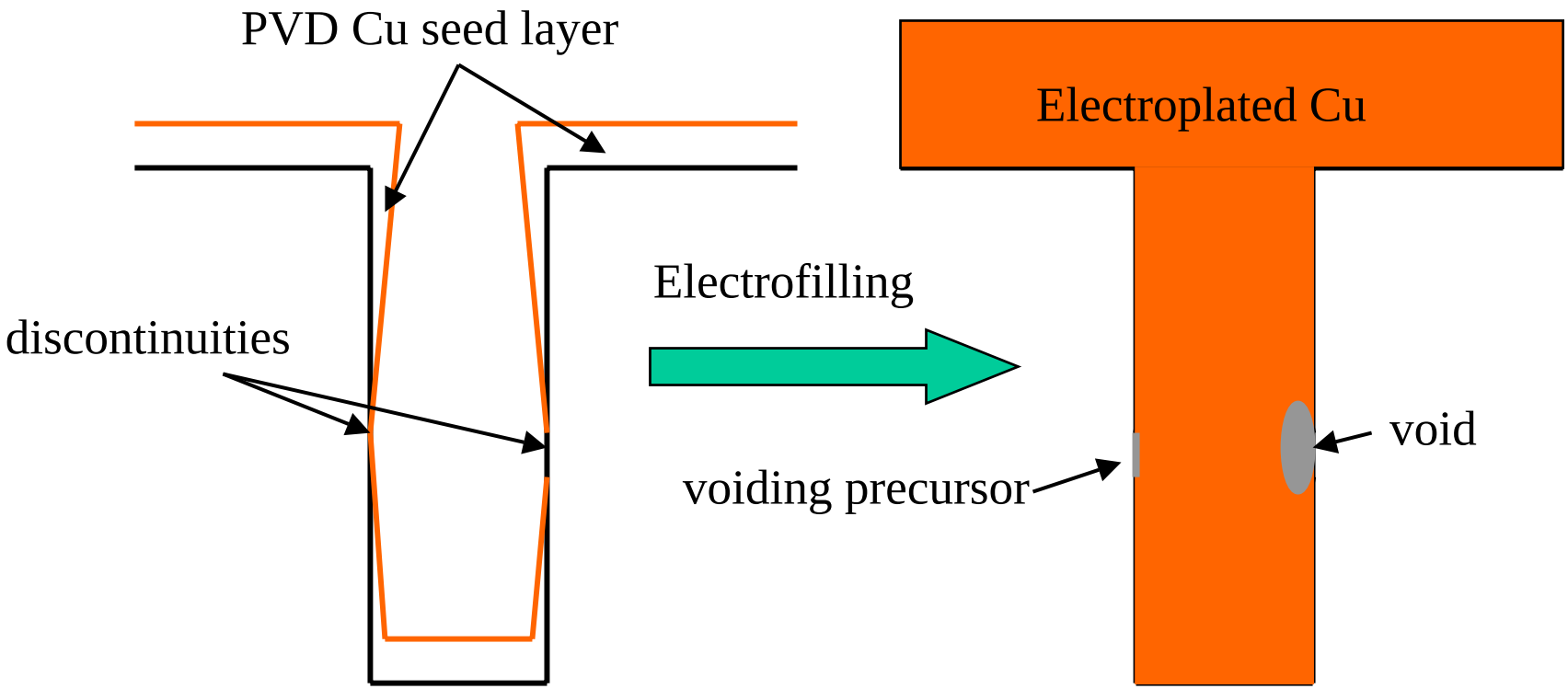
Vias can pull away from the metal layer.

Andiamo bid may rev iSCSI rollout, force Fibre Channel shakeout

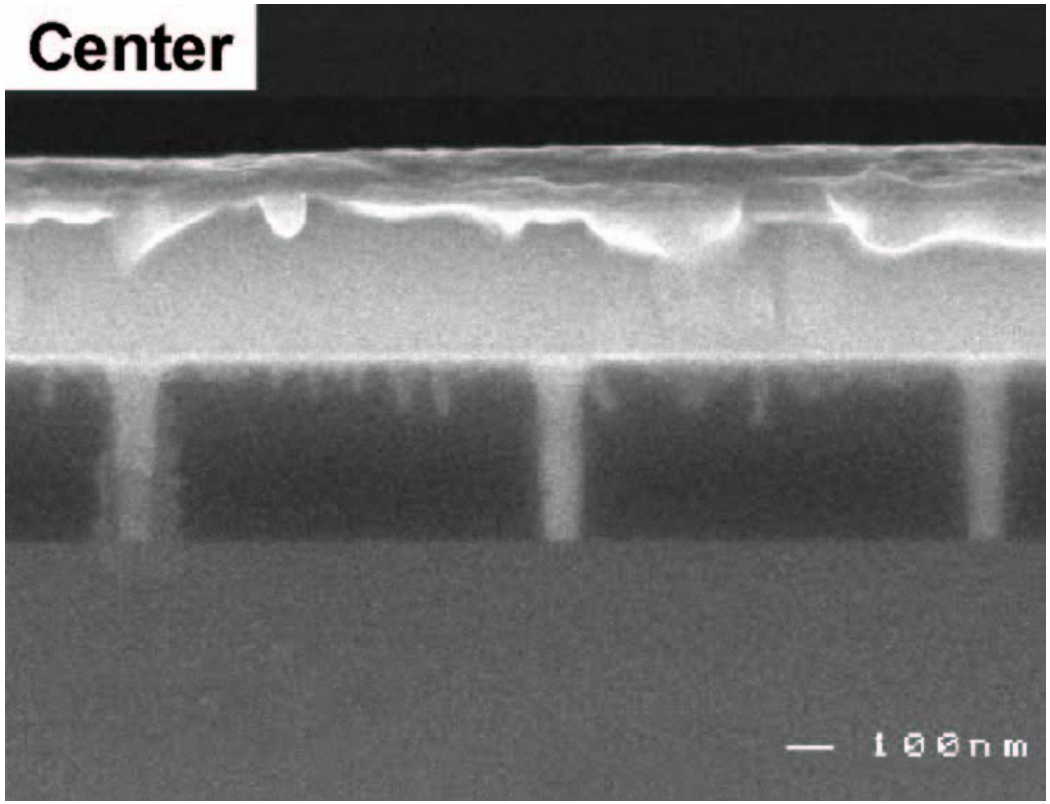
Reference [11]

Problems with Non-Conformal PVD Seed Layers (SL)

High Aspect Ratio (HAR) Opening



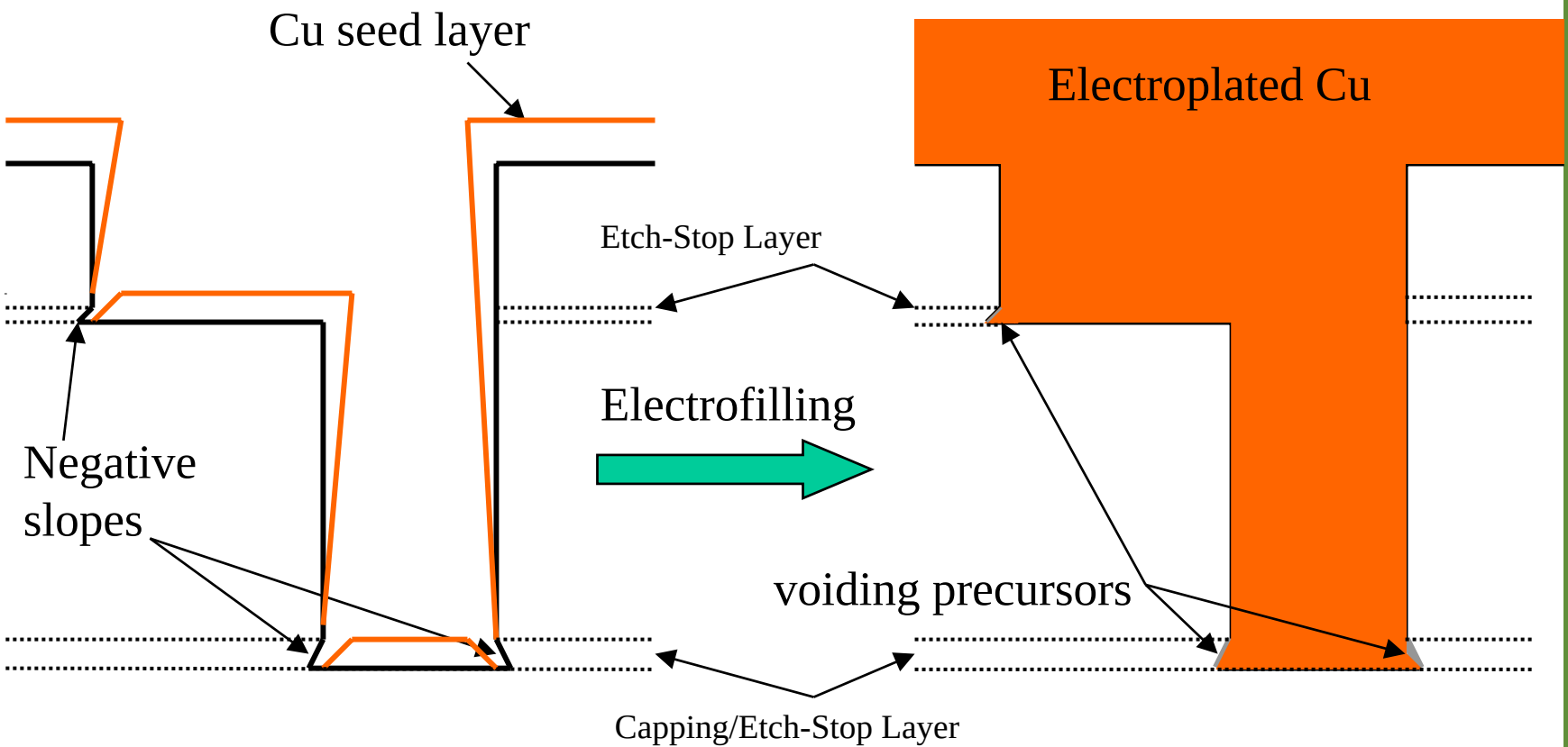
Entrapped Electrolyte In Voids



Gap-Filled Results: 0.10µm, 4.5:1 A/R vias; gap-filled demonstrated using 500Å thick PVD Cu seed – from Applied Materials' Website (Semicon 2003).

Problems with Non-Conformal PVD Seed Layers

Dual Damascene



Problems with Non-Conformal PVD Seed Layers

- PVD Cu S.L. → Low Reliability/Yields
  - Negative slope sidewalls in retrenching features and in undercut crevices, nooks, and recesses[12] (due to over-etched multiple dielectrics in Single and Dual Damascene features)
  - Non-Conformal PVD deposition results in inadequate sidewall (or step) coverage, leading to filling-voids and stress-induced voiding (SIV)[13-15]
  - Simultaneous exposure of barrier and Cu SL to electrolyte accelerates the SL corrosion. Interfacial stress at the SL/Barrier interface also accelerates SL corrosion. Cu SL corrosion leads to filling voids

Problems with Non-Conformal PVD Seed Layers

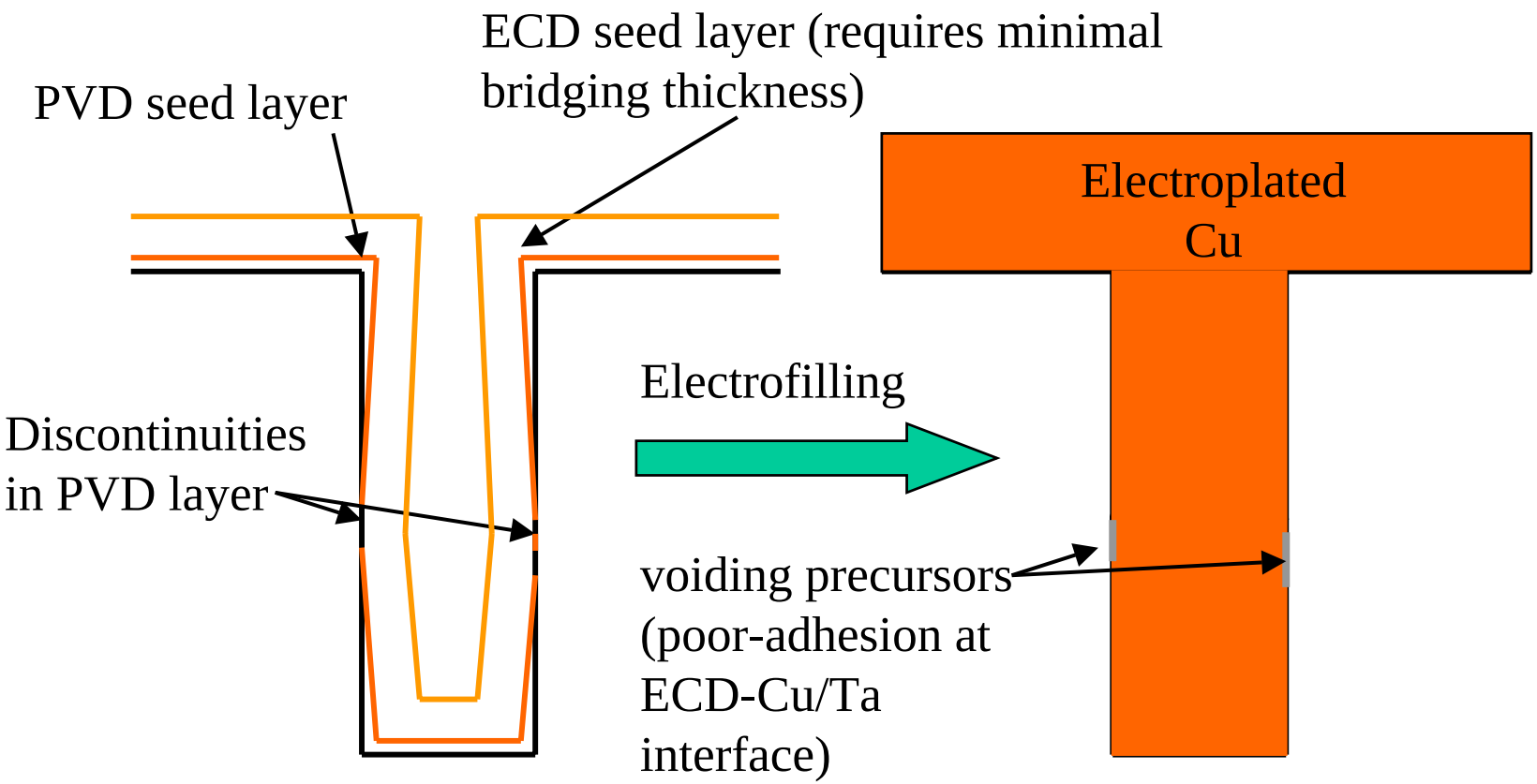
- Preplating activation in the electrolyte is compromised or eliminated, leading to defects & impaired adhesion
- Initial plating current density must be high to suppress SL corrosion. This may result in "terminal effect" and filling voids in the narrowest features
- Interfacial oxides and poor-adhesion of electroplated copper onto exposed barrier sites result in filling-voids and/or SIV-precursors
- Microvoids coalesce (under thermal and/or electrical stresses) to larger voids, resulting in vias void pulls[11]
- Vendors' assertions that a single PVD SL is adequate for future nodes are problematic since it already plays a critical role in poor reliability (SIV and EM) and yields

Problems with Other Seed Layers

- Conformal ALD, CVD, Electroless, and ECD Cu Seed Layers (on barrier)
  - » Slow deposition results in low throughput
  - » Too thick on sidewalls, yet too thin on field
  - » Too thin SL on field: ⇨ "terminal effect" (> 100%), filling-voids, and contact-loss by mechanical wiping and/or bipolar seed dissolution[16]
  - » Poor-adhesion of electroless and ECD Cu on barrier
  - » Poor uniformity and rough deposits (except ALD)
  - » High impurities and resistivity levels
  - » Electroless and ECD require additional equipment

Problems with ECD & Electroless "Repair" Seed Layer

High Aspect Ratio (HAR) Opening



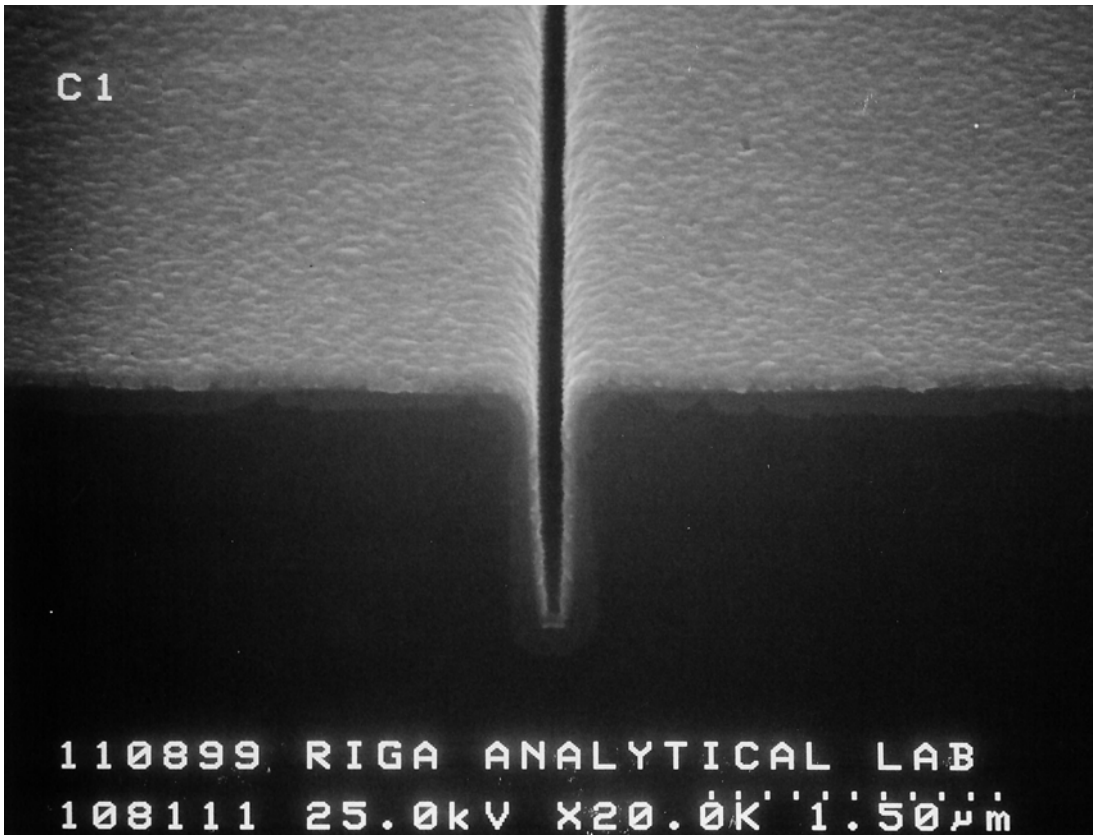
Problems with ECD & Electroless "Repair" Seed Layers

- Electroless or ECD "Repair" SL (on PVD)[17-22]
  - Electroless is extremely hard to control process: Erratic initiation time and deposition rate due to bath aging. Also, hydrogen blistering and high via resistance[22]
  - Require minimum "bridging" thickness of Cu on the sidewalls, thereby limited to certain size features
  - Too thick on sidewalls yet too thin on the field
  - Voiding-precursors at exposed barrier sites due to local formation of Ta-oxide passive film, and poor adhesion of the "repair" ECD or electroless Cu SL to the passive film
  - High level of impurities and resistivity of seed
  - Slow deposition results in low throughput
  - Require additional equipment

Combined Conformal and Non-Conformal Seed Layers[5-10]

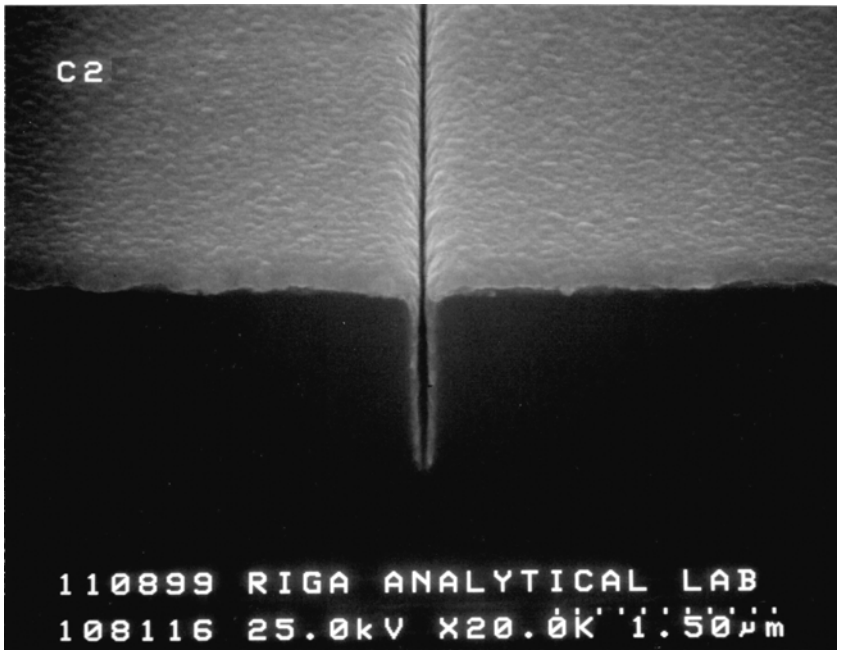
- Independent sidewalls and field coverages
- Fully continuous, thin coverage of bottom and sidewalls (including negative slopes)
- Adequate field thickness for void-free filling and plating uniformity
- Negligible overhangs when PVD SL is not required to provide fully continuous sidewalls coverage
- Excellent adhesion to barrier
- Robust and consistent process with high yields and reliability
- High deposition throughput: ~70 WPH

Combined Seed Layers

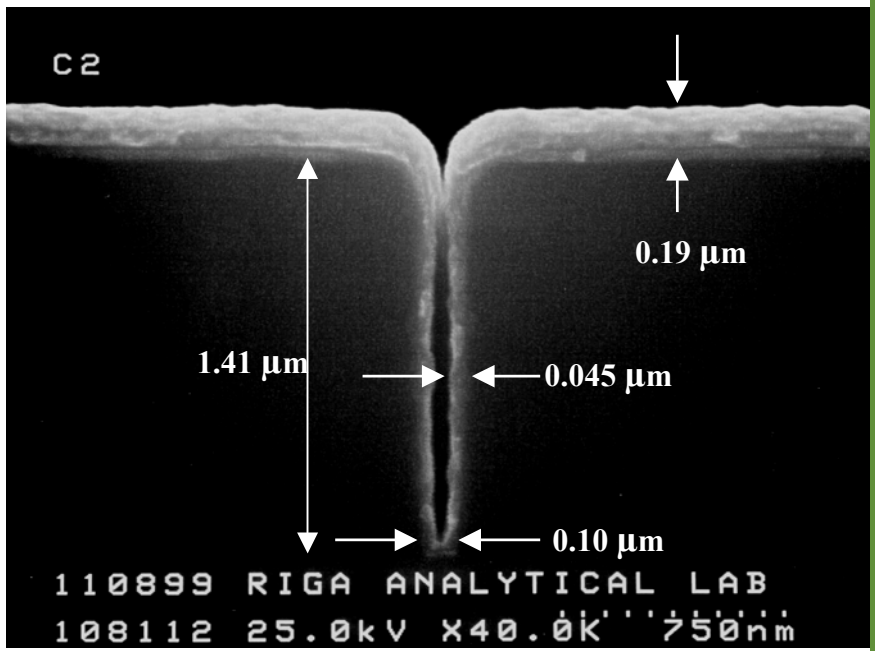


PVD/CVD seed layers: ~450Å (including barrier) on sidewalls and ~1,000Å on field.
Trenches: ~0.13µm wide (bottom); 1.4µm deep; AR ~ 10.8:1; tilt =30°.

Combined Seed Layers



(a)



(b)

PVD/CVD seed layers: ~450Å (including barrier) on sidewalls and ~1,900Å on field. Trenches: 0.10µm wide (bottom); 1.4µm deep; AR = 14:1.
(a) Mag. = 20,000X; Tilt = 30° and, (b) Mag. = 40,000X; No tilt.

Future Seed/Barrier Layers

- PVD/ALD Ta/TaN barrier begins to make inroads
- Excellent conformal bottom and sidewalls coverage for features ≤ 0.10μm: by ALD (or CVD) SL of Cu or Ru
- Adequate field thickness by PVD-Cu, essential for robust electrofilling and adequate wafer uniformity
- Excellent adhesion to the barrier (PVD-Cu, ALD-Ru, or ALD-Cu)
- Robust process and high yields and reliability
- High deposition throughput (~70 WPH)
- PVD-Cu & ALD-Ru (or Cu) seed layer combinations capabilities already exist[23-24]!
- SL combinations will greatly improve reliability and yields, and will enable HAR interconnects and their benefits

Combined ALD/PVD Seed Layers

- **Enable HAR vias and lines with aspect ratio AR ≥ 4:1-10:1 ⇨ to realize HAR benefits**
- **Improve significantly void-free electrofilling and reduce SIV and EM**
- **Robust, reliable, and consistent process**
- **ALD Ru (or Cu) and PVD Cu seed layers capabilities already exist[23-24]**
- **Demand combined ALD/PVD SL from your equipment vendor!**

Summary

Demonstrated:

- **Non-Conformal/Conformal PVD/CVD Cu S.L. for openings ≤ 0.10µm (AR ≥ 14:1), barrier plus seed: ~45nm on sidewalls, and ~190nm on field, with excellent continuous bottom and step coverage**
- **U. Cohen's IP[5]: Six issued Seed Layers Patents and several Pending Patent Applications**

Future:

- **ALD & PVD or CVD & PVD SL combinations will enable robust and reliable HAR interconnects**
- **HAR interconnects will greatly benefit performance and extend the technology beyond current capabilities**

REFERENCES

1. G. B. Alers, “45nm Reliability Issues", Novellus System’s website link: http://www.Novellus.com/NR/rdonlyres/E2C79565-D703-4C08-9A02-D744FAA94A02/0/050605_45nm_reliability_issues.pdf
2. P. A. Kohl, “Air: The Material Of The Future”, Future Fab Int.., Issue 17 (July 2004), pp. 19-21.
3. O. Hinsinger et al., EE Times, June 21, 2004.
4. Yiming Li, et al., Int. Workshop on Computational Electronics (IWCE-10), Purdue Un., Indiana, Oct. 24-27, 2004.
5. U. Cohen, U.S. Patents Nos. 6,136,707 (10/24/00); 6,518,668 (2/11/03); 6,610,151 (8/26/03); 6,903,016 (6/7/05); 6,924,226 (8/2/05); Taiwanese Pat. No. 165310 (3/5/03); and several Pending Applications.
6. U. Cohen et al., 17th Intl. VLSI Multilevel Interconnect Conference (VMIC), pp. 21-26, June 2000.
7. U. Cohen et al., SEMI Technical Symposium, Semicon West, pp. 819-834, July 2001.
8. U. Cohen, 18th Int. VLSI Multilevel Interconnect Conference (VMIC), pp. 165-167, September 2001.
9. C. H. Lee et al., 2000 International Interconnect Technology Conference (IITC), pp. 242-244, June 2000.
10. C. Block et al., 2001 International Interconnect Technology Conference (IITC), pp. 210-212, June 2001.
11. R. Wilson, “Next-gen processes stare into the void”, EE Times, 8/26/02.

REFERENCES (Continued)

12. J-H Son et al., Adv. Metallization Conf. (AMC) 2002, pp. 227-237.
13. J.B. Shaw et al., Yield Management Solutions, pp. 8-12, Winter 2002.
14. P. Marella et al., Yield Management Solutions, pp. 17-28, Spring 2003.
15. M. Data et al., Pat. Appl. Publ. No. US 2002/0064592 (5/3/02).
16. J. Jorne, Semiconductor Fabtech, 11th Ed., pp. 267-271, Feb. 2000.
17. T. Andryuschenko et al., 2001 International Interconnect Technology Conference (IITC), pp. 33-35, June 2001.
18. S. Gandikota et al, 2001 International Interconnect Technology Conference (IITC), pp. 30-32, June 2001.
19. C. Witt et al., 2002 International Interconnect Technology Conference (IITC), pp. 259-261, June 2002.
20. L. L. Chen, U.S. Patent No. 6,197,181 (03/06/01)
21. Andricacos et al., U.S. Patent No. 6,395,164 (05/28/02).
22. P. H. Haumesser et al., “Seed Enhancement: A Bridging Technology”, Future Fab Int., Issue 19 (July 2005), pp. 81-83.
23. B. M. Basol, "System and Method for Defect Free Conductor Deposition on Substrates", Pat. Appl. Publication No. US 2005/0095846 (5/5/2005).
24. S. Ganguli, "Applications of Metal ALD Film in Semiconductor Fabrication", ALD 2005 Conference, San Jose, California, Aug. 8, 2005.