Trikon Technologies, Inc.

CVD deposited low k dielectrics for gap-fill applications.

John Macneil

Contents

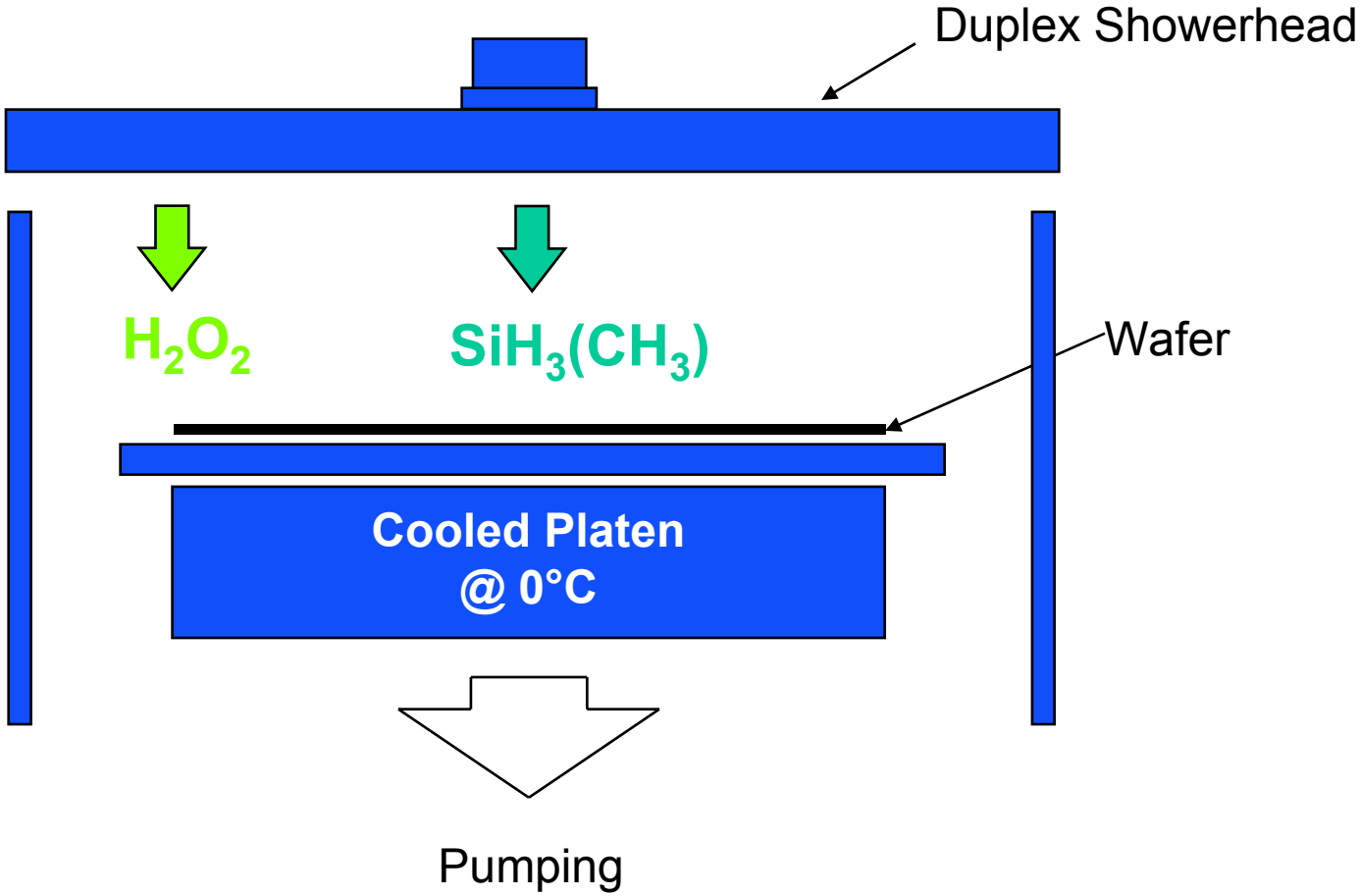
- Application requirements.
- Low k Flowfill deposition process
- Film Properties
- Applications
  - PMD
  - IMD
- Extendibility
- Summary

Application requirements.

	Process	Drivers
STI	Flowfill / Low k Flowfill	gap fill (8:1); temperature (~1000^{o}C), capacitance (?)
PMD	Low k Flowfill	gap fill (10:1); temperature (NiSi) (<400^{o}C); capacitance (k~ 3-3.5)
IMD	Low k Flowfill	gap fill (3-4:1); capacitance (k ~2.5-2.8), temperature ((<500^{o}C);

Low K Flowfill® Process Overview

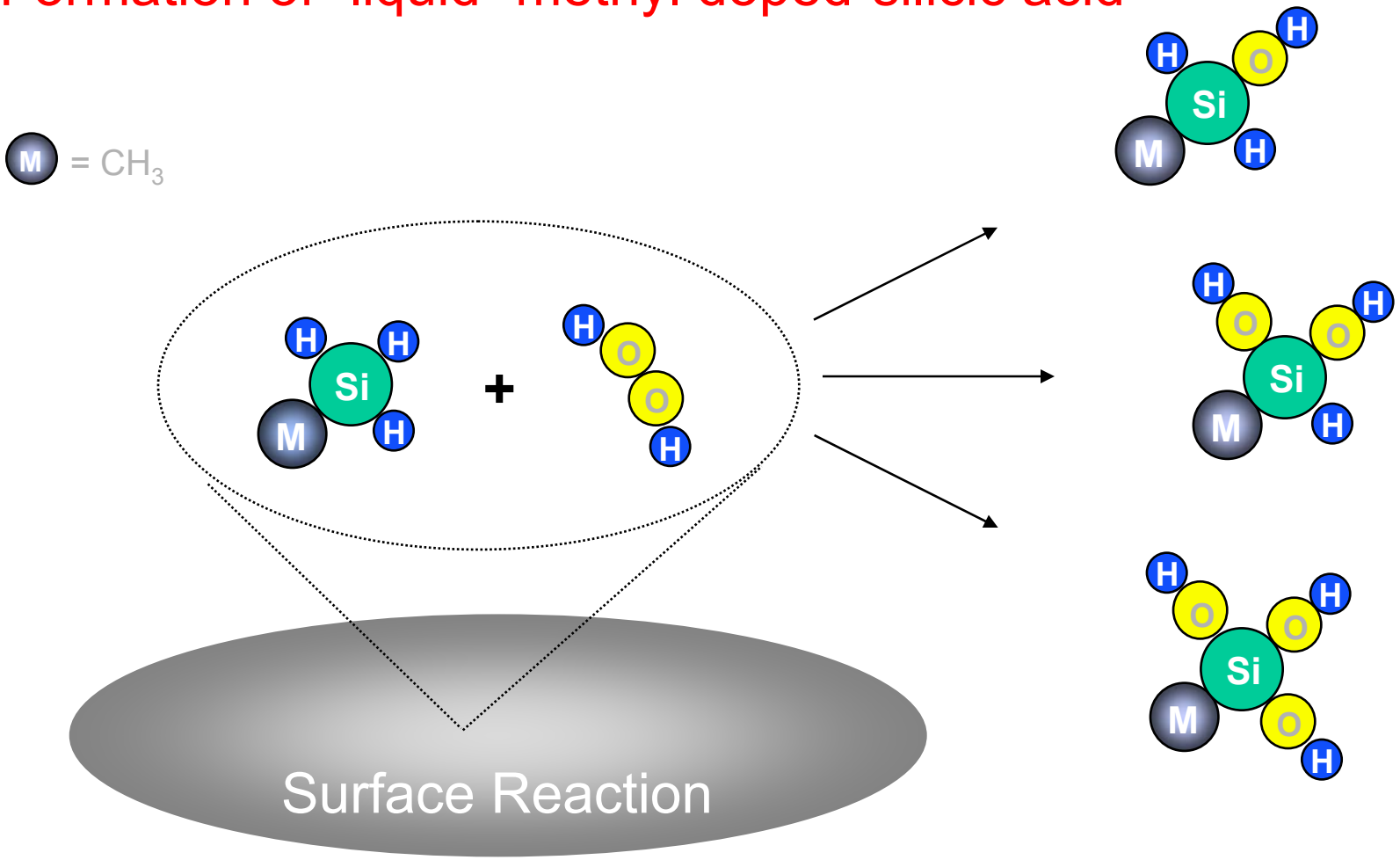
Low K Flowfill Chamber Schematic



- Direct CVD – no plasma enhancement

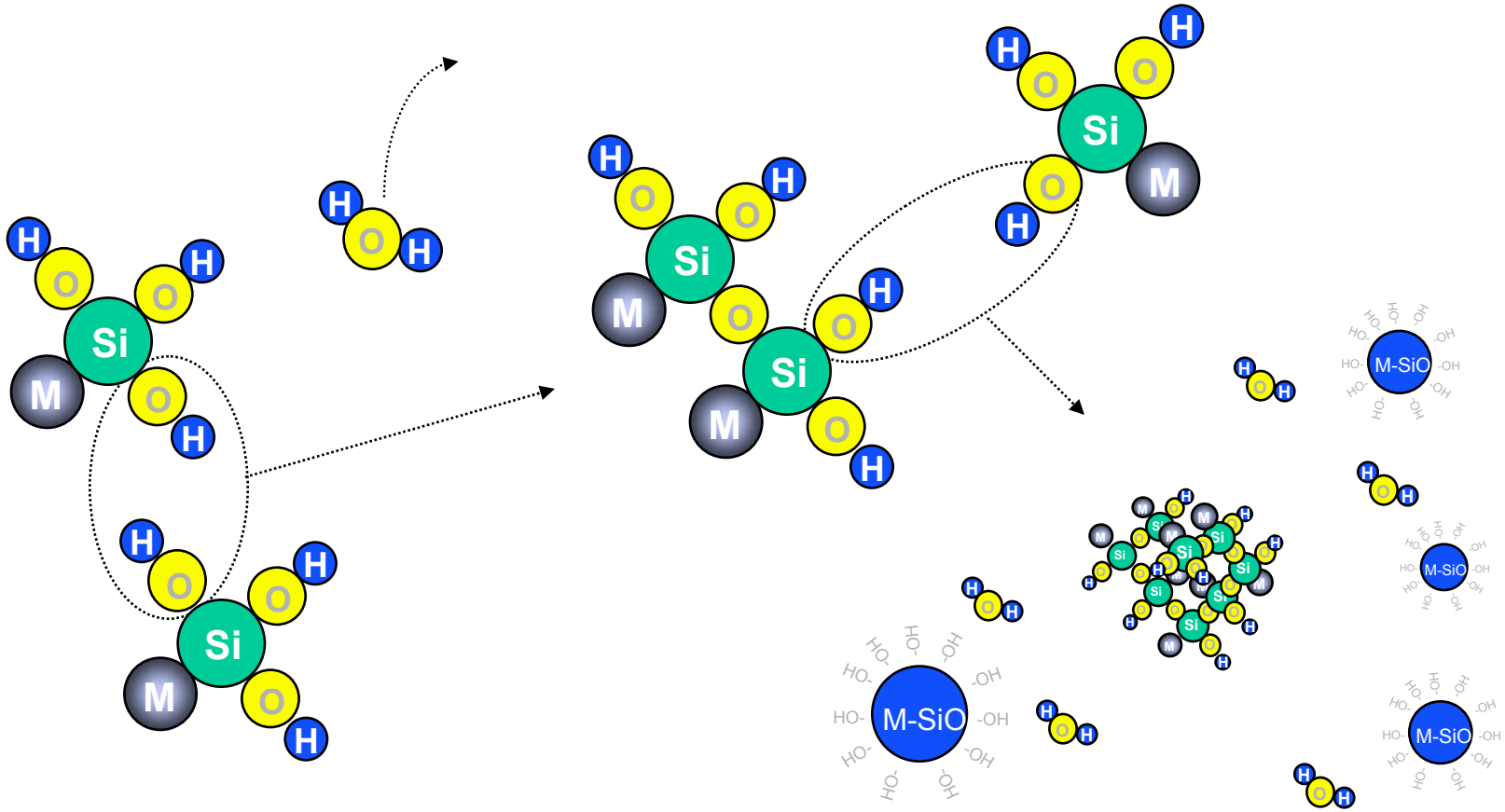
Low-k Flowfill® Chemistry

Formation of “liquid” methyl doped-silicic acid



Low-k Flowfill® Chemistry

Polymerisation via condensation reactions

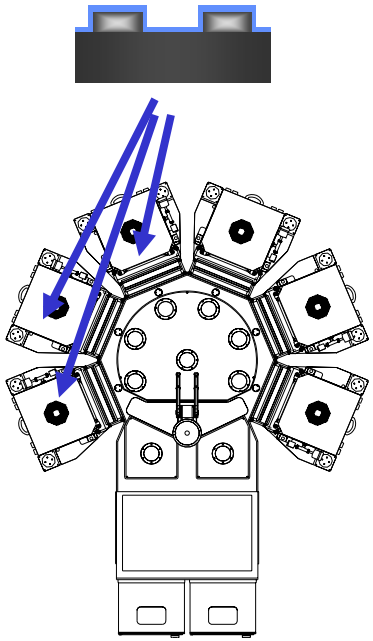


Process Flow

Oxide Base

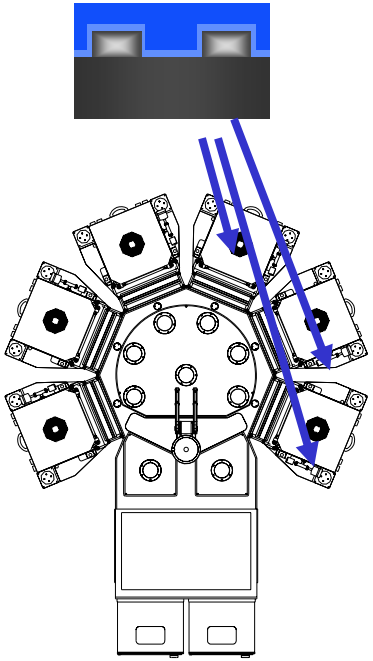
PECVD

- Moisture barrier



Low K Flowfill®

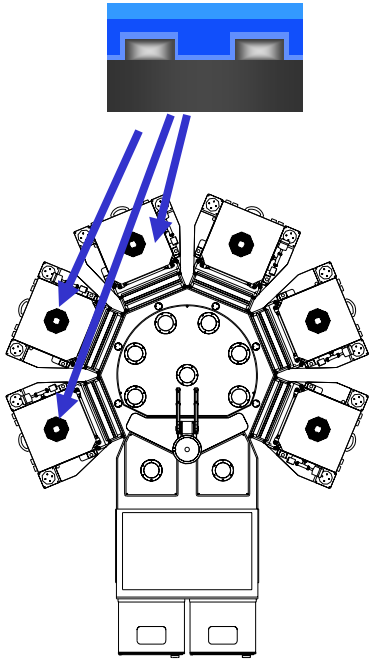
CVD Gap-fill



In-situ plasmaCure

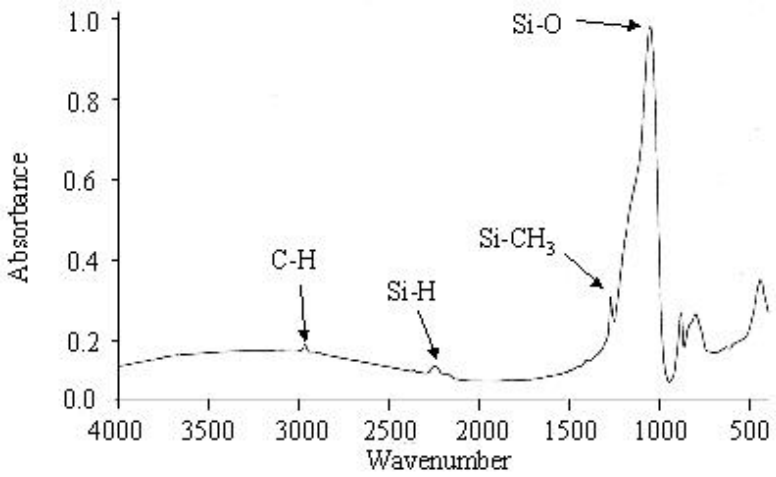
Oxide Cap

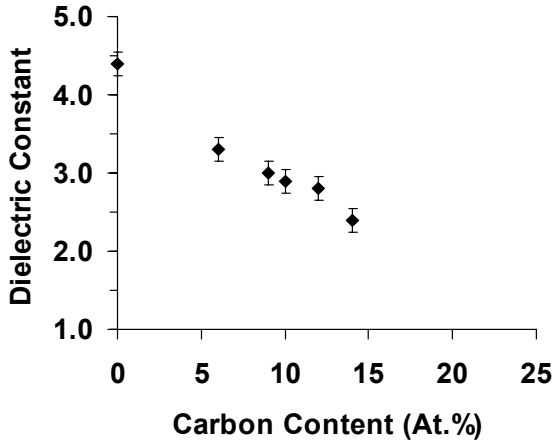
PECVD – CMP stop



Film Properties

Chemical composition & K Value



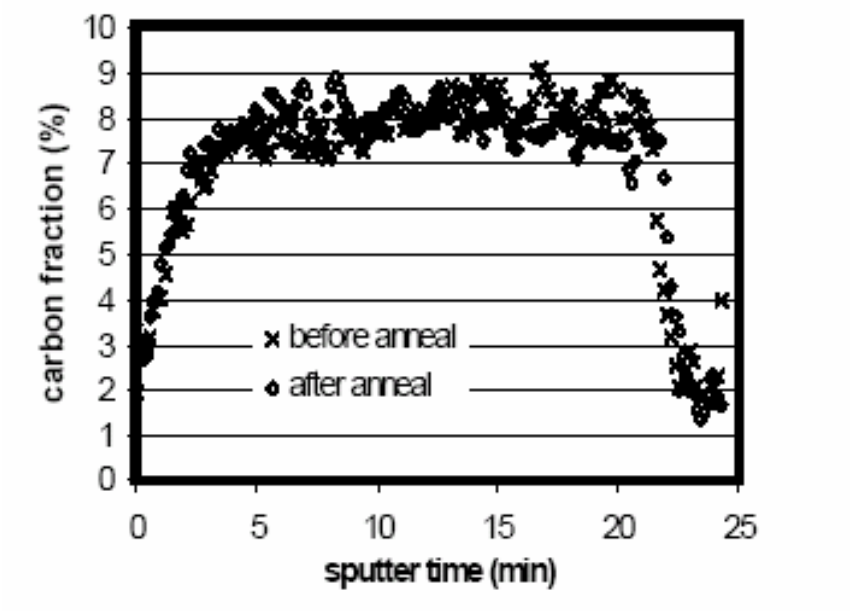


- Generic carbon-doped oxide
- Incorporation of methyl groups

- K value tuneable: 2.8<K<3.3

Thermal stability

- Generically – carbon doped oxide
  - Susceptible to damage during anneal in oxidising ambients
    - Carbon loss
- However…….Stable to >1000°C in inert ambients

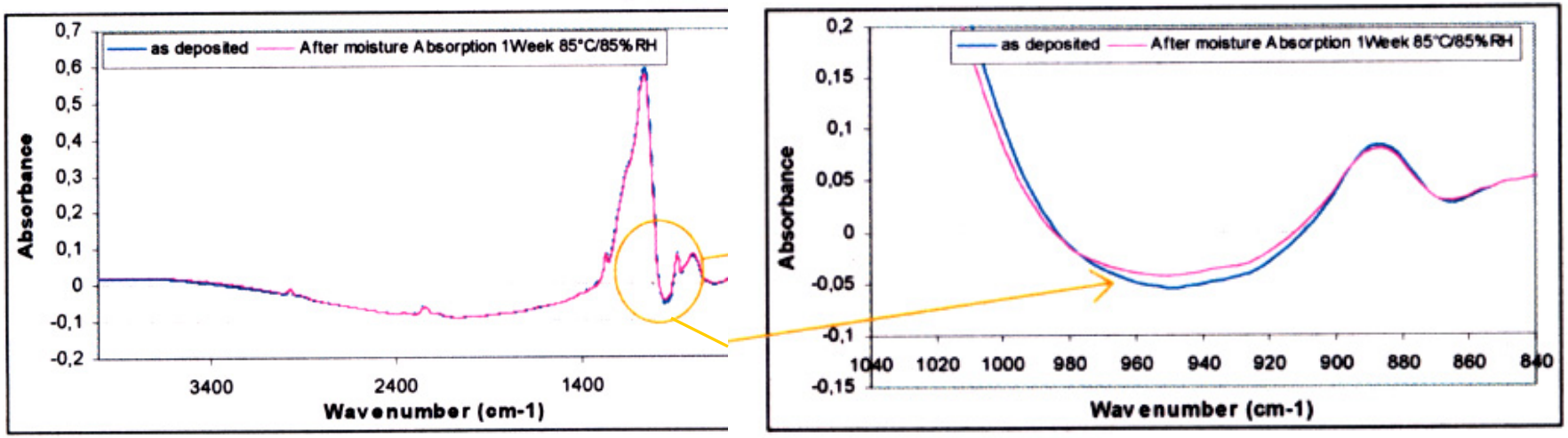


- Investigation of low-k carbon fraction prior to and post anneal in inert atmosphere (1000°C, 30 min, N_2) using depth-profiled-AES.

**Klipp et al; Infineon Technologies, AMC 2004

Moisture Resistance

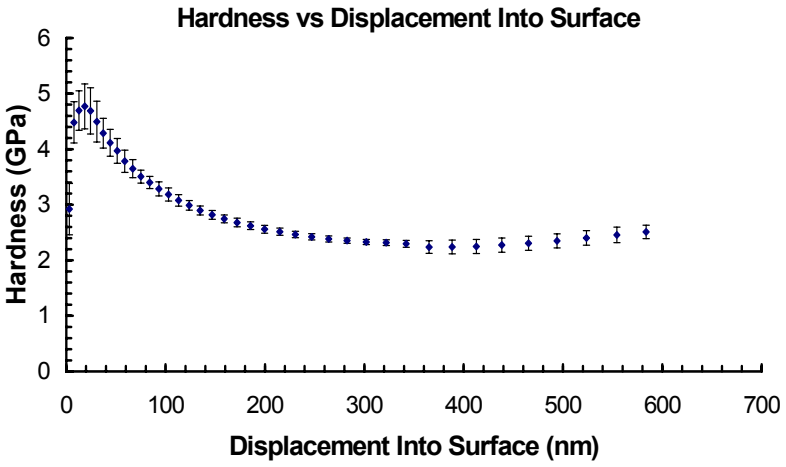
- FTIR spectra before & after moisture / temperature stress

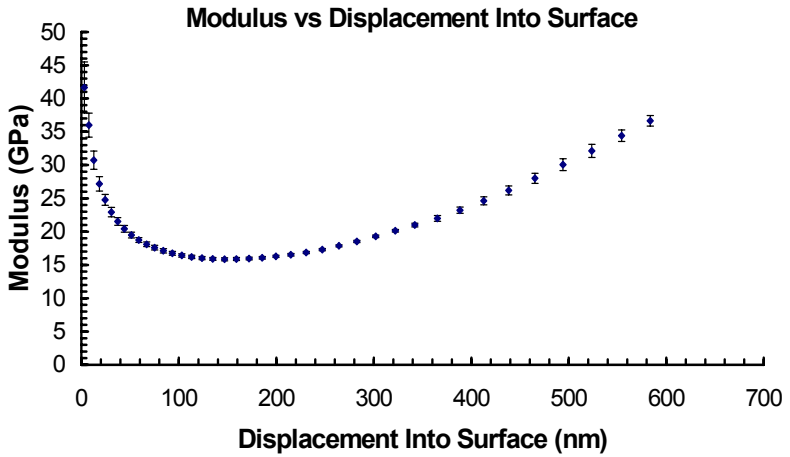


- Uncapped low k Flowfill
- Minimal moisture absorption –
  - 1week 85% RH; 85 °C

Hardness and Elastic Modulus

- H&E vs indent depth for low k Flowfill (k~2.8)

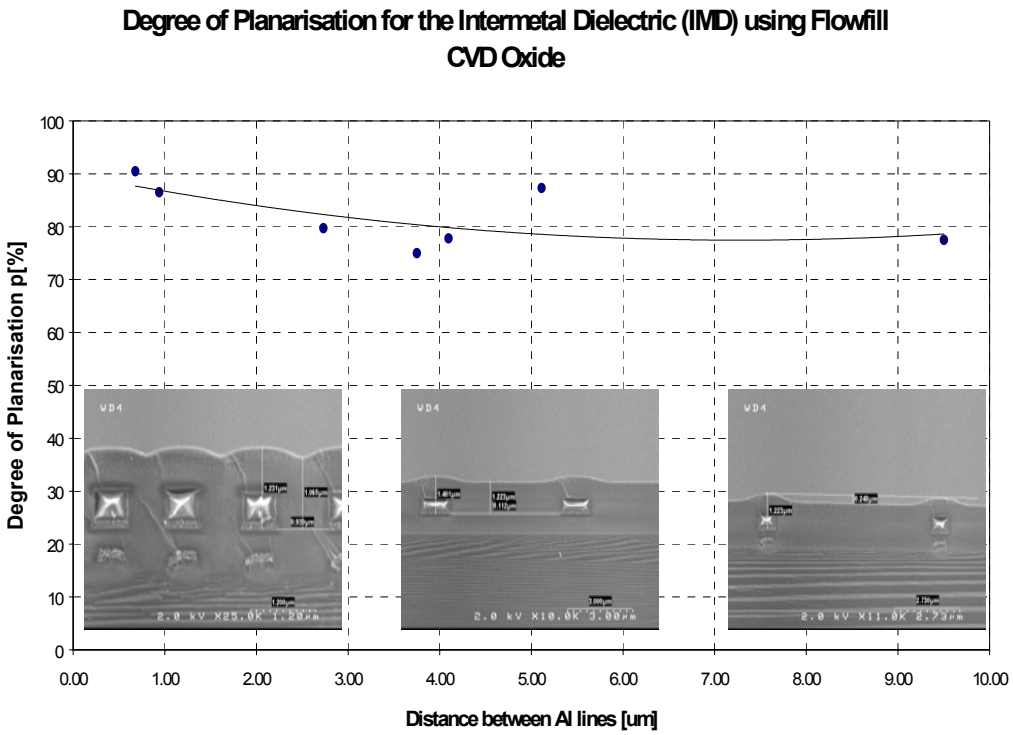


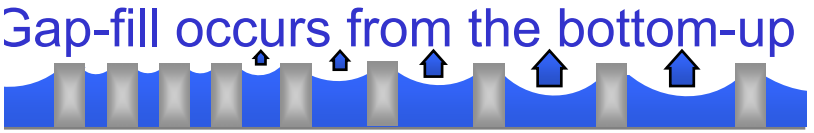


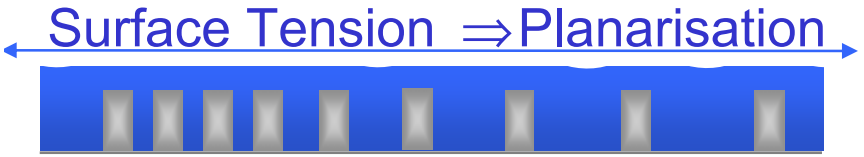
- H>3GPa
- E>15GPa

- Mechanically robust film eases integration

Planarisation





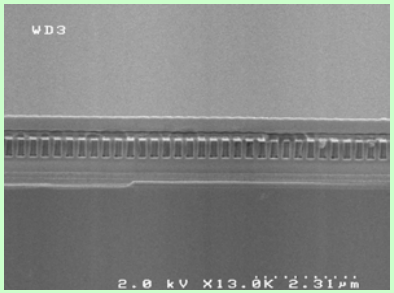


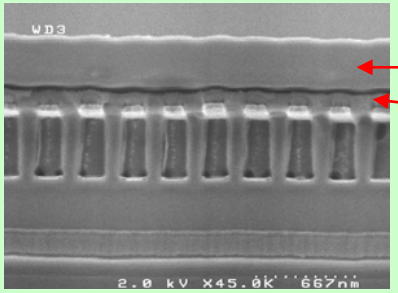
- Planarising capability reduces lessens CMP burden

300mm Gap-fill & Planarisation

DRAM Interconnect Structure

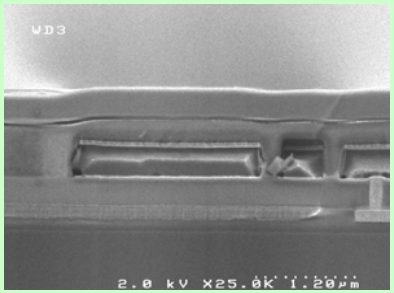
Wafer Centre





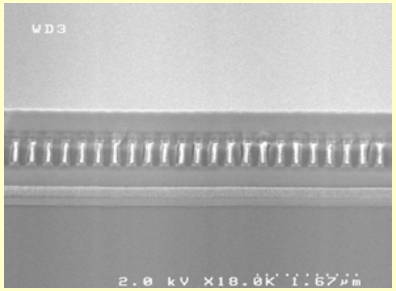
PECVD Cap Oxide

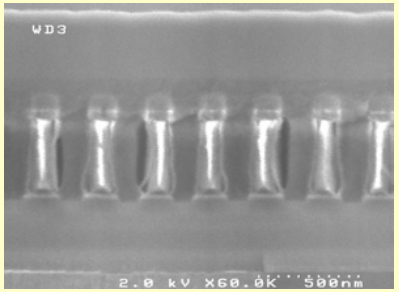
Low-k Flowfill



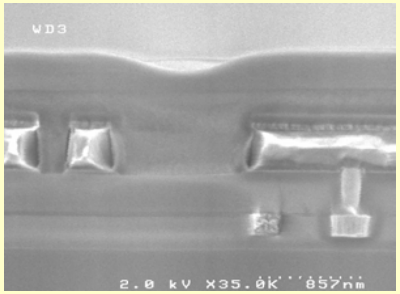
SEMs decorated to show cap interface

Wafer Edge



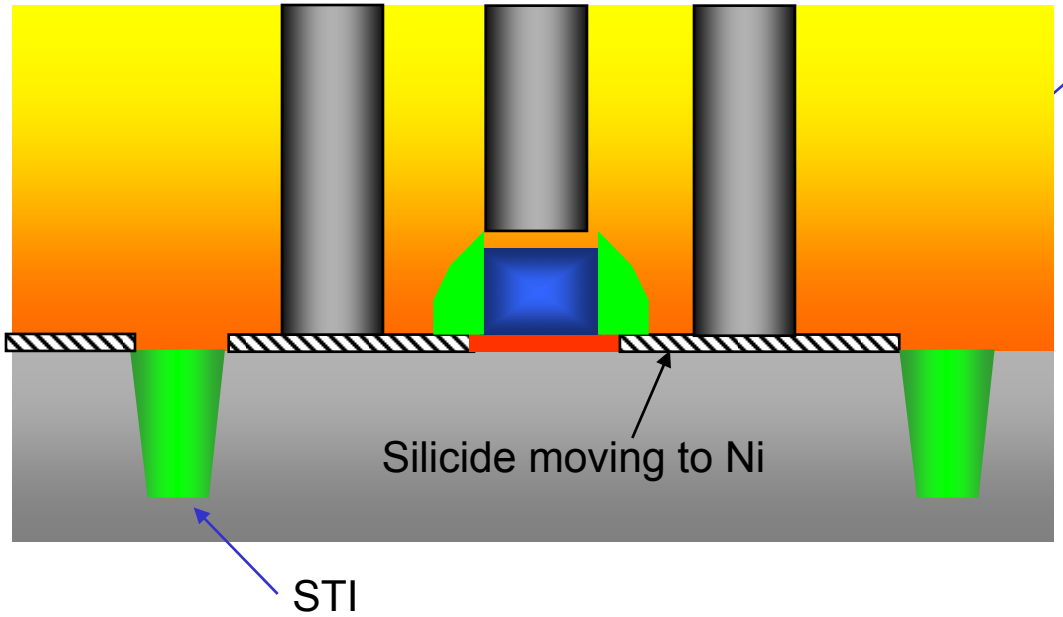


0.25µm min line/space



Pre-Metal Dielectric

Pre-metal dielectric



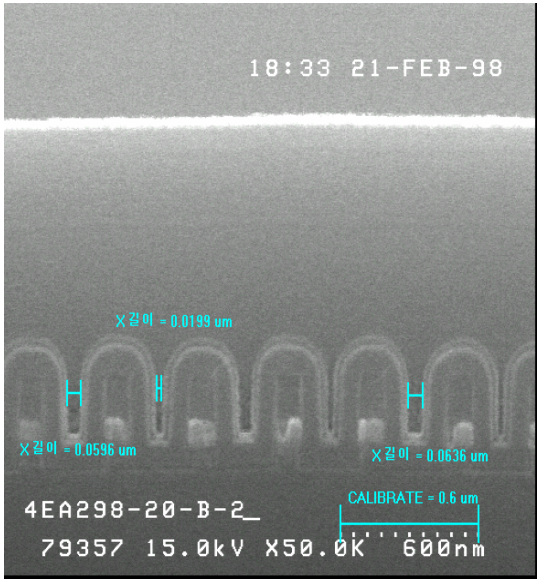
PMD needs

Uniform fill of deep structures
(DRAM, PMD AR 16:1 by 2005)
Low-k to reduce capacitance
(DRAM, Keff 2.7 to 3.1 by 2010)
Temp <450°C to protect NiSi
Zero damage of gate dielectrics

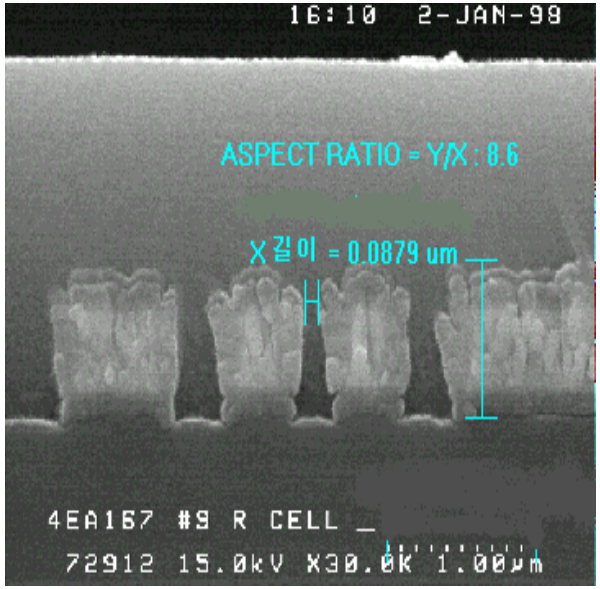
- Traditional HDP / doped silica processes struggling
  - Voiding
  - Plasma damage & high stress
  - Temperature too high for NiSi and metal gates

Pre-Metal Dielectric – Gap Fill

- Flowfill and low k Flowfill both have the gap-filling capability needed for PMD.



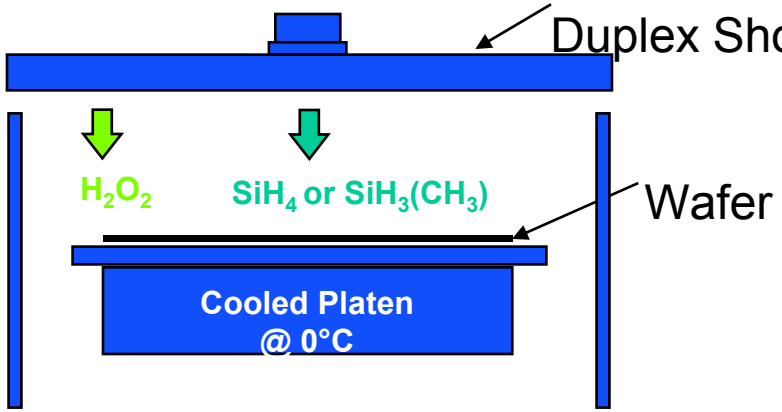
(a) Space 0.02㎛, AR＞10:1(vertical pattern)

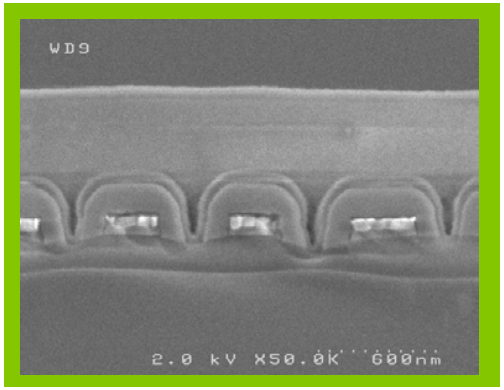


(b) Space 0.09㎛,AR 8.6:1(negative sloped pattern)

PMD - Low Temperature Compatibility

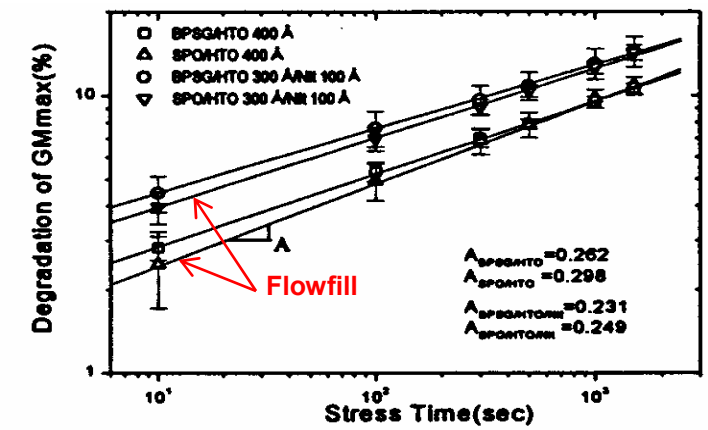
- Flowfill® is deposited cold without a plasma
  - Base films may not be required reducing chances of plasma damage and poly clipping c.f HDP
  - Cure temperature ~400°C
- Reduces thermal budgets at PMD
  - Compatible with new silicide materials e.g NiSi
  - Low k Flowfill preferable to standard Flowfill



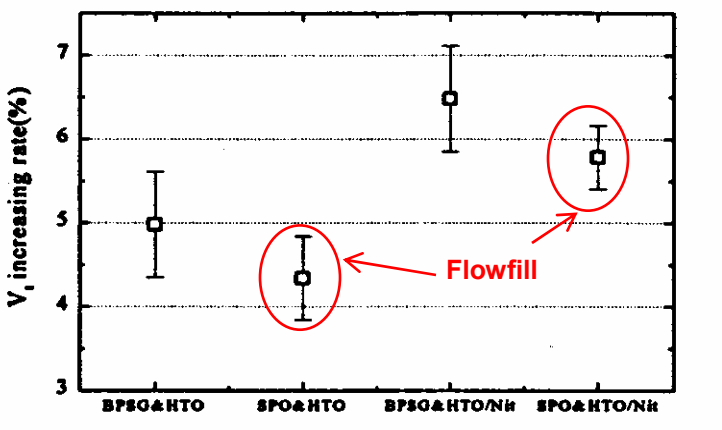


SiH_4 for std Flowfill or $SiH_3(CH_3)$ for low-k Flowfill

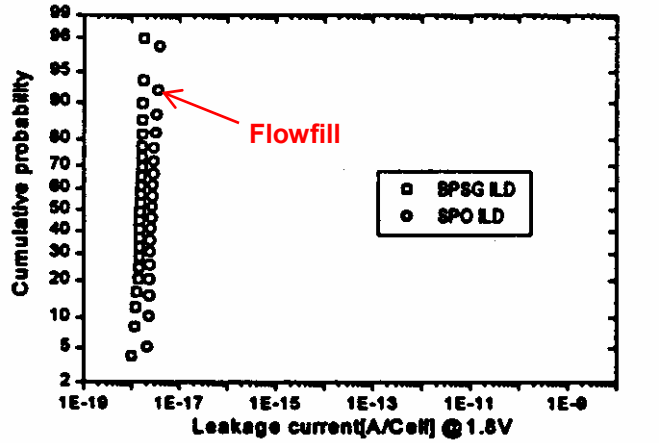
PMD Electricals – standard Flowfill



Degradation of Gm_{max} in NMOS as a function of hot carrier stress time. (W/L=10/0.3um V_G=1.38V, V_D=3.25V)



Variation of threshold voltage in PMOS after BT stress (W/L=10/0.4um V_G=-6.5V, 200^{O}C, 10min)



Leakage current between bit line and top electrode

Transistor reliability and hot carrier hardness comparable to BPSG

GMmax(Maximum Transconductance).

Park et al, Hyundai Electronics, VMIC 98

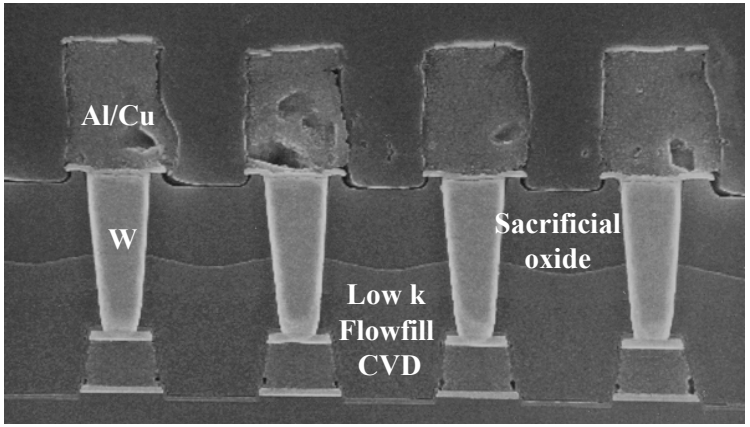
Inter-Metal Dielectric

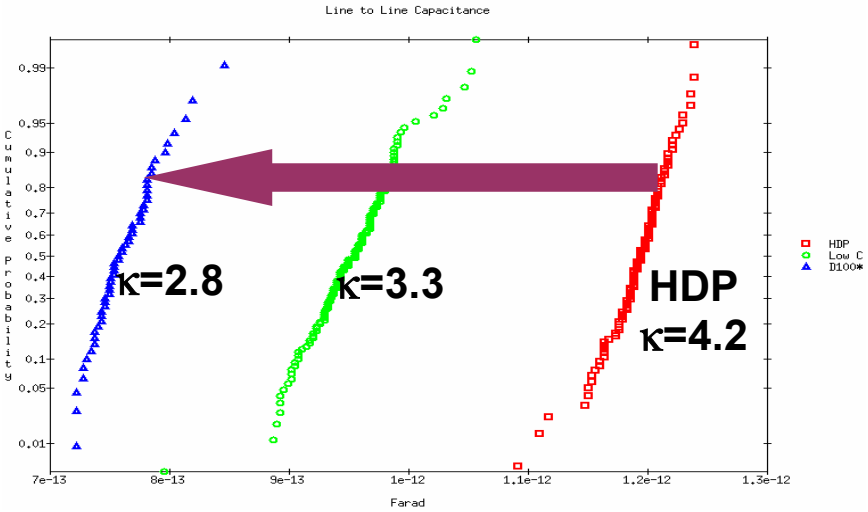
Inter-Metal Dielectric (IMD)

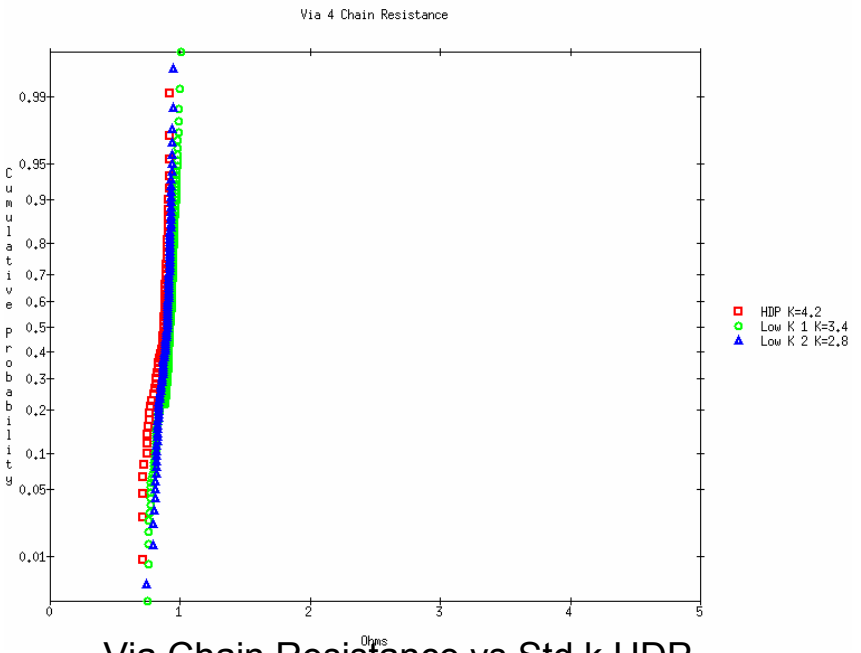
- Most DRAM manufacturers will continue to use Al interconnect in short/medium term
  - Cost
  - Less complex metal routing
    - Shorter lines, lower resistance
- Dielectrics with gap fill capability needed for IMD
- Low K beneficial in high performance devices

Integration at 0.18µm

k~3.0





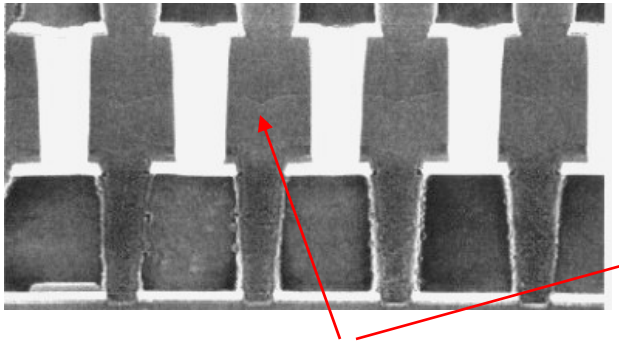


Via Chain Resistance vs Std k HDP

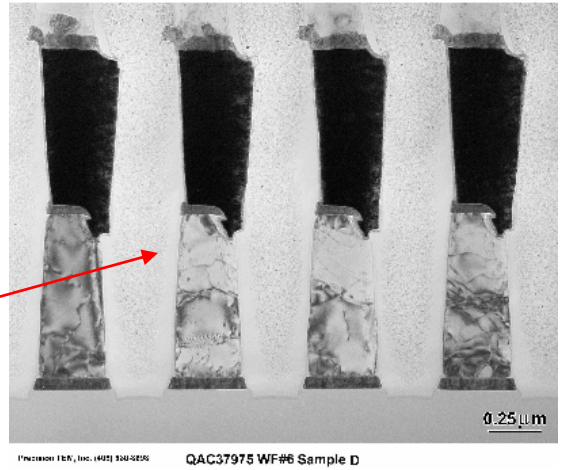
20 - 36% Inter-line Capacitance Improvement

Hsia et al ICAMP 99

Integration at 130nm

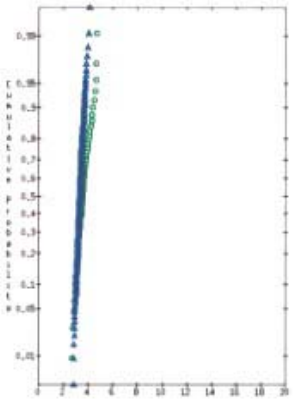


Low-k Flowfill® (k=2.8)

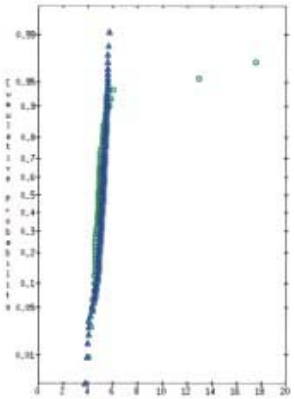


- Embedded SOD low-k sensitive to plasma damage during etch / strip
  - Absorb moisture
  - Out-gass during W dep giving poisoned via / W void
- Low k Flowfill® compatible with zero-overlay designs
  - No poisoned via even for 30% off-set at 130nm

Compatible with Zero Overlay

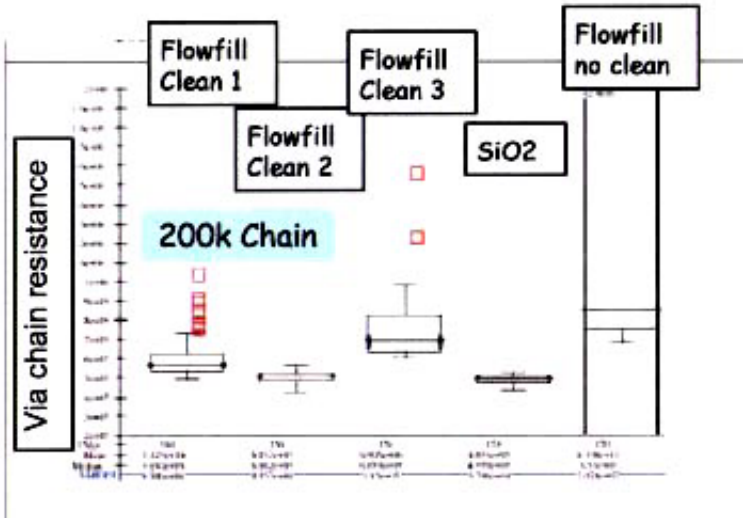


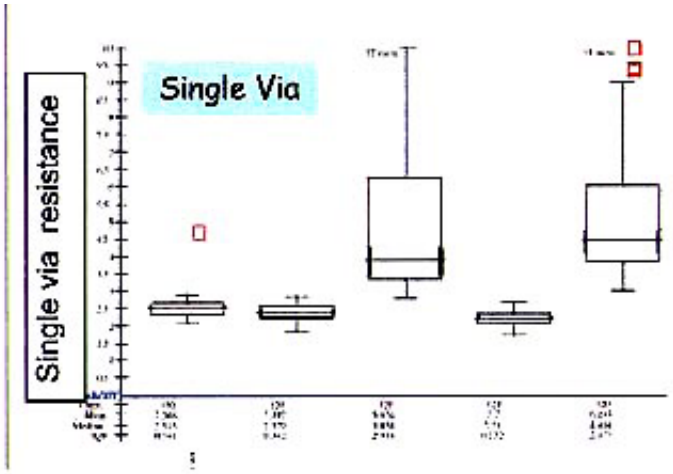
Borderless
Via chain

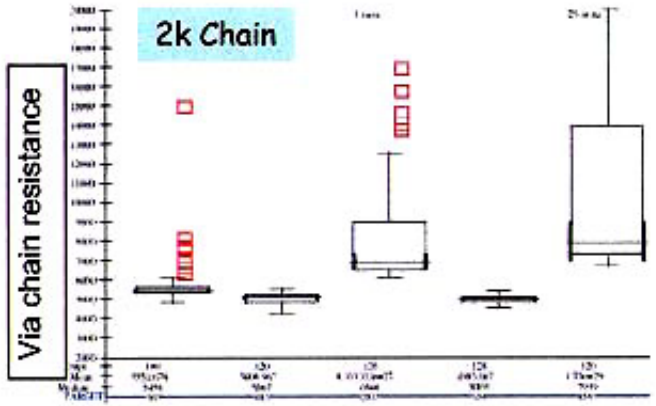


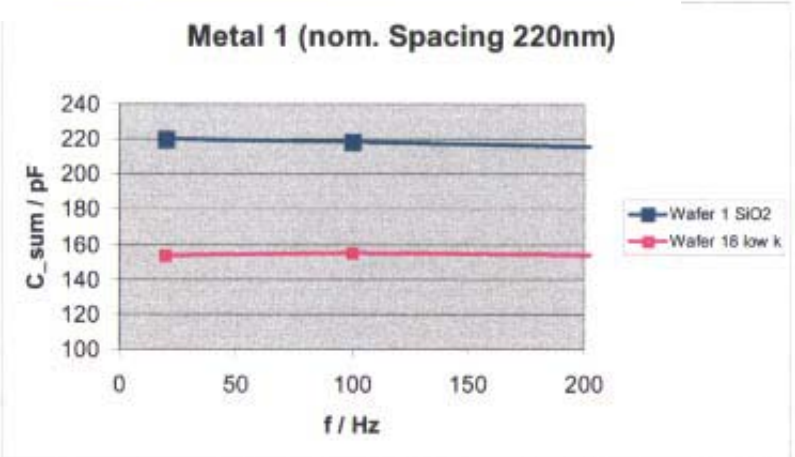
Offset (45 nm)
Via chain

Electrical Performance – DRAM









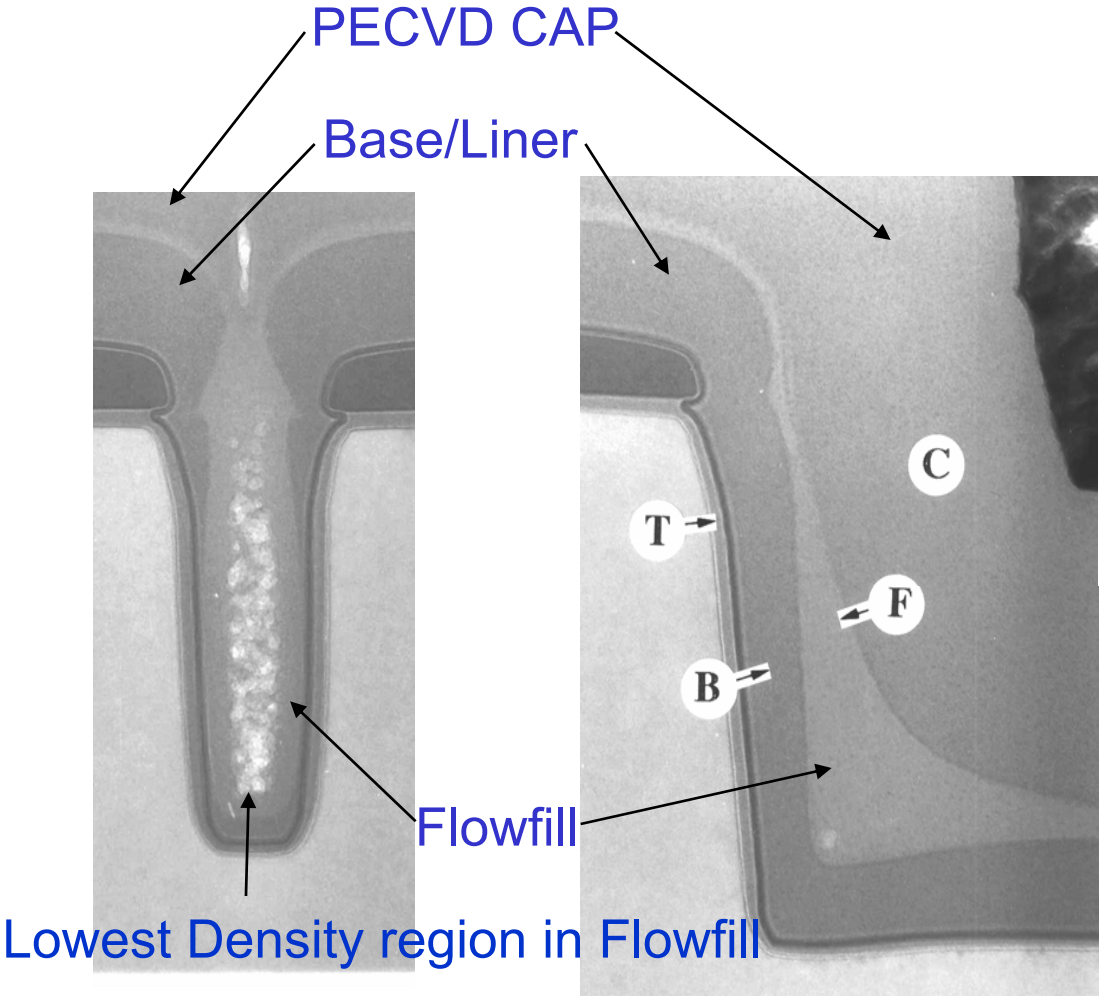
Low-k Flowfill - 29% Capacitance Reduction c.f HDP

Extendibility

Developmental gap fill process

- Objectives:
  - K value reduction c.f. low k Flowfill
    - k ≤2.5
      - DRAM IMD
      - PMD
  - Reduction of μ-porosity in high aspect ratio features
    - Easier integration
      - PMD
      - STI

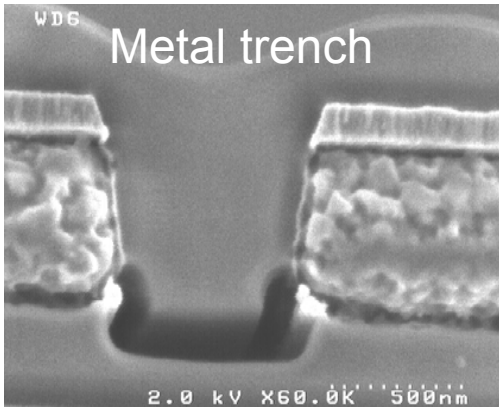
Trench Material – TEM of Standard Flowfill

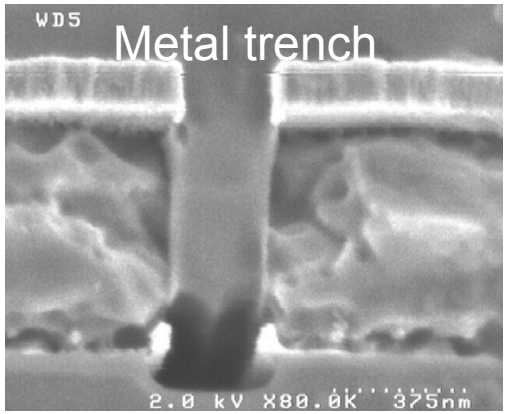


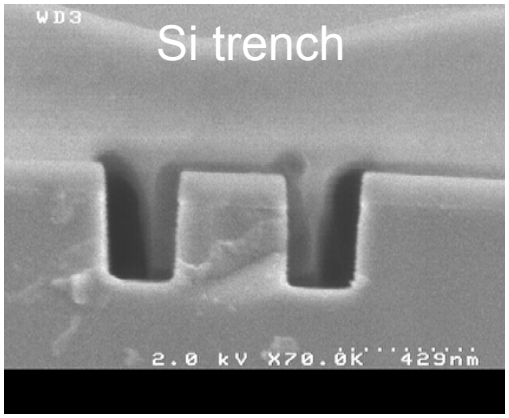
- Behaviour similar for low k Flowfill
- Evidence of porosity in narrow trench
- Narrow trench will have higher wet etch rate
- K value is reduced in small features due to low density region.

Wet etch rate within trenches

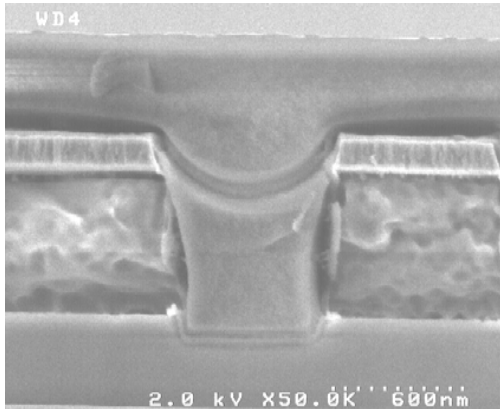
Flowfill

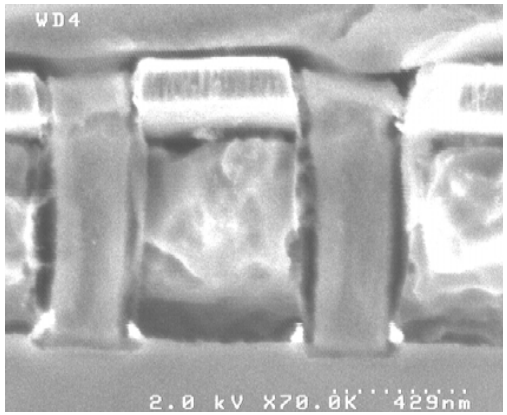


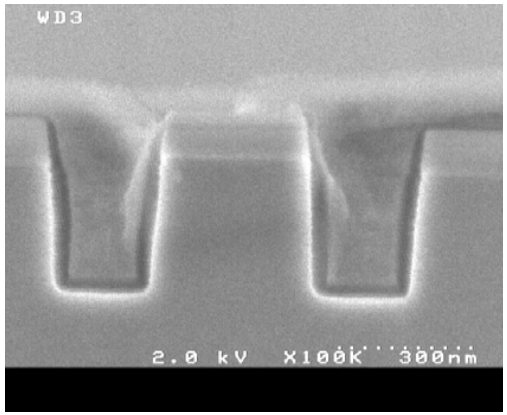




New Process

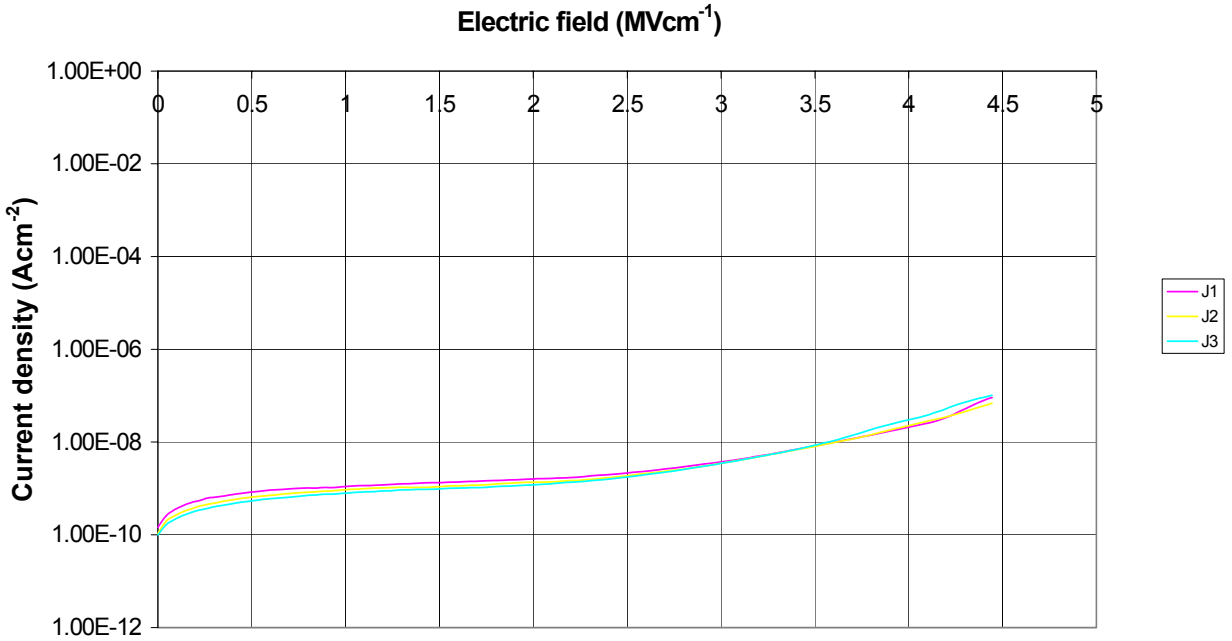






- 10:1 HF etching after sample cleave (30 secs)
- Flowfill shows clear evidence of low density fill in metal & Si trenches
- Developmental process shows no evidence of low density in gaps

Current Density vs Electric Field



- Tested using Al dot MIS capacitance on low resistivity Si wafer.
- Film thickness: ~500nm
- Maximum supply voltage: 200V

} Max electric field available ~4MVcm^{-1}

- Trikon unable to determine true V_{bd} due to film thickness and max voltage limitation
  - Can only say that Vbd > 4MVcm^{-1}

Developmental gap fill process - film properties

Film Property	Low k Flowfill	new low k gap fill	Method
Dielectric Constant	~2.9	~2.5	Al dot MIS capacitor
Non-uniformity (200mm wafer 1_{σ})	4.50%	3.04%	Optiprobe
Deposition Rate (nm/min)	340	600	Optiprobe
Refractive Index	1.415	1.342	Optiprobe
Stress (MPa)	<50	<20	wafer bow
Wet Etch Rate in 10:1 BHF (nm/min)	580	679	wafer piece
Hardness GPa (20% indent depth)	3.1	0.57	Nano-indentation
Modulus GPa (20% indent depth)	22.1	3.92	Nano-indentation
SiC:SiO ratio	0.005	0.0199	FTIR
SiH:SiO ratio	0.011	0.0195	FTIR
CH:SiO ratio	0.009	0.0324	FTIR
Si at%	23.2	20.5	RBS
O at%	38.3	31	RBS
C at%	11.5	14.5	NRA
H at%	27	34	ERDA
V_{BD} ($MVcm^{-1}$)	>8	>4	Al dot MIS capacitor
Leakage (Acm^{-2} @ $1MVcm^{-1}$)	~1E-10	~1E-9	Al dot MIS capacitor

RBS: Rutherford Back-Scattering; NRA: Nuclear Reaction Analysis; ERDA: Elastic Recoil Detection Analysis

New Flowable oxides

- Scope to reduce porosity/low density regions in HAR features by modifying chemistry before it reaches wafer surface.
- As-deposited viscosity is low enough to provide fill.
- K values to <2.5 are possible.
  - Thermal stability (<650^{o}C)is likely to be only sufficient to be of use for IMD/PMD applications.

Summary

- Low k Flowfill CVD technology
  - Unrivalled gap fill performance – PMD & IMD
  - Low k – PMD & IMD
  - Low temperature – PMD & IMD
    - Compatible with NiSi
- There is a continuing need for low k materials with gap fill capability
- PMD and DRAM IMD applications will drive this need for several technology generations to come

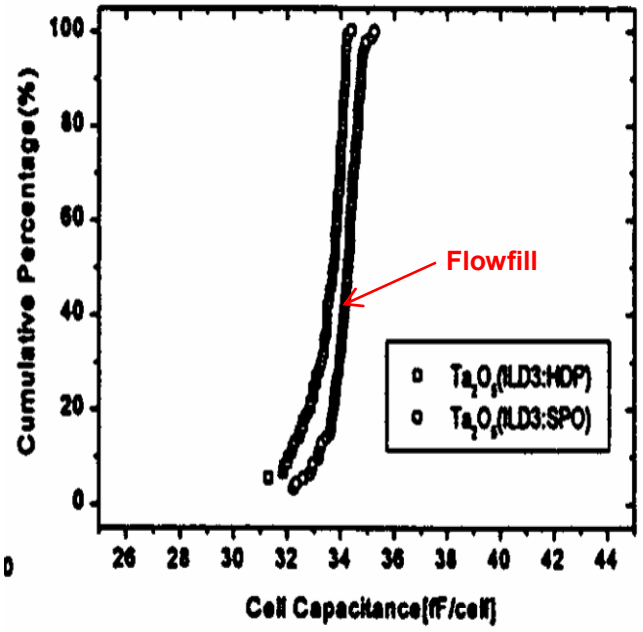
Selected References

PMD / IMD

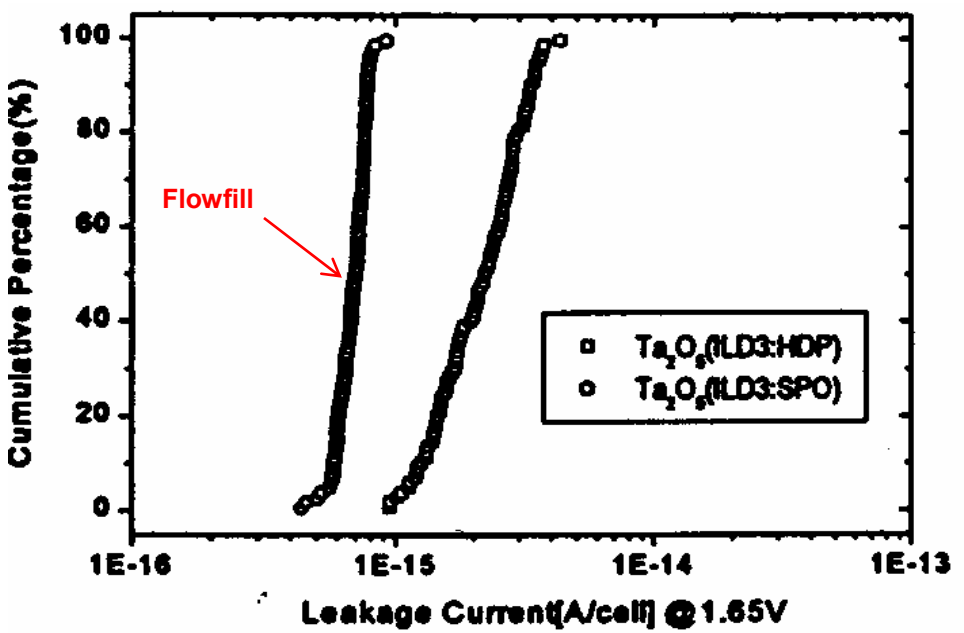
1. Integration of high gapfill, standard and low k, contact level dielectric materials for the 90nm mode and beyond. Spencer et al; Freescale Semiconductor, AMC 2004
2. New integration fields for gap filling low k dielectrics in DRAM – The way from BEOL to MOL to FEOL. Klipp et al; Infineon Technologies, AMC 2004
3. Pre-Metal Dielectric Applications of Low Temperature SPO(Self-Planarization Oxide) By Using SiH_4+H_2O_2 CVD For 0.13㎛ Technology and Beyond. Park et al; Hyundai Electronics (Hynix), VMIC 1998

PMD Electricals – standard Flowfill

1Gbit DRAM Ta_2O_5 capacitor



Capacitance of Ta_2O_5 capacitors for HDP and Flowfill



Leakage current of Ta_2O_5 capacitors for HDP and Flowfill

Superior leakage current and data distribution variance of Ta_2O_5 capacitor c.f HDP.

Attributed to absence of plasma in Flowfill process

Park et al, Hyundai Electronics, VMIC 98