CVD deposited low k dielectrics for gap-fill applications.

John Macneil
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## Application requirements.

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Low K Flowfill® Process Overview
Low K Flowfill Chamber Schematic

- Duplex Showerhead
- Wafer
- Cooled Platen @ 0°C
- Pumping

▲ Direct CVD – no plasma enhancement
Low-k Flowfill® Chemistry

Formation of “liquid” methyl doped-silicic acid

\[ \text{Si} + \text{M} = \text{CH}_3 \]

Surface Reaction
Low-k Flowfill® Chemistry

Polymerisation via condensation reactions
Process Flow

Oxide Base
PECVD
- Moisture barrier

Low K Flowfill®
CVD Gap-fill

In-situ plasmaCure

Oxide Cap
PECVD – CMP stop
Film Properties
Chemical composition & K Value

▲ Generic carbon-doped oxide
▲ Incorporation of methyl groups

▲ K value tuneable: 2.8<K<3.3
Thermal stability

- Generically – carbon doped oxide
  - Susceptible to damage during anneal in oxidising ambients
  - Carbon loss
- However……..Stable to >1000°C in inert ambients

- Investigation of low-k carbon fraction prior to and post anneal in inert atmosphere (1000°C, 30 min, N₂) using depth-profiled-AES.

**Klipp et al; Infineon Technologies, AMC 2004**
Moisture Resistance

▲ FTIR spectra before & after moisture / temperature stress

▲ Uncapped low k Flowfill
▲ Minimal moisture absorption –
  ▲ 1 week 85% RH; 85 °C
Hardness and Elastic Modulus

▲ H&E vs indent depth for low k Flowfill (k~2.8)

▲ H>3GPa  ▲ E>15GPa

▲ Mechanically robust film eases integration
Planarisation

Planarising capability reduces lessens CMP burden

Degree of Planarisation for the Intermetal Dielectric (IMD) using Flowfill CVD Oxide

Gap-fill occurs from the bottom-up

Surface Tension $\Rightarrow$ Planarisation
300mm Gap-fill & Planarisation

DRAM Interconnect Structure

Wafer Centre

- PECVD Cap Oxide
- Low-k Flowfill

SEMs decorated to show cap interface

Wafer Edge

- 0.25µm min line/space
Pre-Metal Dielectric
Pre-metal dielectric

Traditional HDP / doped silica processes struggling
- Voiding
- Plasma damage & high stress
- Temperature too high for NiSi and metal gates

PMD needs
- Uniform fill of deep structures (DRAM, PMD AR 16:1 by 2005)
- Low-k to reduce capacitance (DRAM, Keff 2.7 to 3.1 by 2010)
- Temp <450°C to protect NiSi
- Zero damage of gate dielectrics
Pre-Metal Dielectric – Gap Fill

▲ Flowfill and low k Flowfill both have the gap-filling capability needed for PMD.

(a) Space 0.02 $\mu$m, AR > 10:1 (vertical pattern)  
(b) Space 0.09 $\mu$m, AR 8.6:1 (negative sloped pattern)
PMD - Low Temperature Compatibility

▲ Flowfill® is deposited cold without a plasma
  ▲ Base films may not be required reducing chances of plasma damage and poly clipping c.f HDP
  ▲ Cure temperature ~400°C
▲ Reduces thermal budgets at PMD
  ▲ Compatible with new silicide materials e.g NiSi
  ▲ Low k Flowfill preferable to standard Flowfill

SiH₄ for std Flowfill or SiH₃(CH₃) for low-k Flowfill
PMD Electricals – standard Flowfill

Degradation of $G_{m_{\text{max}}}$ in NMOS as a function of hot carrier stress time. ($W/L=10/0.3\mu m \ V_G=1.38V, \ V_D=3.25V$)

Variation of threshold voltage in PMOS after BT stress ($W/L=10/0.4\mu m \ V_G=-6.5V, \ 200^\circ C, \ 10\min$)

Leakage current between bit line and top electrode

Transistor reliability and hot carrier hardness comparable to BPSG

$G_{m_{\text{max}}}$ (Maximum Transconductance).
Inter-Metal Dielectric
Inter-Metal Dielectric (IMD)

- Most DRAM manufacturers will continue to use Al interconnect in short/medium term
  - Cost
  - Less complex metal routing
    - Shorter lines, lower resistance
- Dielectrics with gap fill capability needed for IMD
- Low K beneficial in high performance devices
Integration at 0.18µm

k~3.0

Al/Cu

W

Low k Flowfill CVD

Sacrificial oxide

κ = 2.8
κ = 3.3
κ = 4.2

Via Chain Resistance vs Std k HDP

20 - 36% Inter-line Capacitance Improvement

Hsia et al ICAMP 99
Integration at 130nm

Low-k Flowfill® (k=2.8)

▲ Embedded SOD low-k sensitive to plasma damage during etch / strip
  ▲ Absorb moisture
  ▲ Out-gass during W dep giving poisoned via / W void
▲ Low k Flowfill® compatible with zero-overlay designs
  ▲ No poisoned via even for 30% off-set at 130nm

Compatible with Zero Overlay
Electrical Performance – DRAM

Low-k Flowfill - 29% Capacitance Reduction c.f HDP
Extendibility
Developmental gap fill process

▲ Objectives:

▲ K value reduction c.f. low k Flowfill
  ▲ k ≤ 2.5
    ▲ DRAM IMD
    ▲ PMD

▲ Reduction of μ-porosity in high aspect ratio features
  ▲ Easier integration
    ▲ PMD
    ▲ STI
Trench Material – TEM of Standard Flowfill

- Behaviour similar for low k Flowfill
- Evidence of porosity in narrow trench
- Narrow trench will have higher wet etch rate
- K value is reduced in small features due to low density region.
Wet etch rate within trenches

Flowfill

New Process

- 10:1 HF etching after sample cleave (30 secs)
- Flowfill shows clear evidence of low density fill in metal & Si trenches
- Developmental process shows no evidence of low density in gaps
Current Density vs Electric Field

- Tested using Al dot MIS capacitance on low resistivity Si wafer.
- Film thickness: ~500nm
- Maximum supply voltage: 200V

Max electric field available ~4MVcm⁻¹

- Trikon unable to determine true $V_{bd}$ due to film thickness and max voltage limitation
  - Can only say that $V_{bd} > 4$MVcm⁻¹
# Developmental gap fill process - film properties

<table>
<thead>
<tr>
<th>Film Property</th>
<th>Low k Flowfill</th>
<th>new low k gap fill</th>
<th>Method</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dielectric Constant</td>
<td>~2.9</td>
<td>~2.5</td>
<td>Al dot MIS capacitor</td>
</tr>
<tr>
<td>Non-uniformity (200mm wafer 1σ)</td>
<td>4.50%</td>
<td>3.04%</td>
<td>Optiprobe</td>
</tr>
<tr>
<td>Deposition Rate (nm/min)</td>
<td>340</td>
<td>600</td>
<td>Optiprobe</td>
</tr>
<tr>
<td>Refractive Index</td>
<td>1.415</td>
<td>1.342</td>
<td>Optiprobe</td>
</tr>
<tr>
<td>Stress (MPa)</td>
<td>&lt;50</td>
<td>&lt;20</td>
<td>wafer bow</td>
</tr>
<tr>
<td>Wet Etch Rate in 10:1 BHF (nm/min)</td>
<td>580</td>
<td>679</td>
<td>wafer piece</td>
</tr>
<tr>
<td>Hardness GPa (20% indent depth)</td>
<td>3.1</td>
<td>0.57</td>
<td>Nano-indentation</td>
</tr>
<tr>
<td>Modulus GPa (20% indent depth)</td>
<td>22.1</td>
<td>3.92</td>
<td>Nano-indentation</td>
</tr>
<tr>
<td>SiC:SiO ratio</td>
<td>0.005</td>
<td>0.0199</td>
<td>FTIR</td>
</tr>
<tr>
<td>SiH:SiO ratio</td>
<td>0.011</td>
<td>0.0195</td>
<td>FTIR</td>
</tr>
<tr>
<td>CH:SiO ratio</td>
<td>0.009</td>
<td>0.0324</td>
<td>FTIR</td>
</tr>
<tr>
<td>Si at%</td>
<td>23.2</td>
<td>20.5</td>
<td>RBS</td>
</tr>
<tr>
<td>O at%</td>
<td>38.3</td>
<td>31</td>
<td>RBS</td>
</tr>
<tr>
<td>C at%</td>
<td>11.5</td>
<td>14.5</td>
<td>NRA</td>
</tr>
<tr>
<td>H at%</td>
<td>27</td>
<td>34</td>
<td>ERDA</td>
</tr>
<tr>
<td>$V_{BD}$ (MVcm$^{-1}$)</td>
<td>&gt;8</td>
<td>&gt;4</td>
<td>Al dot MIS capacitor</td>
</tr>
<tr>
<td>Leakage (Acm$^{-2}$ @ 1MVcm$^{-1}$)</td>
<td>~1E-10</td>
<td>~1E-9</td>
<td>Al dot MIS capacitor</td>
</tr>
</tbody>
</table>

RBS: Rutherford Back-Scattering; NRA: Nuclear Reaction Analysis; ERDA: Elastic Recoil Detection Analysis
New Flowable oxides

▲ Scope to reduce porosity/low density regions in HAR features by modifying chemistry before it reaches wafer surface.

▲ As-deposited viscosity is low enough to provide fill.

▲ K values to <2.5 are possible.
  ▲ Thermal stability (<650°C) is likely to be only sufficient to be of use for IMD/PMD applications.
Summary

▲ Low k Flowfill CVD technology
  ▲ Unrivalled gap fill performance – PMD & IMD
  ▲ Low k – PMD & IMD
  ▲ Low temperature – PMD & IMD
    ▲ Compatible with NiSi

▲ There is a continuing need for low k materials with gap fill capability

▲ PMD and DRAM IMD applications will drive this need for several technology generations to come
Selected References

**PMD / IMD**

1. Integration of high gapfill, standard and low k, contact level dielectric materials for the 90nm mode and beyond. Spencer et al; Freescale Semiconductor, AMC 2004

2. New integration fields for gap filling low k dielectrics in DRAM – The way from BEOL to MOL to FEOL. Klipp et al; Infineon Technologies, AMC 2004

3. Pre-Metal Dielectric Applications of Low Temperature SPO(Self-Planarization Oxide) By Using SiH$_4$+H$_2$O$_2$ CVD For 0.13$\mu$m Technology and Beyond. Park et al; Hyundai Electronics (Hynix), VMIC 1998
PMD Electricals – standard Flowfill

1Gbit DRAM $\text{Ta}_2\text{O}_5$ capacitor

Superior leakage current and data distribution variance of $\text{Ta}_2\text{O}_5$ capacitor c.f HDP.

Attributed to absence of plasma in Flowfill process

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Park et al, Hyundai Electronics, VMIC 98