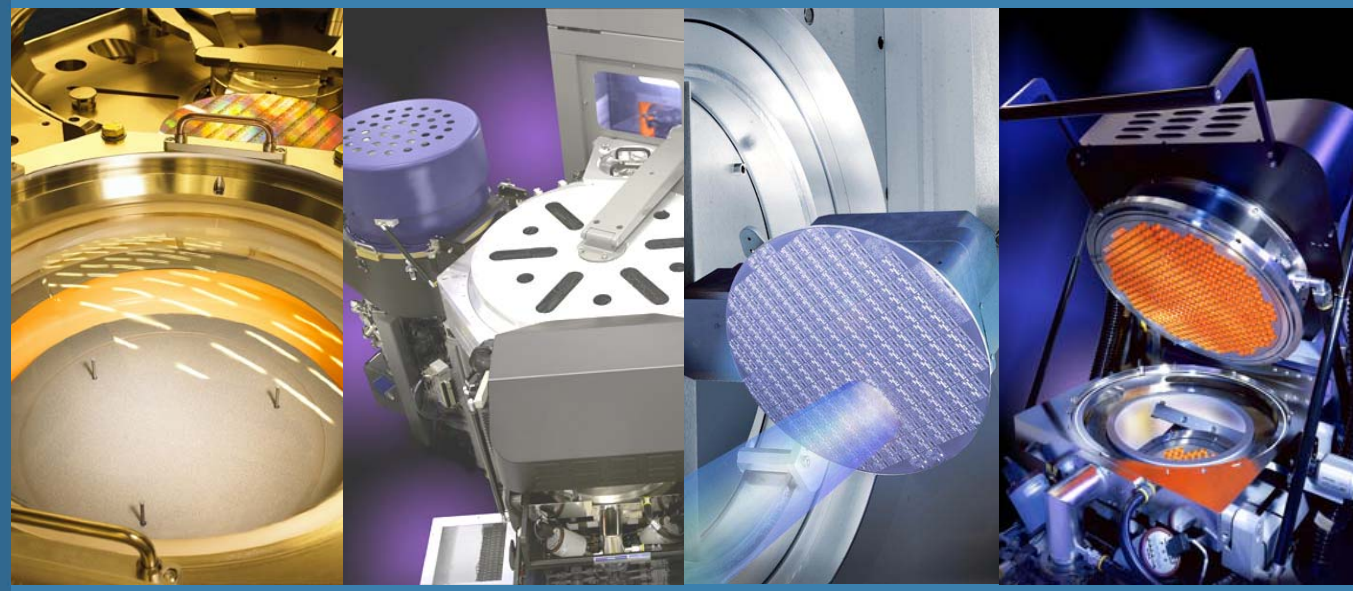


Equipment Supplier's Perspective on the Evolution of Si Technology Development

Gregg S. Higashi, Ph.D.
CTO & Co-Director of the Applications Development Center
Front End Products Group

May 2005

1998: Unit Process Physical Results

ADVANCED TECHNOLOGIES FOR GATE STACK EVOLUTION

Gary Miner, Gary Xing, Satheesh Kuppurao, Dave Lopes
Applied Materials
Santa Clara, California 95054

As device technologies advance to 0.18 μm and beyond, the applications and opportunities for Rapid Thermal Oxidation (RTO) are growing rapidly due to two forces. First, advanced device requirements are becoming more aligned with RTO capabilities, as process flows require a reduced thickness range and tighter thermal budget control. Second, RTO capabilities have expanded due to improved temperature measurement and control as well as the development of new equipment and process technologies. Applied Materials RTP Centura™ features advanced technologies for RTO. Wet oxidation capability has been developed to expand the thickness range of RTO while maintaining the process control and uniformity demonstrated on dry oxides. New technology allows processing with H_2:O_2 ratios not accessible with conventional pyrogenic torches. Processes for advanced oxynitrides have been demonstrated which allow tailoring of the nitrogen profile. These developments are rapidly moving RTO from research into production.

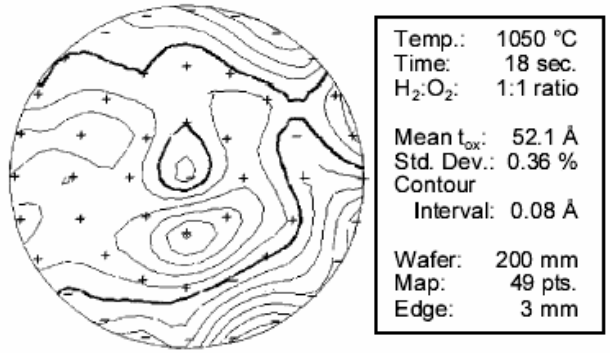


Figure 2. Thin Wet Oxide Uniformity

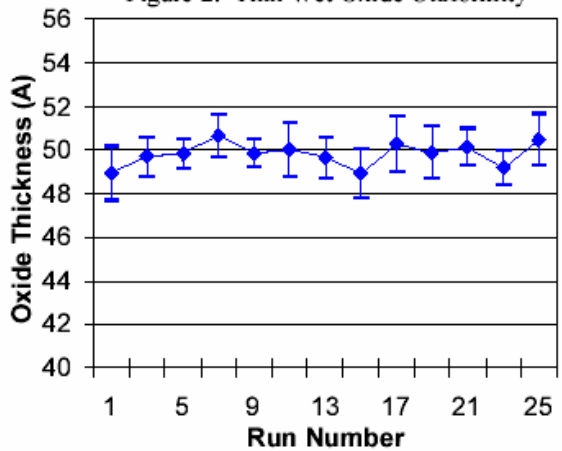


Figure 3. Thin Wet Oxide Repeatability

RTP'98

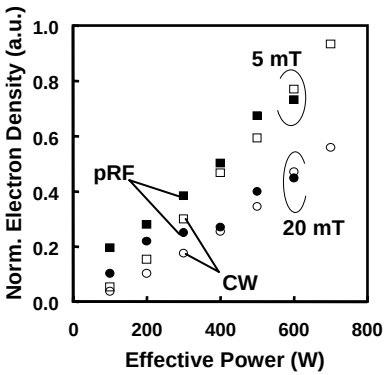
2003: Transistor Electrical Results

Low-energy Nitrogen Plasmas for 65-nm node Oxynitride Gate Dielectrics: A Correlation of Plasma Characteristics and Device Parameters

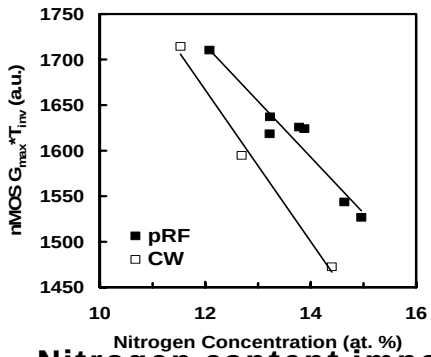
P.A. Kraus[1], K. Ahmed[1], T.C. Chua[1], M. Ershov[2], H. Karbasi[2], C.S. Olsen[1], F. Nouri[1], J. Holland[1], R. Zhao[1], G. Miner[1] and A. Lepert[1]
[1]Applied Materials, Inc., Santa Clara, CA, U.S.A.
[2]PDF Solutions, Inc., San Jose, CA, U.S.A.
Phone 408-563-6363, Fax 408-563-4884, E-mail *philip_kraus@amat.com*

Abstract

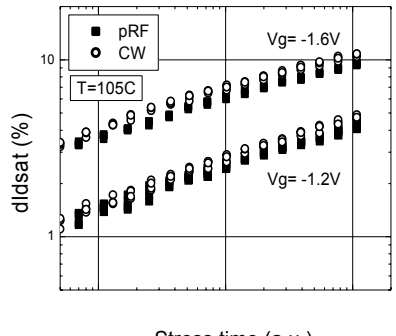
Ultra-thin oxynitride gate dielectrics (EOT 1.1 to 1.2 nm) have been prepared using quasi-remote inductively coupled nitrogen plasmas. A correlation has been established, for the first time, between device characteristics and measurements of the nitrogen plasma characteristics. It is found that reducing the density of high-energy



Plasma electron energy vs. Power



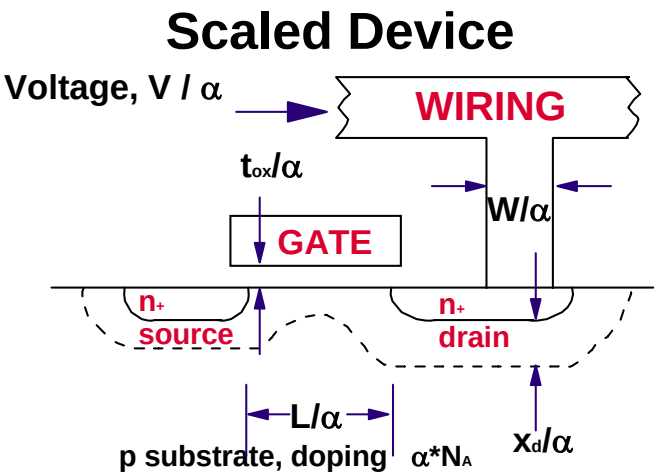
Nitrogen content impact on channel mobility

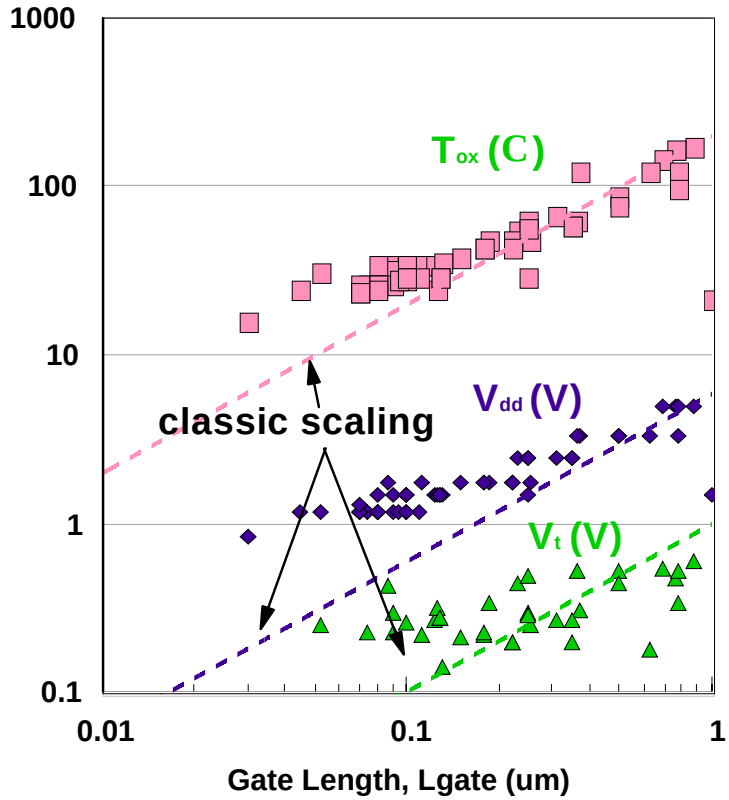


Plasma condition impact on device NBTI

VLSI'03

IBM says, "Classical CMOS Scaling is Dead"





SCALING:

Scaling factor:	α
Voltage:	V/α
Oxide:	tox /α
Wire width:	W/α
Gate width:	L/α
Diffusion:	xd /α
Substrate:	α * NA

RESULTS:

Higher Density:	~α2
Higher Speed:	~α
Power/ckt:	~1/α2
Power Density:	~Constant

Why deviate from "ideal" scaling?

- unacceptable gate leakage/reliability
- additional performance at higher voltages

What's the consequence of this deviation?

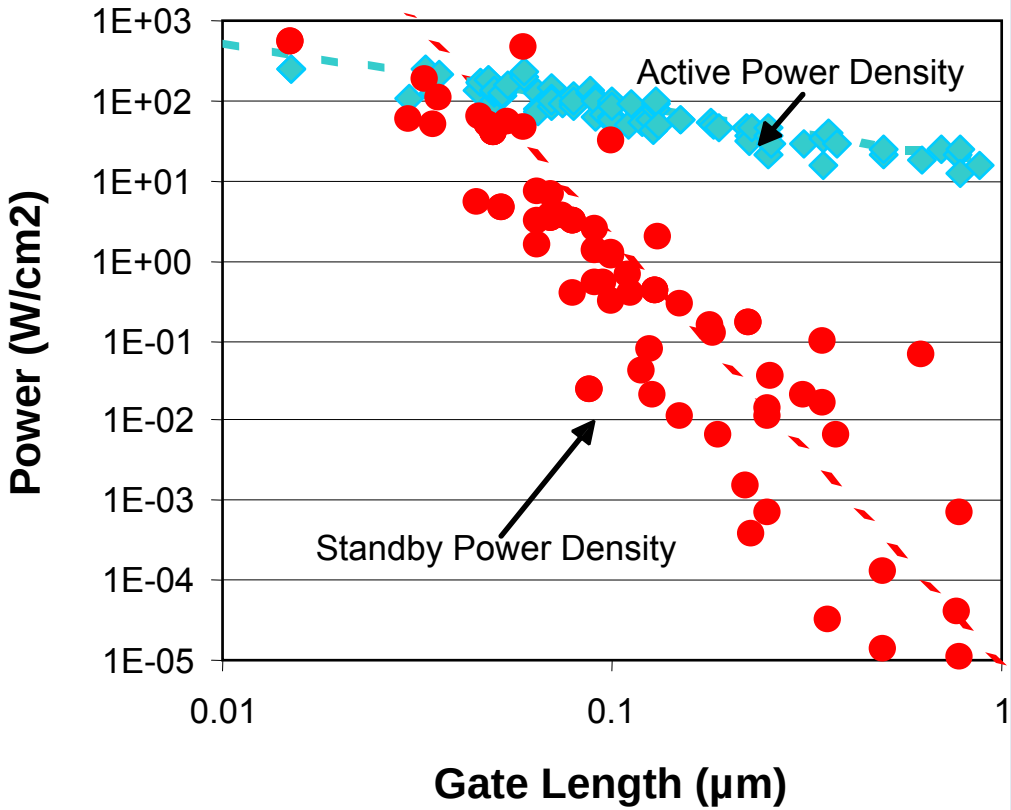
- **a dramatic rise in power density**

B. Meyerson, IBM, Semico Conf., January 2004, Taiwan.

IBM says, "There's a Power Crisis in CMOS"

Leff and Vdd trends result in:

- Active Power Density growth ~1.3X/generation
- Passive Power Density growth ~3X/generation
- Gate Leakage Power Density >4X/generation`



The CMOS Power Crisis:

Simple scaling is no longer an option, as we have hit a "power cliff"

B. Meyerson, IBM, Semico Conf., January 2004, Taiwan.

Implications of Power Crisis

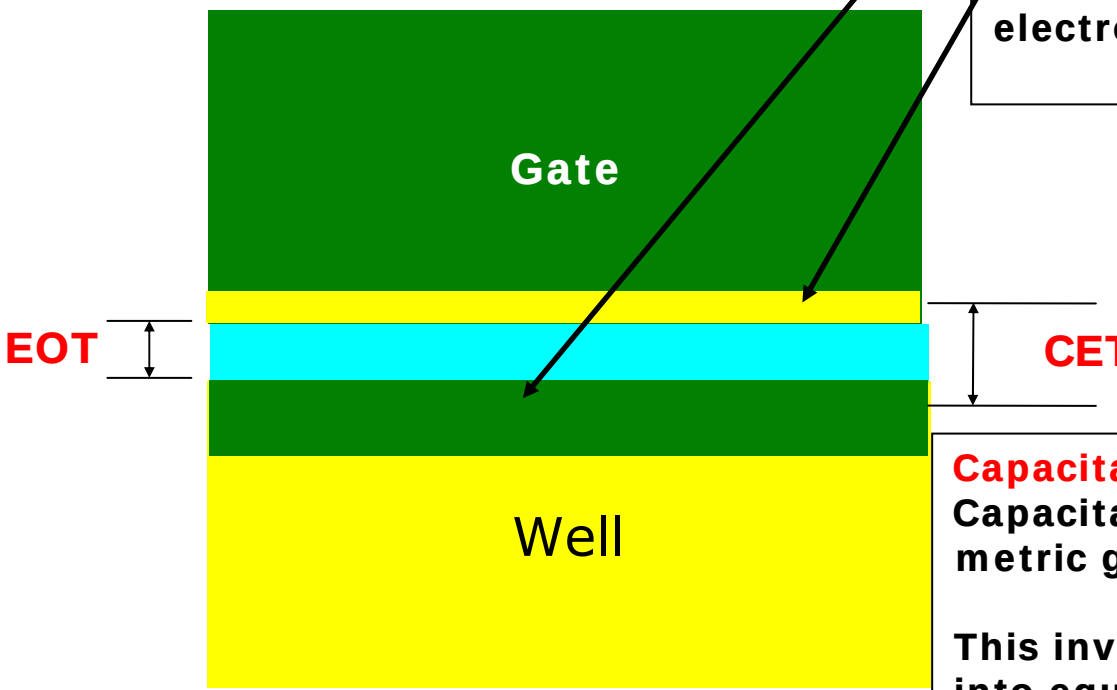
- New materials will be introduced
  - Plasma Nitrided Gate Dielectric
  - High-k Gate Dielectric
  - Metal Gate
- New processes will be introduced
  - Co-implantation of species to suppress diffusion
  - Diffusion free annealing processes
  - High-tilt high current implantation
- Processed induced strained silicon will be adopted
  - SiN overlayers
  - Recessed SiGe source/drain extensions

Gate Stack Opportunities

More Detailed Look at Gate Stack

Gate Stack Bias Causes:
Inversion layer to form in Si under the gate oxide.

Small depletion layer to form in poly-Si electrode



Capacitance Equivalent Thickness (CET):
Capacitance in inversion is the true metric governing device performance.

$$Q = CV$$

This inversion capacitance translated into equivalent oxide thickness as CET or Tox inversion.

CET/Tox Inversion Governs Transistor Drive Current

Gate Capacitor Considerations

$$C = k\varepsilon_0 A/t$$

k = dielectric constant
ε_0 = permittivity of free space
A = capacitor area
t = thickness of capacitor

$$1/C_{inversion} = 1/C_{dielectric} + 1/C_{inversion\ layer} + 1/C_{poly\ depletion}$$

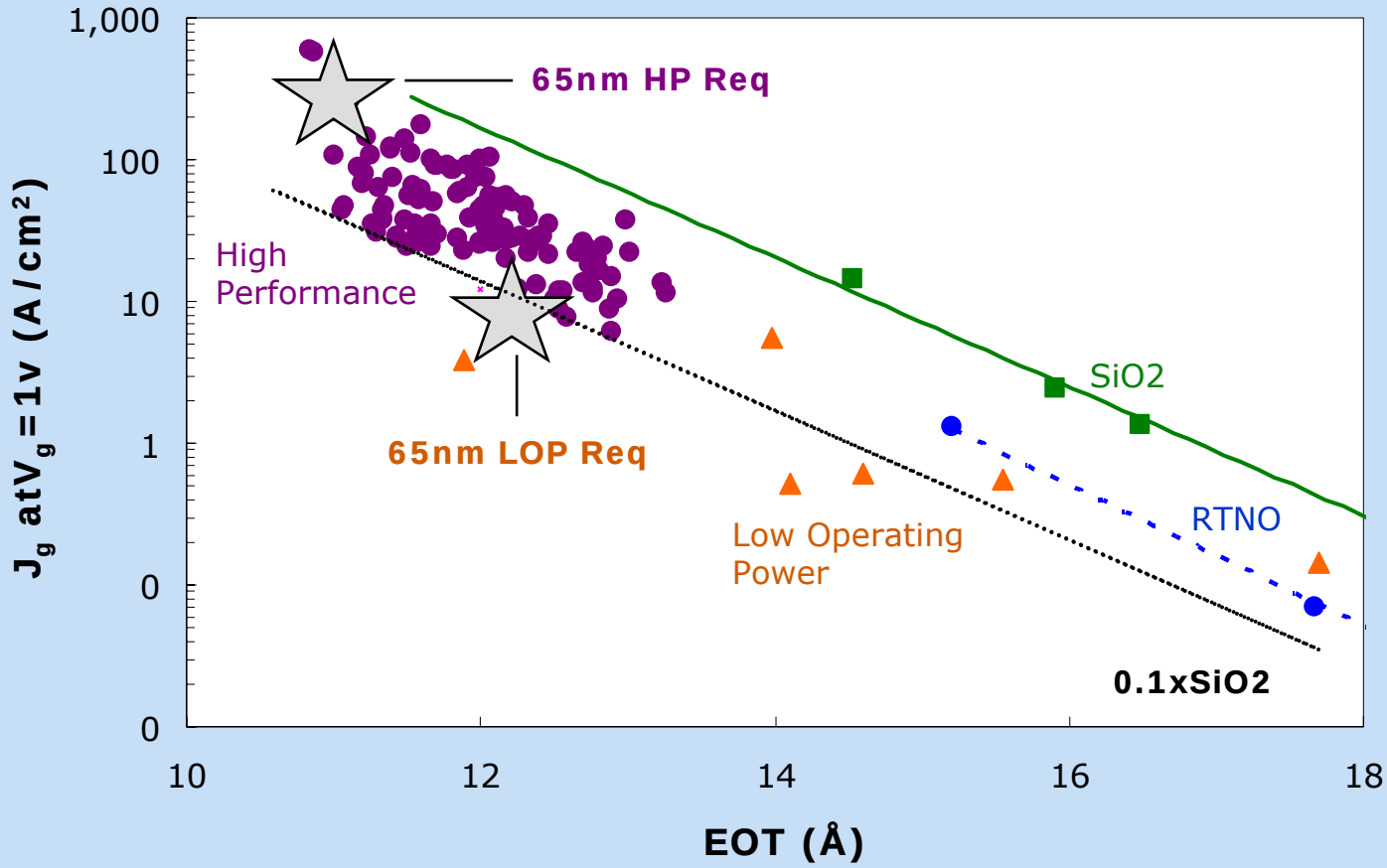
Assuming equal k's:

$$CET = EOT + t_{inversion\ layer} + t_{poly\ depletion}$$

CET	$J_{g\text{-}reduction}$	$t_{dielectric}$	EOT	$t_{inv.\ layer}$	$t_{poly\ depl.}$	Technology
20Å	1x	12Å	12Å	4Å	4Å	Oxide/Poly
20Å	10x	12Å	12Å	4Å	4Å	Oxinitride/Poly
20Å	10,000x	30Å	12Å	4Å	4Å	Hi-k/Poly
16Å	10,000x	30Å	12Å	4Å	0Å	Hi-k/Metal Gate

Industry driving toward high-k and metal gates

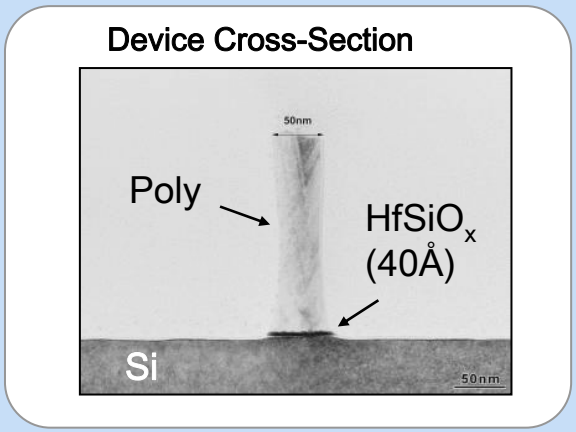
Plasma Nitrided Gate Stack: Scaling to 65nm

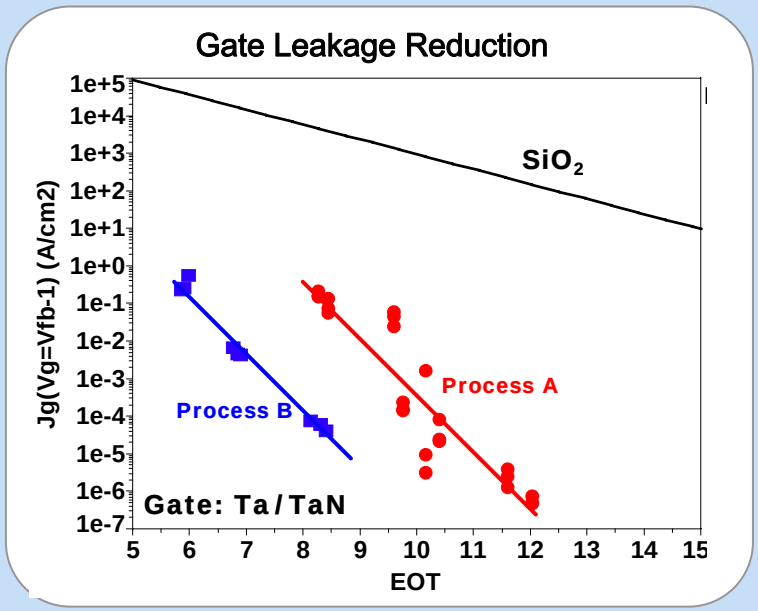


DPN gate nitridation meets 65nm HP and LOP device requirements.

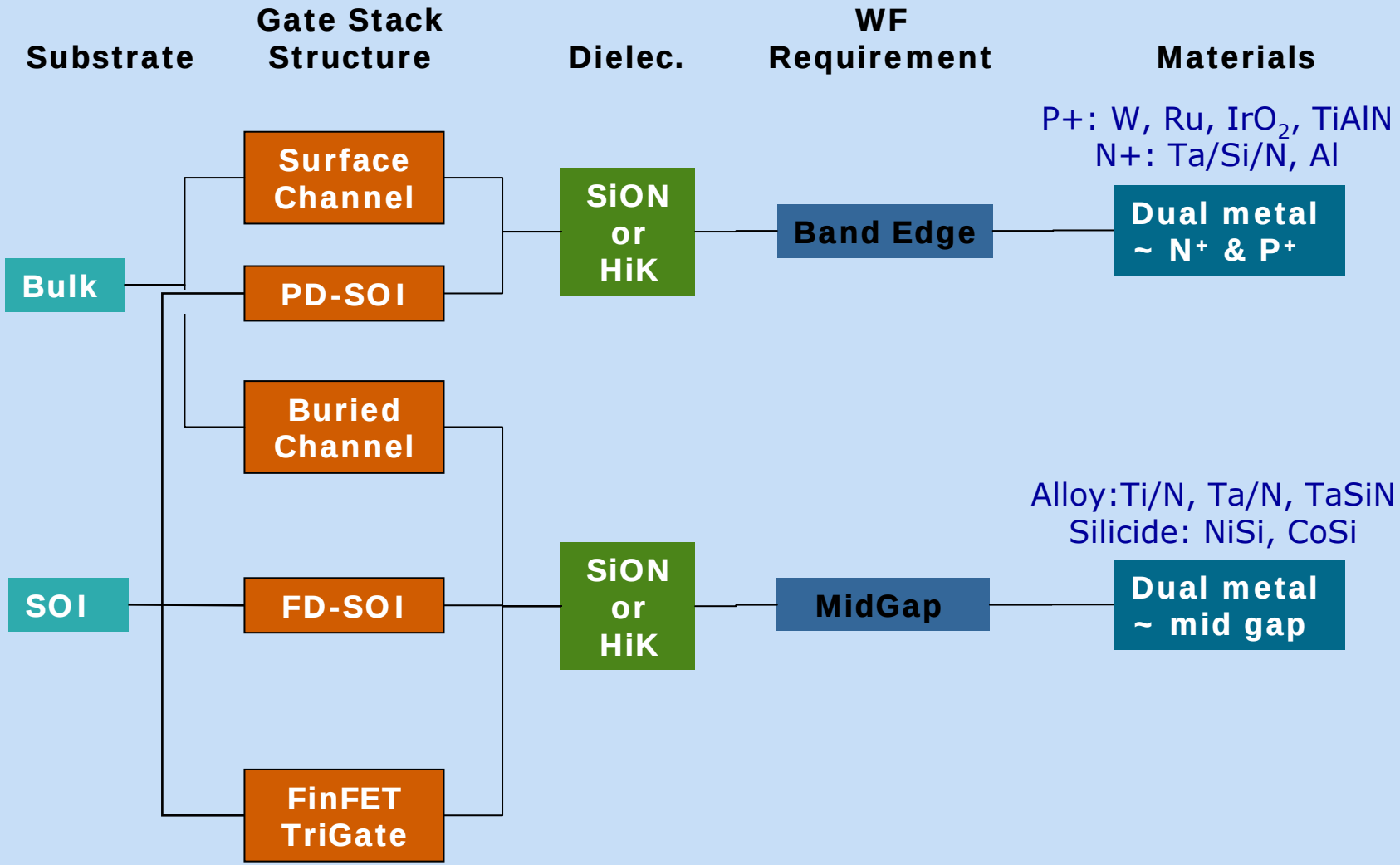
Gate Dielectric Leakage Reduction with High-k/Metal Gate

ITRS Roadmap	45nm
EOT (Å)	8
Poly depletion + QM (Å)	4
Gate Leakage (A/cm^2)	2,000





45nm Gate Stack Technology Landscape



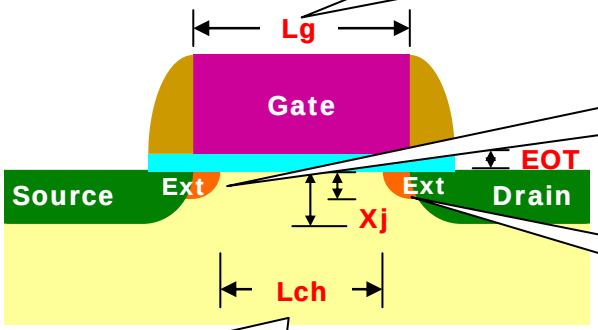
Ultra-Shallow Junction

Device Scaling and Doping Drivers

Key Parameters for Transistor Improvement

- **Speed: Ion / Idsat : Increase** → **Resistance : Rs : Decrease** → **Higher Doses, Higher Anneal Temp.**
- **Leakage: Ioff : Reduce** → **Junction Depth: Xj : Decrease** → **Lower Implant Energies, Shorter Anneal Time**

Gate Length: **Requirement = smaller**
Physical gate length. Typically, Lg is smaller than design rule (technology node).



Contact / Extension / Channel Resistance: **Requirement = lower**
Reducing resistance in Contact/Extension/Channel path
Increases conductance and raises switching speed

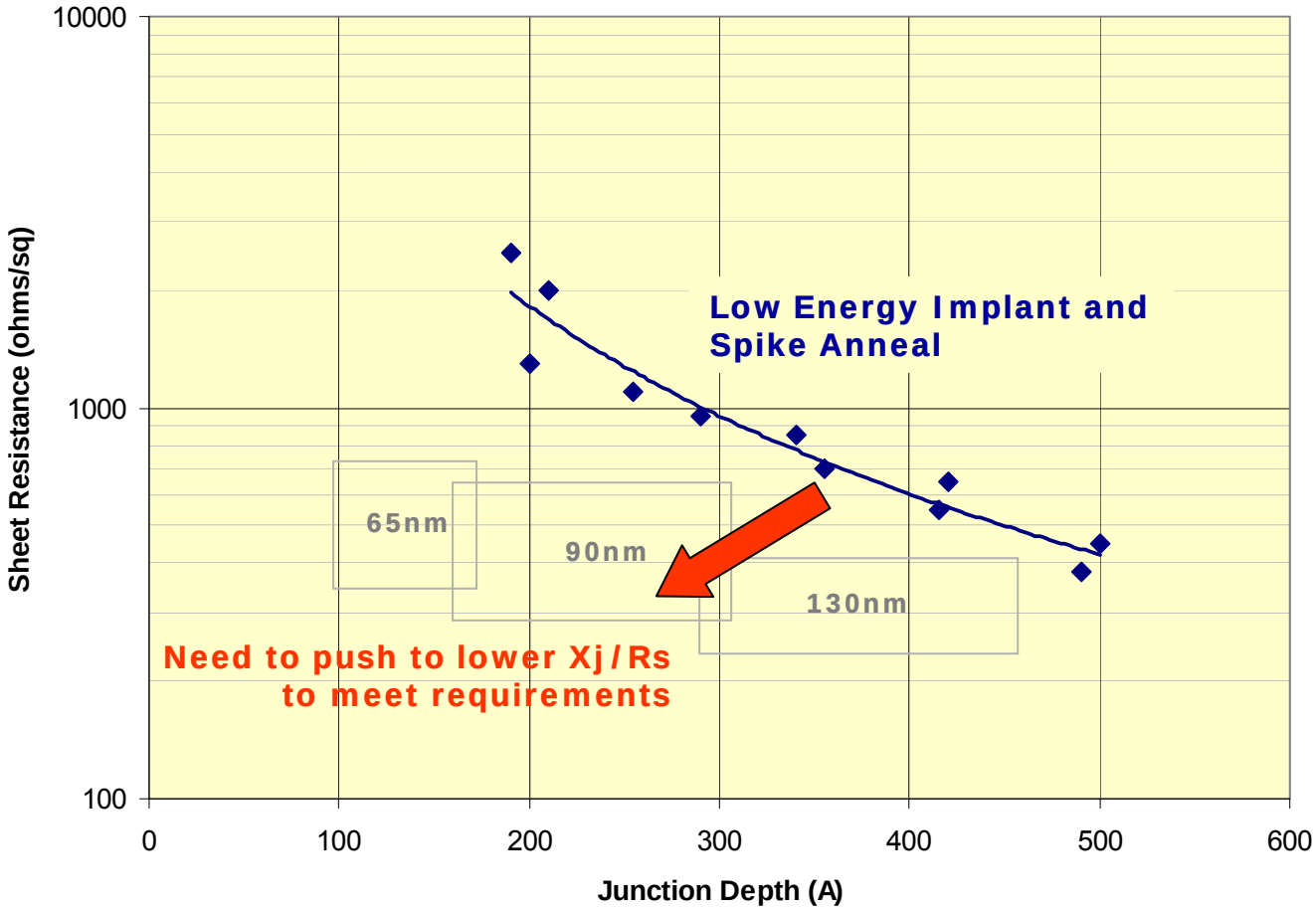
Channel Length: **Requirement = smaller**
Effective gate length, which is smaller than Lg.

Junction Depth: **Requirement = shallower**
As channel length decreases, electric field interaction results in leakage from Drain to Source when transistor is Off (Short Channel Effect – SCE).
Shallower Xj reduces SCE leakage

Scaling Challenges Implant and Anneal Systems

Technology Curve for Current PTORs and Process

- Boron TED is a limiting factor to USJ formation
- Solid solubility limit of B in Si and fast diffusion of B must be overcome
- Shallow and Abrupt implant profiles required
- Productivity is challenge for USJ doping
  - lower energies
  - higher doses
  - additional implants



Current Generation tools and typical low energy implant/spike anneal process do not meet ITRS requirements

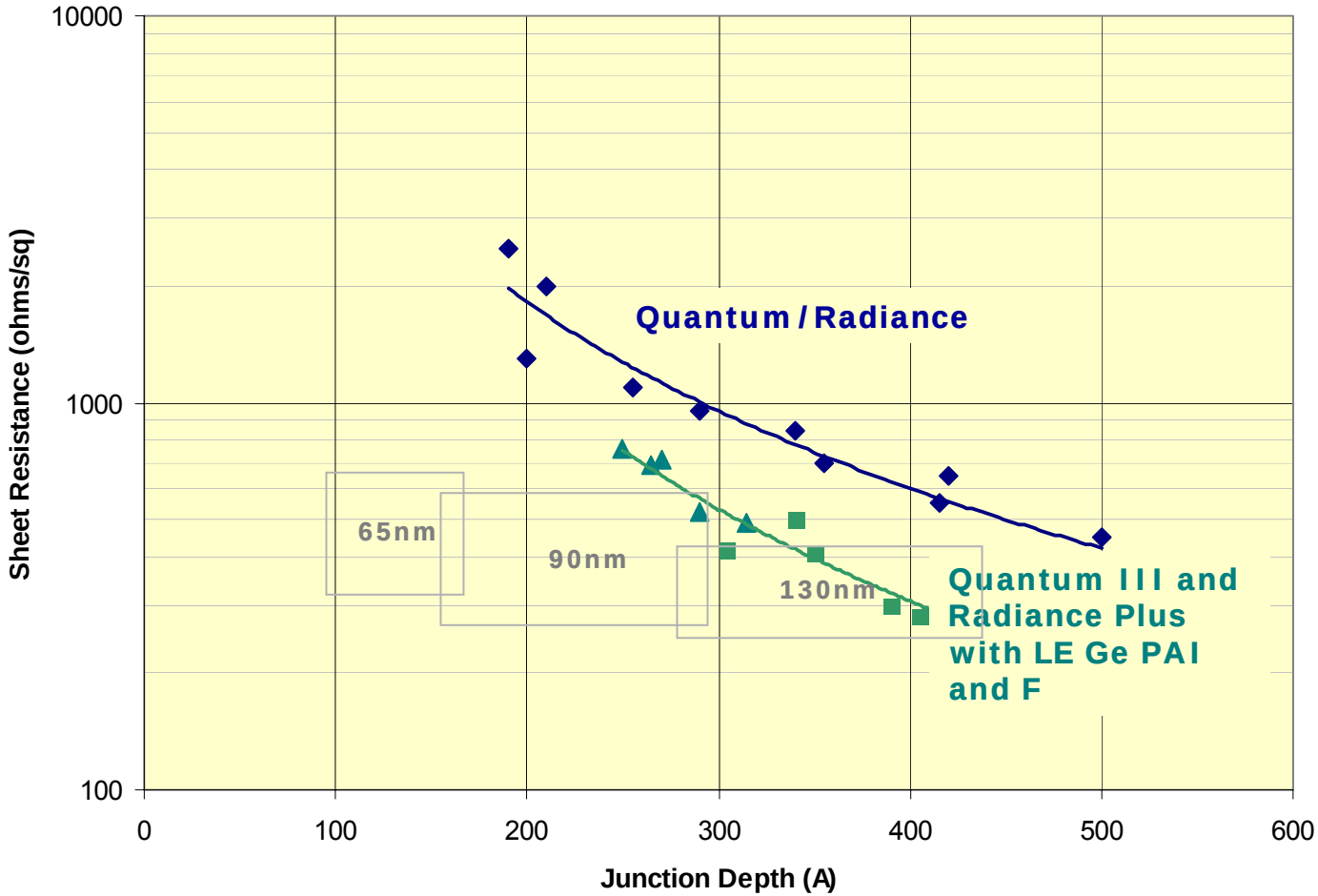
Technology Curves for Shallow Junctions

Key Metrics/trend

- Xj ↓
- Rs ↓
- Abruptness ↓

Challenges

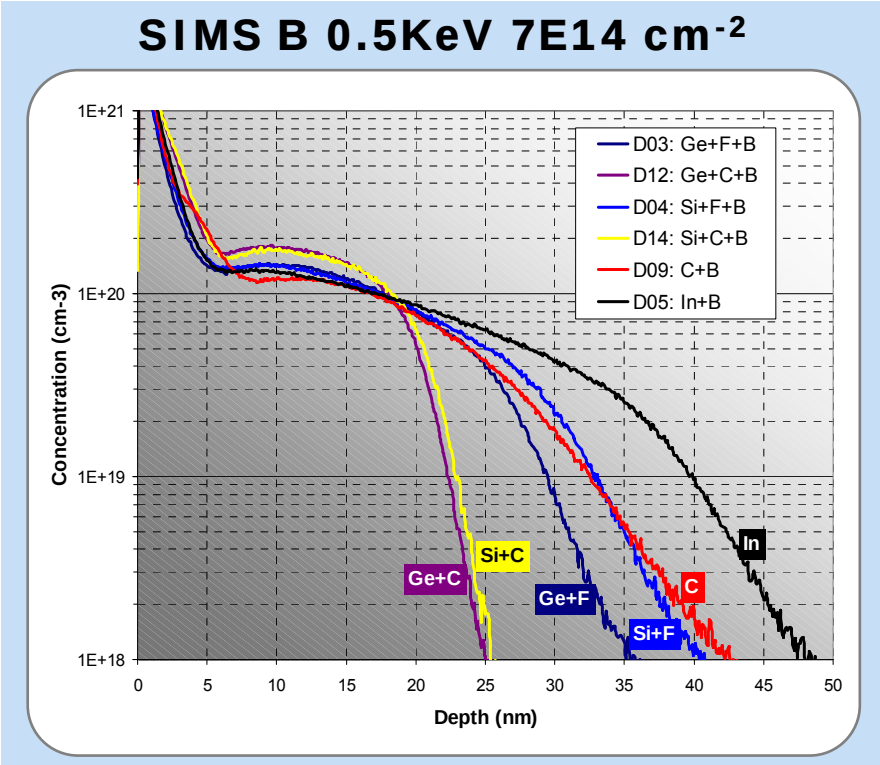
- Implant Productivity
- Minimizing diffusion during activation step
- Overlap formation without diffusion
- Channel Strain Tailoring



Process and hardware improvements extend Quantum and Radiance to 90nm

65nm USJ: Carbon Co-Implant + Spike Anneal

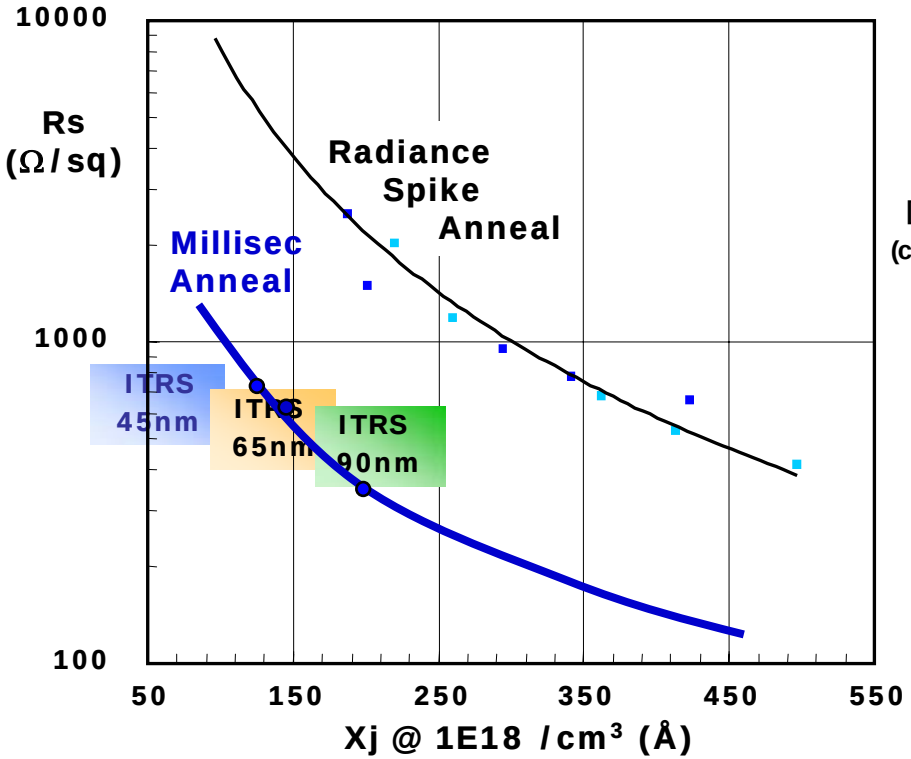
Partnership with IMEC

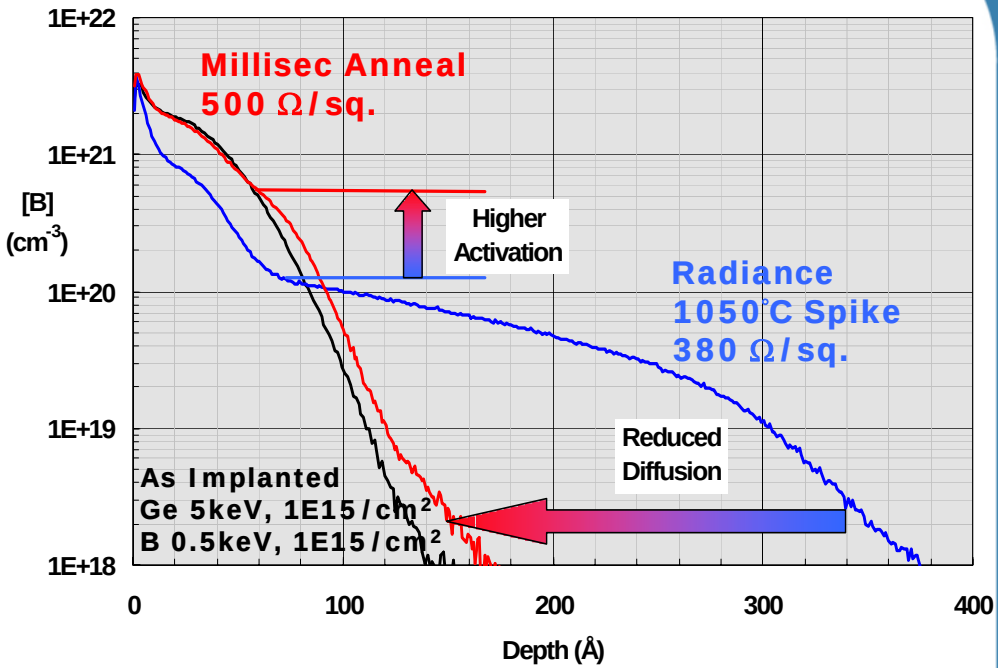


- Junction depth and abruptness improved with C co-implant

Quantum X + Radiance*Plus*
extend to meet customers' 65nm requirements.

Millisecond Anneal Capability for 65nm USJ





Tech. Node	90nm	65nm	45nm	30nm
Rs	<660Ω/sq	<760Ω/sq	830Ω/sq	940Ω/sq
Xj	<250Å	<170Å	<100Å	<70Å
Abruptness	4.1nm/dec	2.8nm/dec	2.0nm/dec	1.4nm/dec

Technology: spike | transition | Advanced

Advanced Annealing Potential:

- Preserves as-implanted profile with <25Å diffusion
- High activation due to peak temp ~1200°C
- High throughput (>40 wph/chamber)
- Lower total power required than Radiance

***Activation without Diffusion* will extend USJ to the 45nm node**

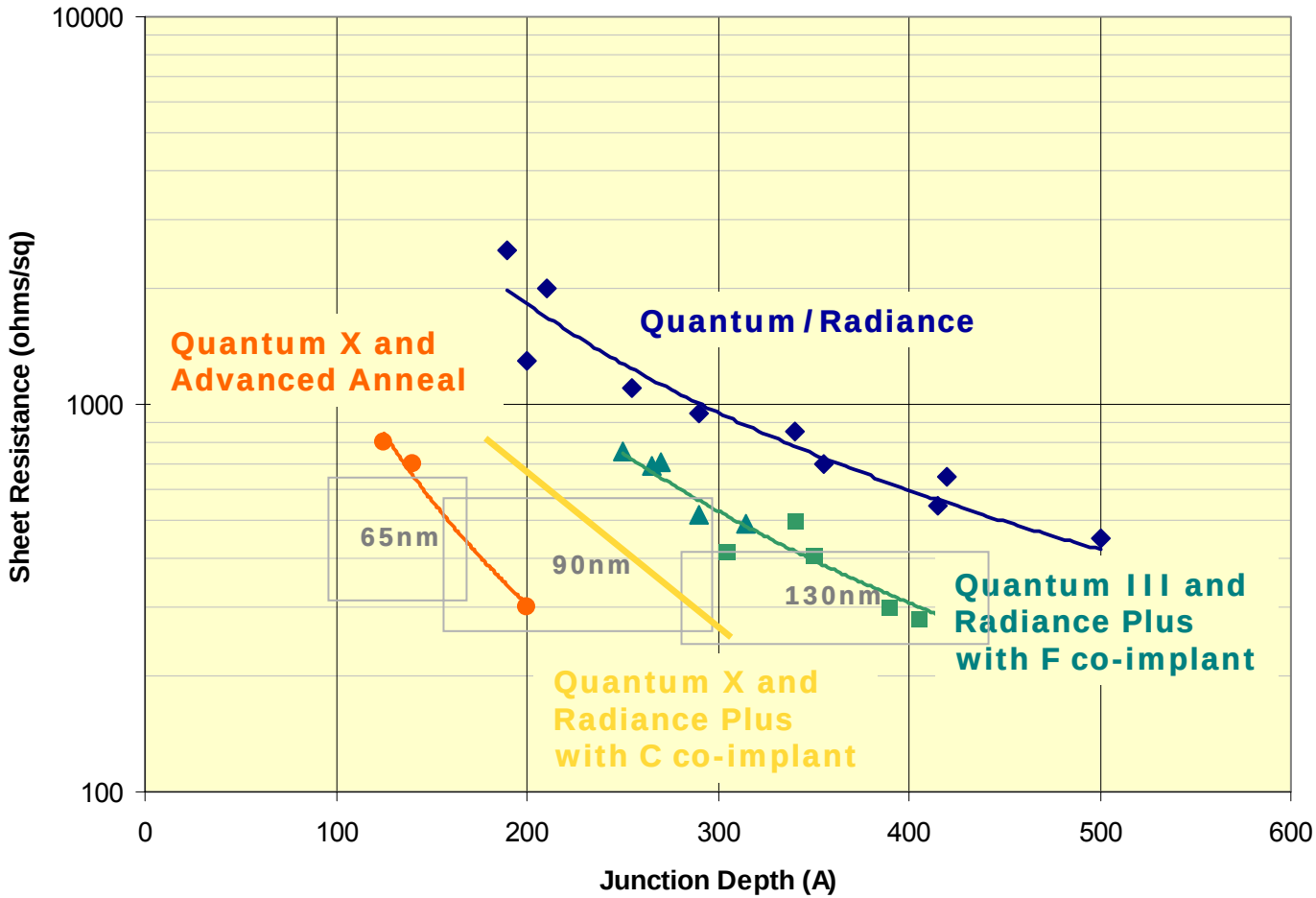
Technology Curves for Shallow Junctions

Key Metrics/trend

- XJ ⬇
- Rs ⬇
- Abruptness ⬇

Challenges

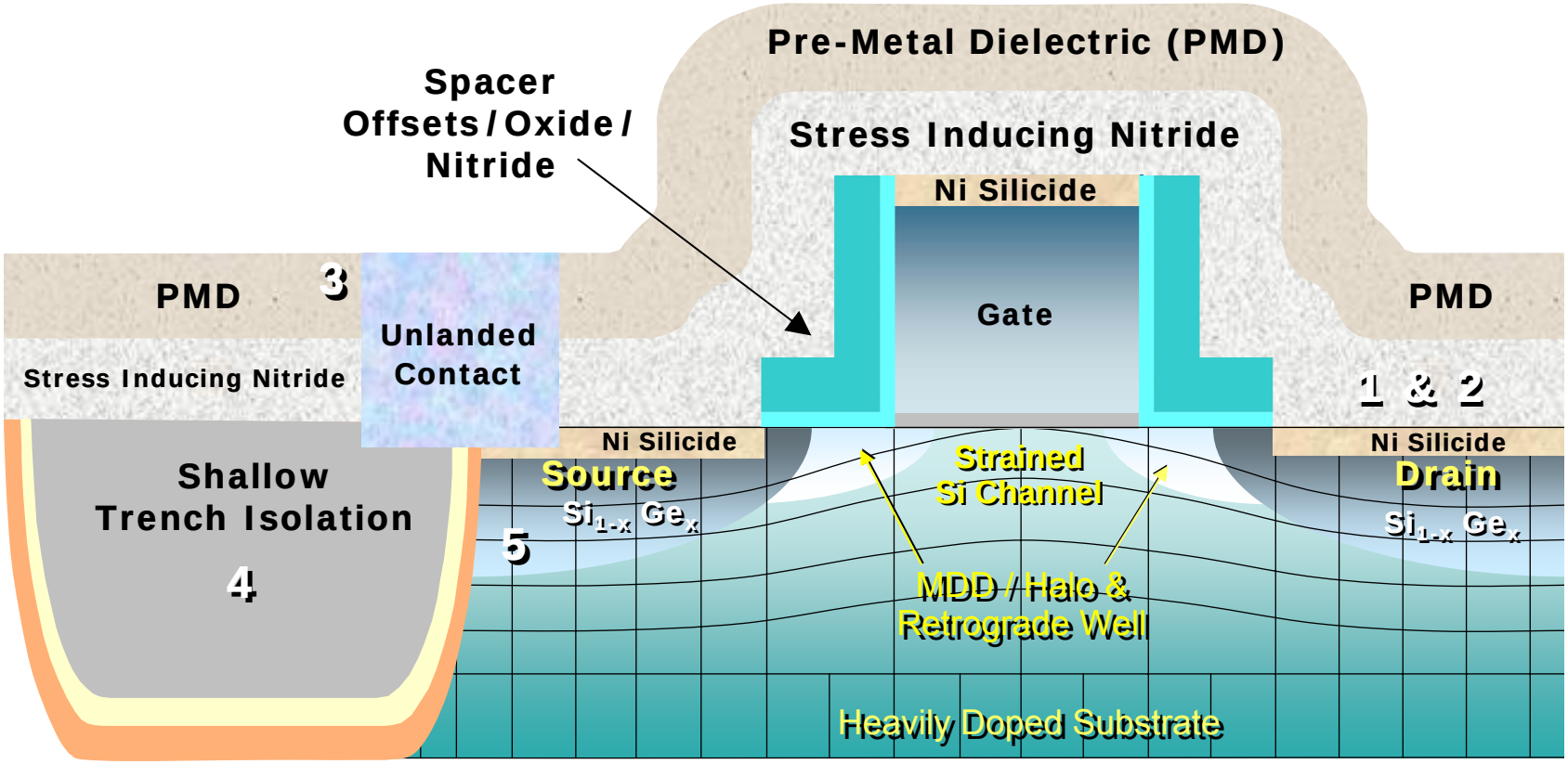
- Implant Productivity
- Minimizing diffusion during activation step
- Overlap formation without diffusion
- Channel Strain Tailoring



Process and hardware improvements extend Quantum and Radiance to 90nm
New technology development enables Xj / Rs scaling to continue

Strained Silicon

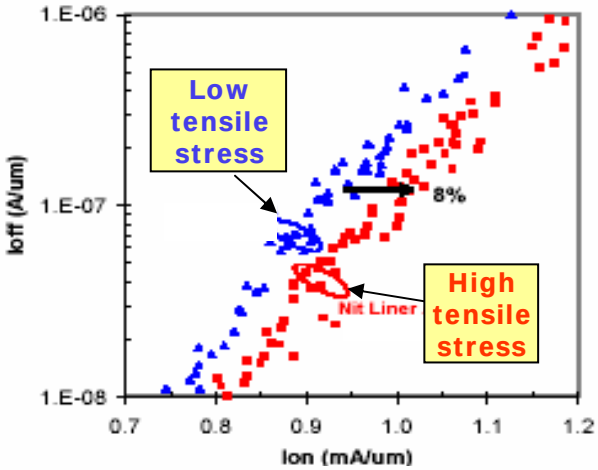
Applied Materials Suite of Stress Inducing Films



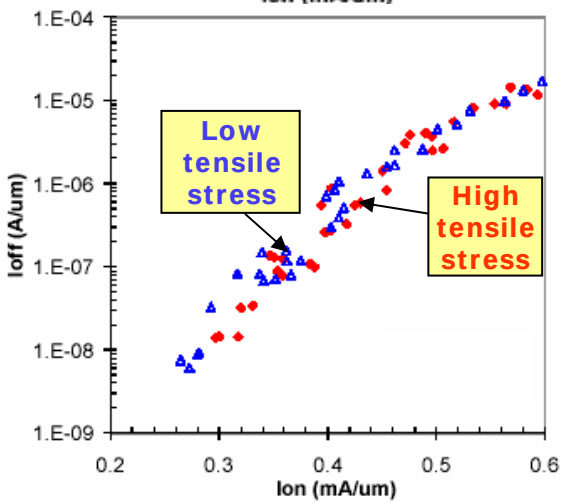
1. Tensile Silicon Nitride (NMOS)
2. Compressive Silicon Nitride (PMOS)
3. Tensile - HARP PMD
4. Tensile - HARP STI
5. Selective Epitaxial Silicon Germanium

High Stress Nitride for NMOS/PMOS Ion-Ioff (IBM, 2003)

NMOS

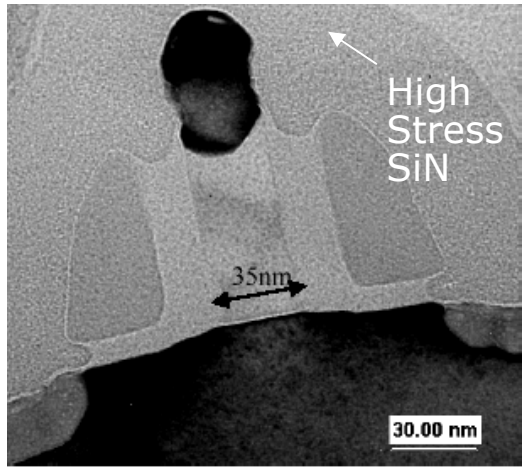


PMOS



Better NMOS performance (8%) and no PMOS degradation.

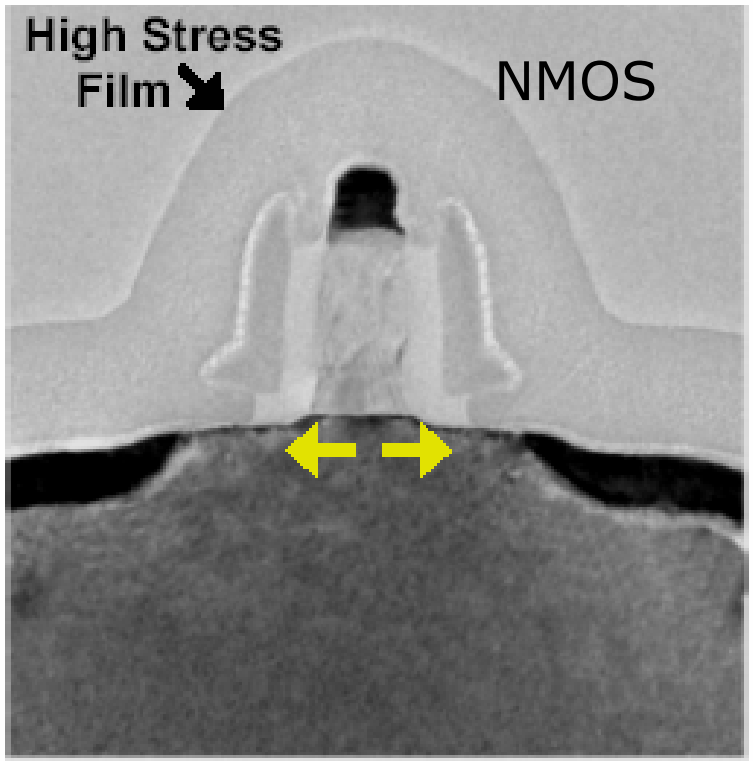
90nm MOSFET, Tensile stress 1.4GPa in etch stop (Conventional <0.7Gpa)



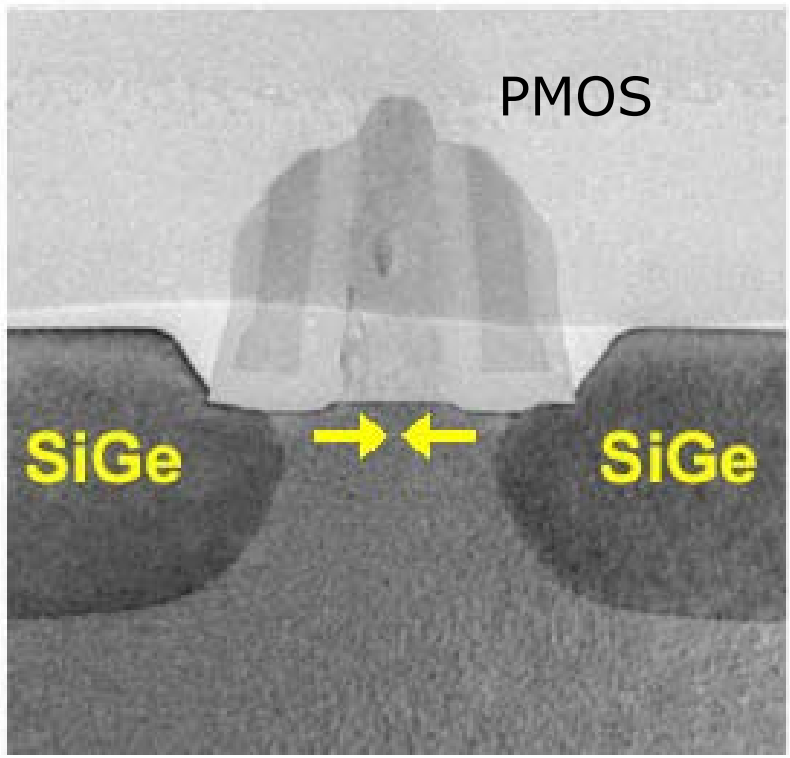
Optimized strain engineering enabling high performance NMOS with no impact on PMOS performance with minimum manufacturing complexity.

Ref.: V. Chan et al, "High speed 45nm Gate Length CMOSFETs Integrated Into a 90nm Bulk Technology Incorporating Strain Engineering," IBM Microelectronics (SRDC), IEDM 2003, Washington DC.

Strain Engineering for High Performance Logic



TEM of 45 nm gate length device using SiN in tensile stress to improve NMOS drive current (10% improvement in Idsat))

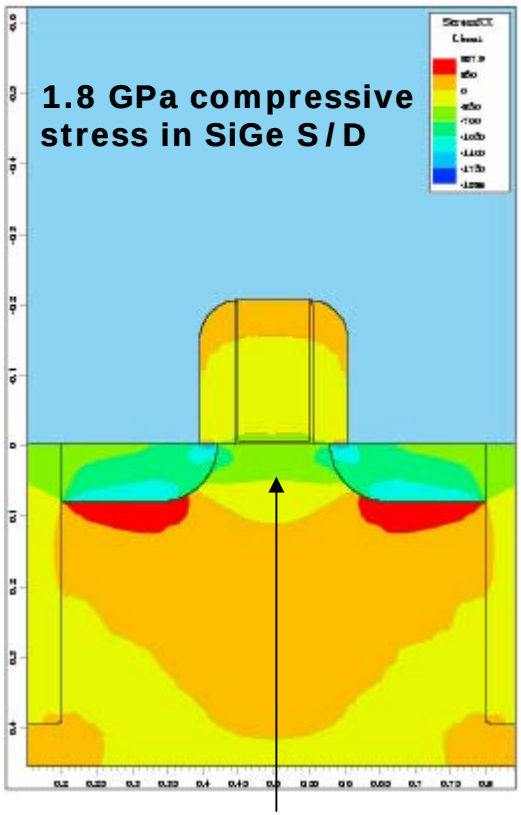


TEM of PMOS device where SiGe in the source/drain areas are used to induce compressive stress in the Si channel (25% improvement in Idsat)

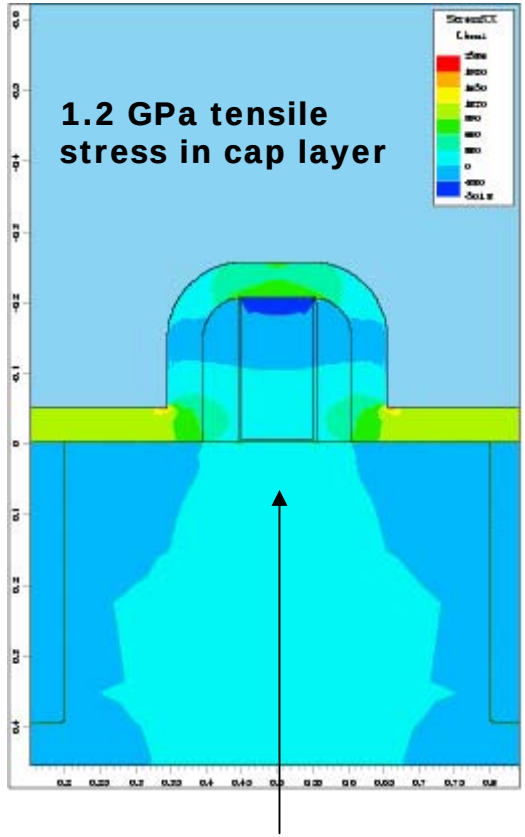
Ref.: T. Ghani et al, "A 90 nm High Volume Manufacturing Logic Technology Featuring Novel 45nm Gate Length Strained Silicon CMOS Transistors," Intel Corp., IEDM 2003, Washington, D. C.

Intel uses both SiN overlayer and SiGe recessed S/D for strained Si

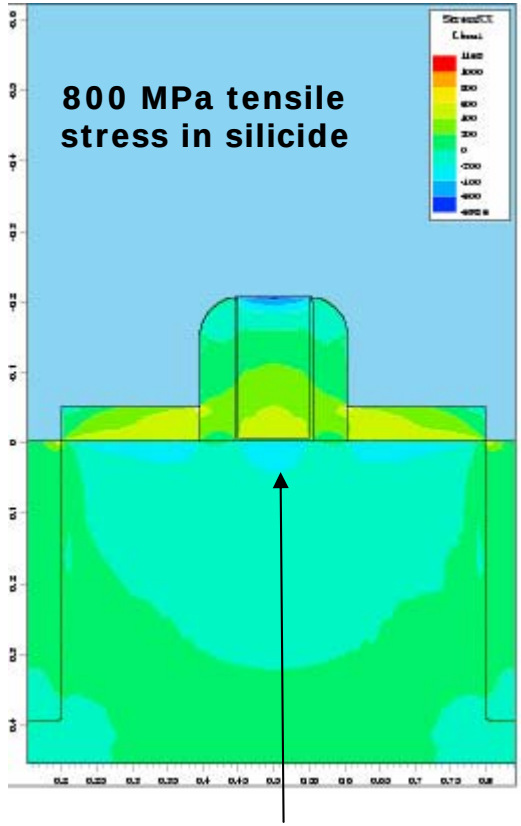
Modeling Localized Strain



Compressive stress
in channel



Tensile stress in channel

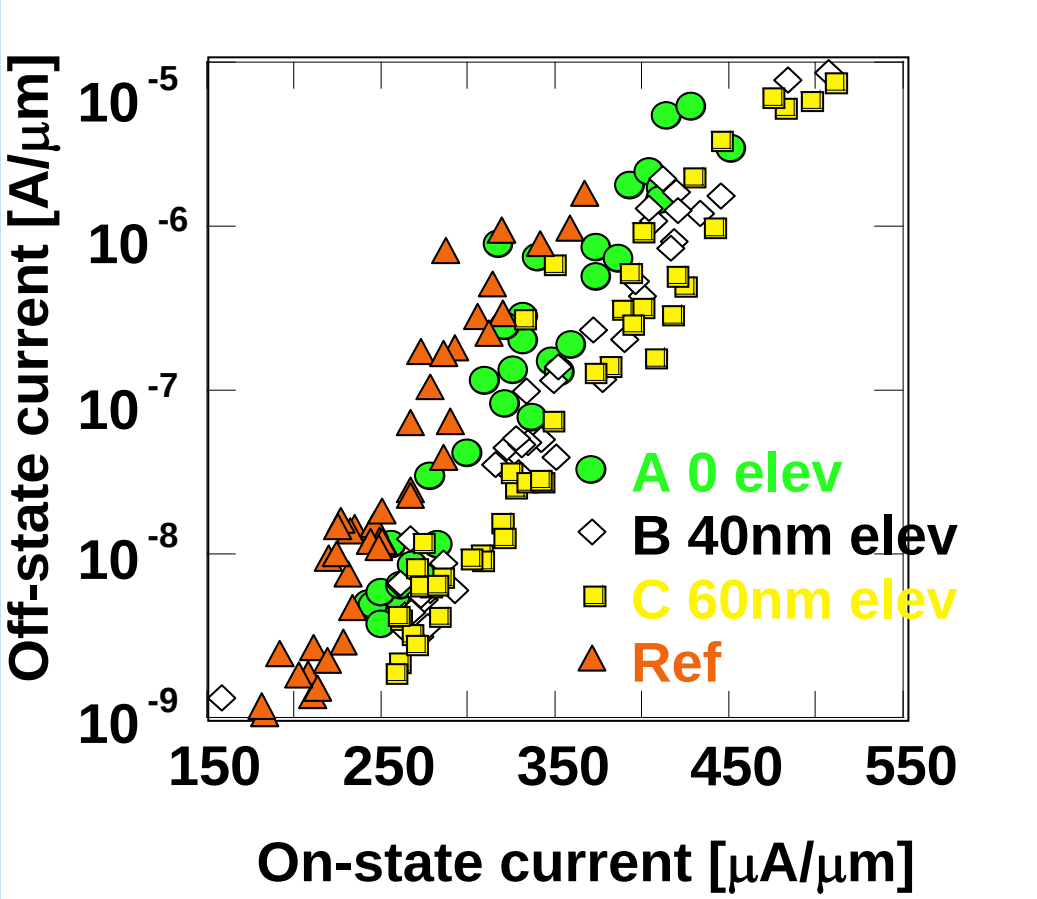


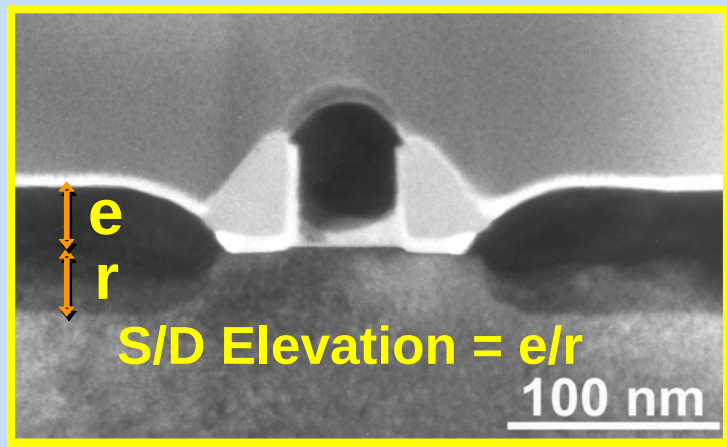
Compressive stress
in channel

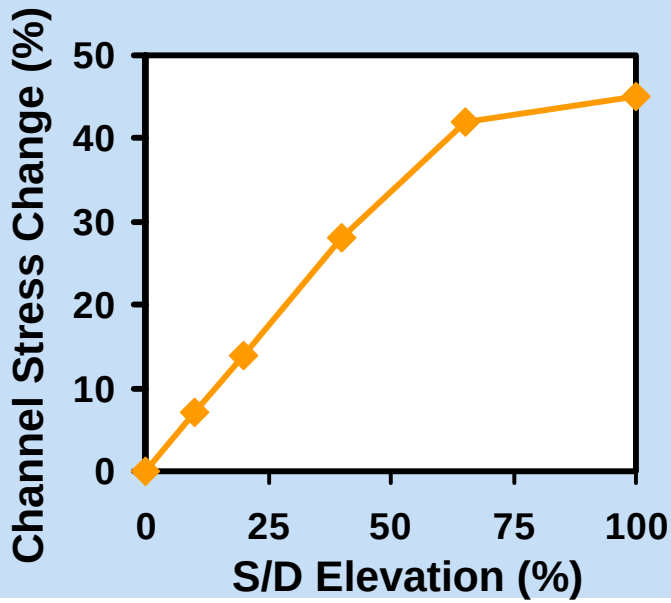
Simulations courtesy of Synopsys

JDP with Synopsys provides understanding for process optimization

Elevation improves device performance



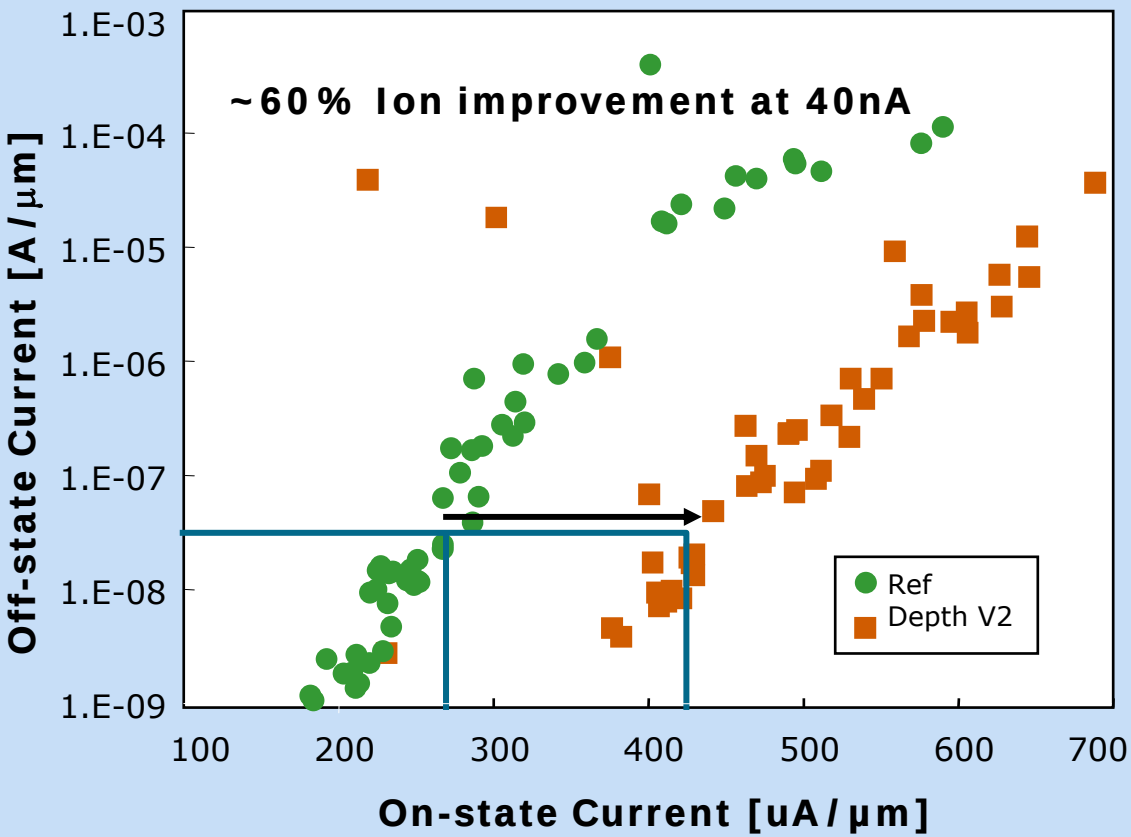


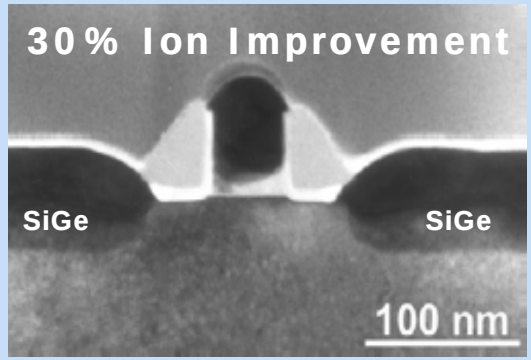


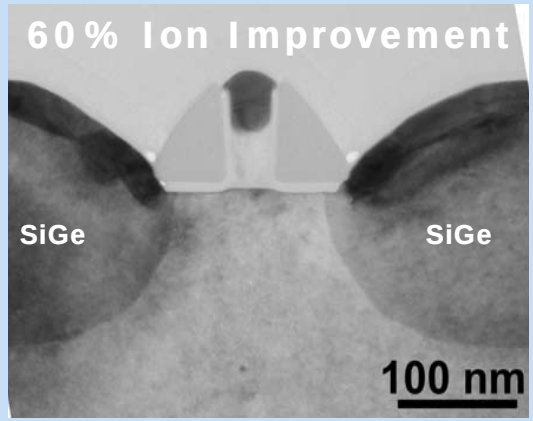
Applied/IMEC/Synopsys Collaboration

S/D elevation improves drive current but the effect saturates at ~40nm

Recent Recessed SiGe IMEC Transistor Data







Applied/IMEC/Synopsys Collaboration

60% drive current improvement demonstrated with 120nm recessed etch.

AMAT / IMEC / Synopsys Strained Si IEDM 2004 Paper

A Systematic Study of Trade-offs in Engineering a Locally Strained pMOSFET

F. Nouri, P. Verheyen[1], L. Washington, V. Moroz[2], I. De Wolf[1], M. Kawaguchi, S. Biesemans[1], R. Schreutelkamp, Y. Kim, M.Shen, X. Xu[2], R. Rooyackers[1], M. Jurczak[1], G. Eneman[1,3,4], K. De Meyer[1,3,4], L. Smith[2], D.Pramanik[2], H.Forstner, G. Higashi

Applied Materials, Sunnyvale, CA USA; [1] IMEC, Leuven, Belgium; [2]Synopsys, Mountain View, CA USA; [3]Research assistant of The Fund for Scientific Research - Flanders (Belgium); [4]K.U.Leuven, ESAT-INSYS, 3001 Leuven, Belgium

Abstract

We present results of a study on the impact of process parameters on strain-enhanced performance of a pMOSFET with recessed SiGe S/D. Recess depth, layout sensitivity, and the subsequent impact on strain and hole mobility are explored. Micro-Raman Spectroscopy (μRS), process and device simulations and electrical results are discussed.

is still very uniform, but at a lower level of 622 MPa. Mobility enhancements and degradations due to the different stress components is summarized in Fig.8. This table is obtained based on the classic piezoresistance model [7], which is reported to provide reasonable accuracy in [8] as well as in this work.

The piezoresistance model for the stress enhanced hole mobility has been applied to the simulation of 40nm pMOSFET performance in

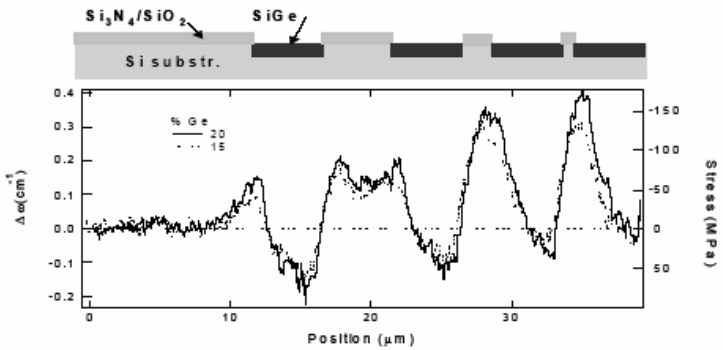


Figure 2: Influence of %Ge on stress in the channel measured by Raman spectroscopy. The stress is calculated from the Raman shift assuming uniaxial stress. Both samples have 70nm etch depth and no undercut.

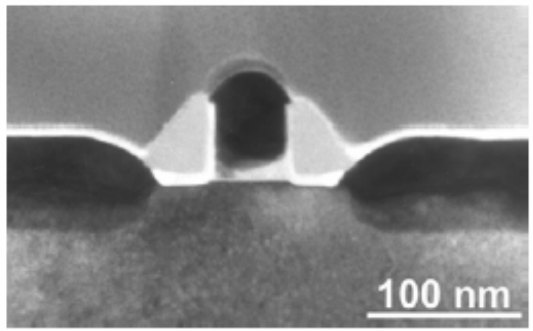
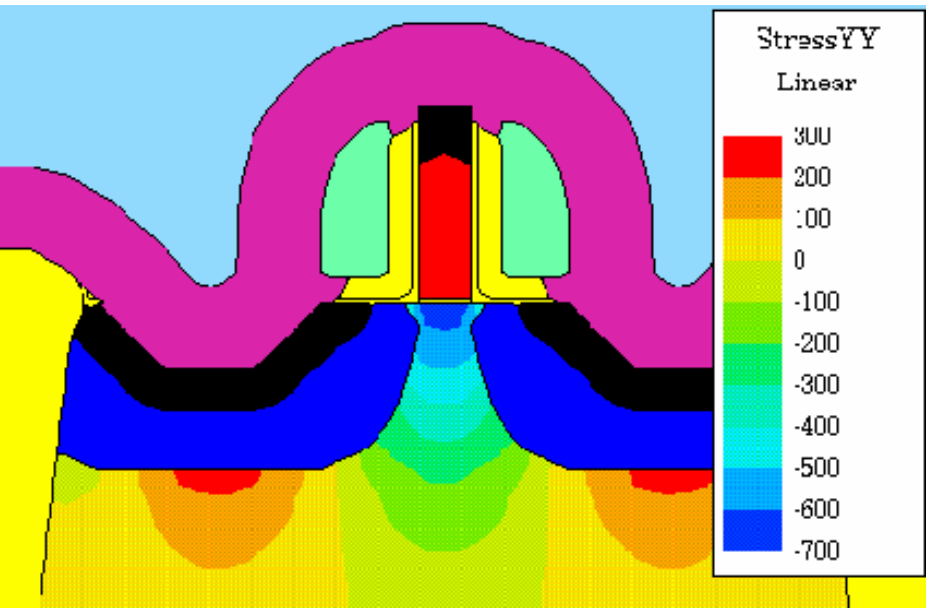


Figure 3: Cross section TEM showing SiGe in the source/drain area

Leading Development on Recessed S/D Strained SiGe

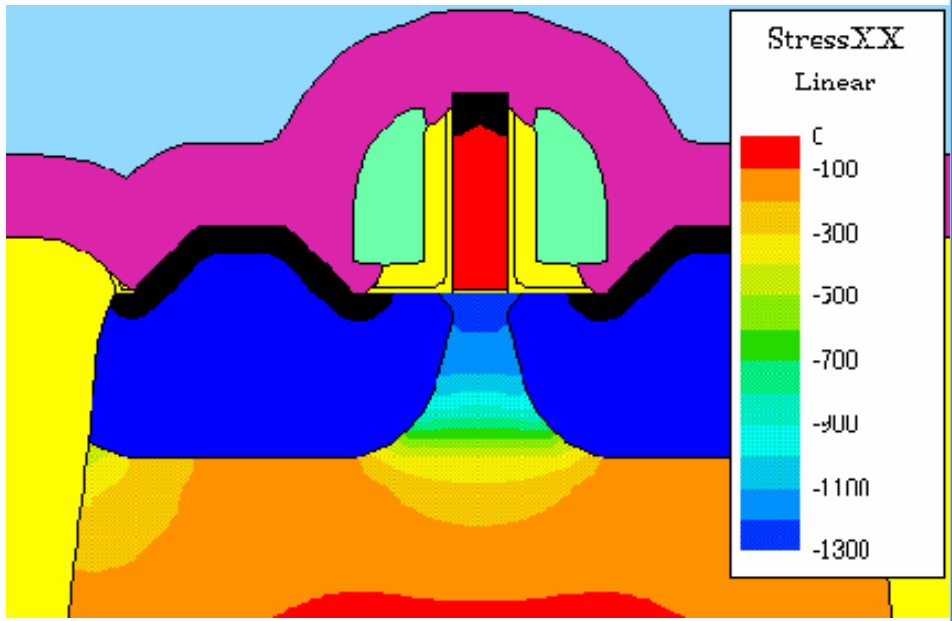
nMOS and pMOS stress contours

nMOS Geometry



Includes stress from
tesile STI and tensile ESL

pMOS Geometry



Includes stress form tensile STI,
SiGe and compressive ESL

Courtesy of Synopsys