Jets-ECD (JECD) and Multiple Seed Layers For Copper Interconnects < 0.10µm

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Jets Plating Cell

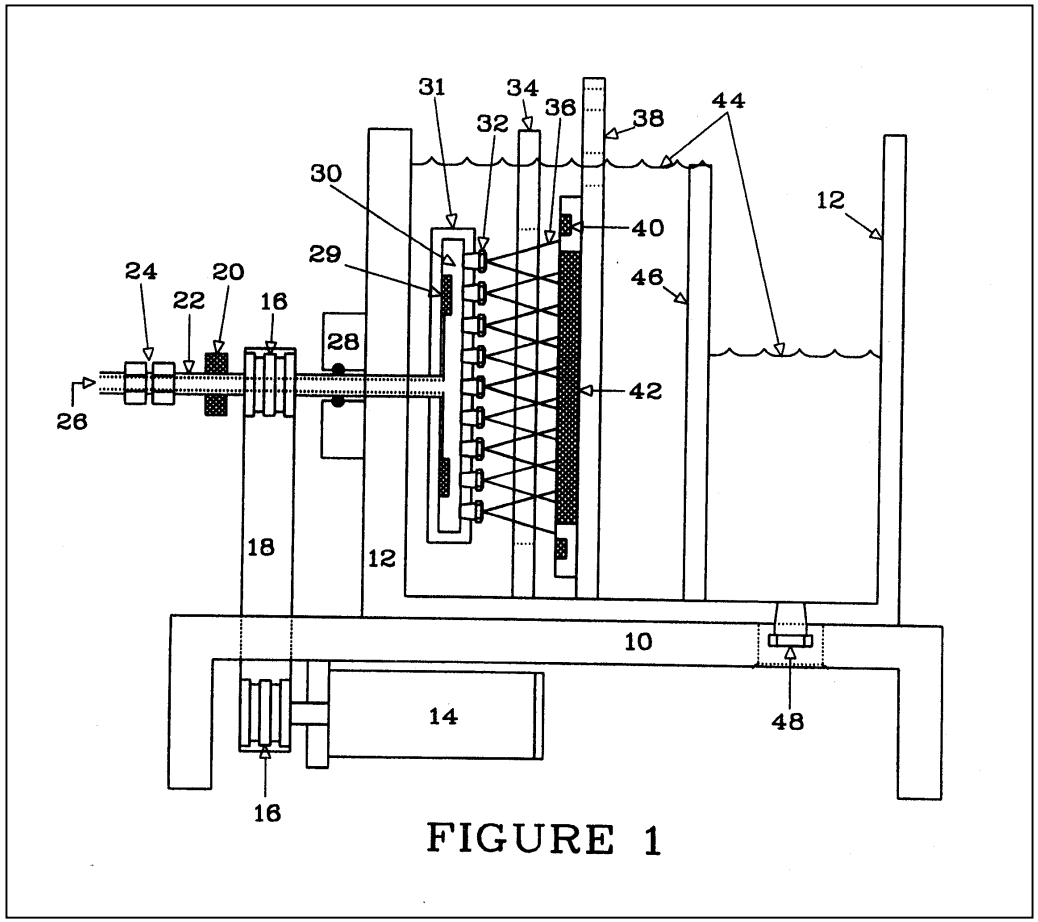
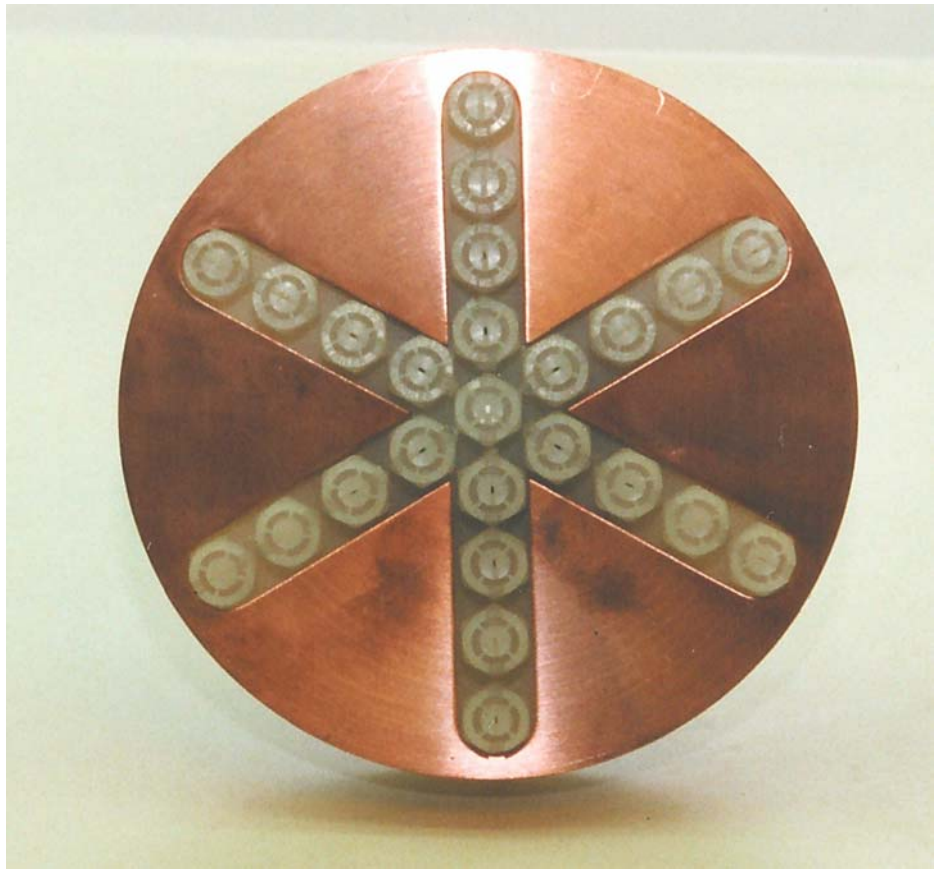


FIGURE 1

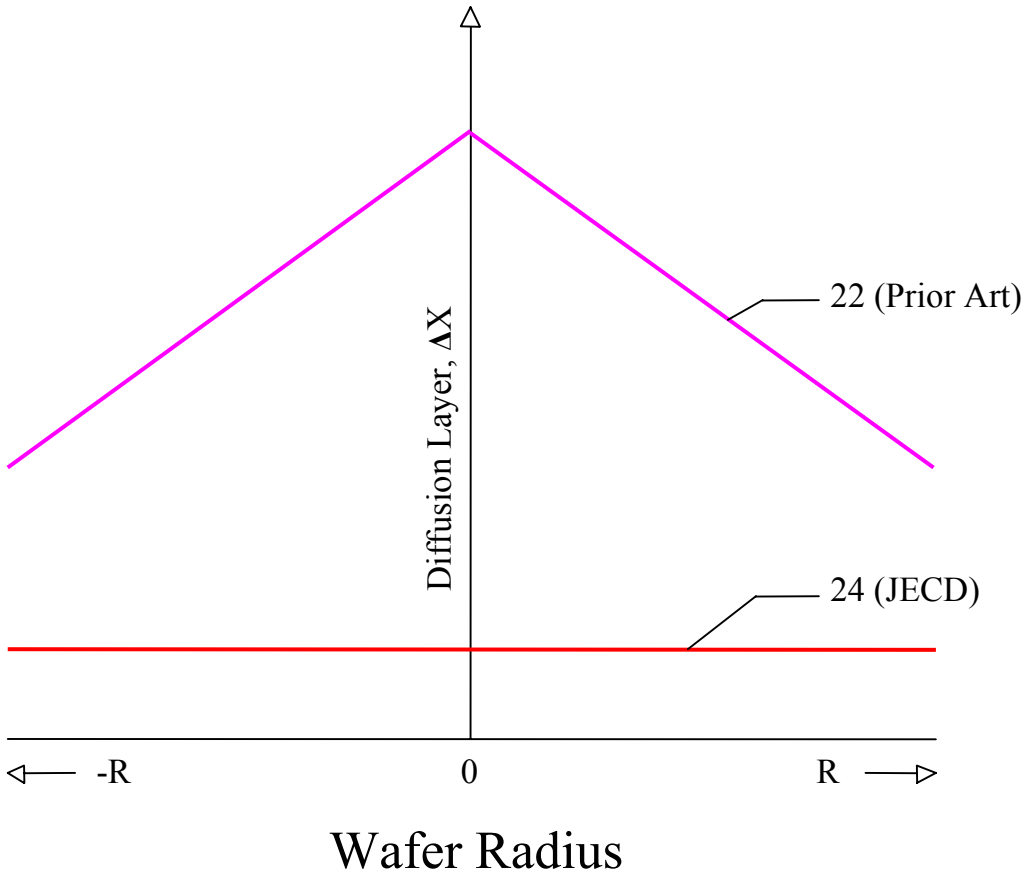
US Patent 5,421,987

Anodes/Jets Assembly

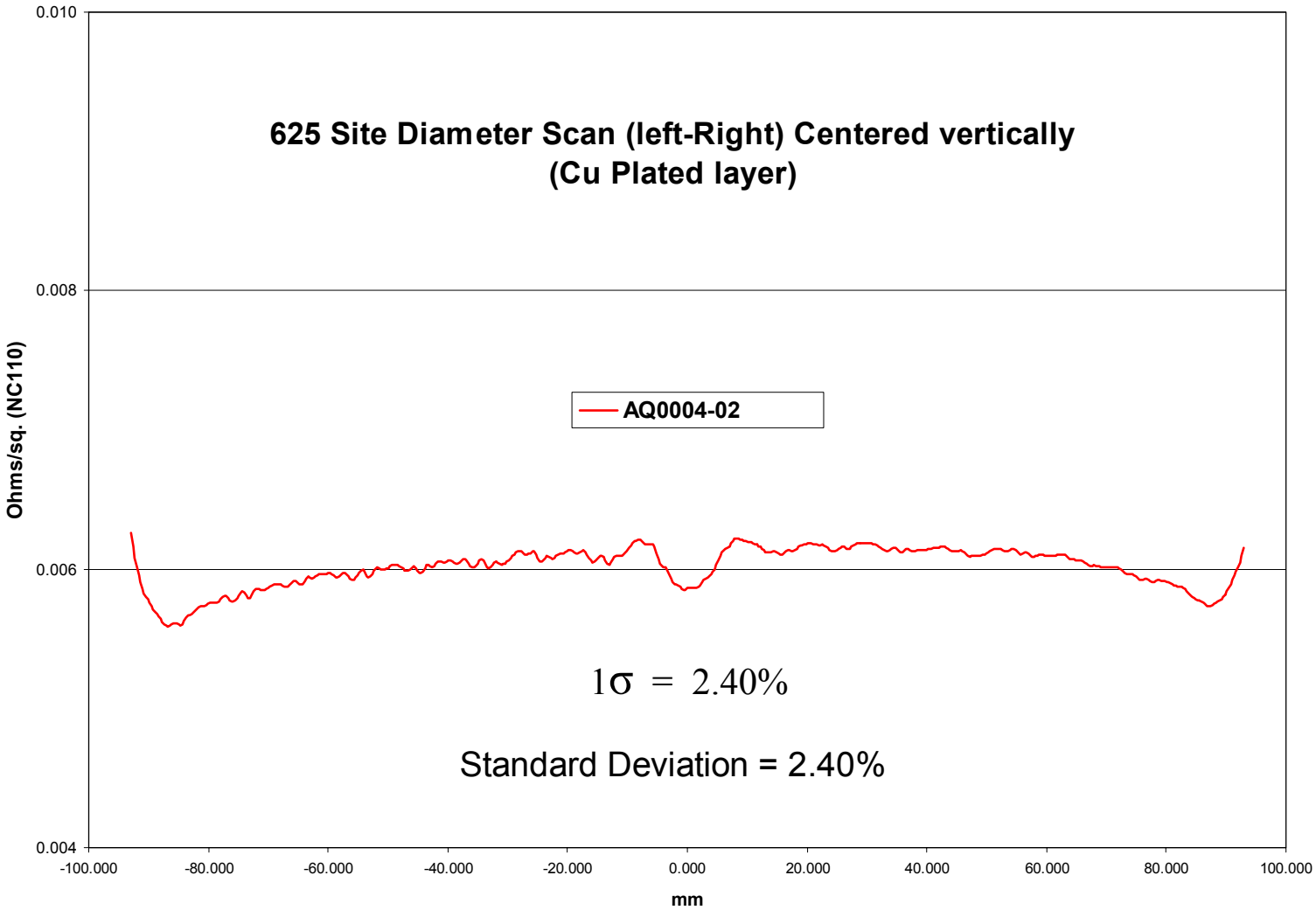


Anodes/Jets Assembly. U.S. Patent 5,421,987.

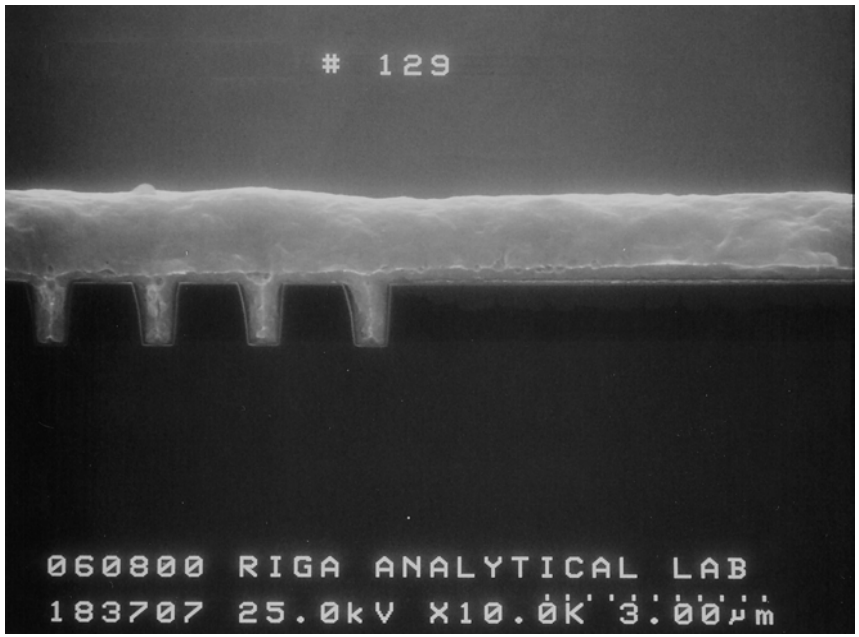
Diffusion Layer Distributions



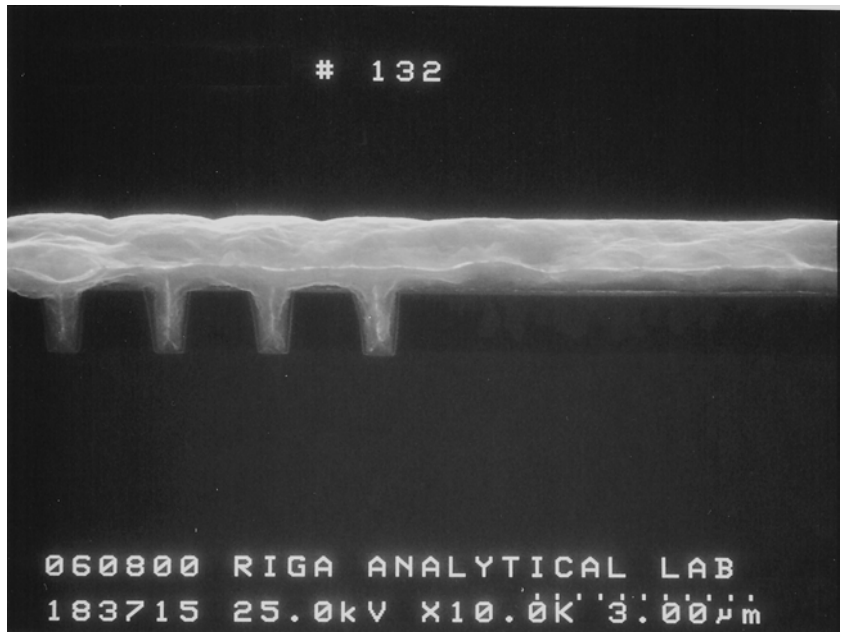
Wafer Uniformity



Transitions: Field to Trench Array



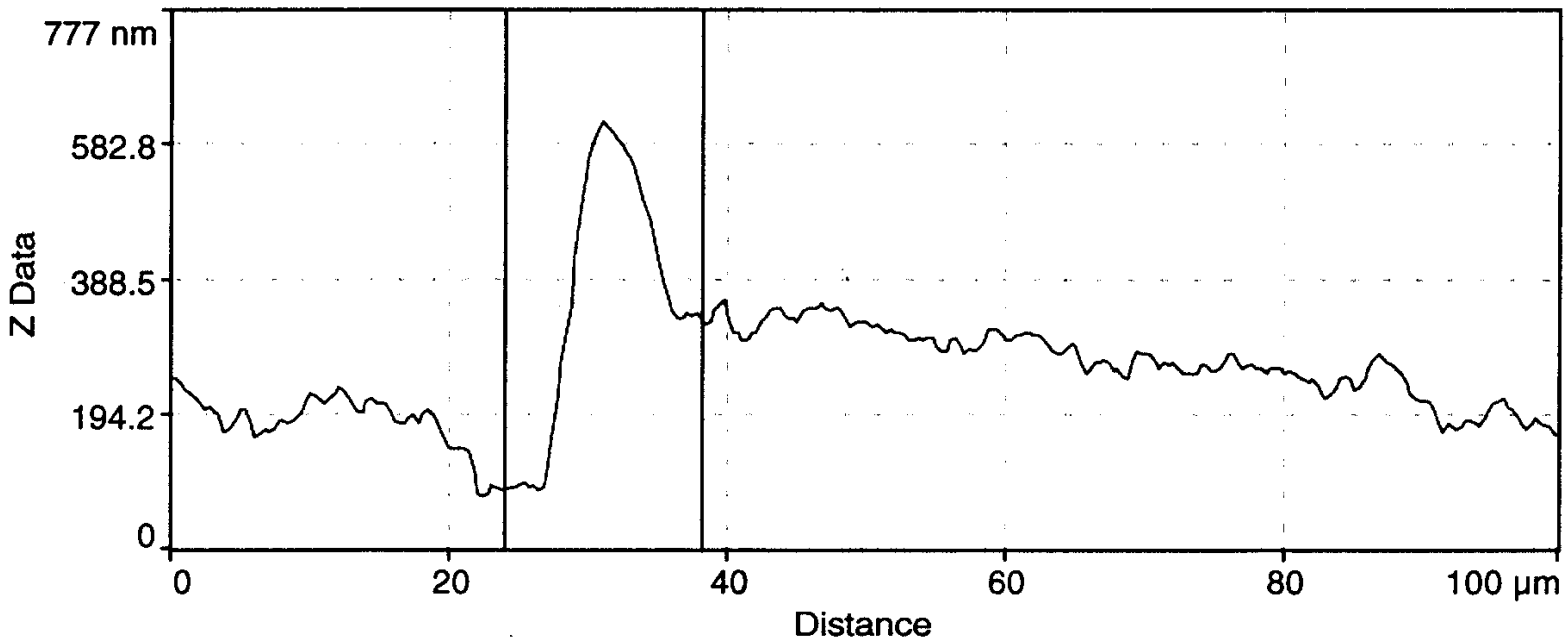
Plating Rate: 15 mA/cm^2 ~ 0.35 µm/min.



Plating Rate: 120 mA/cm^2 ~ 2.8 µm/min.

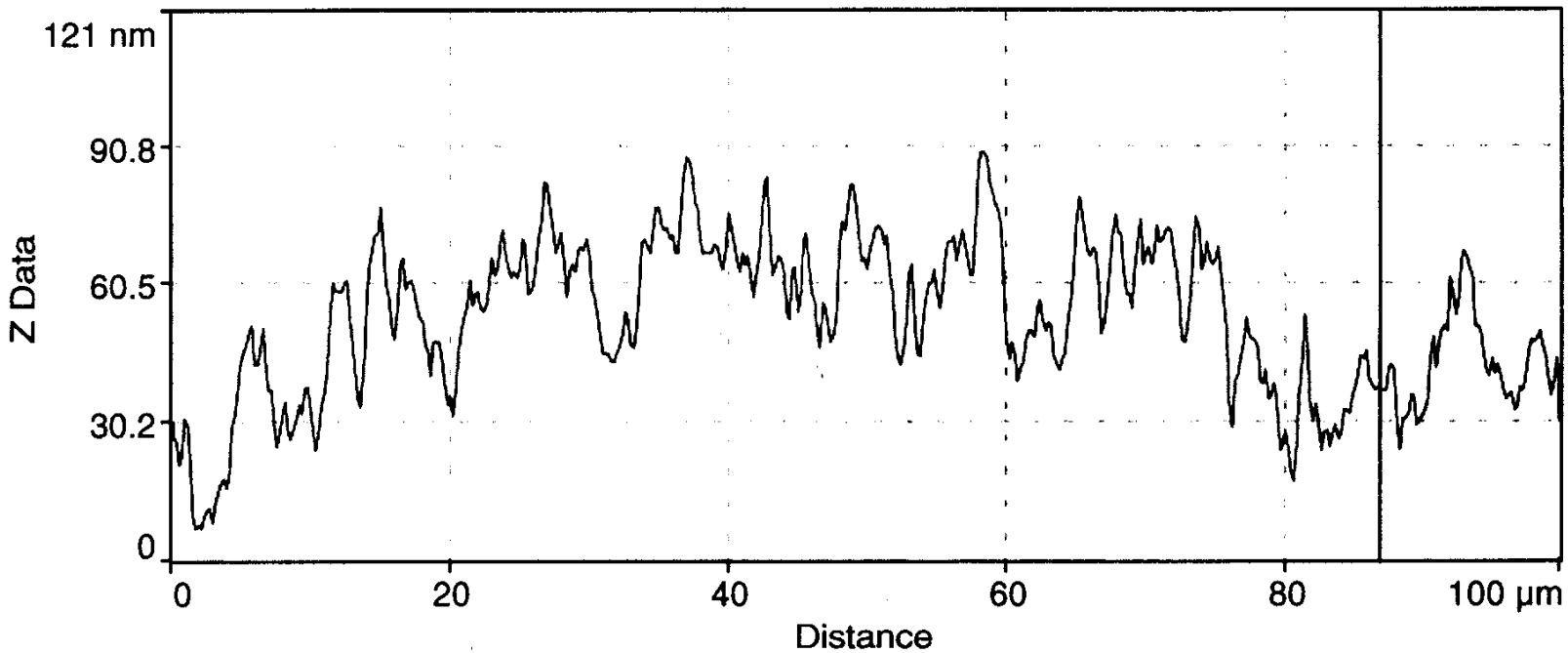
Profile Scan: Field to 0.35/0.35µm

Leading Vendor's Tool

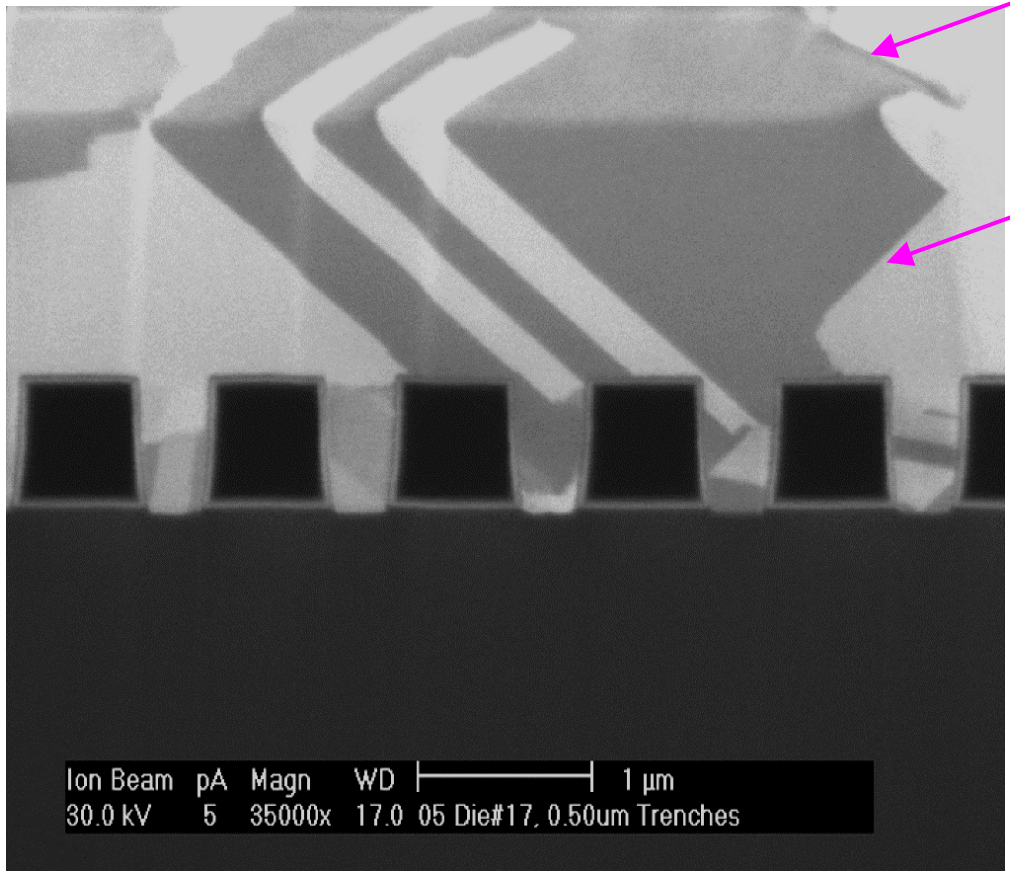


Profile Scan: Field to 0.35/0.35µm

JECD Tool

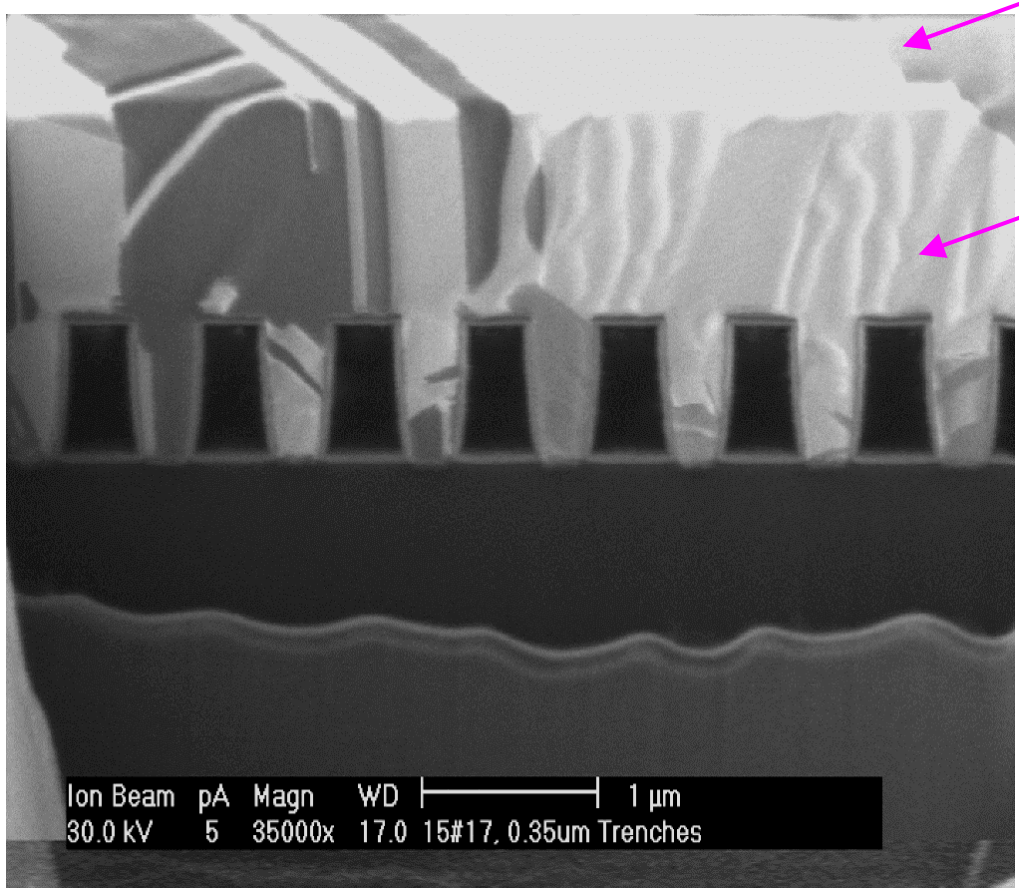


FIB Cross-Section



Courtesy of Accurel, Inc.

FIB Cross-Section



Courtesy of Accurel, Inc.

AFM Surface Roughness, 120 mA/cm²

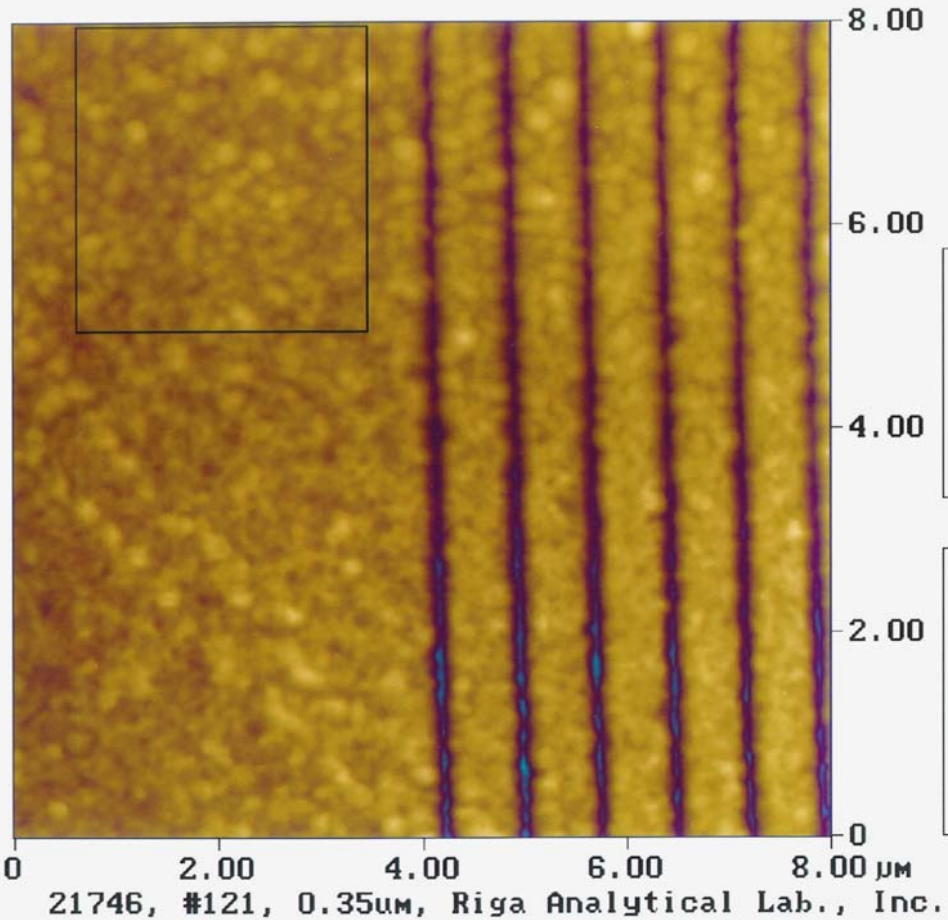


Image Statistics

Z range	192.34 nm
Mean	0.235 nm
Rms (Rq)	22.425 nm
Mean roughness (Ra)	15.869 nm
Max height (Rmax)	192.08 nm
Surface area	

Box Statistics

Z range	70.825 nm
Mean	1.782 nm
Rms (Rq)	9.609 nm
Mean roughness (Ra)	7.286 nm
Max height (Rmax)	70.067 nm
Box x dimension	2.875 µm
Box y dimension	3.031 µm

AFM Surface Roughness, 15 mA/cm²

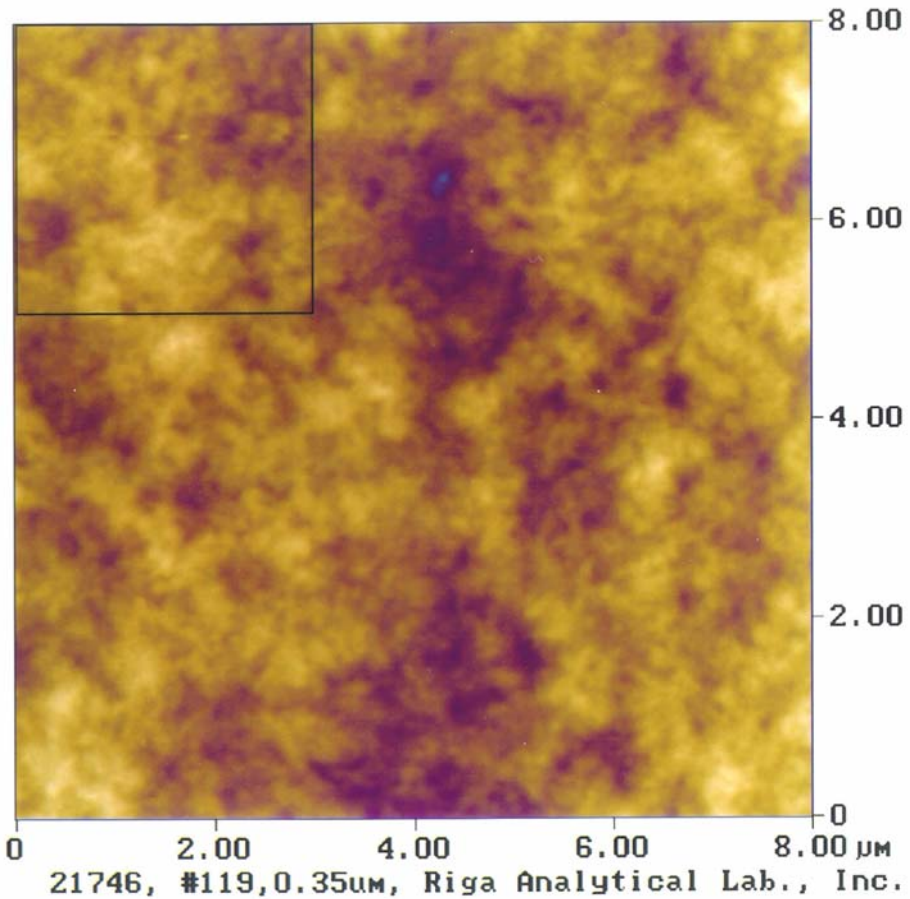


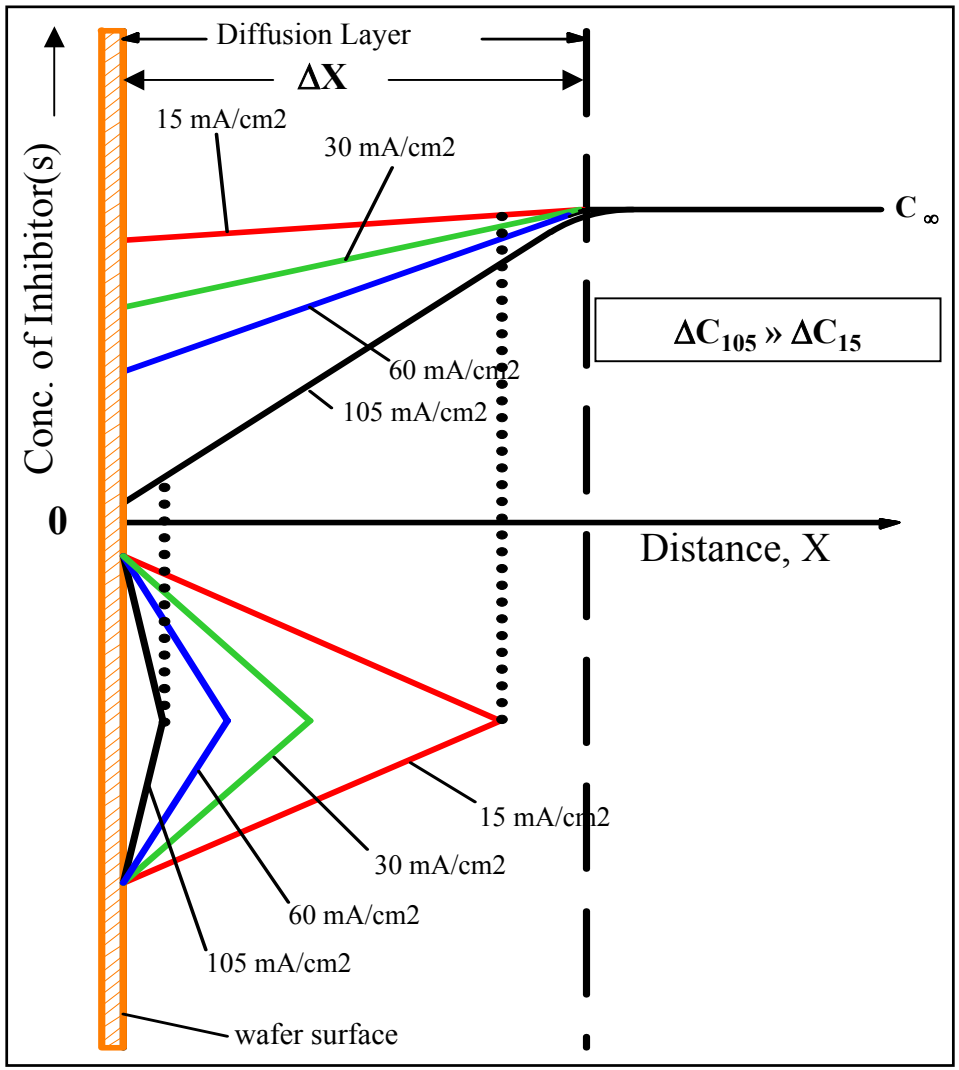
Image Statistics

Z range	136.61 nм
Mean	-0.0002 nм
Rms (Rq)	17.746 nм
Mean roughness (Ra)	14.212 nм
Max height (Rmax)	136.56 nм
Surface area	

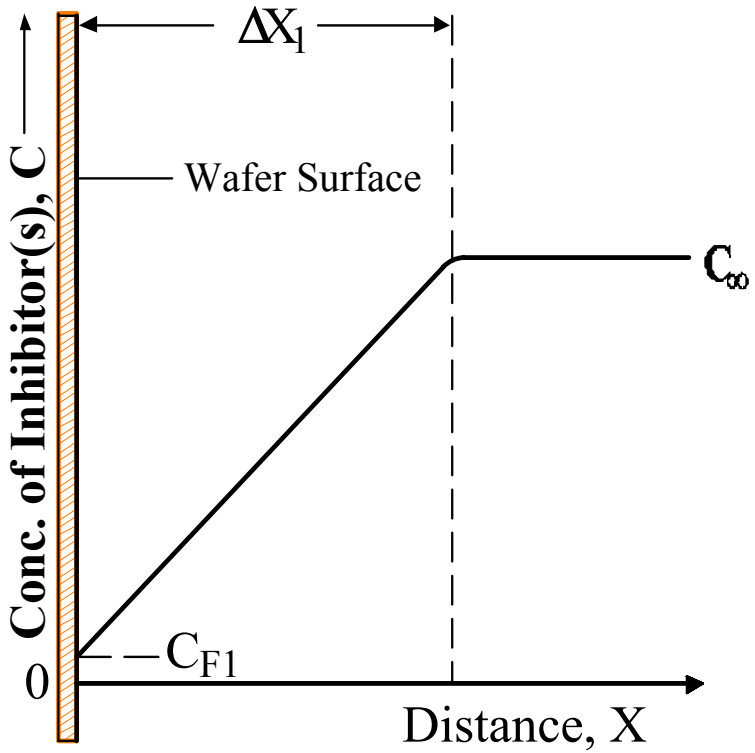
Box Statistics

Z range	86.594 nм
Mean	4.215 nм
Rms (Rq)	15.254 nм
Mean roughness (Ra)	11.237 nм
Max height (Rmax)	93.342 nм
Box x dimension	3.000 µм
Box y dimension	2.938 µм

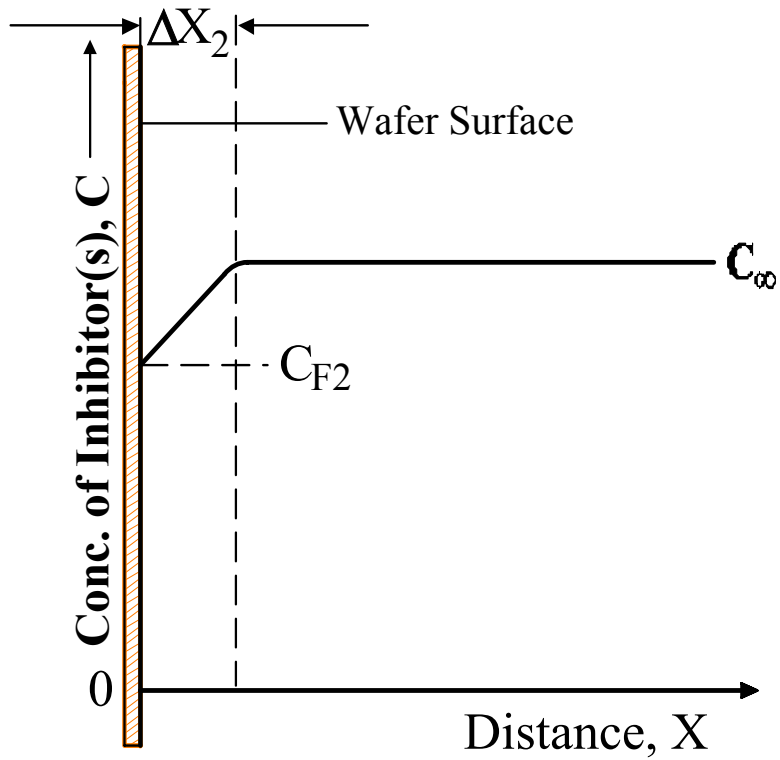
Model of Inhibition Leveling



JECD Enhanced Superfill Model



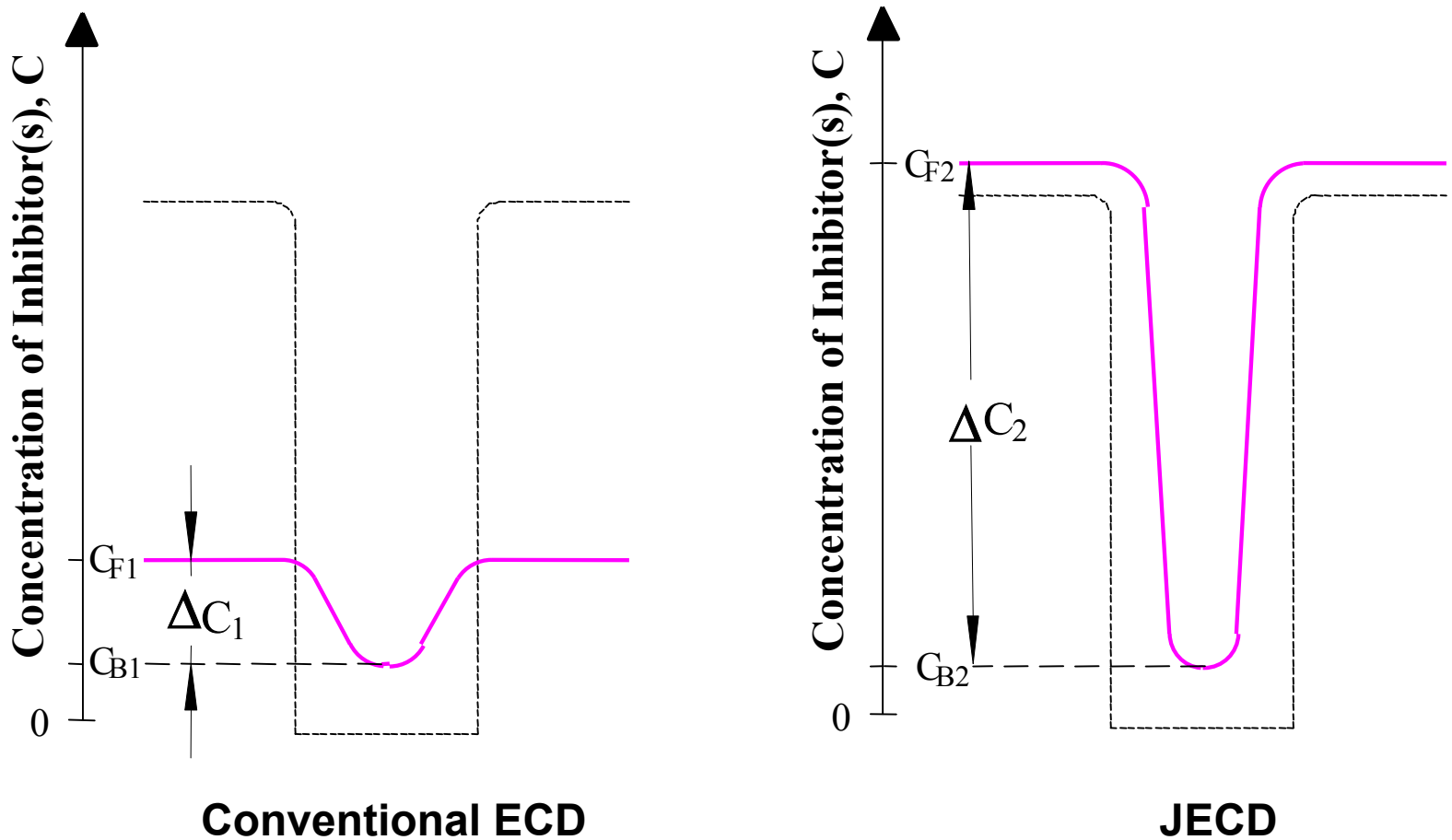
Conventional ECD



JECD

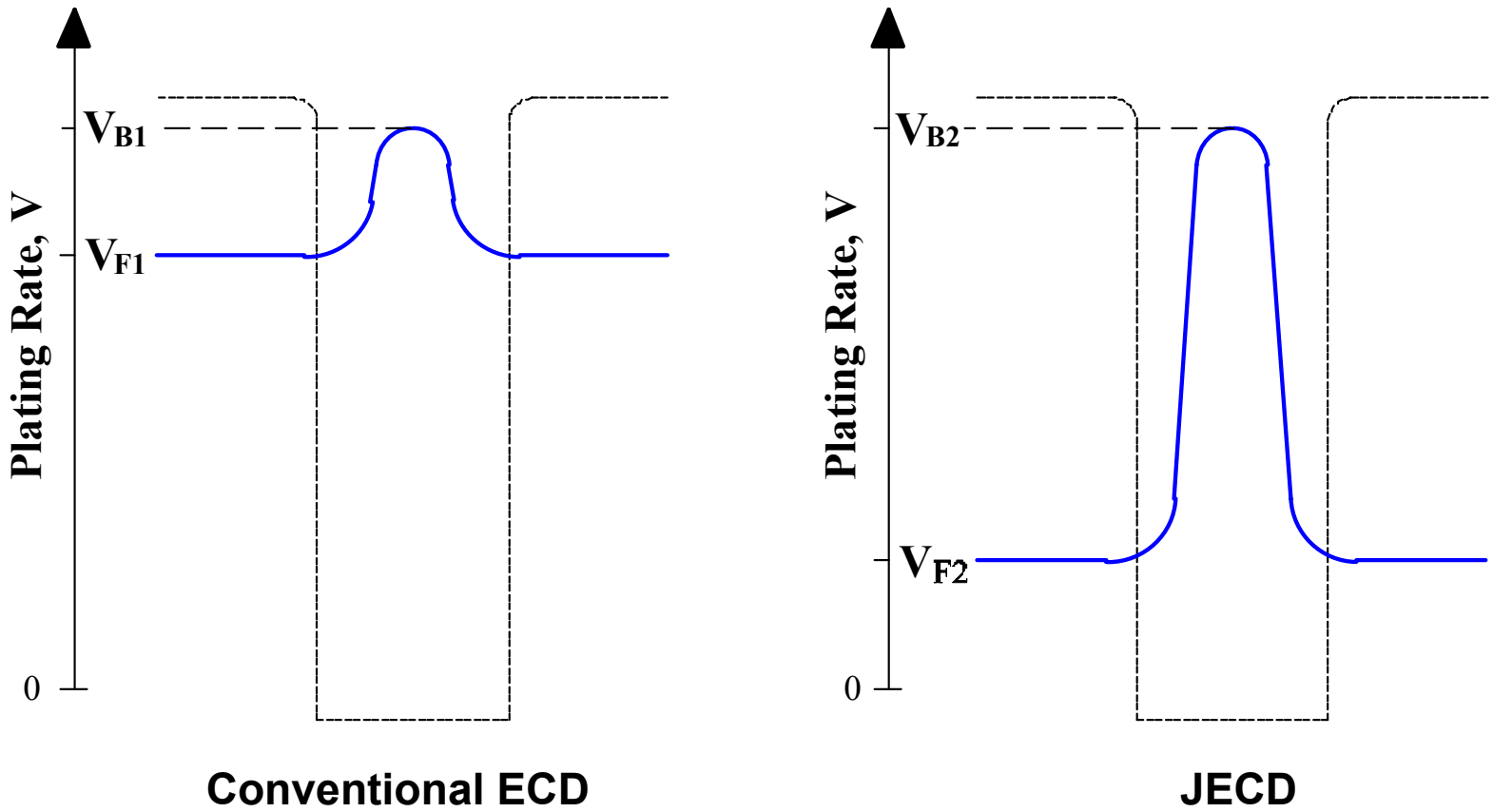
$$\Delta X_1 \gg \Delta X_2$$

JECD Enhanced Superfill Model



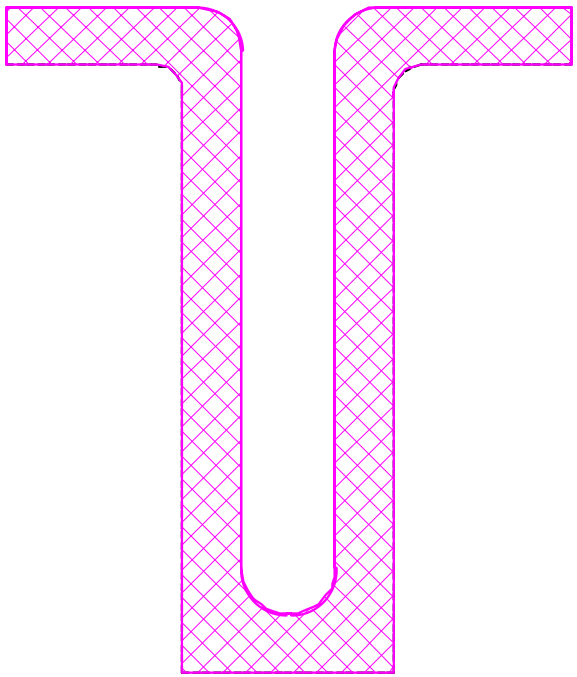
$$\Delta C_2 \gg \Delta C_1$$

JECD Enhanced Superfill Model

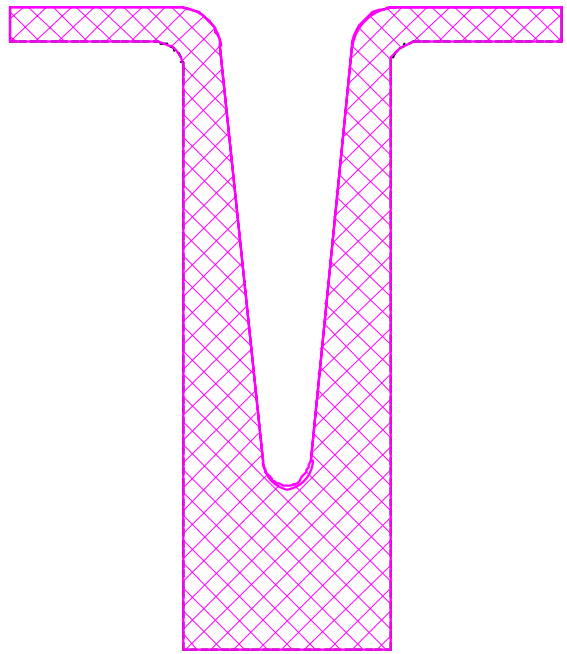


$$V_{B1} / V_{F1} ; \quad V_{B2} » V_{F2}$$

JECD Enhanced Superfill Profile



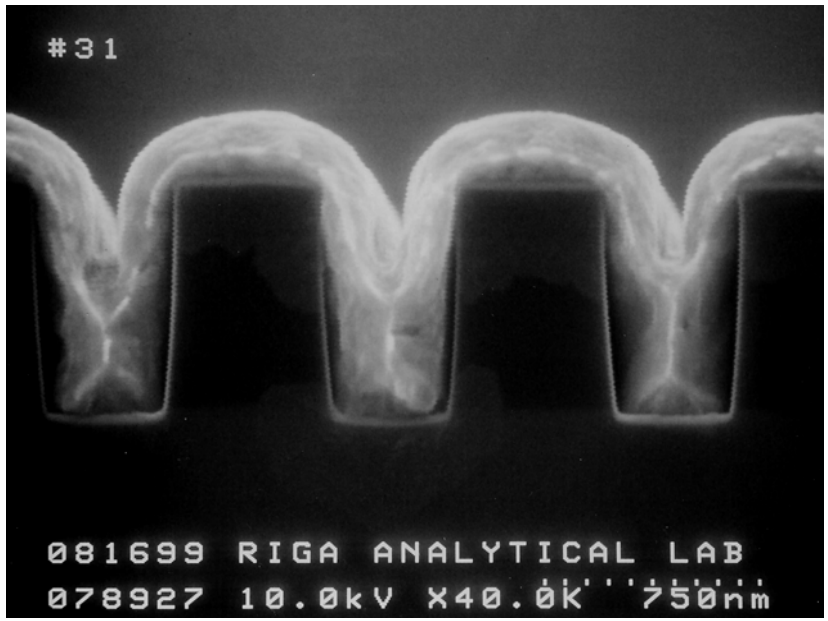
Conventional ECD



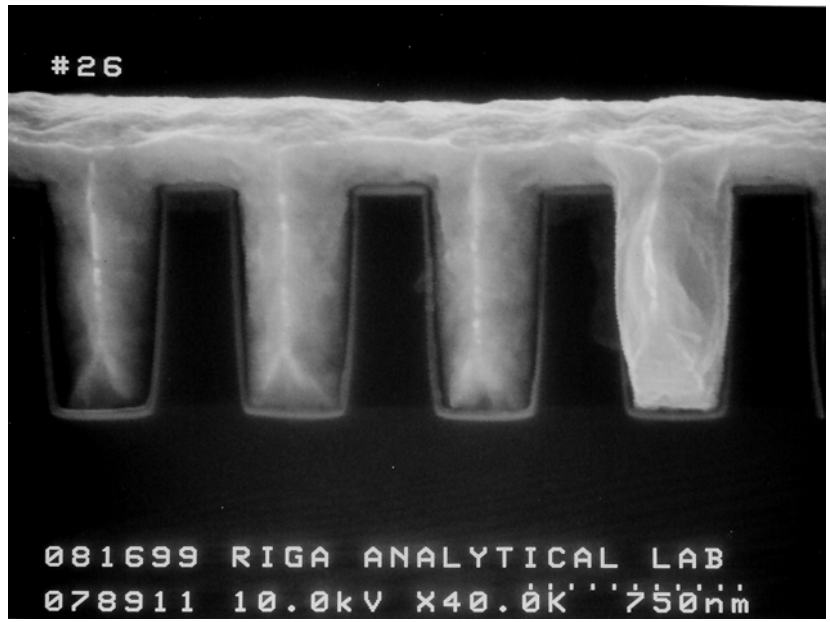
JECD

Superfilled Trenches

(a)

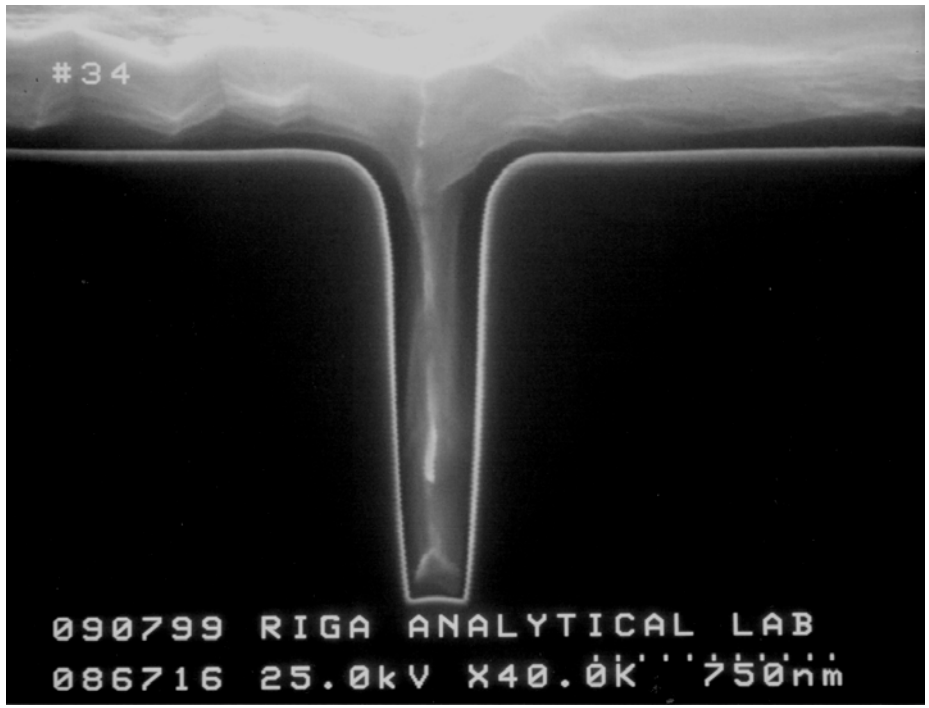


(b)



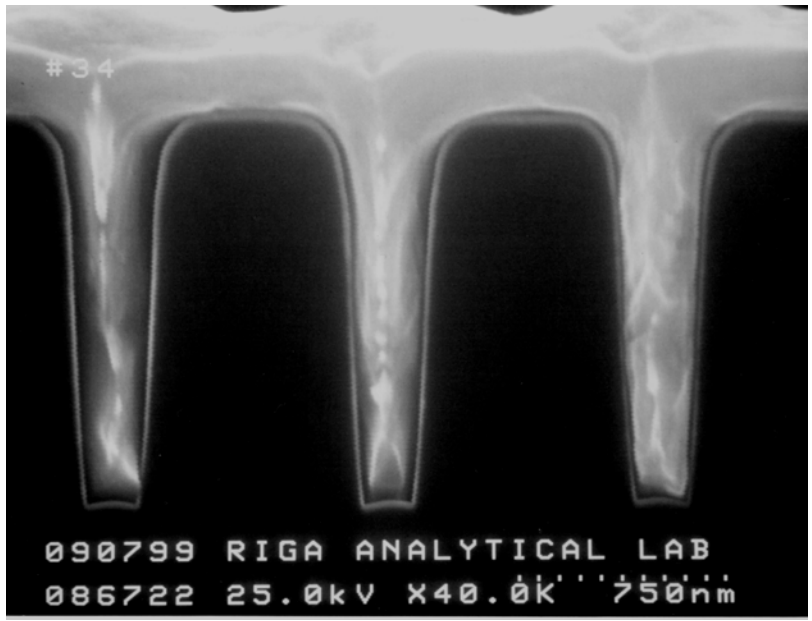
Cleaved samples plated at 120 mA/cm^2 (~2.8 µm/min), showing superfilled trenches after: (a) partial filling, and (b) complete filling.

Jets-ECD Isolated Trenches

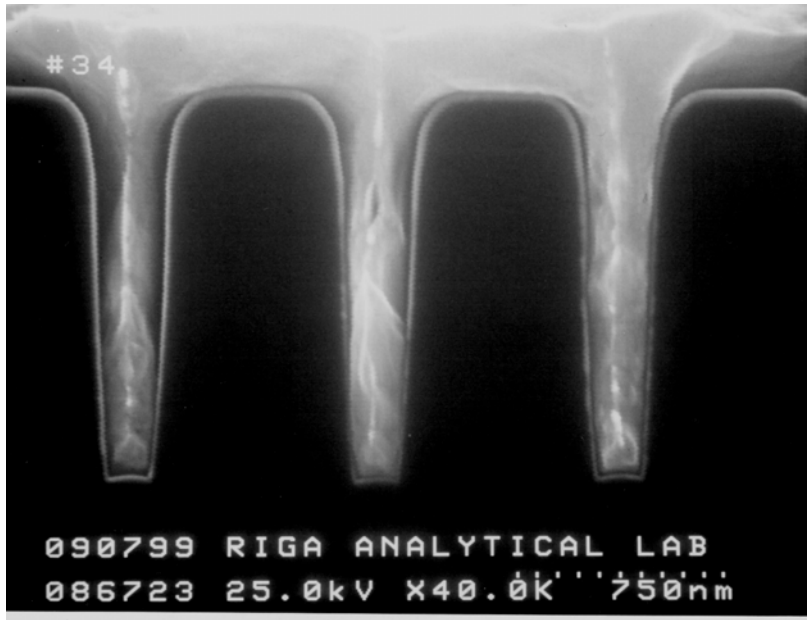


0.175µm wide (bottom); 1.4µm deep; AR = 8.0:1

Jets-ECD Dense Trenches

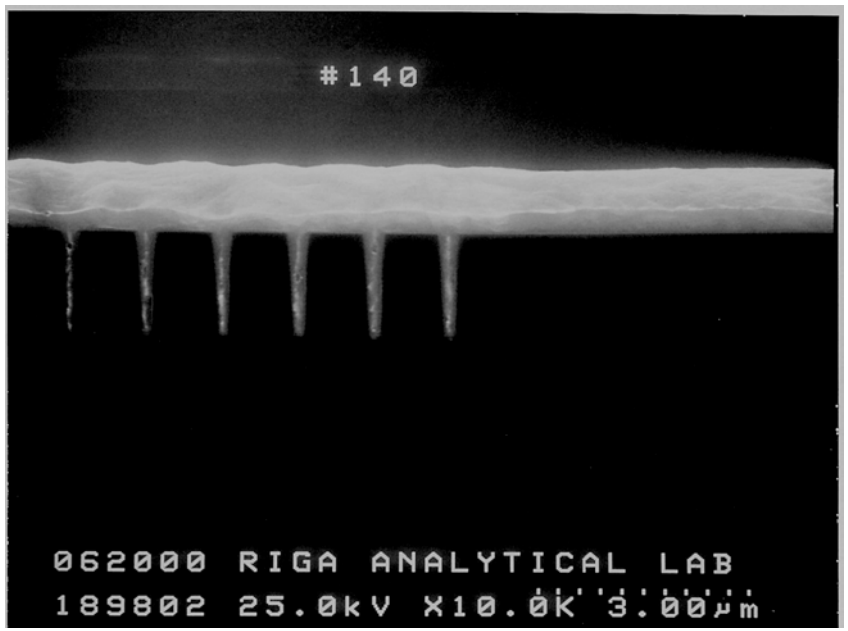


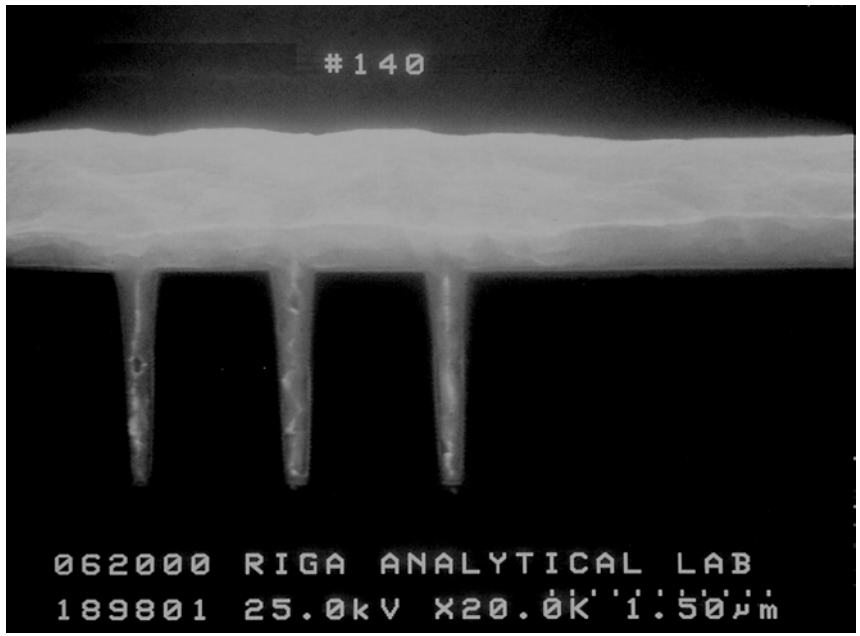
0.19µm wide (bottom); 1.4µm deep;
AR = 7.37:1



0.16µm wide (bottom); 1.4µm deep;
AR = 8.75:1

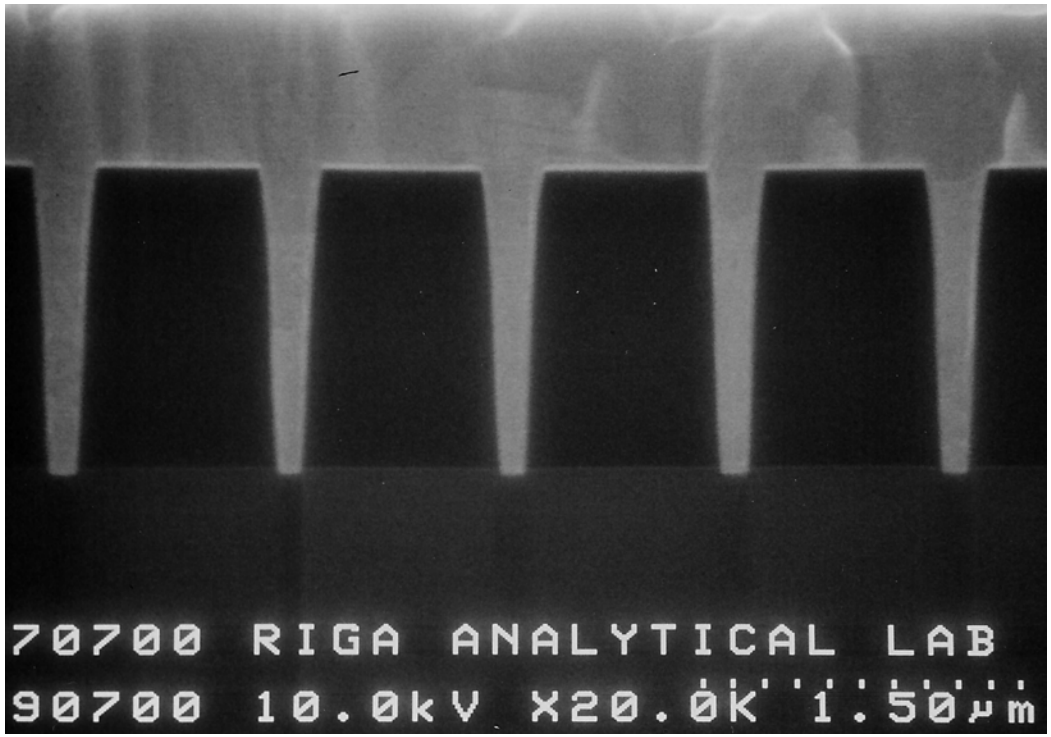
Jets-ECD Dense Trenches





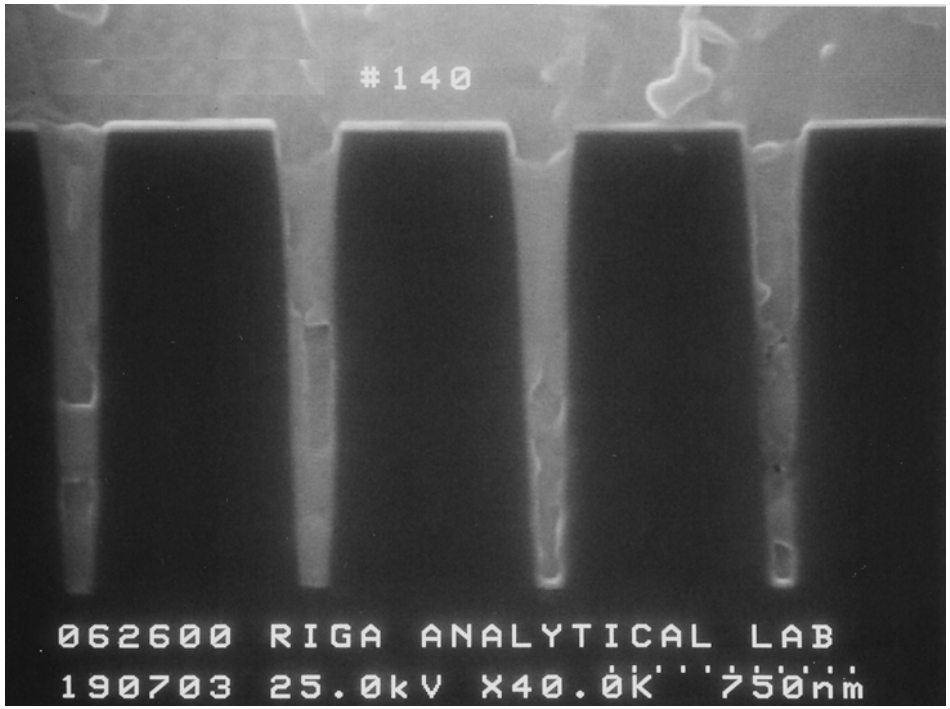
Transition: Field to trench array. Trenches: ~0.125µm wide (bottom); ~1.41µm deep; AR ~ 11.3:1.

Jets-ECD Dense Trenches



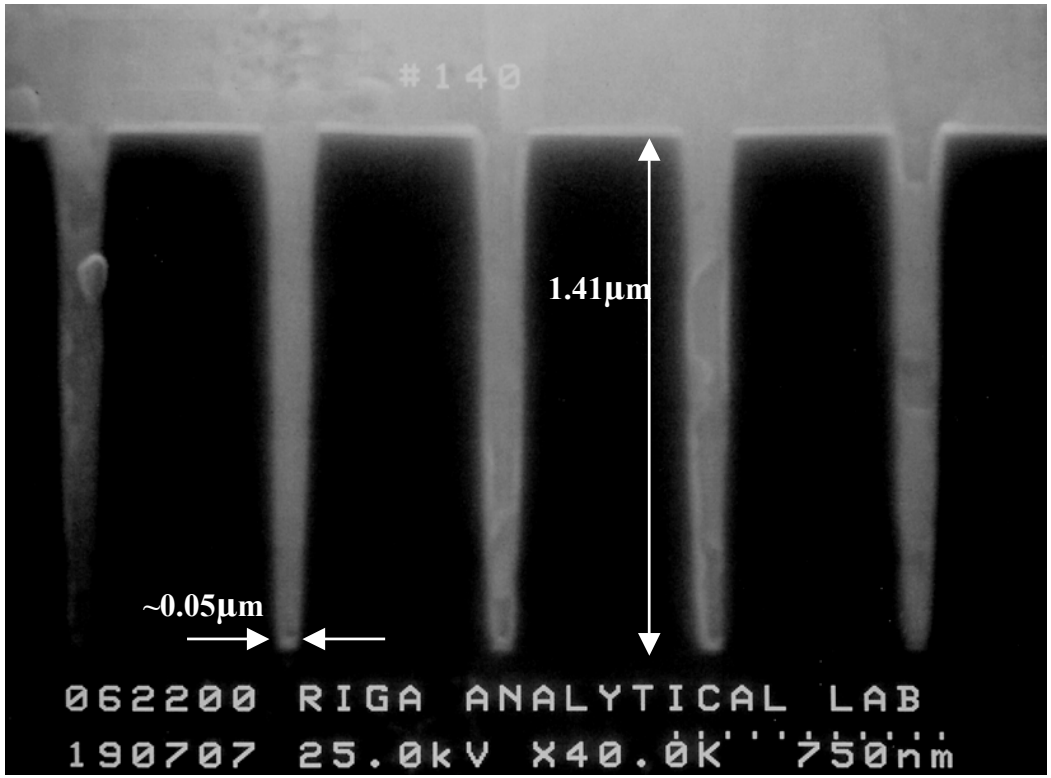
FIB cross section. Filled trenches: ~0.10µm wide (bottom); ~1.41µm deep; AR ~ 14:1

Jets-ECD Dense Trenches



Etched cross-section. Trenches: ~ 0.07µm wide (bottom); ~1.41µm deep; AR ~ 20:1.

Jets-ECD Dense Trenches



Lightly etched cross-section. Trenches: ~ 0.05µm wide (bottom); ~ 1.41µm deep; AR ~ 28:1.

JECD Summary

Demonstrated:

- **Jets-ECD (JECD) filling of openings down to ~ 0.05µm, with AR ~ 28:1**
- **JECD plating rate of up to 2.8 µm/min (8X faster than others), with smooth bright deposits; no spikes, bumps, or humps, using 2 additive system (others use a third "leveler" additive component)**
- **Smooth anodic dissolution, without particle generation**
- **Very wide JECD process latitude (>100% of additives, and >400% of current density)**
- **One Issued Patent and two Pending Applications**

Problems with Cu Seed Layers

ELECTRONIC ENGINEERING

EE TIMES

Issue 1233 www.eet.com The industry newspaper for engineers and technical management Monday August 26, 2002

Telcos' future: automation up, staffing down

By Craig Matsumoto

SAN JOSE, CALIF. – Telecom carriers must make severe changes–wholesale job cuts among them–for optical networking to fulfill its promise, speakers told the Opticon conference last week.

'The telecom vendors are just now learning how to live in a cyclical industry.'

A traditional, labor-intensive network is too expensive to maintain, these speakers insisted, so carriers must instead go to an automated, point-and-click operation.

Staggering through telecom's first down cycle after decades of steady if unspectacular growth, optical networking executives and engineers gathered here to assess the state of their battered industry. Understandably, the plunge was compared to the chip world's rhythmic ups and downs.

Via failures plague copper interconnect at 130 nm, forcing changes in design practice

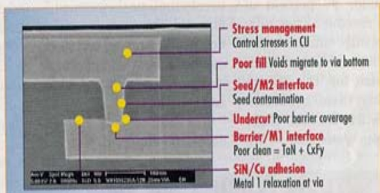
Next-gen processes stare into the void

By Ron Wilson

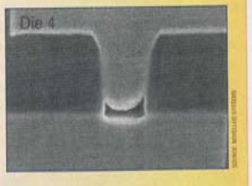
SAN MATEO, CALIF. – Yield and reliability issues threaten the touted dual-damascene copper interconnect structures of leading 130-nanometer processes, having caused both poor yields at wafer sort and unacceptable failure rates over the life of apparently good chips, according to a wide range of industry sources.

Some of the mechanisms leading to those problems can be controlled by an unprecedented level of attention to processing steps, and leading foundries have demonstrated such devotion to detail in recent months. But other problems are inherent in the structure of the new interconnect stacks and can be addressed only by design rule changes and by changes in design practice, some reaching clear back to the architectural levels of design.

Thus, what first appeared in mid-2001 to be a detailed process issue has become an architectural consideration for chip connect stack. The failures are specific to dual-damascene copper metal stacks, and the issues involved appear to affect all current processes, though foundry response to the problems has reportedly varied by vendor.



A slew of detailed process problems can lead to via failures.



Vias can pull away from the metal layer.

Early in the progress of 130-nm production, it was observed that some vias–even though they appeared to be correctly imaged and formed–were not connected or presented such a high resistance that they had a major electrical impact on the circuit. Later, it was discovered that those effects could appear during ac-

engineers–infant mortality.

"In some cases we were still seeing new failures after 300 hours of stress testing," reported one insider at a fabless vendor.

It was necessary to identify the failure modes and correct the problem before declaring 130-nm processes fully production-ready. Yet the lack of surface defects–the usual cause of circuit failures in ICs–or of visible surface abnormalities concerned process integration engineers.

The problem turned out to be a confluence of several failure mechanisms, according to Bob Havemann, vice president of technology, process integration and applications at Novellus Systems Inc. (San Jose, Calif.). "It's ironic that copper was ballyhooed for its superior reliability in IC interconnect," Havemann observed. "It can in fact be highly reliable, and it's not as subject to some of aluminum's problems,

➤CONTINUED ON PAGE 98

Andiamo bid may rev iSCSI rollout, force Fibre Channel shakeout

Reference [1]

Ideal Seed Layers (SL)

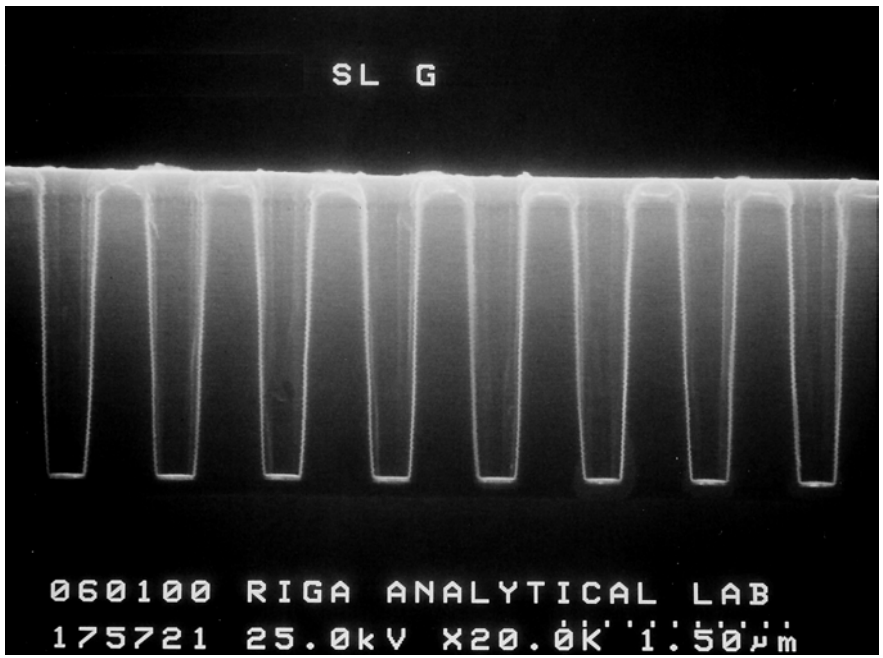
- Fully continuous sidewalls and bottom coverage of high-AR (HAR) openings with negative slopes, yet thin enough inside openings to avoid pinching-off or sealing the features
- Sufficient thickness on the field for adequate surface conduction (to minimize "Terminal Effect") for good plating uniformity
- Excellent adhesion to the barrier, without any poor-adhesion spots, such as on negative slopes
- Consistent, robust, and highly reliable process
- High throughput deposition equipment

Combined Conformal and Non-Conformal Cu Seed Layers[2-7]

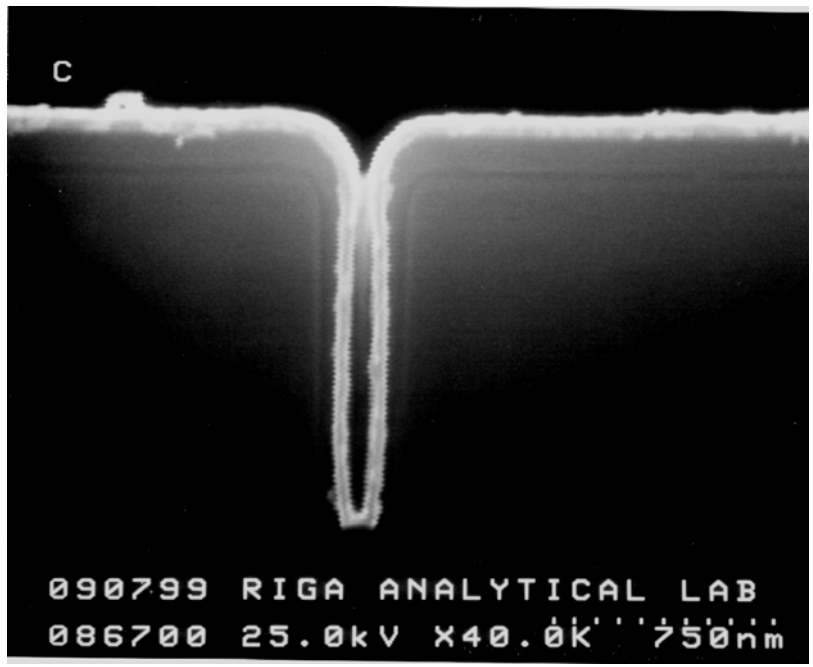
- Independent sidewalls and field coverages
- Fully continuous, thin uniform coverage of bottom and sidewalls (including negative slopes)
- Adequate field thickness for void-free filling and plating uniformity
- Excellent adhesion to barrier
- Robust and consistent process with high yields and reliability
- High deposition throughput: ~70 WPH

Conventional Seed Layers

(a)



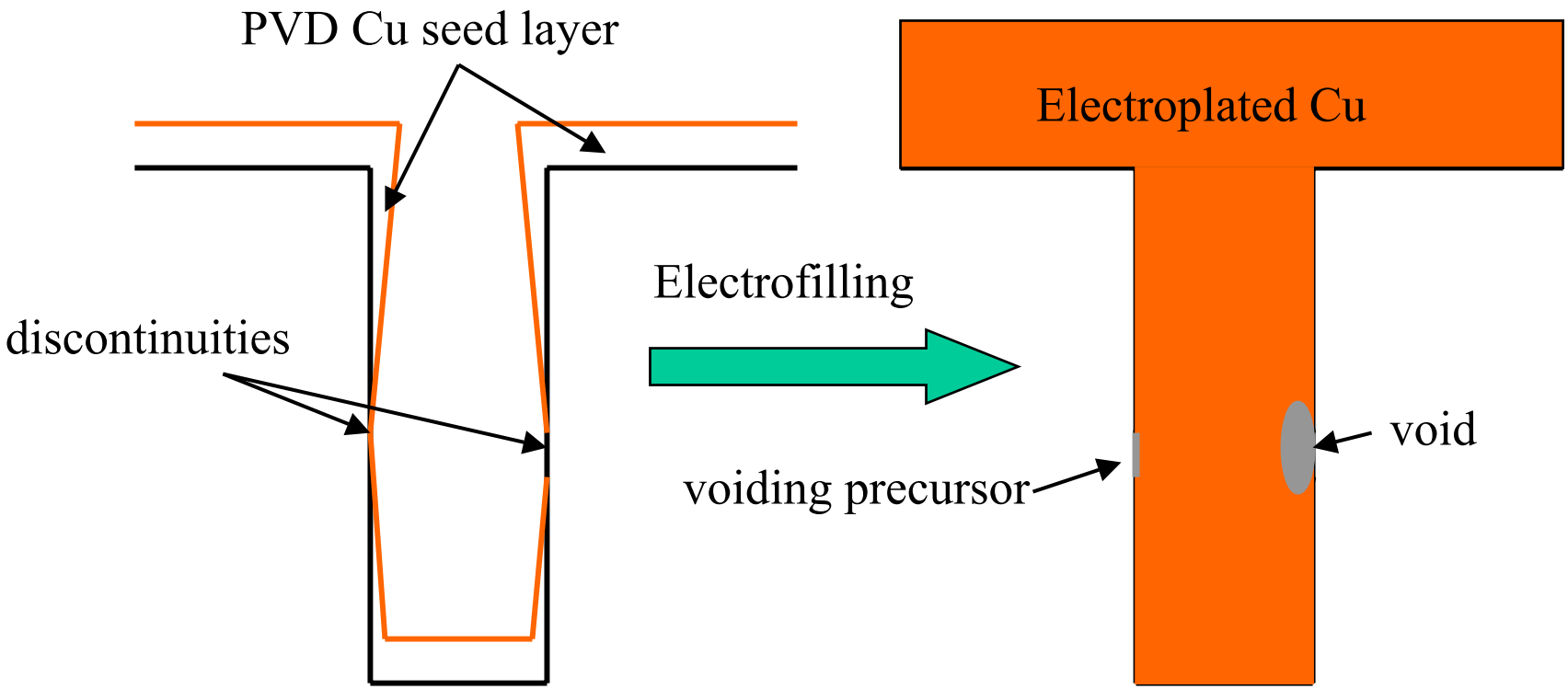
(b)



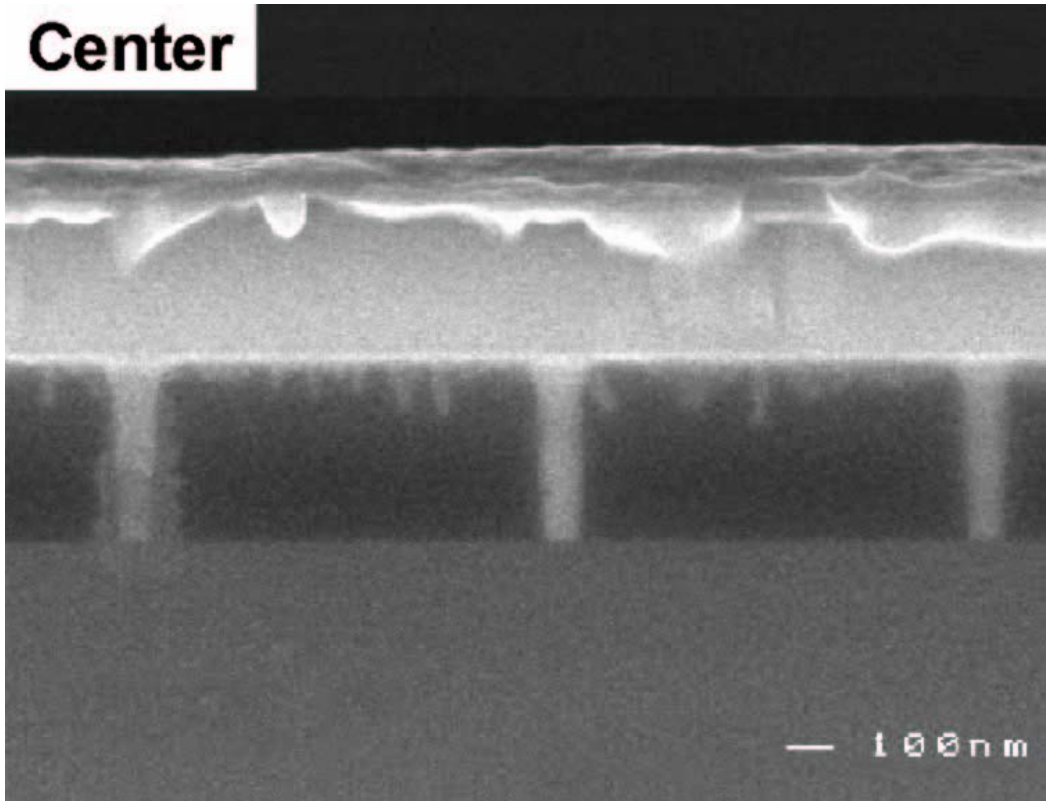
Conventional Cu seed layers. (a) PVD seed layer; combined (Cu plus barrier): ~2,000Å on field and . 100Å on lower sidewalls; vias: ~0.25µm wide; 1.90µm deep; AR ~ 7.6:1. (b) CVD seed layer; combined (Cu plus barrier): ~450Å on field and sidewalls; trenches: ~0.13µm wide; 1.4µm deep; AR ~ 10.8:1

Problems with a Non-Conformal PVD Seed Layer

High Aspect Ratio (HAR) Opening



Entrapped Electrolyte In Voids



Gap-Filled Results: 0.10µm, 4.5:1 A/R vias; gap-filled demonstrated using 500Å thick PVD Cu seed – from Applied Materials' Website (Semicon 2003).

Problems with a Non-Conformal PVD Seed Layer

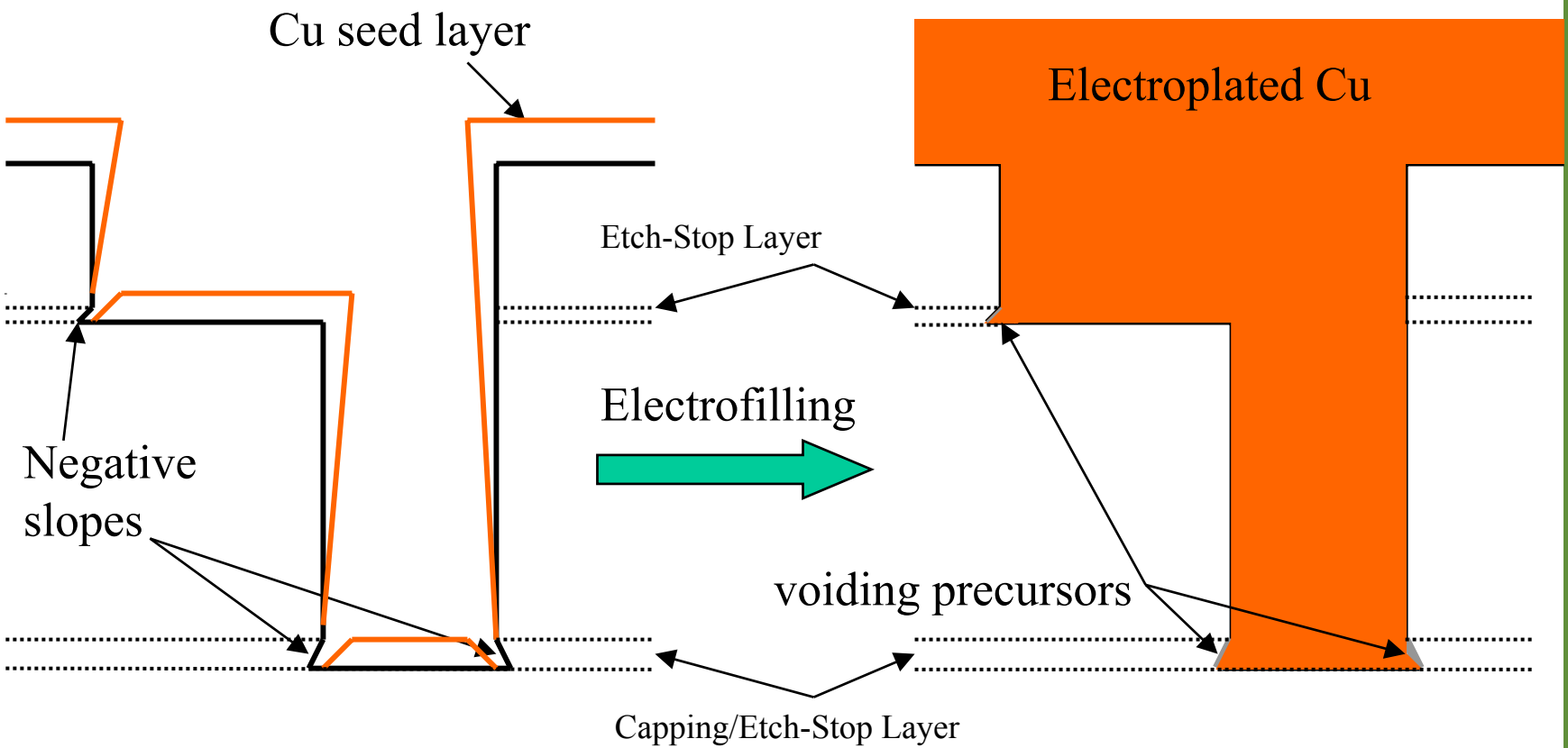
- PVD Cu S.L. → Low Reliability/Yields
  - Negative slope sidewalls in retrenching features and in undercut crevices, nooks, and recesses[8] (due to over-etched multiple dielectrics in Single and Dual Damascene features)
  - Non-Conformal PVD deposition results in inadequate sidewall (or step) coverage, leading to filling-voids and stress-induced voiding (SIV)[9-11]
  - Simultaneous exposure of barrier and Cu SL to electrolyte accelerates the SL corrosion. Interfacial stress at the SL/Barrier interface also accelerates SL corrosion. Cu SL corrosion leads to filling voids

Problems with a Non-Conformal PVD Seed Layer

- Preplating activation in the electrolyte is compromised or eliminated, leading to impaired adhesion. Also, initial plating current density must be high enough to suppress SL corrosion. This may result in "terminal effect" and impair superfilling capability
- Interfacial oxides and poor-adhesion of electroplated copper onto exposed barrier sites result in filling-voids and/or SIV-precursors
- Microvoids coalesce (under thermal and/or electrical stresses) to larger voids, resulting in vias void pulls[1]

Problems with a Non-Conformal PVD Seed Layer

Dual Damascene

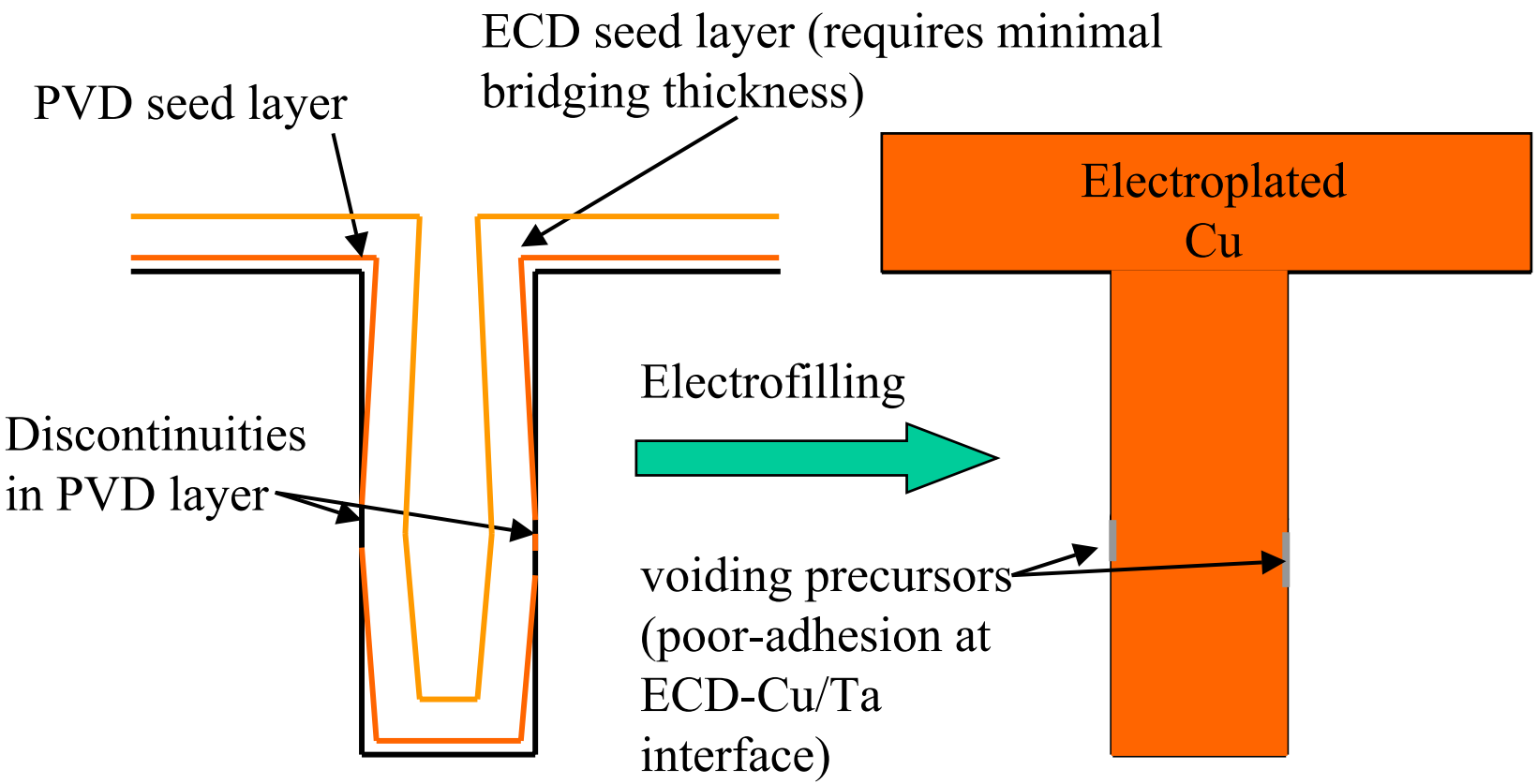


Problems with Other Seed Layers

- Conformal ALD, CVD, Electroless, and ECD Cu Seed Layers (on barrier)
  - Slow deposition results in low throughput
  - Too thick on sidewalls, yet too thin on field
  - Too thin SL on field: ⇨ "terminal effect" (> 100%), filling-voids, and contact-loss by mechanical wiping and/or bipolar seed dissolution[12]
  - Poor-adhesion of electroless and ECD Cu on barrier
  - Poor uniformity and rough deposits (except ALD)
  - High impurities and resistivity levels
  - Electroless and ECD require additional equipment

Problems with ECD & Electroless "Repair" Seed Layer

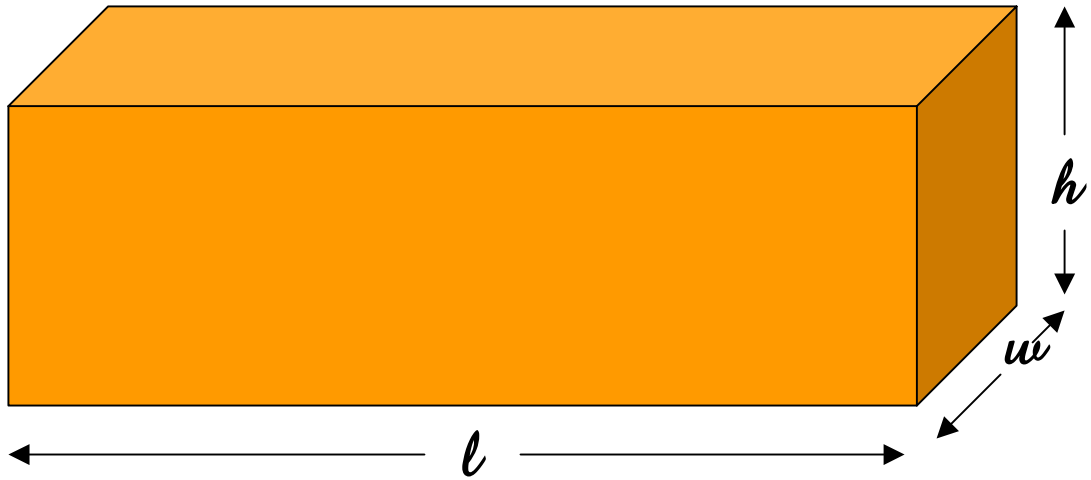
High Aspect Ratio (HAR) Opening



Problems with ECD & Electroless "Repair" Seed Layers

- Electroless or ECD "Repair" SL (on PVD)[13-17]
  - Electroless is extremely hard to control process: Erratic initiation time and deposition rate due to bath aging. Also, hydrogen blistering problems
  - Require minimum "bridging" of Cu on the sidewalls, thereby limited to certain size features
  - Too thick on sidewalls yet too thin on the field
  - Voiding-precursors at exposed barrier sites due to poor-adhesion between ECD or electroless Cu and Ta barrier
  - High level of impurities and resistivity of seed
  - Slow deposition results in low throughput
  - Require additional equipment

Surface/Volume Ratio Increases With Shrinking line hight



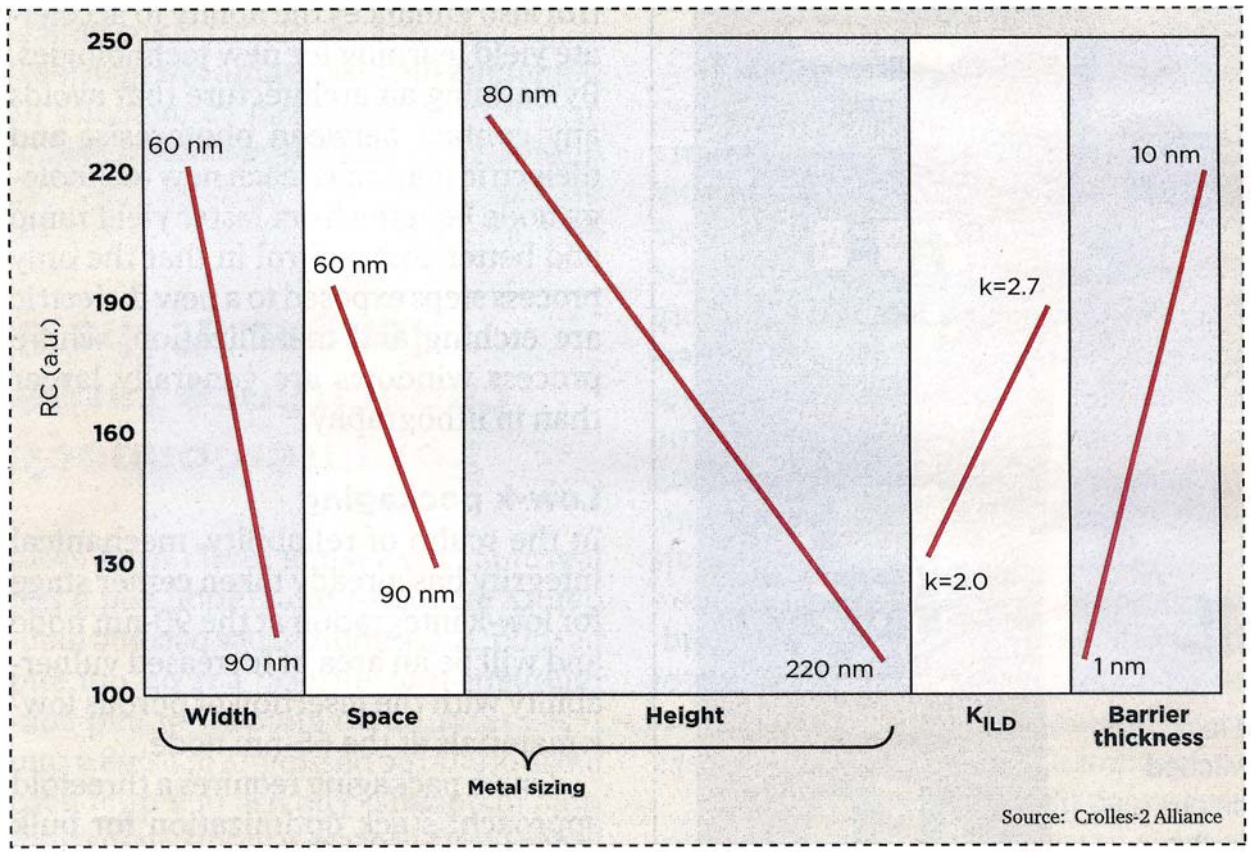
$R = A/V = 2(lw + lh + wh)/lwh \approx 2(w + h)/wh$

Assume: $h_1 = w$ $(AR = 1:1)$; ⇨ $R_1 \approx 4.0/w$

Assume: $h_2 = 4w$ $(AR = 4:1)$; ⇨ $R_2 \approx 2.5/w$

$R_1/R_2 \approx 4.0/2.5 = 1.60$ (60% higher!)

RC Reduction by Thicker Lines



A single parameter variation influences modeled interconnect RC performance. Metal sizing and barrier thickness have a paramount effect on RC due to the exponential increase in copper resistivity.

O. Hinsinger et al., "Trade tips for scaling interconnects", EE Times, June 21, 2004[20]

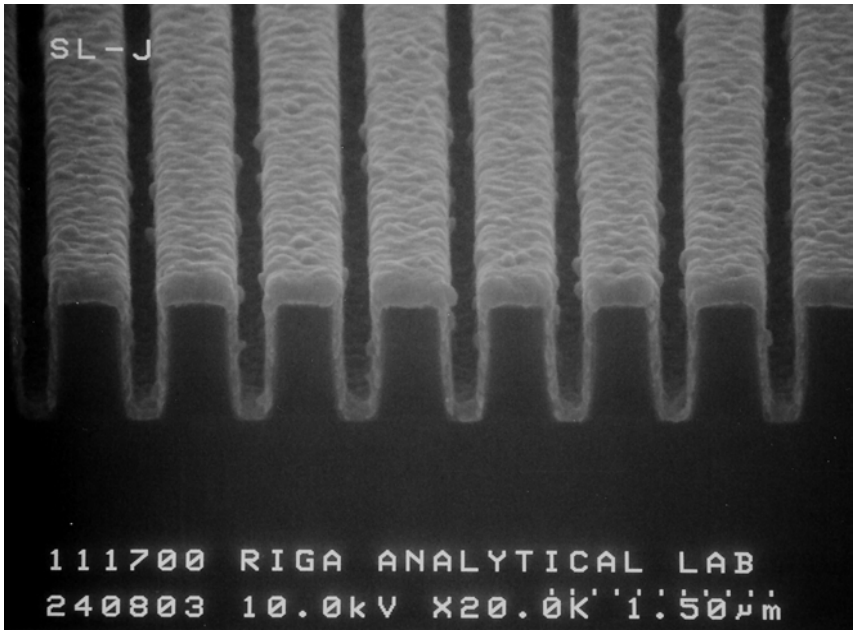
Low-AR Double-Whammy

- **Vias: Capacitance is inversely proportional to the dielectric thickness (d): C = kA/d**
  - » Low-AR shallow vias increase capacitive (noise) coupling between adjacent metallization levels!
- **Lines: Low-AR shallow trenches impair lines resistance: R = ρl/wh**
  - » For line width **w** < 0.10μm, line resistivity **ρ** increases exponentially due to *surface and grain boundaries scatterings* (longer aneals can reduce grain boundaries)
  - » RC delays increase with shrinking **w** and/or **h**
  - » Excessive power dissipation and heating ⇨ EM & SIV
  - » Signal/noise (integrity) degradation (due to IR-drop)
- **The only reason for not using high-AR (HAR) is inadequacy of non-conformal PVD seed on HAR**

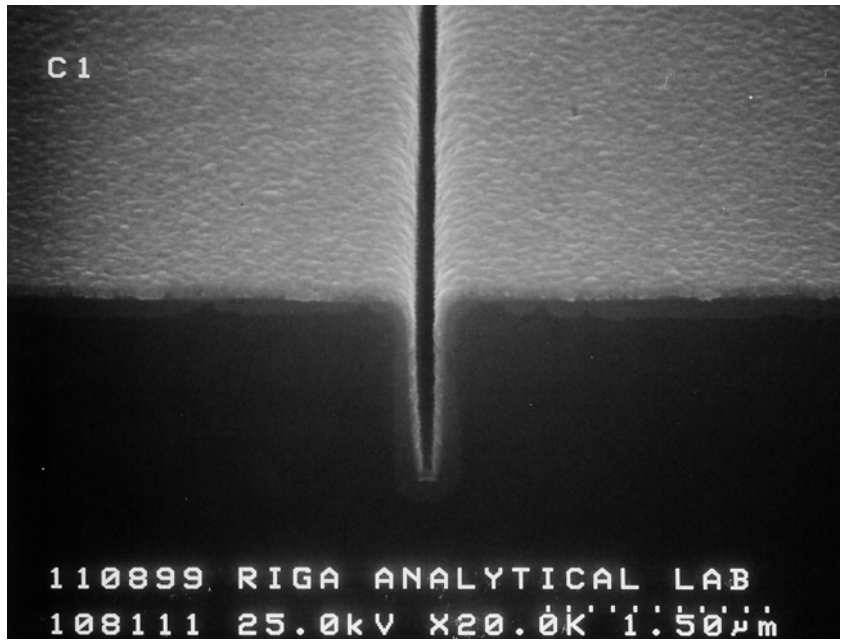
Combined Conformal and Non-Conformal Cu Seed Layers[2-7]

- Independent sidewalls and field coverages
- Fully continuous, thin uniform coverage of bottom and sidewalls (including negative slopes)
- Adequate field thickness for void-free filling and plating uniformity
- Excellent adhesion to barrier
- Robust and consistent process with high yields and reliability
- High deposition throughput: ~70 WPH

Multiple Seed Layers

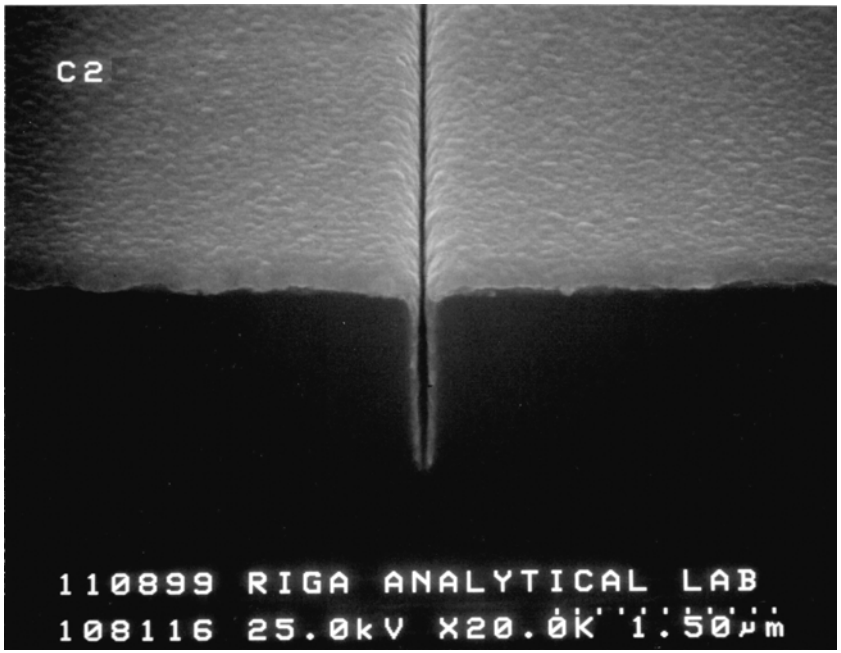


PVD/CVD seed layers: ~600Å (including barrier) on sidewalls and ~1,700Å on field. Trenches: ~0.23µm wide (bottom); 0.85µm deep; AR ~ 3.7:1; tilt =30°.

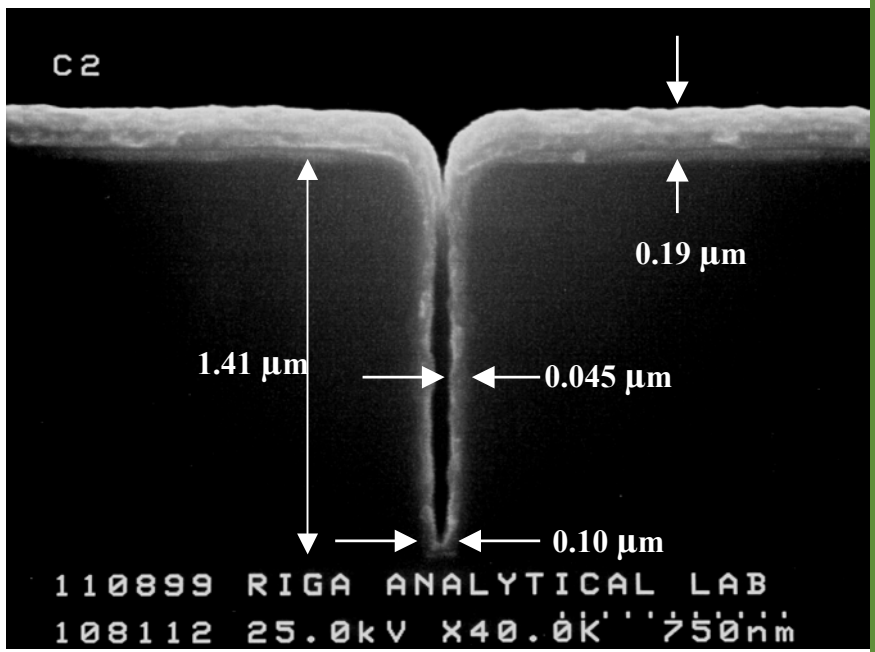


PVD/CVD seed layers: ~450Å (including barrier) on sidewalls and ~1,000Å on field. Trenches: ~0.13µm wide (bottom); 1.4µm deep; AR ~ 10.8:1; tilt =30°.

Multiple Seed Layers



(a)



(b)

PVD/CVD seed layers: ~450Å (including barrier) on sidewalls and ~1,900Å on field. Trenches: 0.10µm wide (bottom); 1.4µm deep; AR = 14:1.
(a) Mag. = 20,000X; Tilt = 30° and, (b) Mag. = 40,000X; No tilt.

Future Seed/Barrier Layers

- ALD/PVD TaN/Ta barrier begins to make inroads
- Excellent conformal bottom and sidewalls coverage for features # 0.10μm: by ALD (ALCVD) or CVD Cu
- Adequate field thickness by PVD Cu, essential for robust electrofilling and wafer uniformity
- Excellent adhesion to the barrier (PVD or ALD Cu)
- Robust process and high yields and reliability
- High deposition throughput (~70 WPH)
- PVD & ALD or PVD & CVD Cu Seed combinations already provide all of the above!

Seed Layers Summary

Demonstrated:

- **Non-Conformal/Conformal PVD/CVD Cu S.L. for openings # 0.10μm (AR / 14:1), barrier plus seed: ~45nm on sidewalls, and ~190nm on field, with excellent continuous bottom and step coverage**
- **Future: ALD & PVD or CVD & PVD combinations**
- **U. Cohen's IP[2]: Four issued Cu Seed Layers Patents and four Pending Patent Applications**

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