Driving the Communications Revolution

MRAM: A NEW TECHNOLOGY FOR THE FUTURE

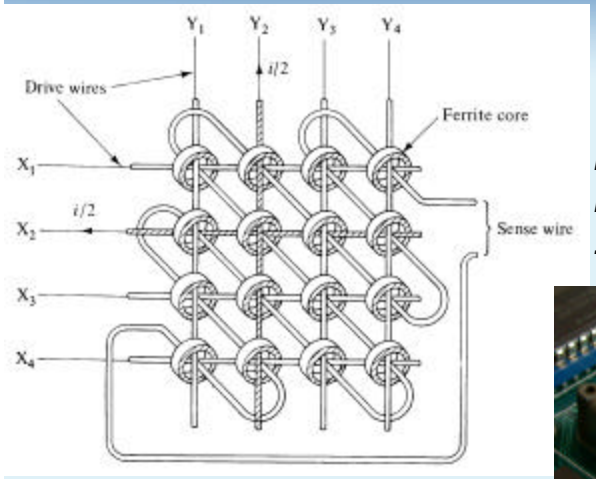
Kamel Ounadjela, Cypress Semiconductor

Future is Today

OUTLINE

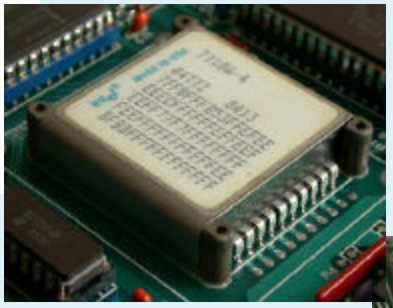
- WHY MRAM?
- ISSUES TO MAKE A WORKING MRAM
  - Read Yield Dependencies:
    - MTJs in MRAM
      - IMPORTANCE OF WITHIN-ARRAY MATCHING
      - CAN WE DO BETTER?
  - Write Yield Dependencies:
    - HOW TO INCREASE THE WRITE MARGIN
    - THEORY OF ZERO DEFECTS
      - ZERO NEEL COUPLING SWITCHING: IMPROVED LAYER MORPHOLOGY
      - ZERO POLES FROM PINNED LAYER: CRITICAL ETCH STEPS
  - Product Pulsing Sequencing
- SCALABILITY
- CONCLUSION

Magnetic Memory: Historical Perspective

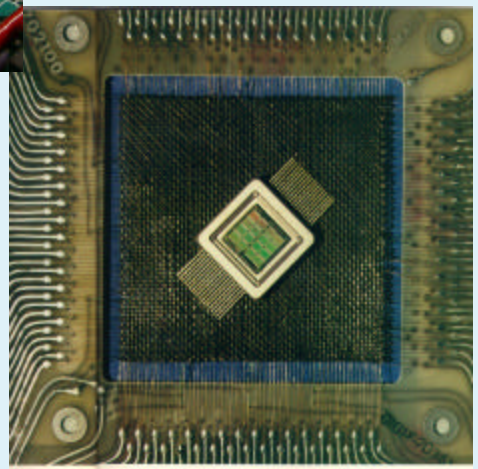


Control Data Corp.
1Kbits Ferrite Core Memory
1965

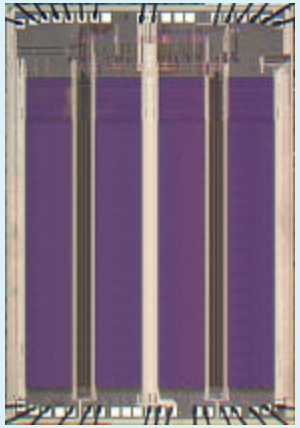
Intel 1 Mbits
Magnetic Bubble Memory
1980



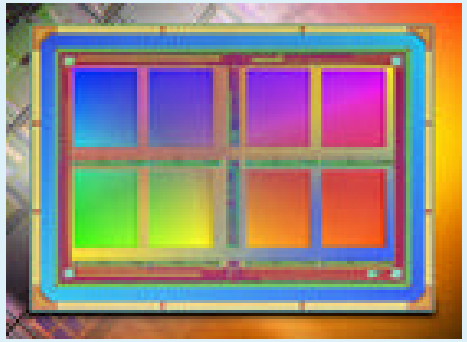
Honeywell
16Kbits MRAM Chip
AMR Technology 1994



CypressSemi, 256kb MRAM Chip,
MTJ, 4Mb, 2003



Motorola 4Mbits MRAM Chip,
MTJ, 4Mb, 2003



WHY MRAM?

- **MRAM Will Become A :**

  MAINSTREAM MEMORY TECHNOLOGY

- **High Performance NON VOLATILE Storage Element With FAST READ / WRITE And NO WEAR OUT Will Add Value To All Areas Of The Semiconductor Technology**

- **HOW DO WE KNOW:**
  - Check www.cnn.com about the 10 technologies to watch in 2004 in all areas ranging from medicine, house networking, energy, supply chain, computer memory, software, wireless broadband … MRAM is in there and is described as:
    - Magnetoresistive random acces memory is (in theory, anyway) more than 1,000 times faster than the fastest current nonvolatile flash memory and nearly 10 times faster than DRAM. "Nonvolatile" means it retains memory when the power is off. Add in its low power consumption, and it's perfect for use in an upcoming crop of computers and cell phones.

Emerging Memories

- **Industry's Quest - The Search for the PERFECT Memory:**

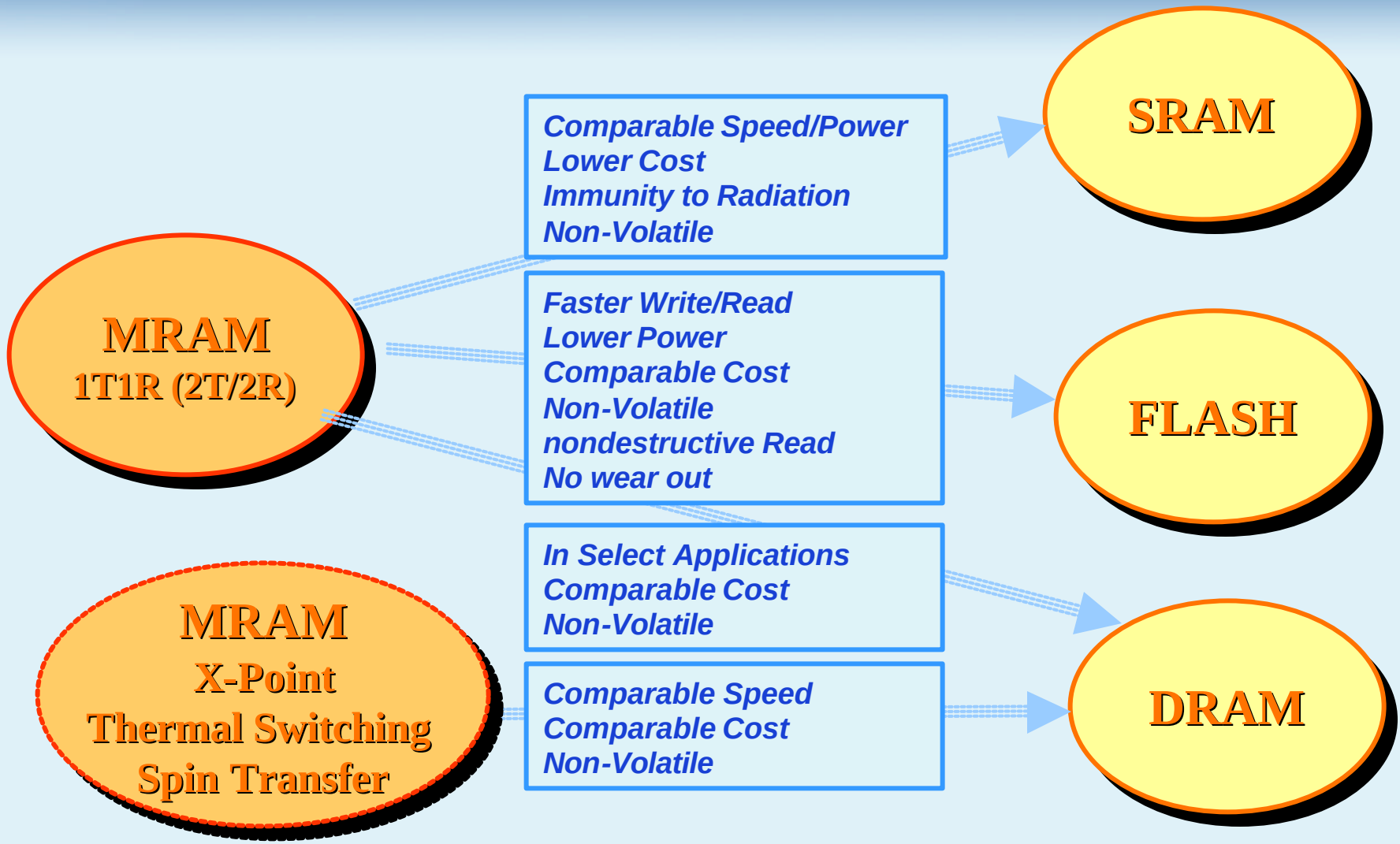
  Low Cost, High Volume, Low Power, NV,

  Compatible with Established CMOS Technologies

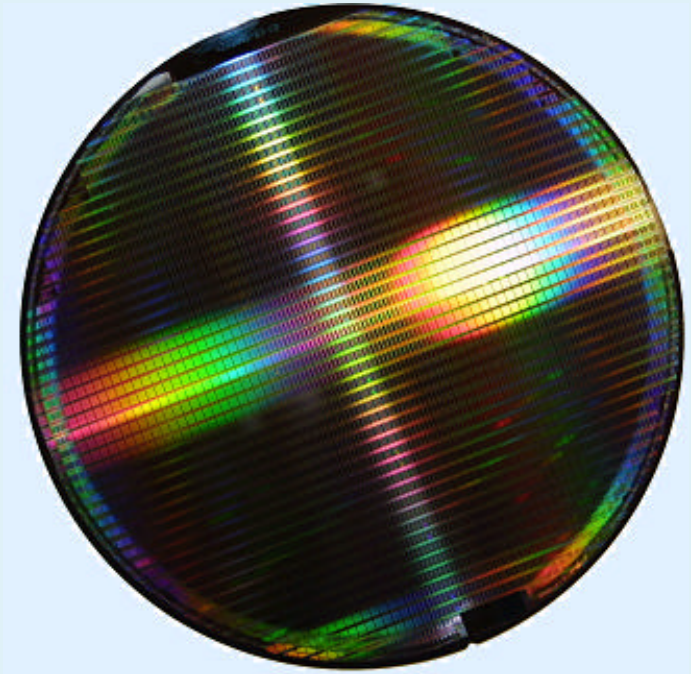
- **Several Non Volatile Technologies in Development: FeRAM, OUM**
- **MRAMs Close to Ideal**

▲ Worst ● Good ○ Best	DRAM	SRAM	FLASH	FRAM	MRAM	OUM
Cost	○	▲	●	●	●	○
Access Time	●	○	●	●	○	●
Write Time	●	○	●	●	○	●
Active power	○	○	▲	○	○	○
Stand By	▲	○	○	○	○	○
Non Volatile	▲	▲	●	●	○	●
Endurance	○	○	▲	●	○	●

MRAM OPPORTUNITIES



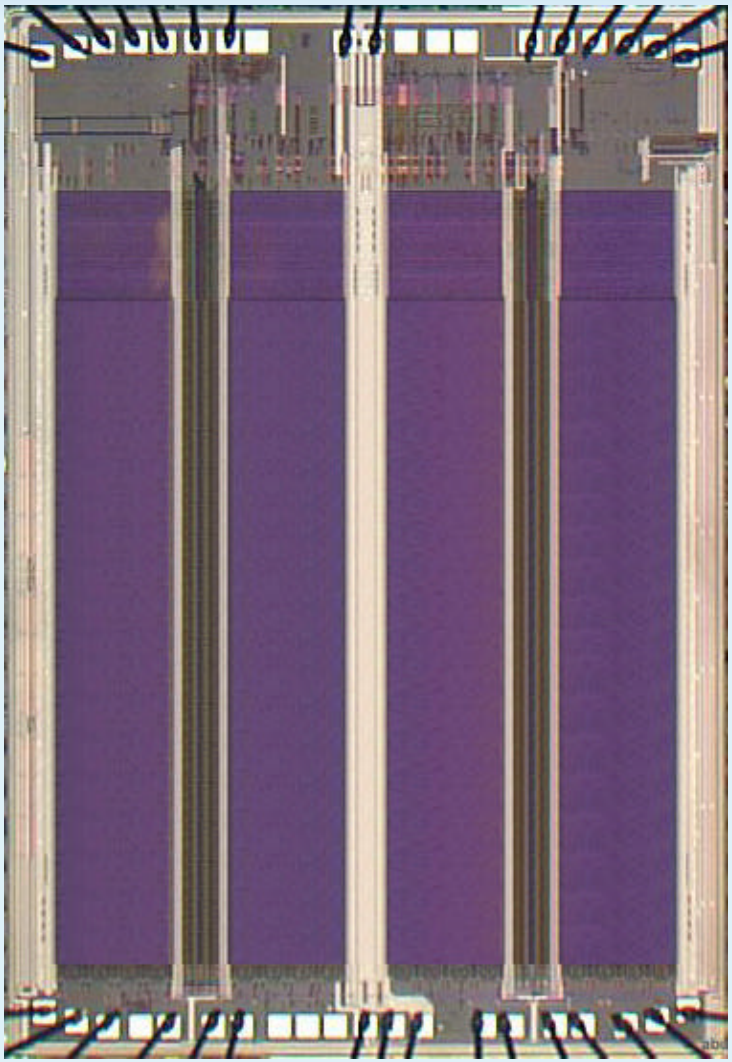
Cypress Objectives



- **Deliver 256K Working MRAM Memory**
- **High Density MRAM Memory On Mainstream SRAM Technology**
  - High Density 1.8V and 3V Design for Industrial Applications (cell phones and others)

256K MRAM PRODUCT DESCRIPTION

CY9C62256



- **5V 256K MRAM**
- **Form, Fit & Functionality Compatible with Micro Power 256K RAM (CY62256)**
- **Industrial Temperature Range**
- **Additional MRAM Functionality**
  - Non-Volatile Memory Storage
  - Infinite Endurance & Data Retention

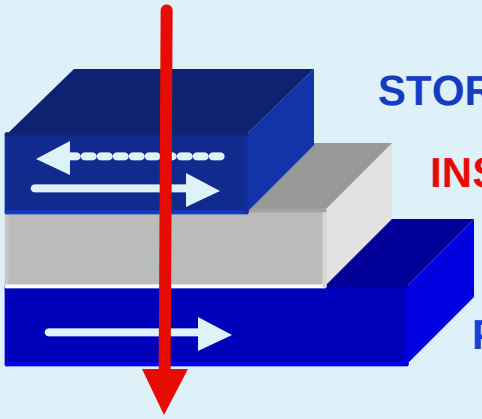
- For additional information www.siliconmagnetics.com

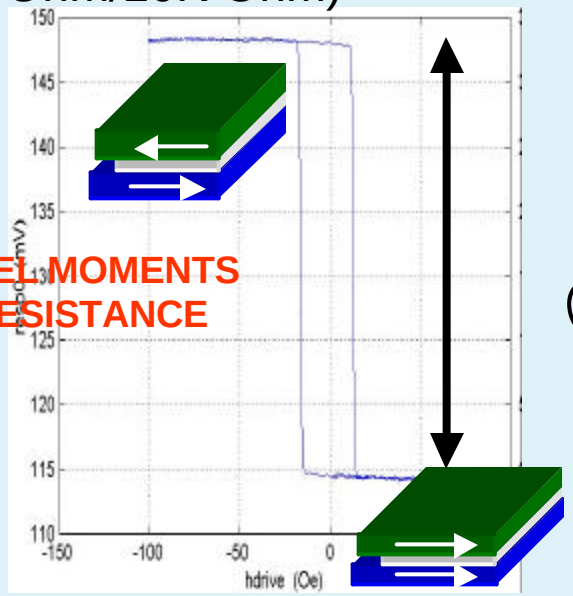
MRAM BASICS (1): THE MTJ

MTJ Magneto Resistive Effect

- Bottom Pinned Layer Has Electron Spin Fixed In One Direction
- Top Layer Electron Spin Can Be Either Parallel or Anti parallel To Pinned Layer Depending on The Switched State
- When Electron Spins Tunnel Across Tunnel Junction, Tunneling Electrons See Spin Polarization Dependent of the Magnetization Orientation
- This Gives The MR Ratio ?R/R (Example: 3K Ohm/10K Ohm)

Magnetic Tunnel Junction





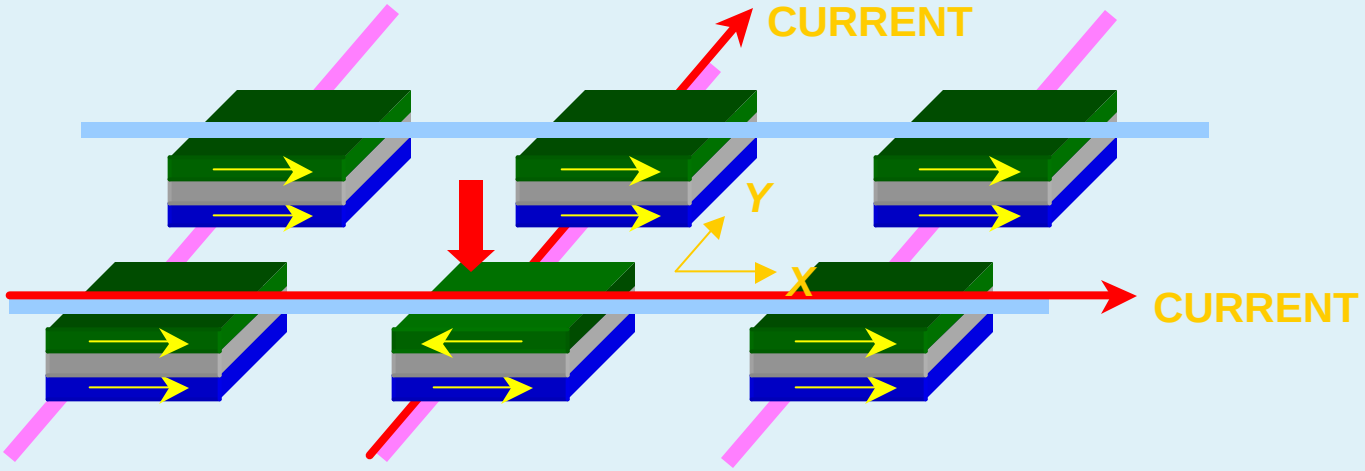
? R/R=28% @300mV

MRAM BASICS (2): Reading And Writing

✍ **Reading: Relies on the determination of the low or high resistance state of the MTJ**

✍ **Writing:**

ONLY THE ELEMENT AT THE INTERSECTION IS WRITTEN



MRAM BASICS (3): WRITING DATA

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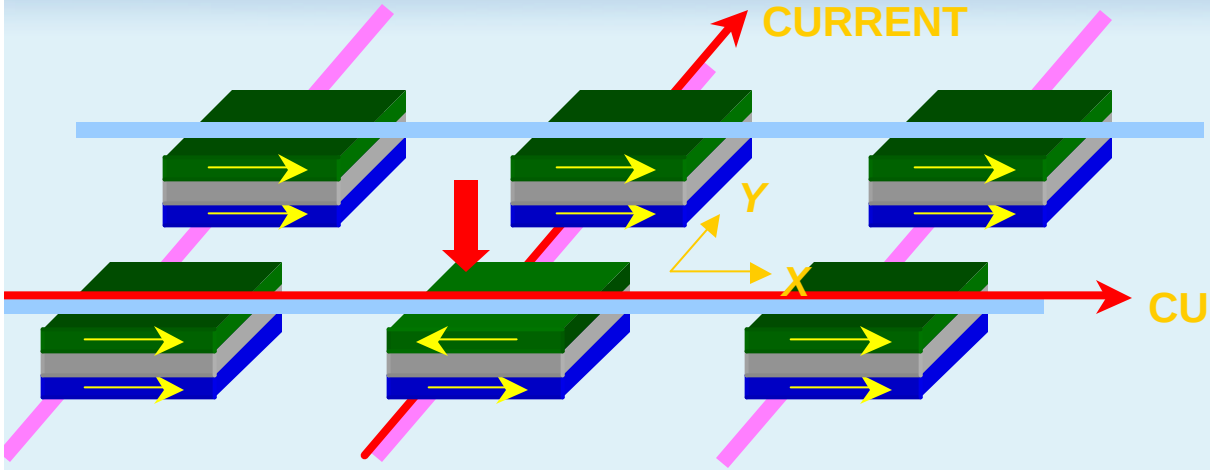
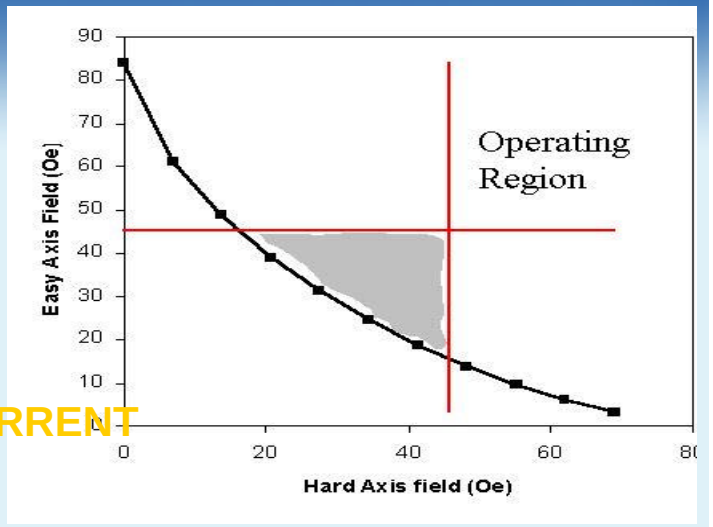
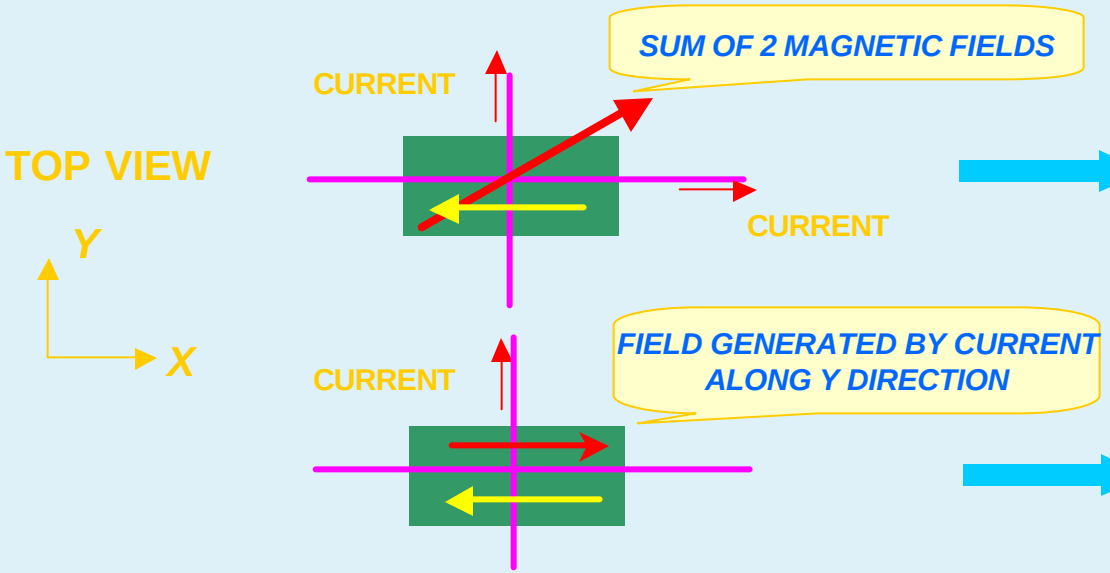




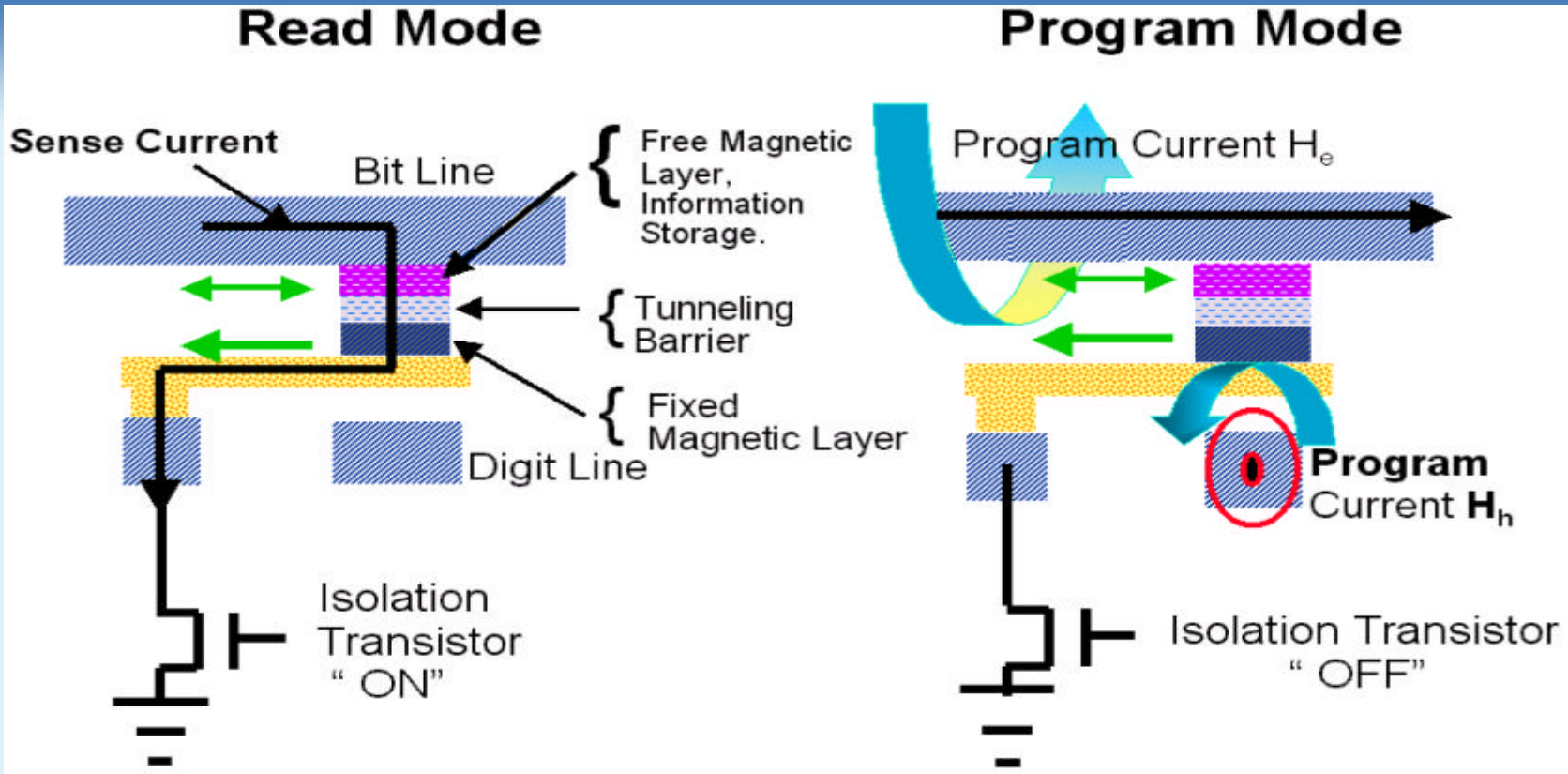
ONLY THE ELEMENT AT THE INTERSECTION IS WRITTEN



MAGNETIZATION SWITCH IN STORAGE LAYER

MAGNETIZATION REMAINS UNCHANGED IN STORAGE LAYER

Memory Cell: Write And Read Operation



Read Mode

Detection of the MR effect:
Read 0: Spins aligned
Read 1: Spins opposing

Write Mode

Write 0: Aligned current pulses in bit and word lines: Spins aligned
Write 1: Opposed current pulses in bit and word lines: Spins opposing

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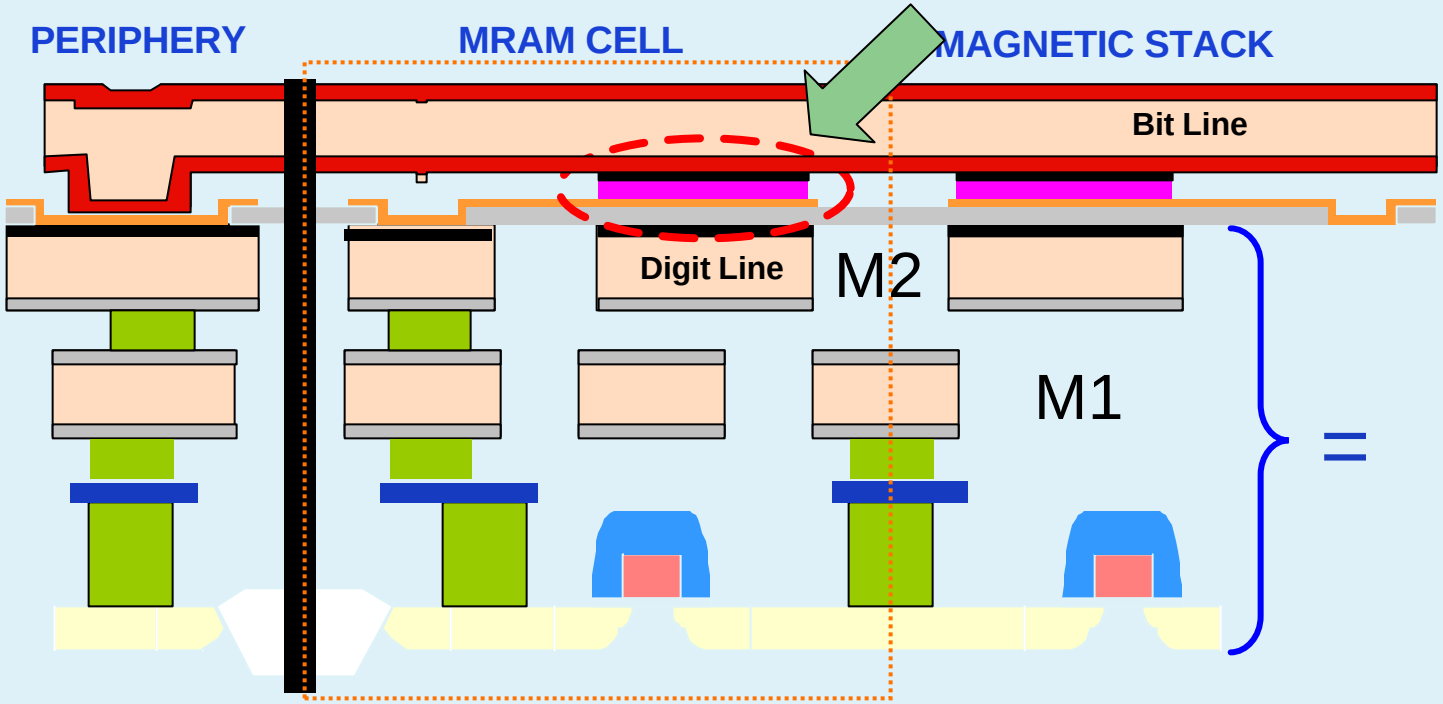
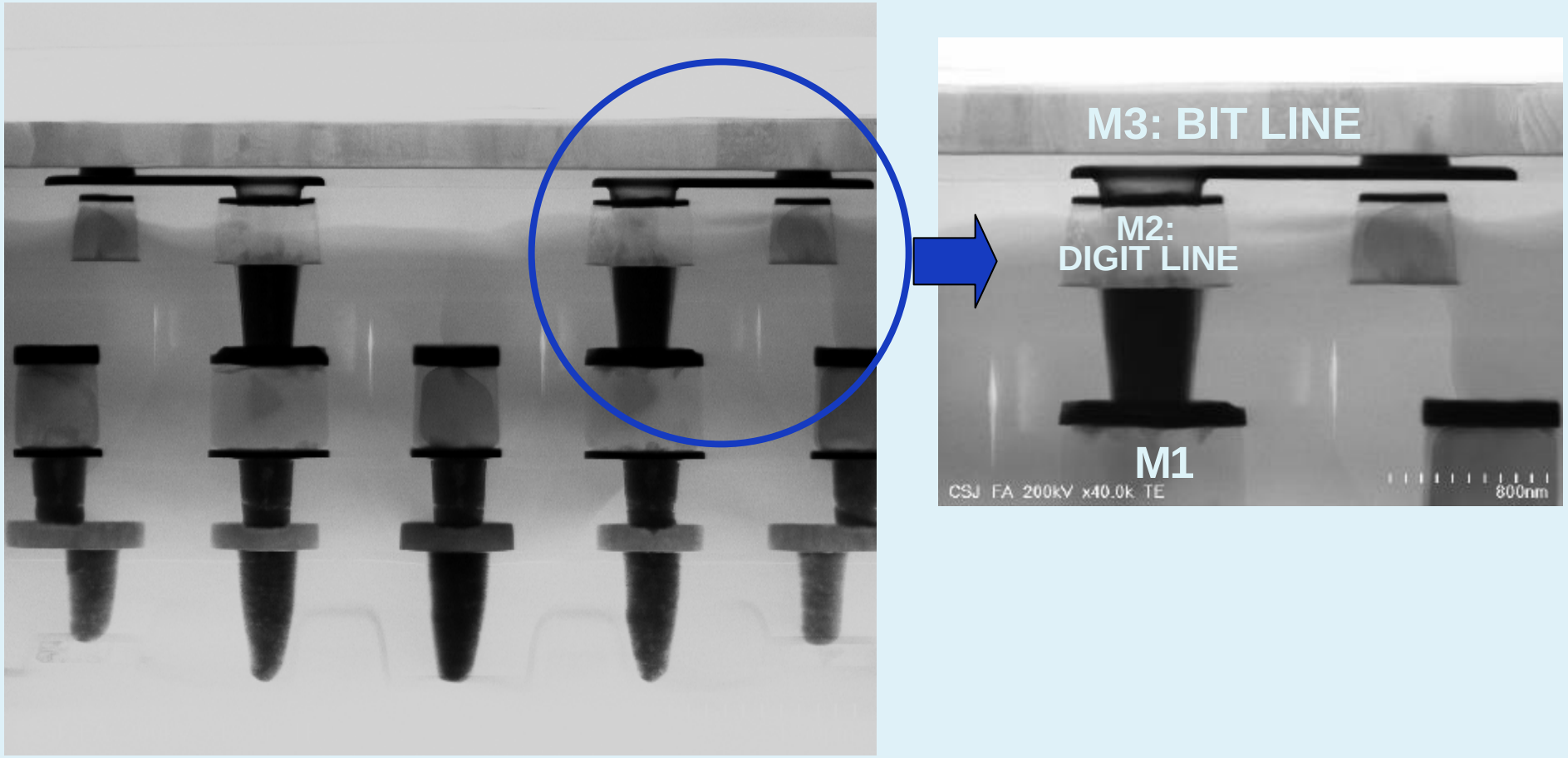
STANDARD MRAM PROCESS



= ST CMOS Process

ADDS ON TO STANDARD LOGIC AND/OR MEMORY PROCESS

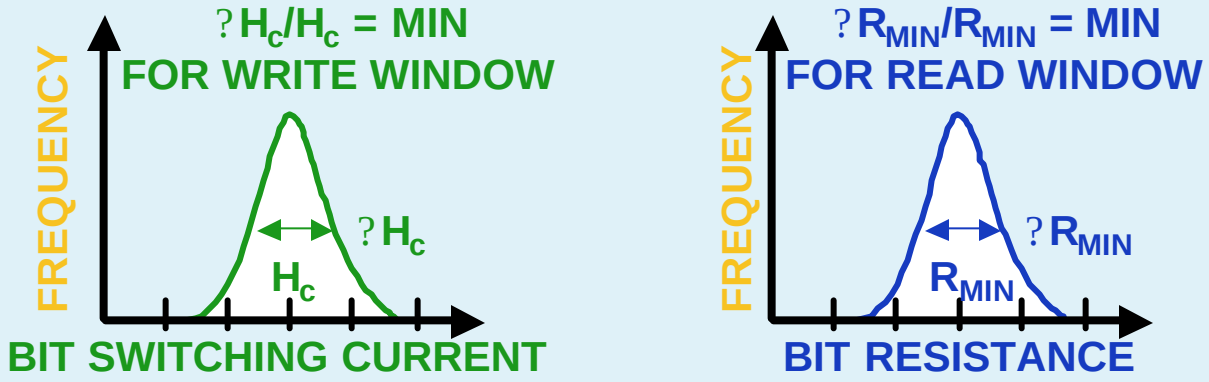
MRAM PROCESS And INTEGRATION



IMPORTANCE OF WITHIN-ARRAY MATCHING

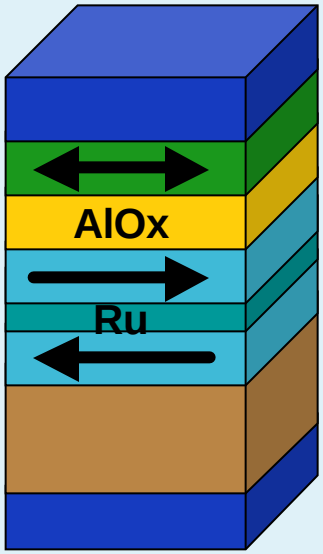
- **BASIC FEASIBILITY PROVEN – SINGLE MRAM BIT *IS* WORKING (THIS IS NOT A TRIVIAL STATEMENT…)**
- **CHALLENGE FOR A VIABLE MRAM PRODUCT:**
  MAKING ALL BITS IN A DIE SUFFICIENTLY IDENTICAL
  - **CELL & BIT DESIGN FOR OPTIMUM MARGIN**
  - **IMPROVED MTJ MATERIALS**
  - **PROCESS INTEGRATION**

DESIRED WITHIN-ARRAY DISTRIBUTIONS



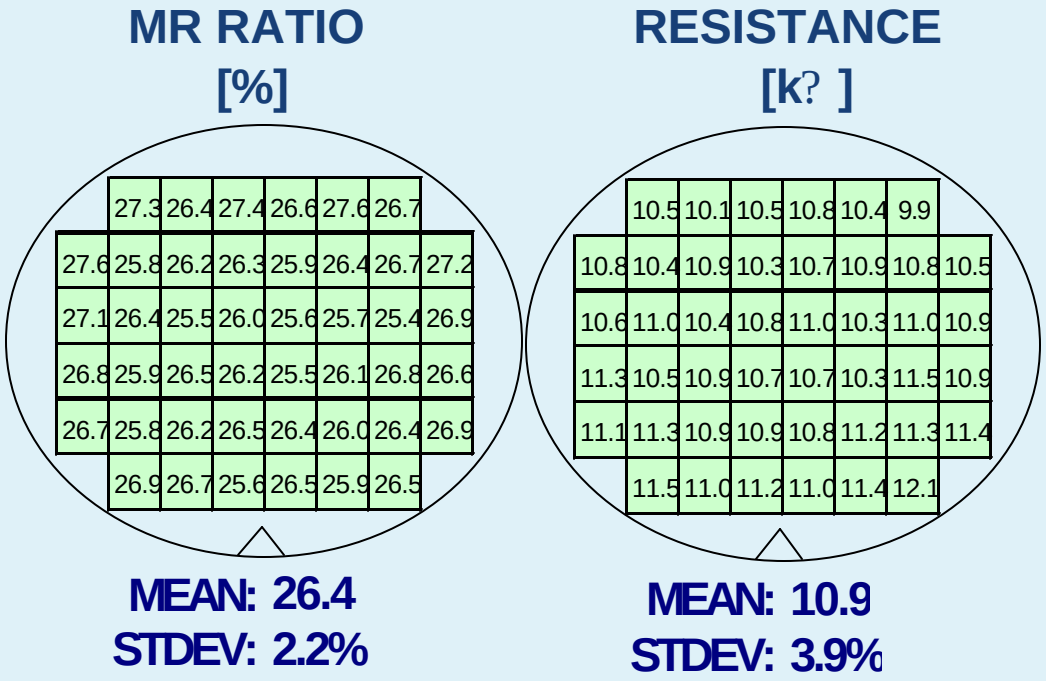
READ YIELD: MTJ STACK

SCHEMATIC LAYER STRUCTURE



- TOP ELECTRODE
- FERROMAGNET
- FERROMAGNET
- FERROMAGNET
- ANTI-FERROMAGNET
- BOTTOM ELECTRODE

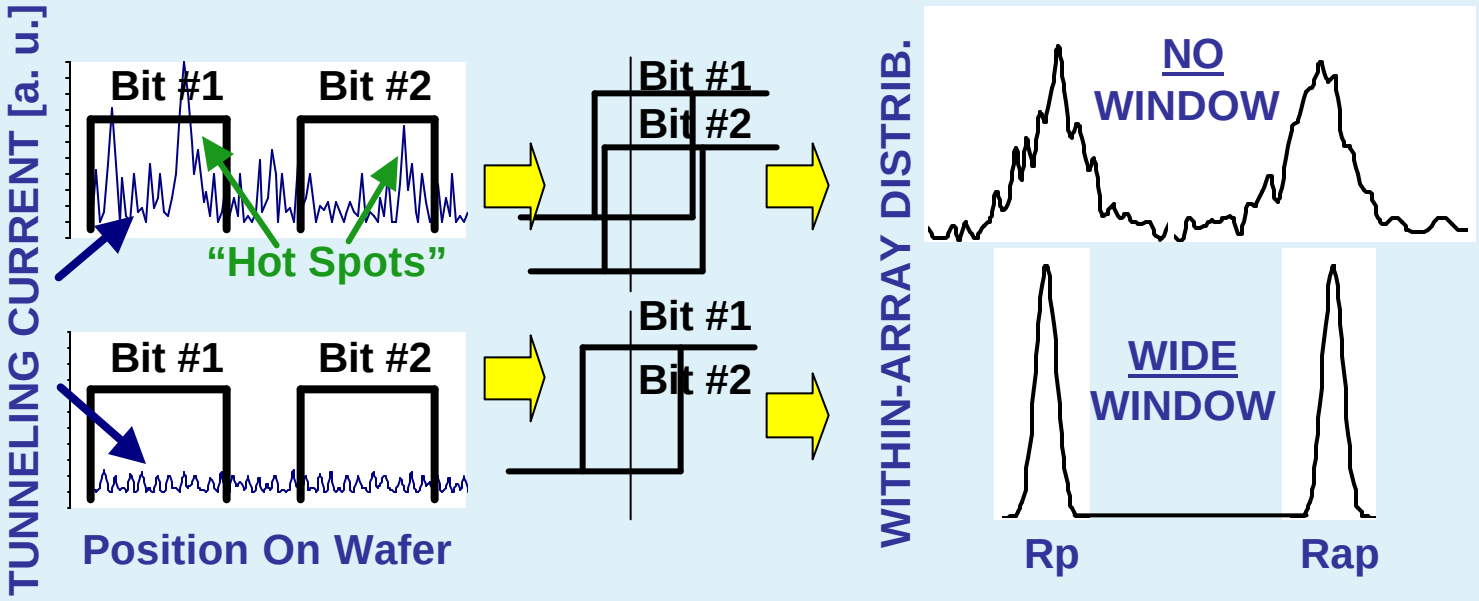
TYPICAL X-WFR DATA (8") @ 300 mV



- RA ~3 k? -?m², MR @ 300 mV ~25-40% (MATERIAL DEPENDENT)

READ YIELD: HOMOGENEITY OF TUNNEL BARRIER

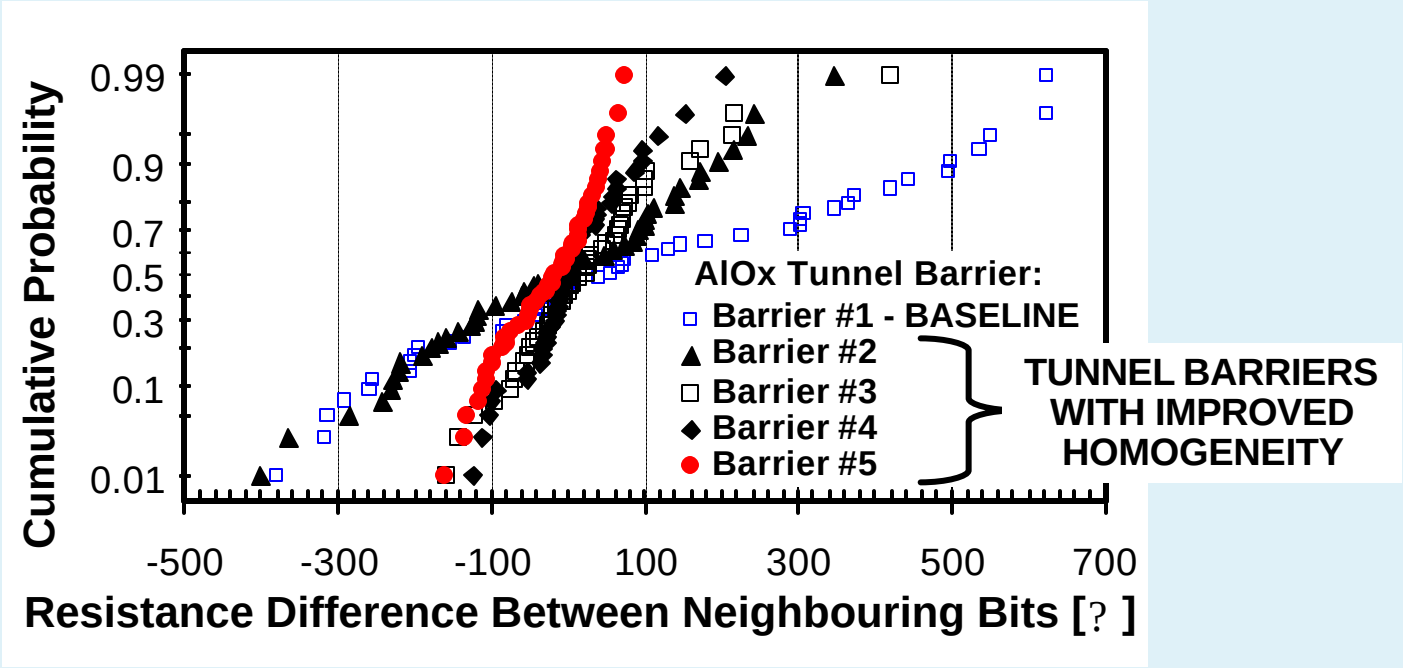
- **MTJ BARRIER INTEGRITY IS CRITICAL FOR WIDE SEPARATION OF WITHIN-ARRAY RESISTANCE DISTRIBUTIONS**



- **DIFFERENCES MAY NOT BE SIGNIFICANT AT THE SINGLE BIT PERFORMANCE LEVEL (MR, RA), BUT…**

HOMOGENEITY OF TUNNEL BARRIER

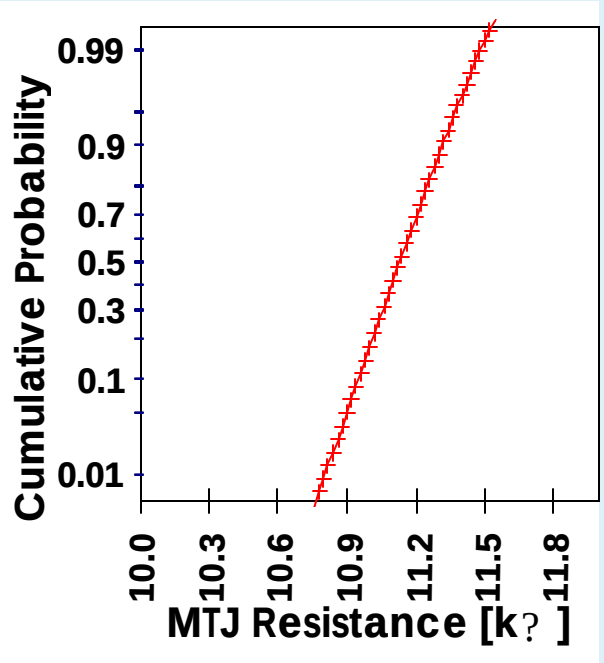
- **…IN LARGE BIT POPULATIONS, IMPROVED BARRIER SHOWS REDUCED BIT-TO-BIT VARIABILITY**

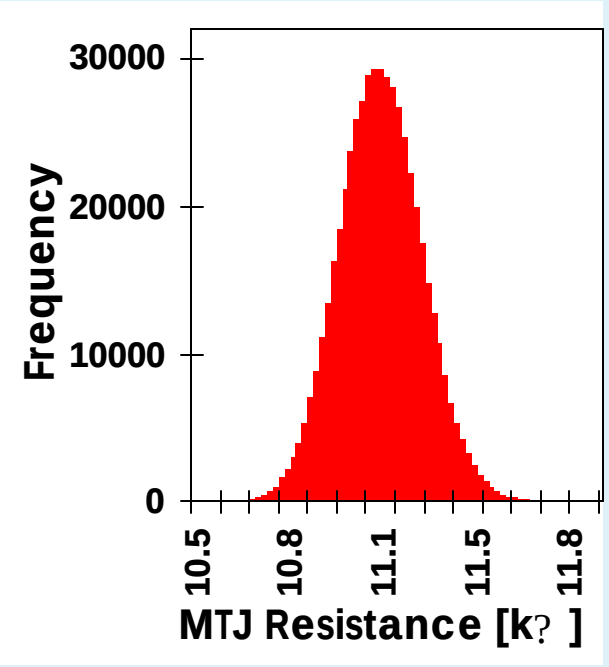


CUMULATIVE PROBABILITY PLOTS OF RESISTANCE DIFFERENCE BETWEEN NEIGHBOURING BITS SAMPLED FROM THE ARRAYS OF MTJs WITH ALOx BARRIER PREPARED IN VARIOUS WAYS

HOMOGENEITY OF TUNNEL BARRIER

- **WITH MTJs OF IMPROVED MICROSTRUCTURE, A TIGHT CONTROL OF WITHIN-ARRAY BIT RESISTANCE CAN BE ACHIEVED**



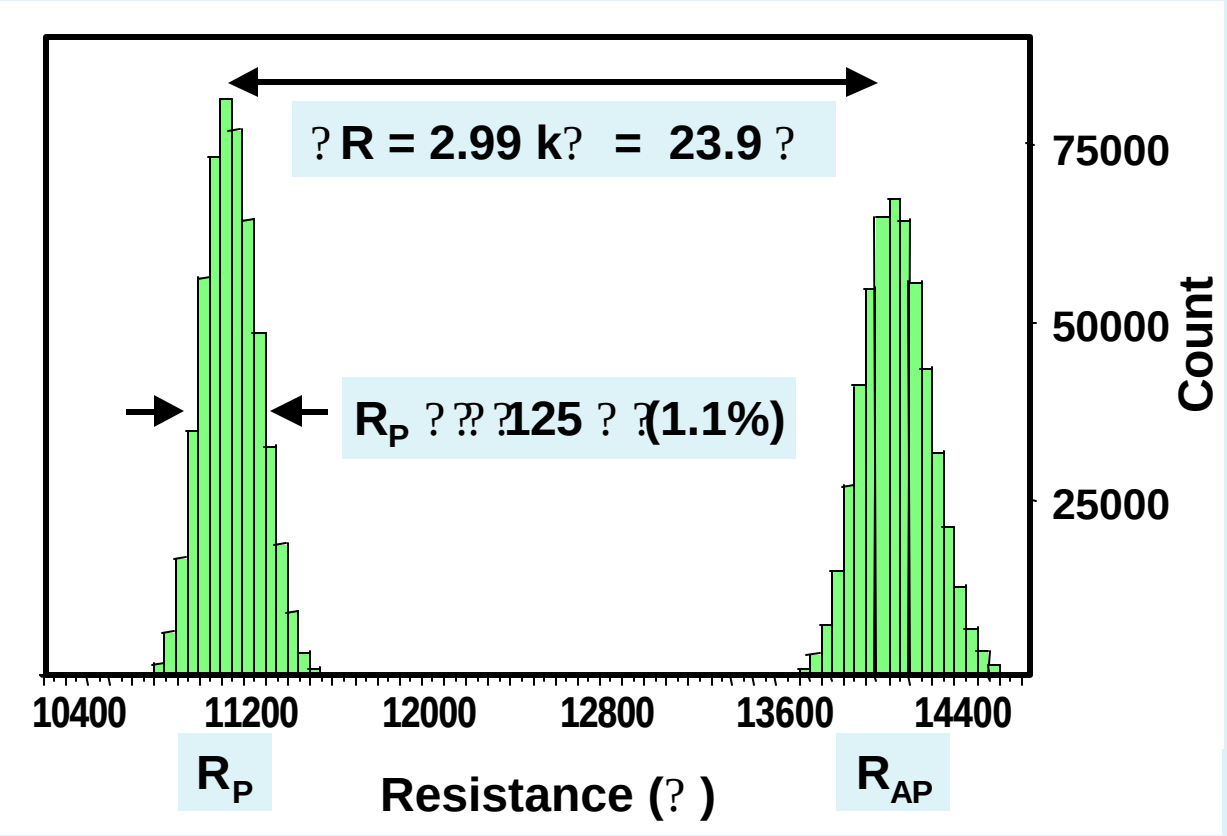


524,288 MTJs
1? = 1.1%
ZERO OUTLIERS

- **MTJ RESISTANCE VARIATION WITHIN A FULLY INTEGRATED 256K DIE: NORMAL DISTRIBUTION (1.1%), NO OUTLIERS**

HOMOGENEITY OF TUNNEL BARRIER

- **"LOW" AND "HIGH" RESISTIVITY DISTRIBUTIONS WITHIN A 256K MRAM DIE SHOW A DISTINCT SEPARATION (>23?)**



CYPRESS
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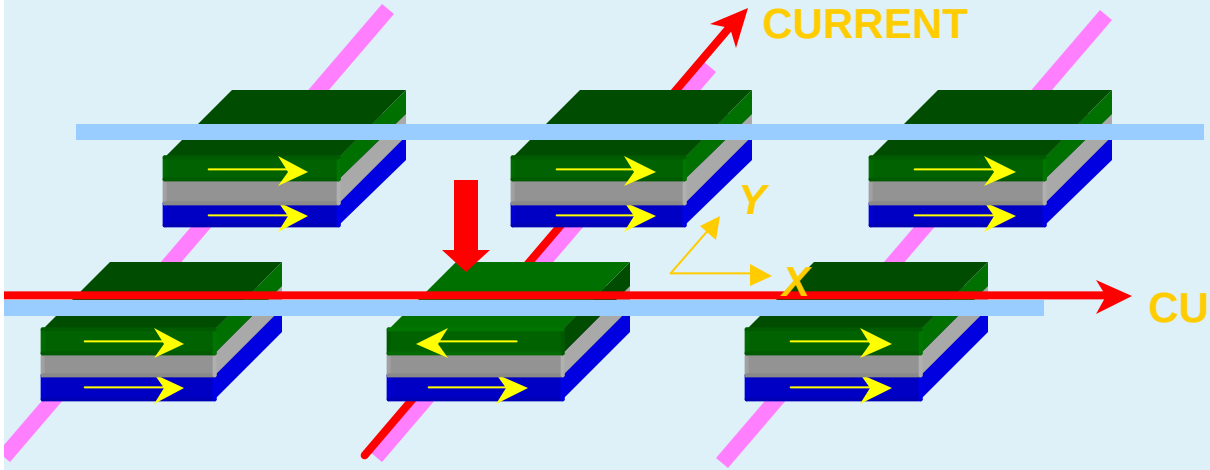
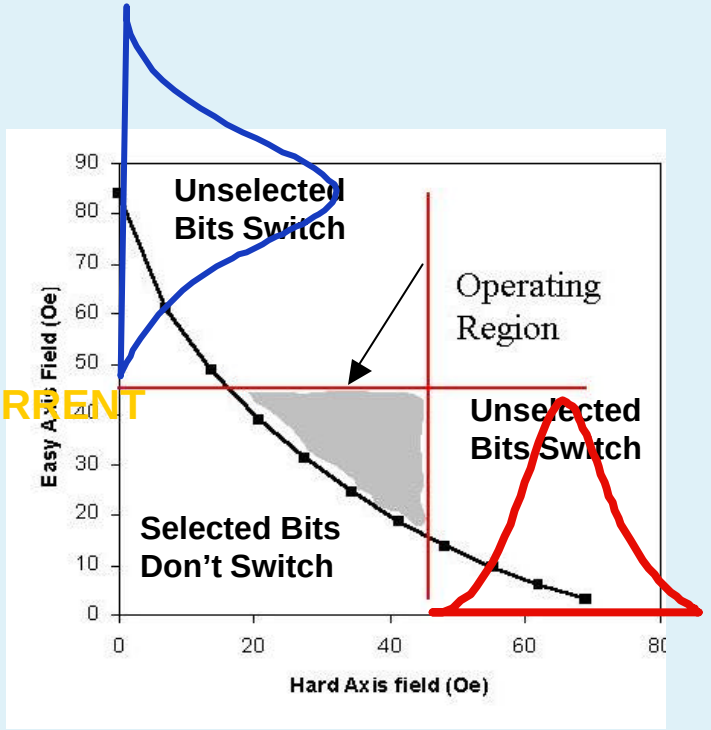
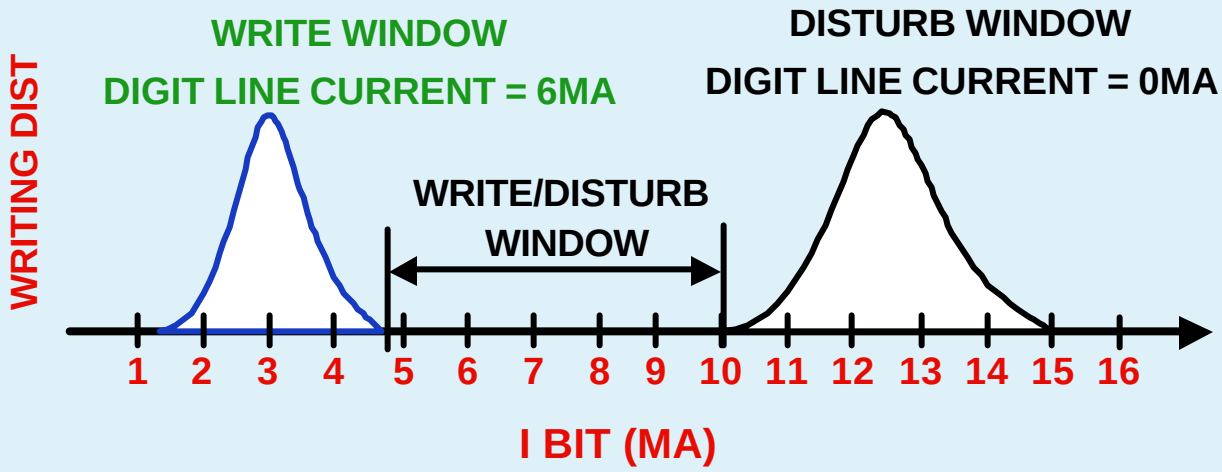
The Half Select Problem:

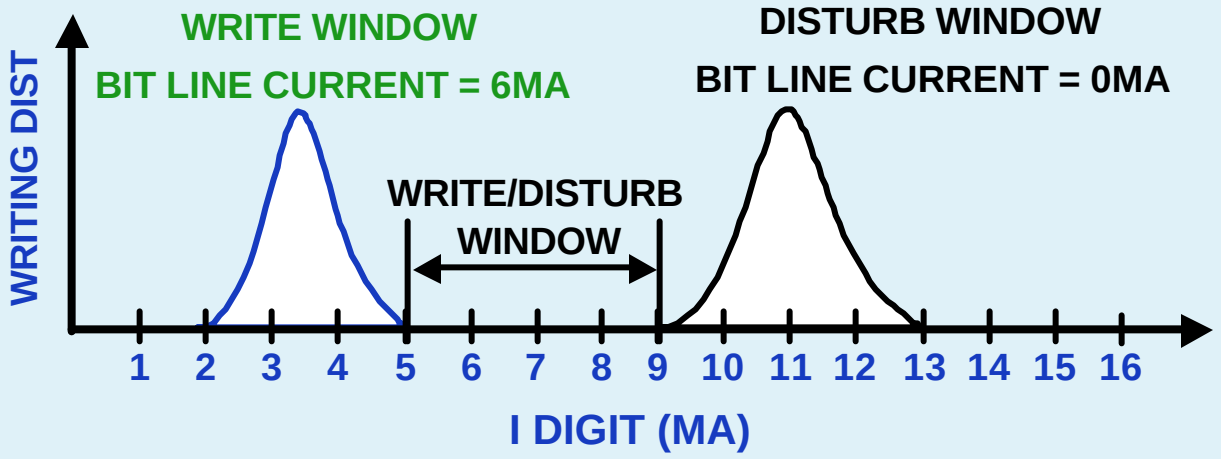
- **Switching Distribution is a killer => Needs to be tighten to increase writing Margin**





IDEAL WRITE/DISTURB WINDOW

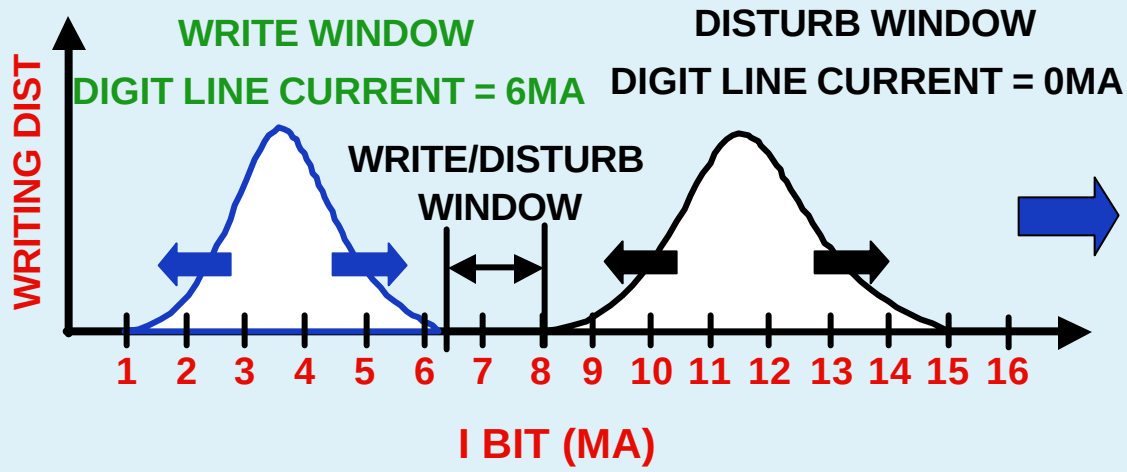




WRITE/DISTURB DISTRIBUTIONS: What are the problems

PROBLEM#1

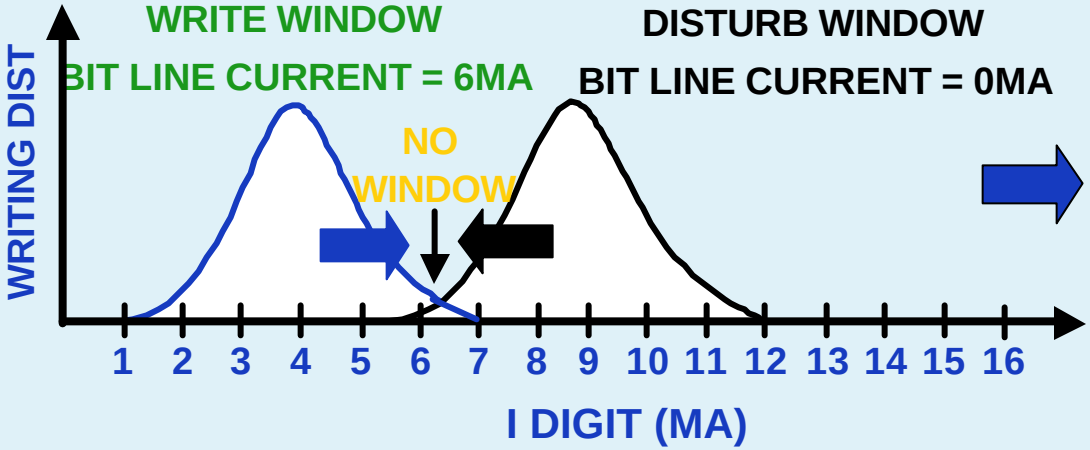
BIT MATCHING VARIABILITY



Define New Scheme for Dot Shape

PROBLEM#2

INTERLAYER COUPLING SHIFT



Improve Integration

SORT TEST FOR BL & DL DISTURB

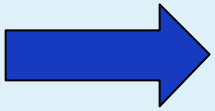
0	1	0
1	0	1
0	1	0

Writing Checkerboard

1	0	1
0	1	0
1	0	1

Writing Inverse checkerboard

COMPARE



✍	✍	✍
✍	✍	✍
✍	✍	✍

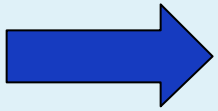
Bit counts = 9

0	1	0
1	1	1
0	0	1

Writing Checkerboard

1	1	1
0	1	0
1	0	1

Writing Inverse checkerboard

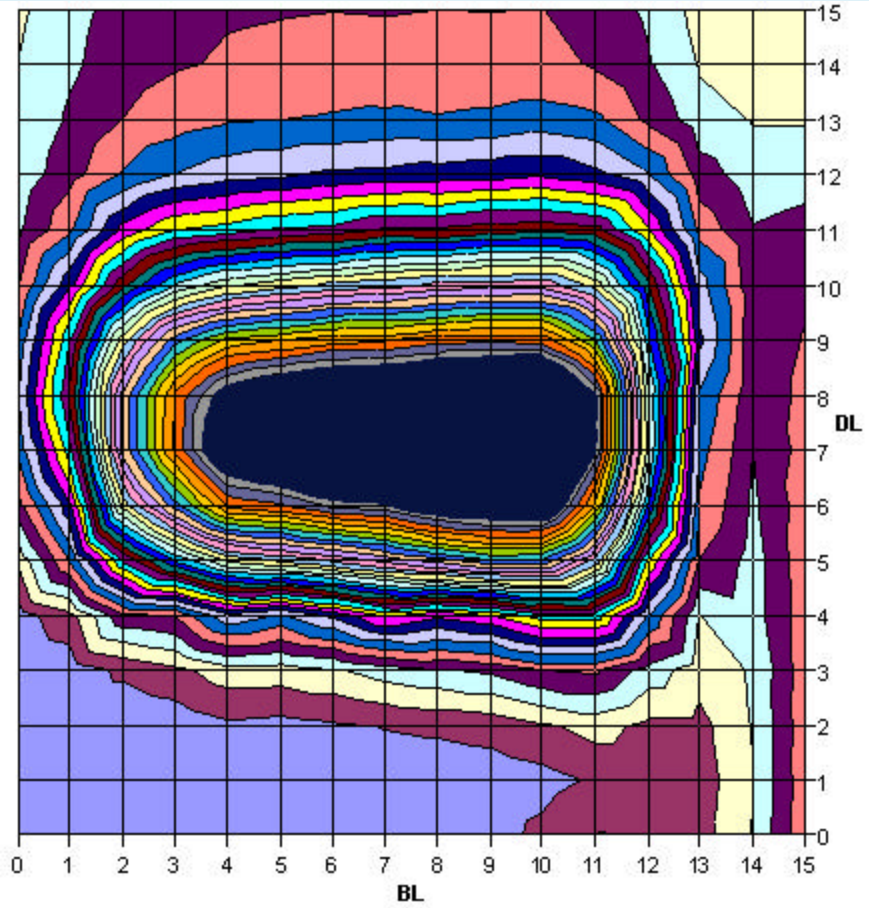


✍	?	✍
✍	?	✍
✍	?	?

Bit counts = 5

- **Allow to check multiple disturbs and select on each site**
- **Output is range of current at which select/Disturb is best**

1 DIE SORT YIELD W/ BL & DL DISTURB



Cy shape:

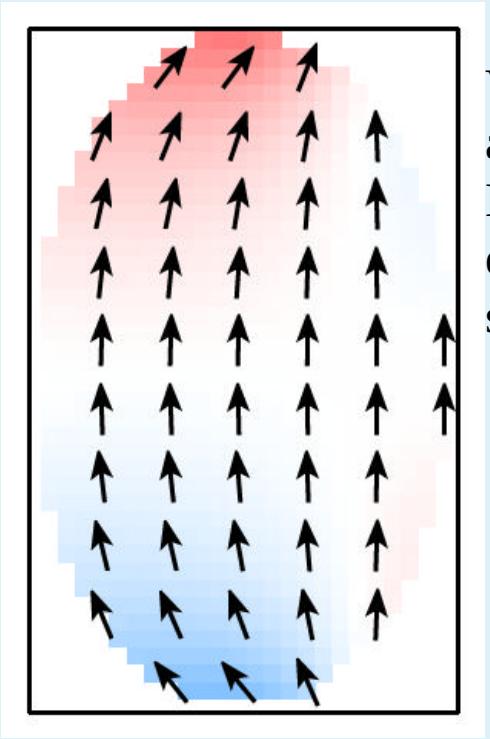
Uses the S state for the writing and the C state for the disturb.

- Good operating window
- Shape designed to have the C state stable at rest for improving the Bit Line Disturb (Vortex formation).
- Needs the Digit Line current to reach the S state

Improved Shape: Uses C and S states[18]

Magnetic states very close in energy. Small perturbations (defects for instance) may force to stabilize in one states at the expense of the other.

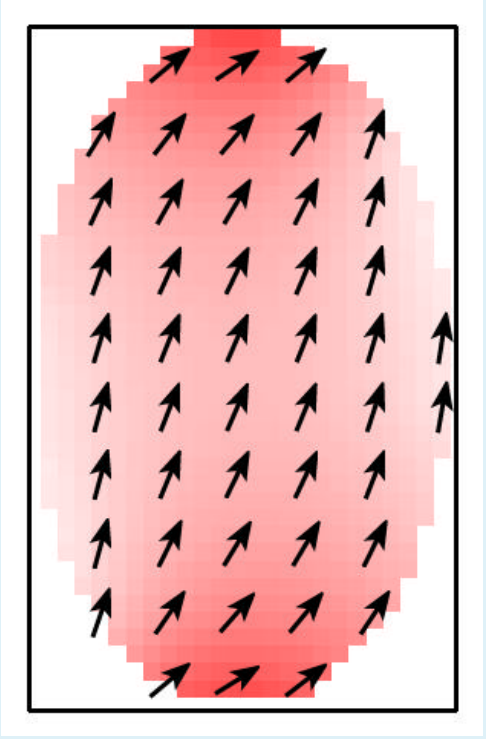
C state



Vortex formation and annihilation. High cost in energy. High switching field.

Relaxed state: No field applied

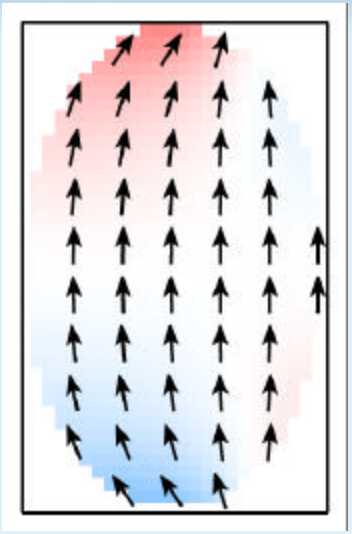
S state



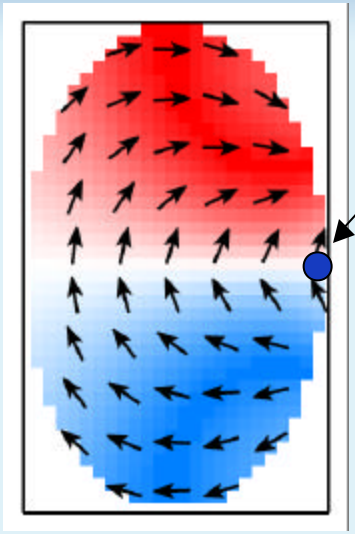
Coherent rotation. Low cost in energy. Low switching field.

Transverse Field applied

How reversal occurs when starting from C states…

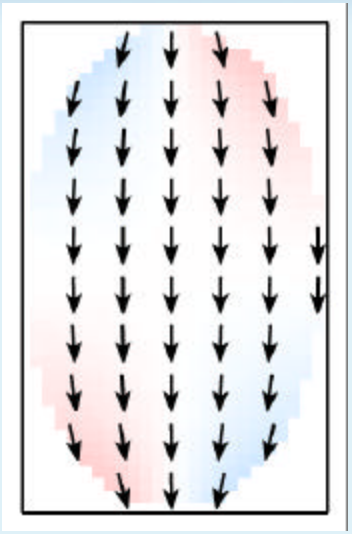


Relaxed state
No current

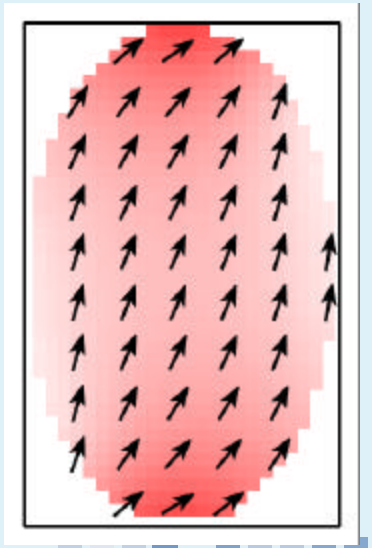


Vortex formation

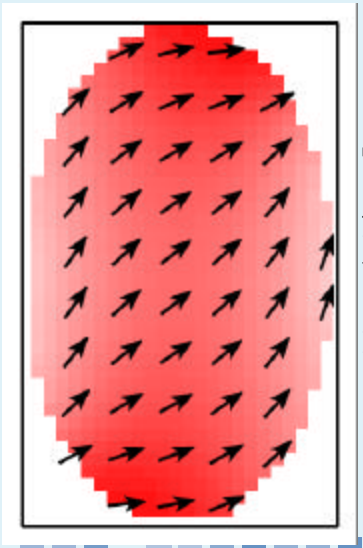
Before reversal



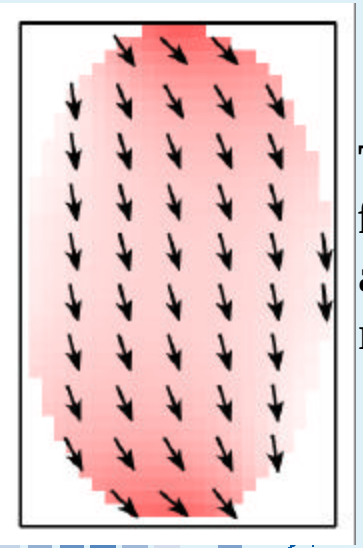
After reversal



Transverse field
I_{DL}=10Oe
I_{BL}= 0 mA



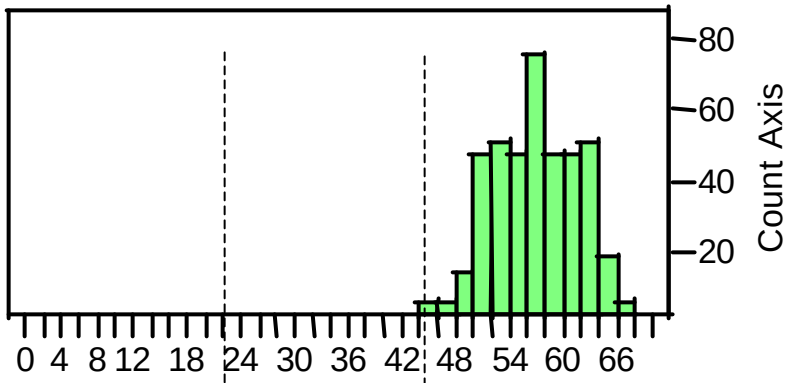
Transverse field just before reversal

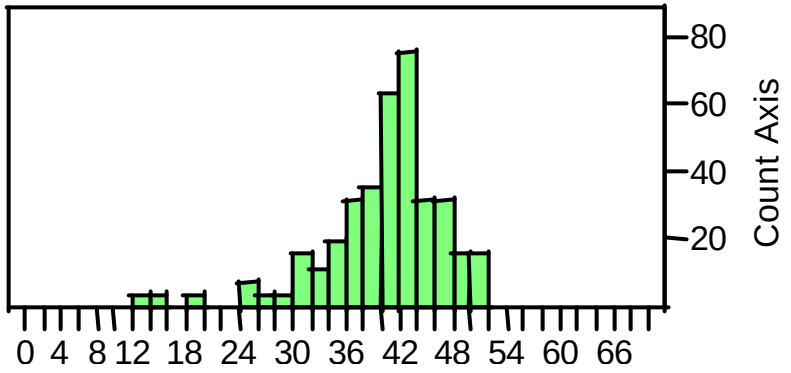


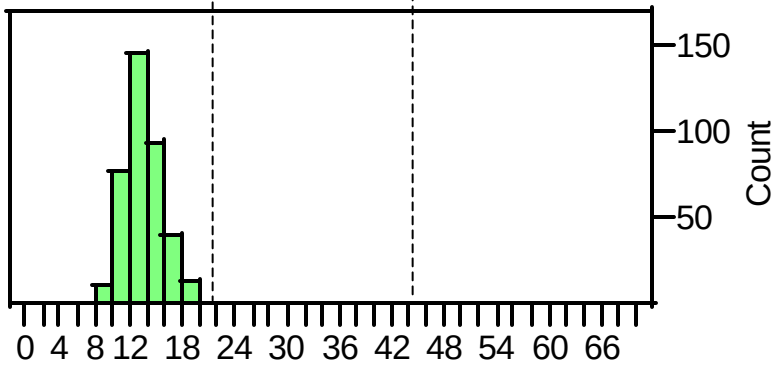
Transverse field just after reversal

Select and Disturb Behavior

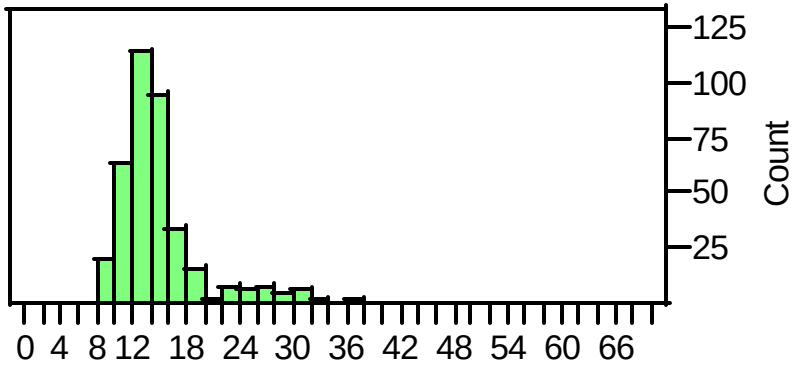
Improved Free Layer+Integration





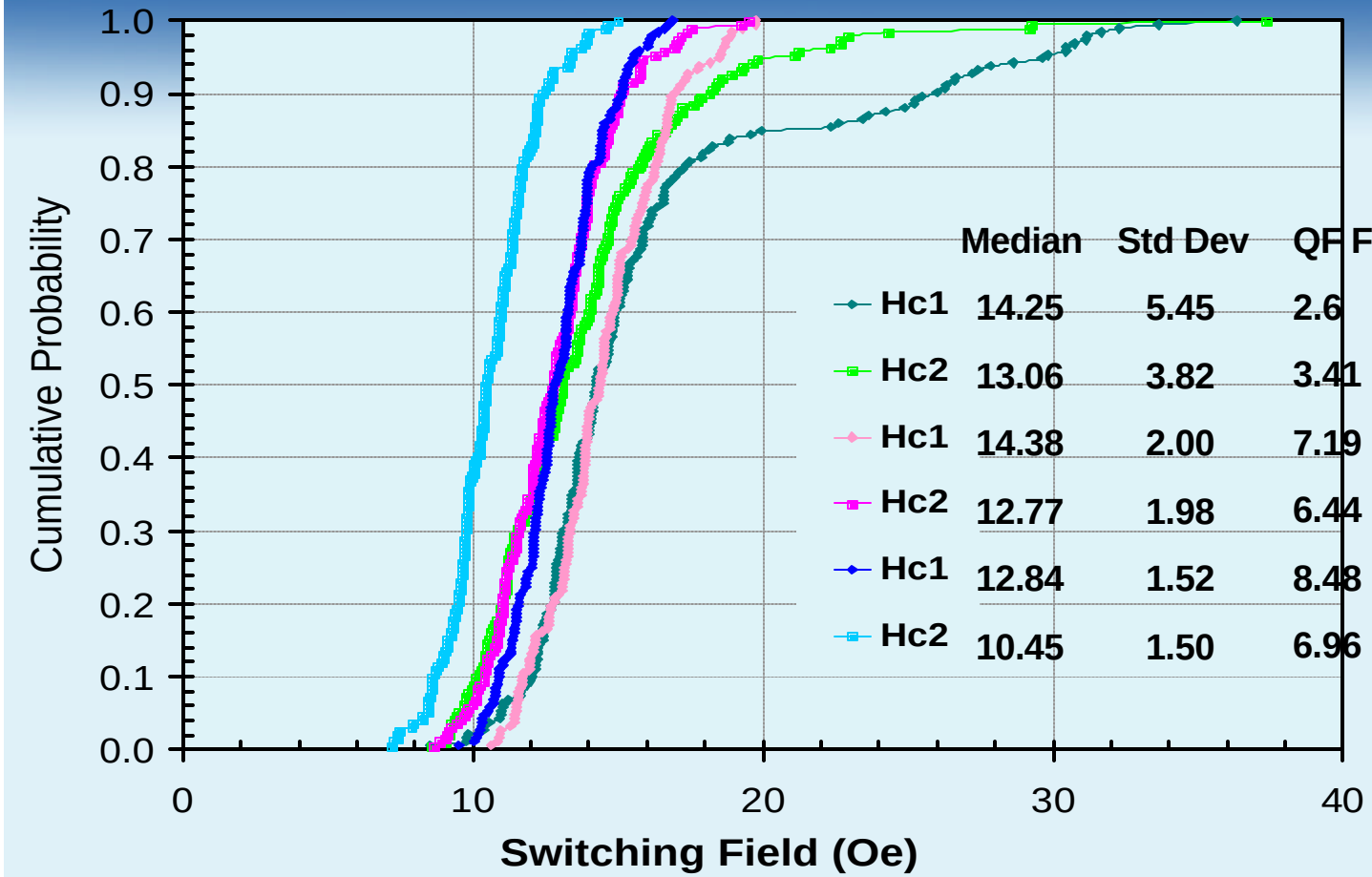


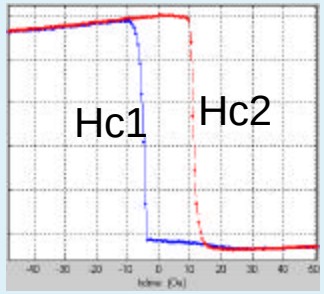
22Oe Window X-wafer



No Window X-wafer

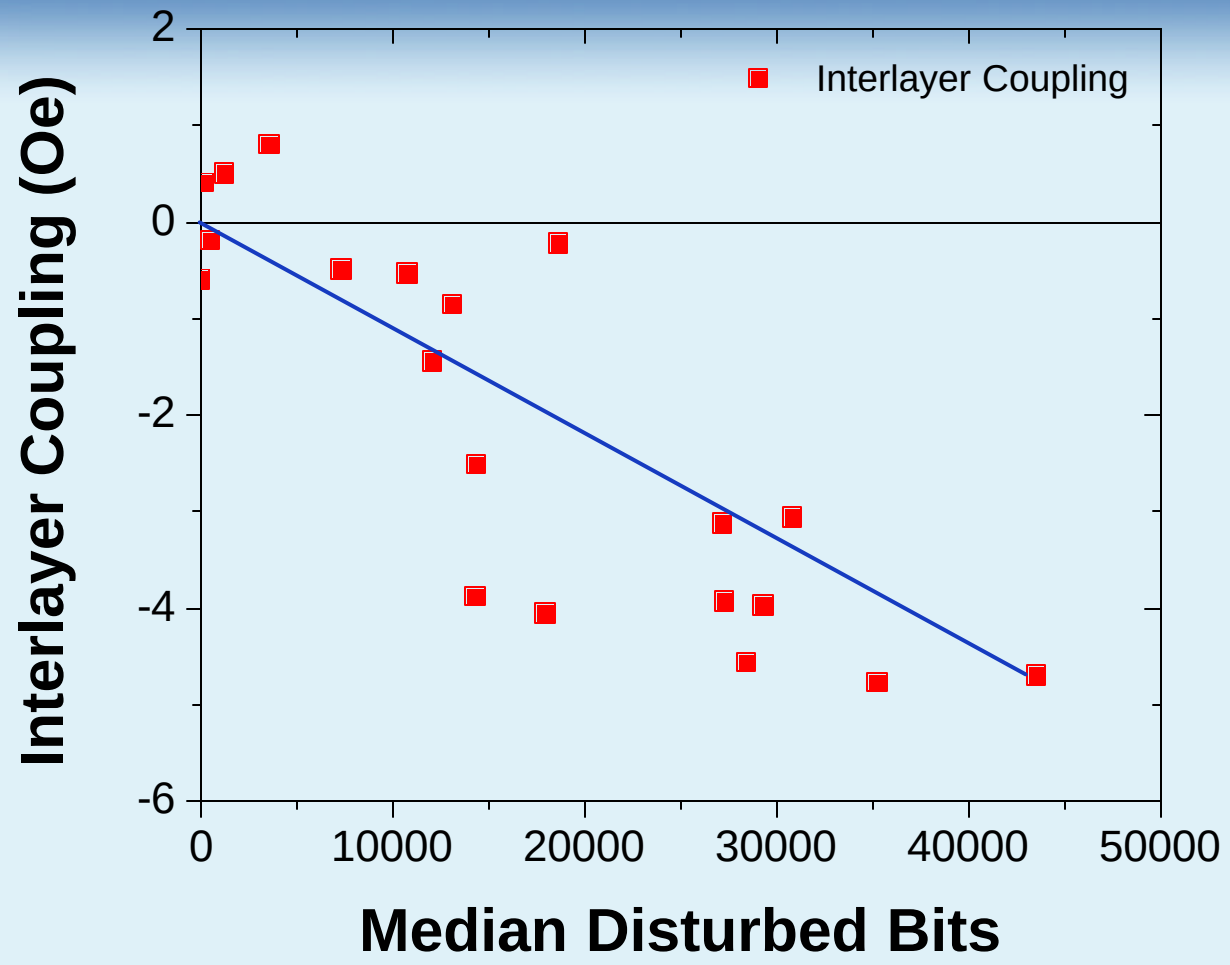
Switching Distribution





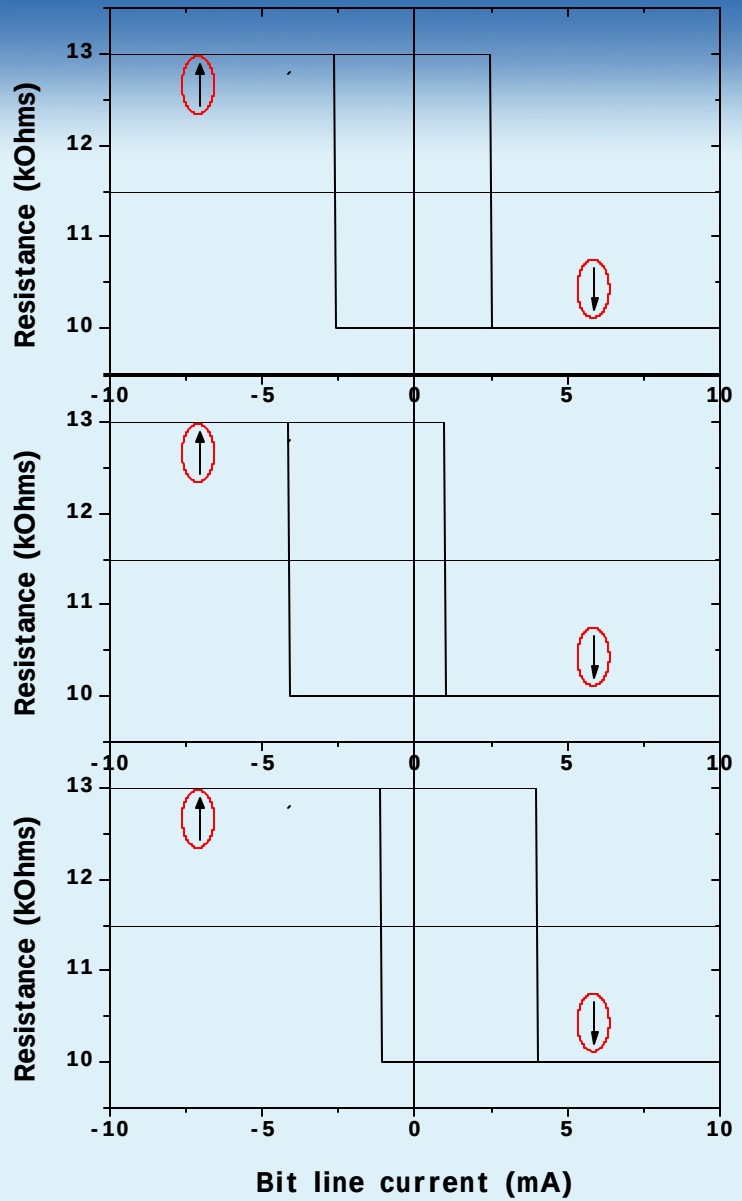
- **What could be the Factors of Improvement**
  - **Optimizing Dot Shape**
  - **Reducing Interlayer coupling by Optimizing Integration (Etch + Material Stack**

X- Wf Interlayer Coupling vs Disturbed Bits In Dies



- Larger the interlayer coupling, larger is the median Disturbed Bits
- Having an Interlayer Coupling close to Zero is not good enough

Simple Picture for Interlayer Coupling



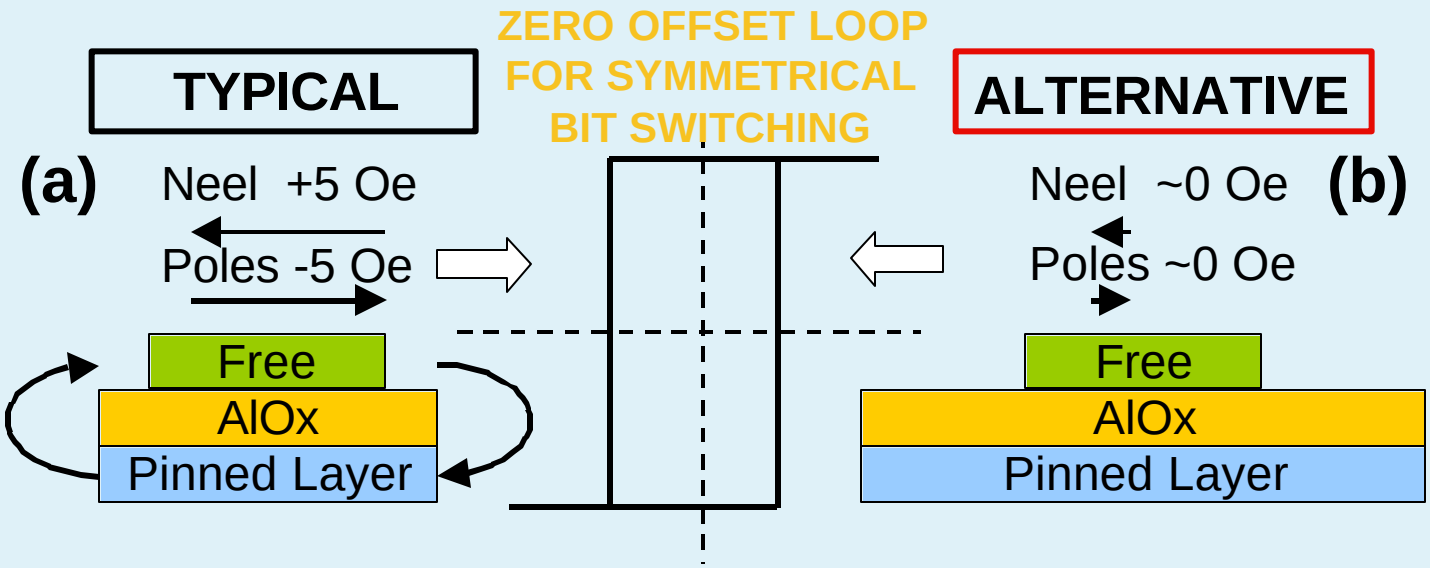
No Interlayer Coupling

Positive Interlayer Coupling: Neel Coupling
Favor the parallel State

Negative Interlayer Coupling: Poles due to Pinned Layer
Favor Antiparallel State

BIT SWITCHING BALANCING SCHEMES

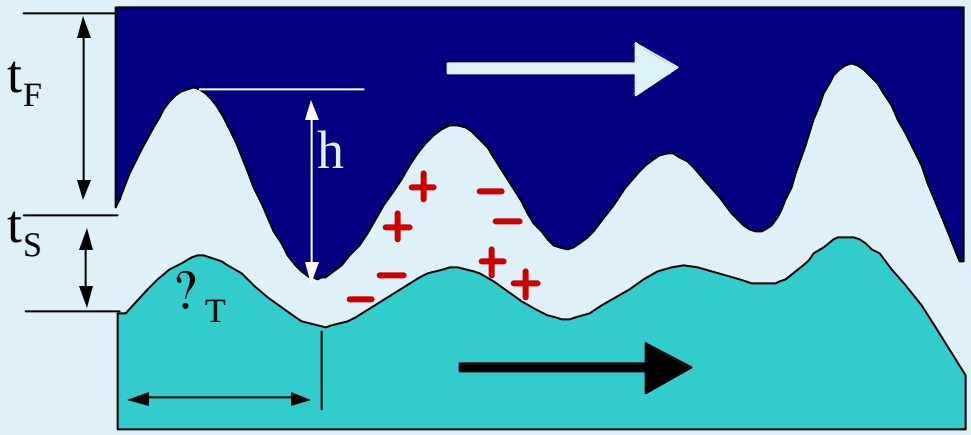
- **BALANCED BIT HYSTERESIS LOOP IS DESIRED FOR SYMMETRICAL AND STABLE BIT SWITCHING**



- **THE TWO BALANCING SCHEMES ARE ALMOST IDENTICAL AT THE SINGLE BIT SWITCHING LEVEL, BUT…**

Origin of interlayer coupling (1)

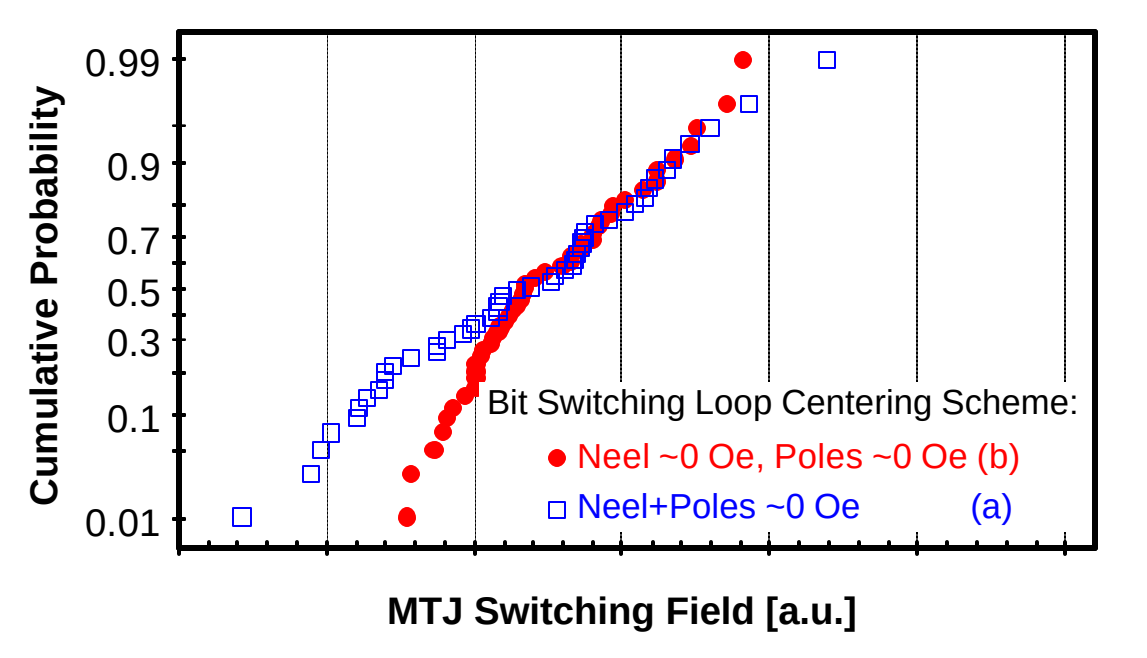
- **Orange Peel coupling (Neel type)**
  - Originates from roughness during deposition of magnetic films.
  - Interlayer coupling is negative (Favors Parallel state)
  - Uniformity dictated by the roughness height and wave length. Today,we are able to achieve a Neel Coupling close to 1Oe by making extremely smooth and uniform stacks.



$$H = \frac{\pi^2}{\sqrt{2}} \left(\frac{h^2}{t_F} \right) Ms \exp\left(-2\pi \sqrt{2}\, t_S / \lambda \right)$$

BIT SWITCHING BALANCING SCHEMES

- **…IN LARGE BIT POPULATIONS, ZERO NEEL COUPLING ALLOWS FOR NARROWER BIT SWITCHING DISTRIBUTION**

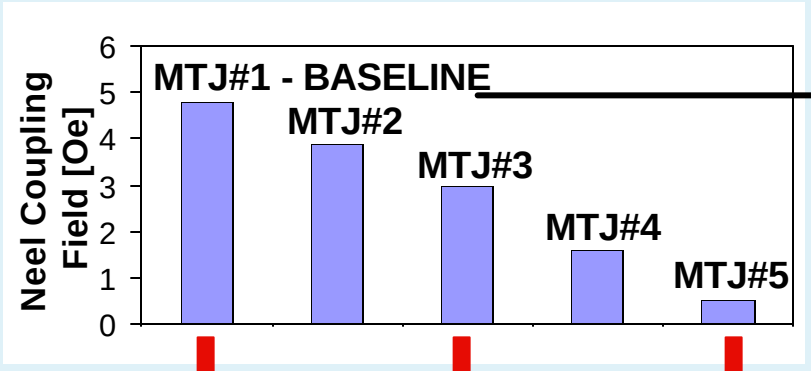


CUMULATIVE PROBABILITY PLOTS OF BIT SWITCHING DISTRIBUTIONS SAMPLED FROM THE ARRAYS OF MTJs PATTERNED USING DIFFERENT LOOP CENTERING SCHEMES

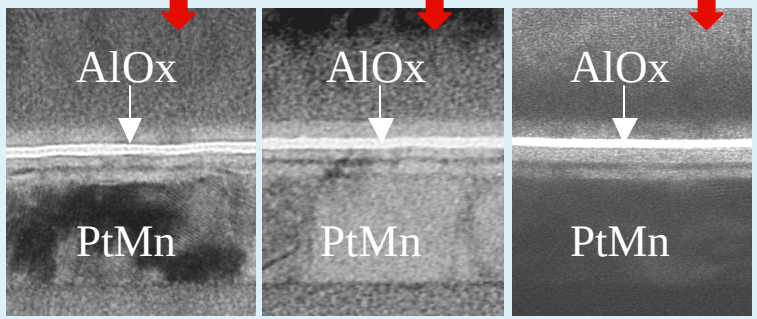
✍ **BETTER CONTROL OF BIT-TO-BIT VARIABILITY**

NEAR-ZERO NEEL COUPLING

- **LOW NEEL COUPLING POSSIBLE WITH NANOCRYSTALLINE AND SMOOTHER MTJ LAYERS**



NANOCRYSTALLINE (OR AMORPHOUS) AND SMOOTHENED LAYERS



CONTRARY TO CIP DEVICES (SPIN VALVES), MTJs DO NOT FACE LIMITATIONS IN USING MORE HOMOGENEOUS, BUT OF HIGHER RESISTIVITY, NANOCRYSTALLINE OR AMORPHOUS MATERIALS

- ✍ **LOW NEEL COUPLING CORRELATES WITH MORE HOMOGENEOUS MTJs (TEM CROSSECTIONS)**

SCALABILITY

- Technology Elements:
  - 100nm Technology Node: Cell Size Below 0.2 ?m2
  - TJ Size Metal Limited
  - Magnetic cladding on top of Metal Line to Boost the magnetic field provided by the current
- Scaling Challenges
  - Reaching the Superparamagnetic limit (Making the dot smaller)
    1. Data Retention and Error Rate. Needs new scheme to go beyond this limit
  - Switching
    1. Increased switching current: Need Magnetic Liners To Boost Magnetic Field (4X) with the same current
    2. Patterning Control
  - Junction Resistance
    1. Need extra control on RA product and higher MR ratio: Need New Magnetic Stack and Better Etch control

Driving the Communications Revolution

SUMMARY

- Most of the issues to make a manufacturable MRAM Part have been resolved: Working parts have been demonstrated. Still Some problems subsist such as Yield Increase (Compared to SC Technology)
- 3 Vectors of Optimization
  - Dot Shape optimization:
  - Stack and Integration optimization:
    - Materials and thickness
    - Interlayer Coupling: Critical issues are Control of Poles Thru
      - Pinned layer: Avoid any poles to affect switching of the free layer
      - Smoothness, Smoothness and Smoothness again
    - Limit Thermal Degradation
  - Programming Conditions
    - Pulse width
    - Time delay between DL and BL pulses found critical to have a sharp transition between write and no write

CYPRESS
Driving the Communications Revolution

Acknowledgements:

Witek Kula
Fred Jenne
Bettye Wadkins
Hualiang Yu
Bill Koutny
Helen Chung
Sam Geha
Eugene Chen
Biju Parameshwaran
Mehran Sedigh
Ben Schwarz
Chang Ju Choi
June Sananikone
Jeff Kaszubinski