Microelectronics Division

Challenges in Cu/Low K Integration for Multilevel BEOL Wiring

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Outline

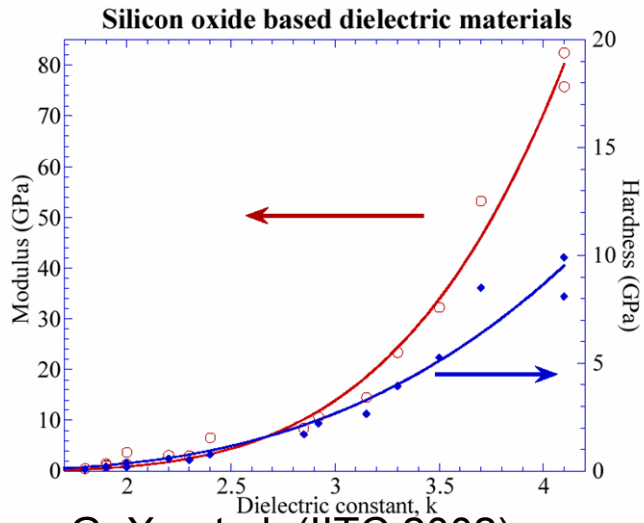
- **Introduction**
  - Material property trends
  - Effect on choice of integration scheme
- **Example Dual Damascene Low K Integration Scheme**
- **Unit Process Considerations**
  - RIE
  - Metallization
  - CMP
- **Metal Deformation in Low K BEOL processing**
- **Summary**

Introduction

Low K – Why and What Impact?

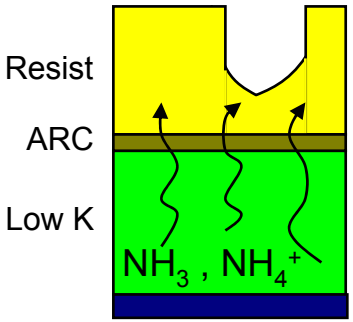
- **BEOL performance improvements (lower RC delay, power dissipation, cross talk) is the primary driver for introduction of low K materials into integrated circuit wiring levels**
- **Decreasing K generates concomitant reductions in density, modulus, hardness, and strength**
- **The relatively open structure of Low K dielectrics facilitates mass transport (e.g. of moisture, amines, plasmas)**

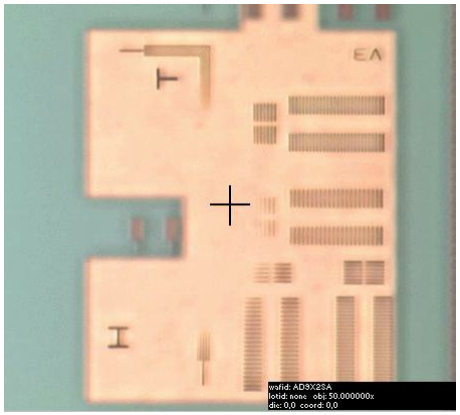
  →Drives choice of integration scheme



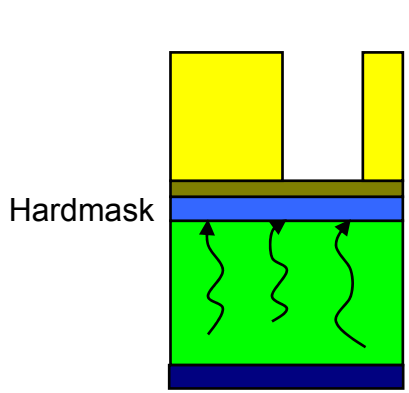
G. Xu et al. (IITC 2002)

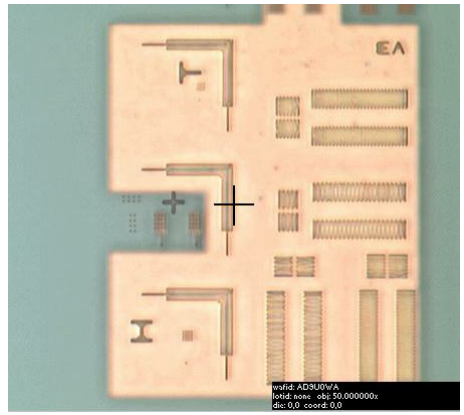
Example: Amine Poisoning of Photoresist





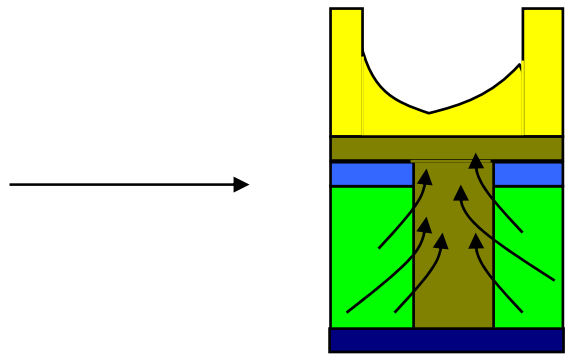
ARC/Photoresist applied directly onto SiCOH (K=3) dielectric – images fail to develop properly





ARC/Photoresist applied onto oxide hardmask over SiCOH (K=3) dielectric – images develop properly

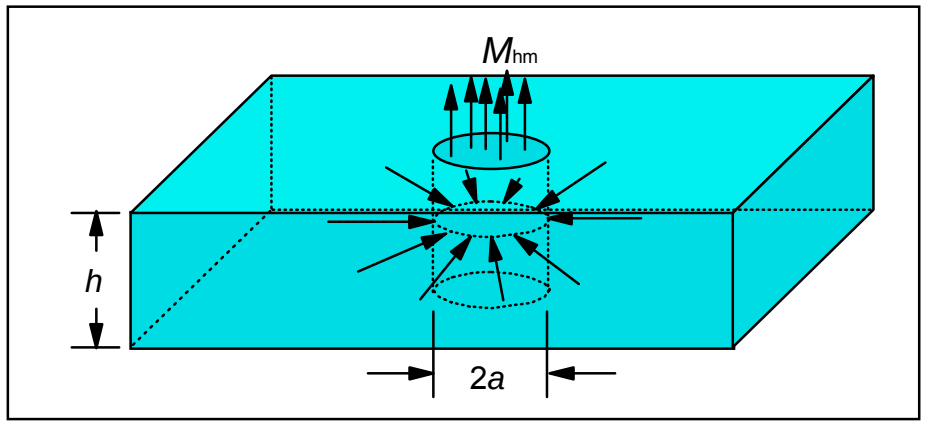
A single hardmask can prevent poisoning for 1st litho, but for 2nd litho (i.e. in dual damascene/inlay) the problem can be aggravated.



Flux Enhancement through Iso Vias

- **Flux through sidewall**

$$J = C_0\sqrt{\frac{D}{\pi t}}$$



- **Total amount diffused out after bake time t_b**

$$M_{\text{hm}} = 2\pi ah\int_0^{t_b} J\,\mathrm{d}t = 4ahC_0\sqrt{\pi Dt_b}$$

- **Amount diffused out of same area in absence of hardmask**

$$M_0 = 2a^2C_0\sqrt{\pi Dt_b}$$

$$\frac{M_{\text{hm}}}{M_0} = 2\left(\frac{h}{a}\right) \approx 10$$

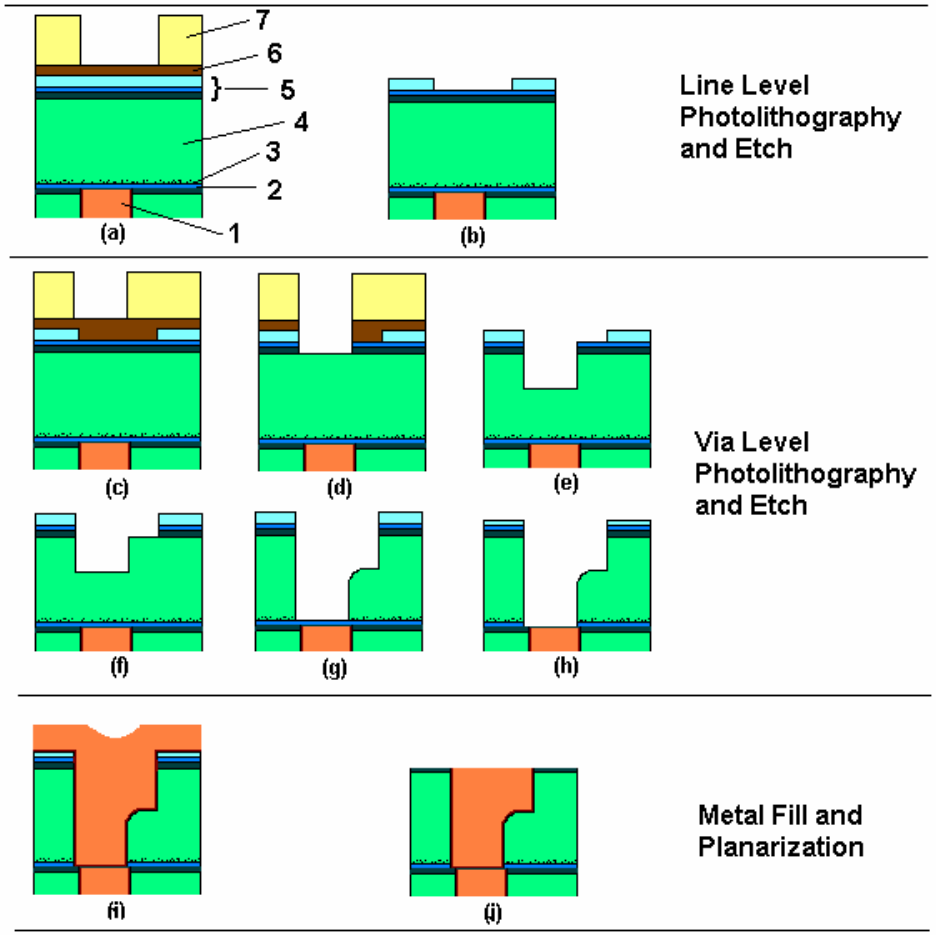
~10x local enhancement of amine flux thru isolated vias

Net

- Low K materials generally require some kind of hardmask integration scheme, not just for resist poisoning issues, but photolithographic rework, plasma damage mitigation ….
- Dual damascene/inlay schemes requires more than a simple, single hardmask
- Some materials require a permanent hardmask for CMP compatibility issues.

Example Dual Damascene Low K Integration Scheme

Multilayer Hardmask Integration Scheme



Key:

1. Lower level wire
2. Etchstop/barrier
3. Adhesion promoter
4. Low-K Dielectric
5. Hardmask stack
6. Anti-reflective coating
7. Photoresist

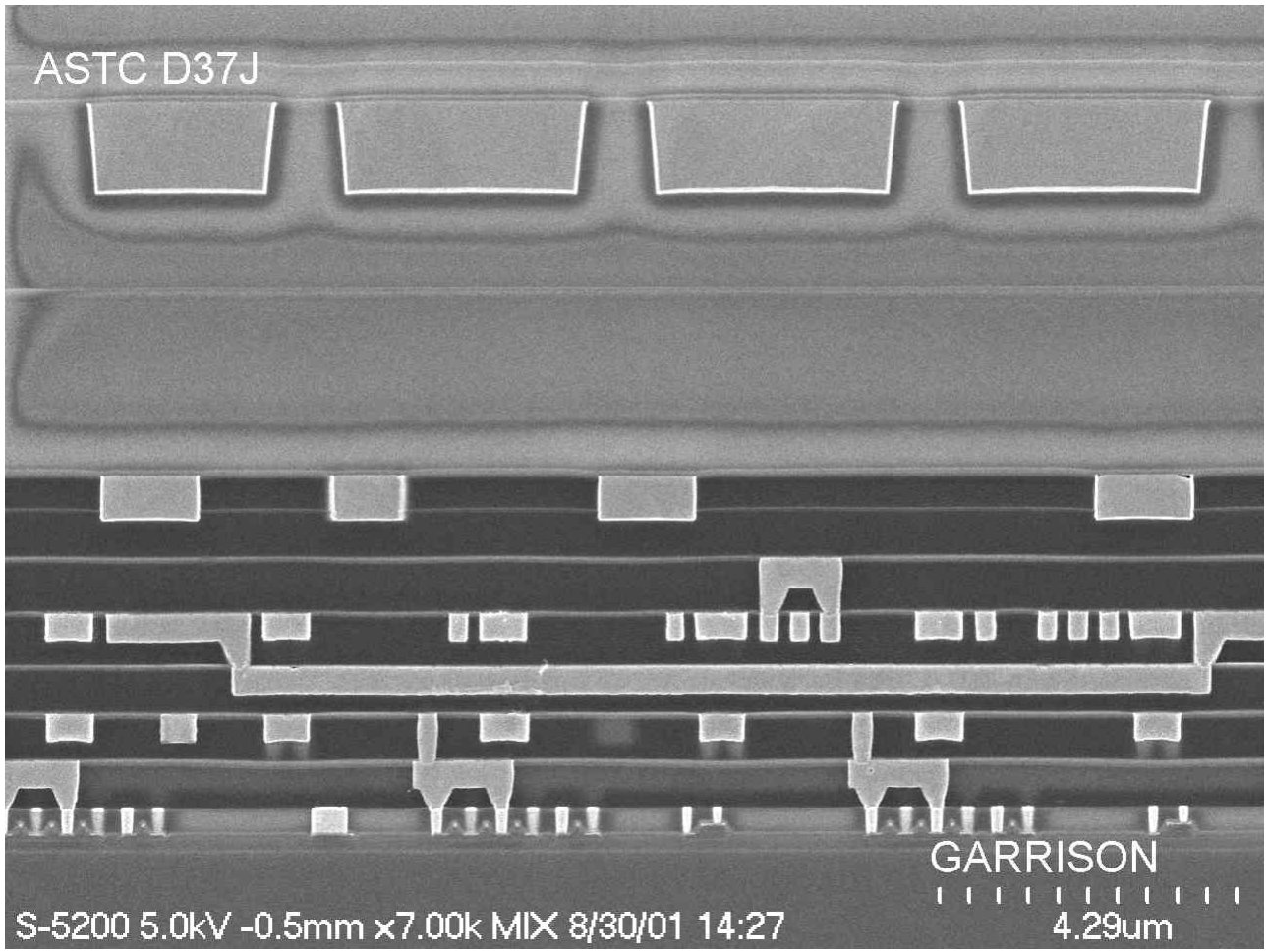
This particular scheme protects

- Litho from Low K
- Low K from ashing
- Low K from CMP

Multilevel Cu/ Low K Built with Hardmask Integration Scheme

Oxide

Low K

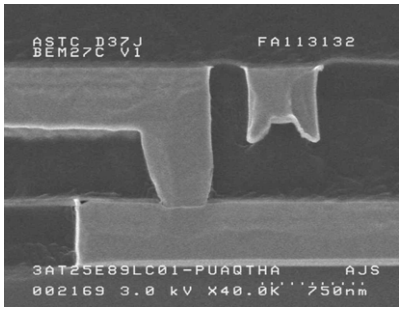


Unit Process Considerations

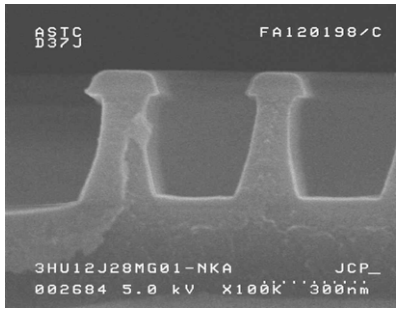
Basic RIE Requirements for Low K

- **Profile control**
  - No undercut, bowing, microtrenching, pitting or other structural anomalies which impact metallization
  - Selective chemistries as needed
- **Minimal ILD damage**
  - Low impact etch and strip chemistries to avoid increase in ILD dielectric constant
- **Minimal residue formation**
  - Any film or residue which needs removal exposes the ILD to potentially damaging plasma or wet chemistries

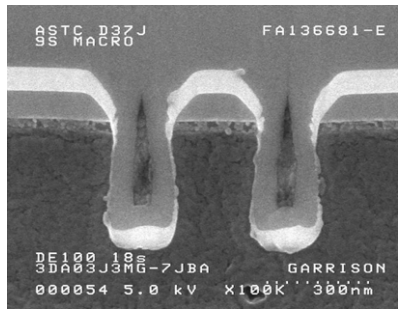
RIE Profile Challenges



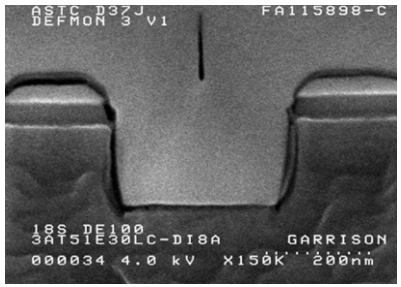
(A) Microtrenching



(B) Undercut

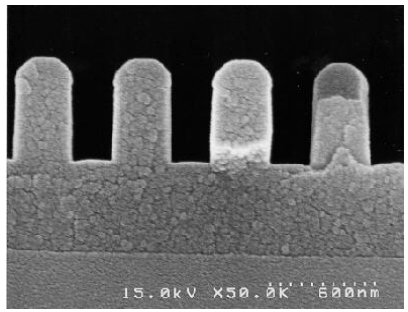


(C) Retrograde



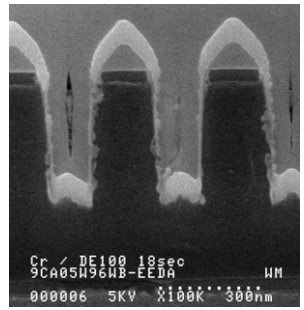
(D) Desired

Tool 1
Chemistry 1



(E) Desired

Tool 1
Chemistry 2



(F) Desired

Tool 2
Chemistry 3

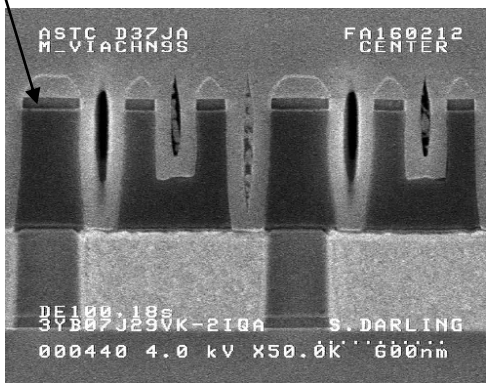
Metal reliability depends on good sidewall coverage.

Basic Metallization Requirements for Low K

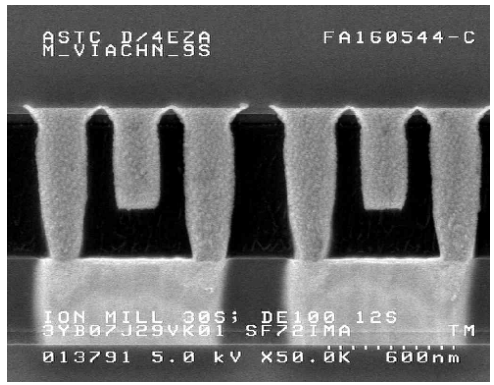
- **Compatibility with ILD**
  - Good adhesion, no penetration into pores if present
- **Continuity**
  - High conformality of liner/seed along all surfaces/interfaces
  - No metal process-induced roughness or profile changes which can impact coverage or downstream processing (e.g. CMP)

Metallization-induced profile changes

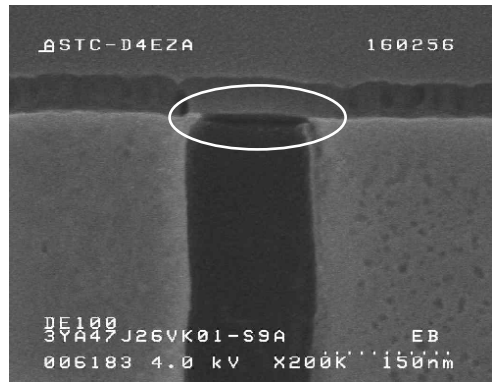
CMP stopping layer



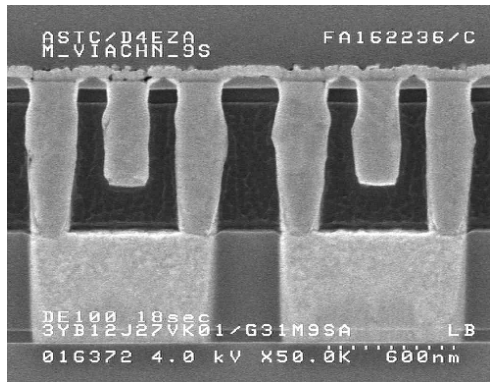
Post-RIE



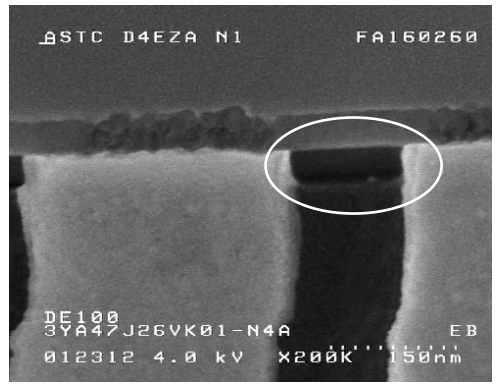
Metal process “A”



Severe Erosion at CMP



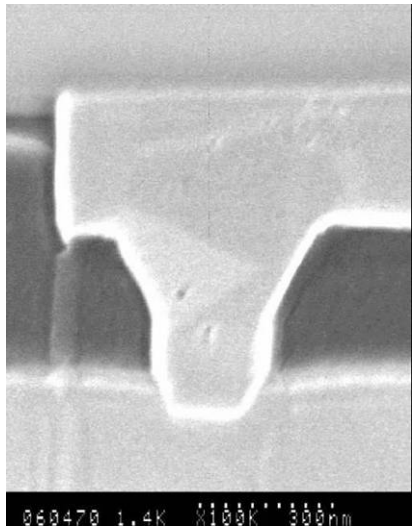
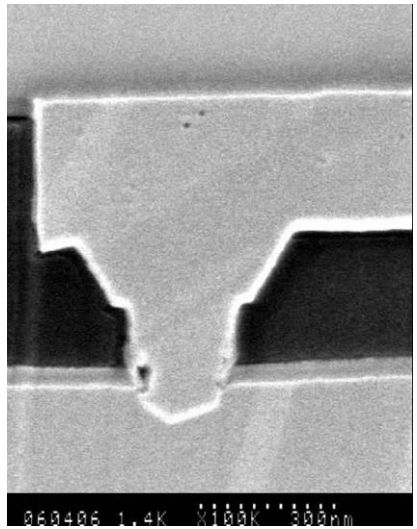
Metal process “B”



Retention

Beyond intrinsic yield and reliability implications, metal process can also influence profiles, impact downstream processing

Process Interactions: Reliability

	RIE Process A	RIE Process B
Test macro construction analysis (unstressed samples)		
Stress Migration Fails @ 1000 hrs	0 %	95 %
Thermal Cycle Fails @ 1000 cycles	0 %	63 %

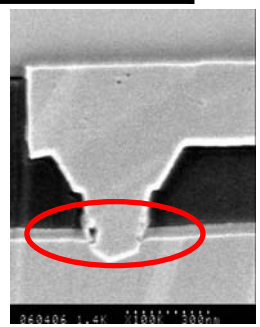
Metal coverage is strongly influenced by RIE Profile

Process Interactions: Reliability (cont.)

Statistical Analysis: Significance of Process Factor Effects

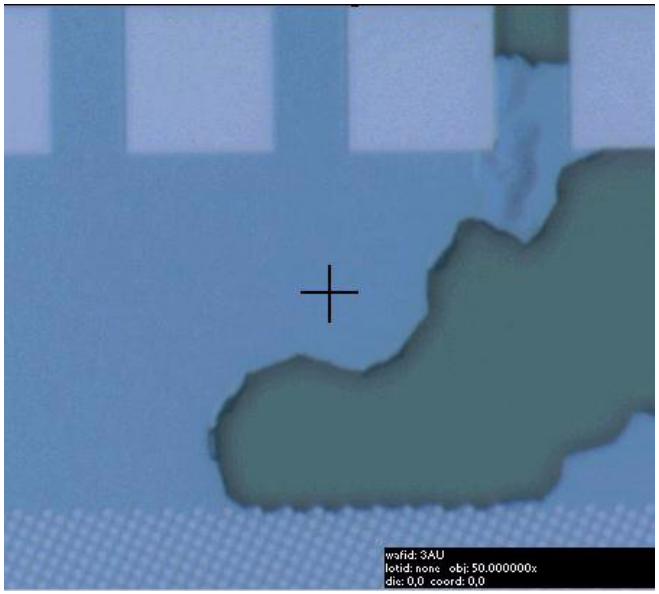
Factor	Significance of Effect	
	Stress Migration	Thermal Cycle
RIE Process	99 %	99 %
Via Etchstop Deposition Process	99 %	< 90%
Metal Liner Deposition Process	-	-
RIE x Via Etchstop Interaction	99 %	95 %

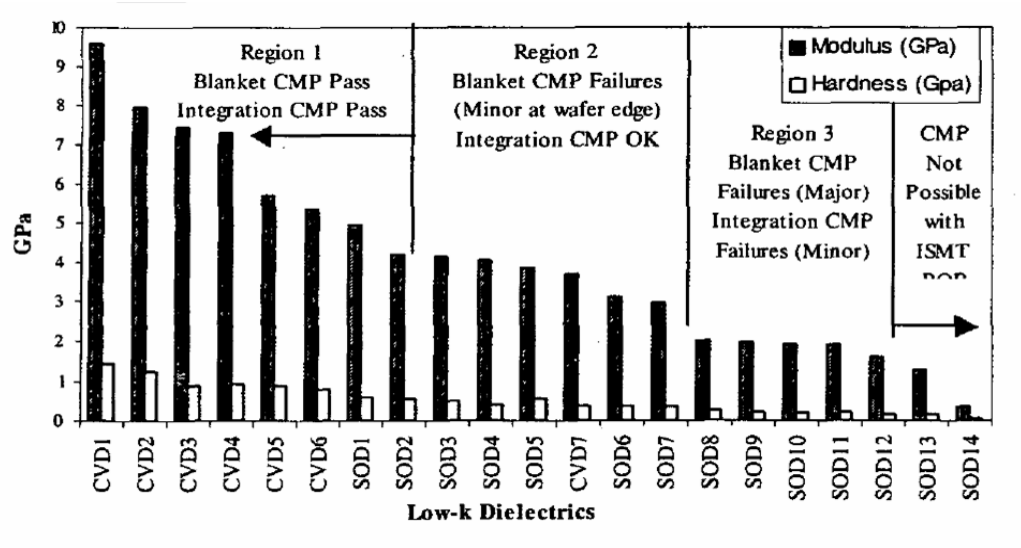
Reliability was not modulated by liner process change, but was strongly influenced by the combination of RIE and Via etchstop deposition processes



CMP

- **CMP-induced failure often observed with low K**
- **In general, the delamination tendency is found to increase with decreasing modulus**





J.E. Wetzel et al. (IEDM 2001)

- **Processes need to scale with modulus**

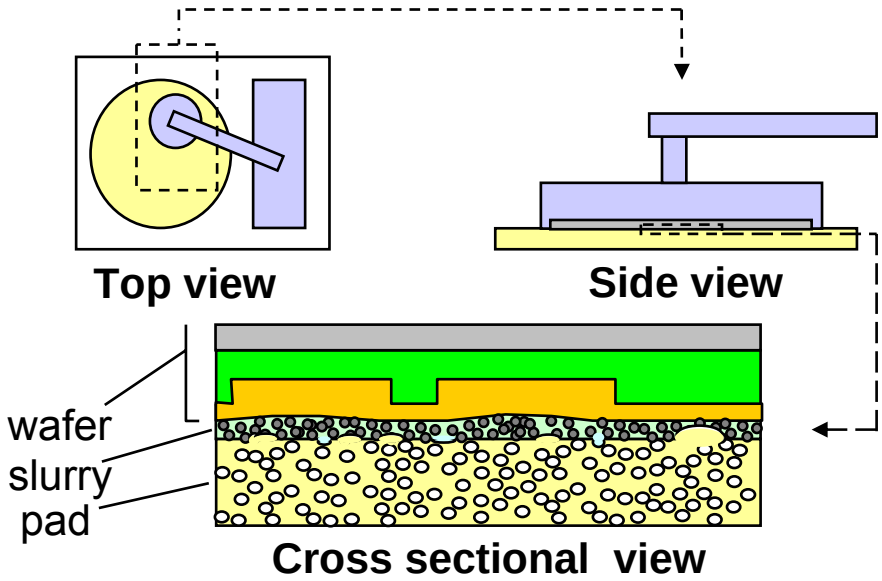
Integration Options for CMP

- **Permanent Hardmask:**
  - Useful for protecting low K films in several process areas, but has disadvantages
    - Reduced performance due to higher K
    - New failure modes (e.g. interfacial adhesion)
    - Process control (e.g. thickness tolerances)
- **Direct CMP:**
  - Most desirable option in terms of process complexity
  - Forces issues of chemical and mechanical compatibility
  - The relatively open structures of low K dielectrics may lead to additional complications, e.g. slurry ingress

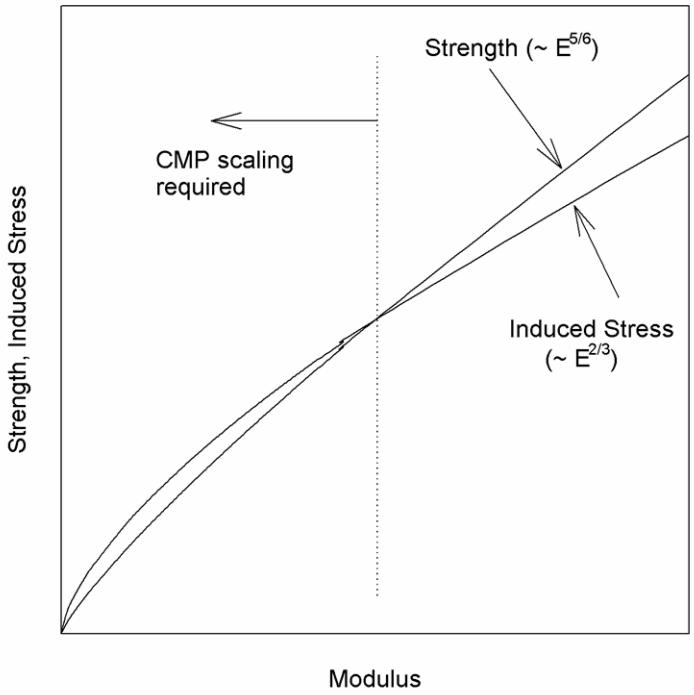
Examine Requirements for Direct CMP…

CMP-Induced Stresses

- **Typical CMP downforce is ~ 5 psi (35 kPa)**
- **Yield strength of ILD is ~1000x → 10,000x greater**
  - organic polymers at low end, SiO_2 at high end
- **CMP-induced damage is therefore related to stress concentration**
  - slurry particles
  - pad asperities
  - wafer edge effects
  - defects



CMP Scaling



- **Contact models indicate that induced stresses scale with the 2/3 power of modulus**
- **Fracture theory predicts that strength scales with the 5/6 power of modulus**
- **Net: there will always be a crossover point where CMP scaling is required**
- **Actual fracture behavior is strongly influenced by environment and design, in addition to ILD properties**

(Additional details in the Appendix)

Metal Deformation in Low K BEOL Processing

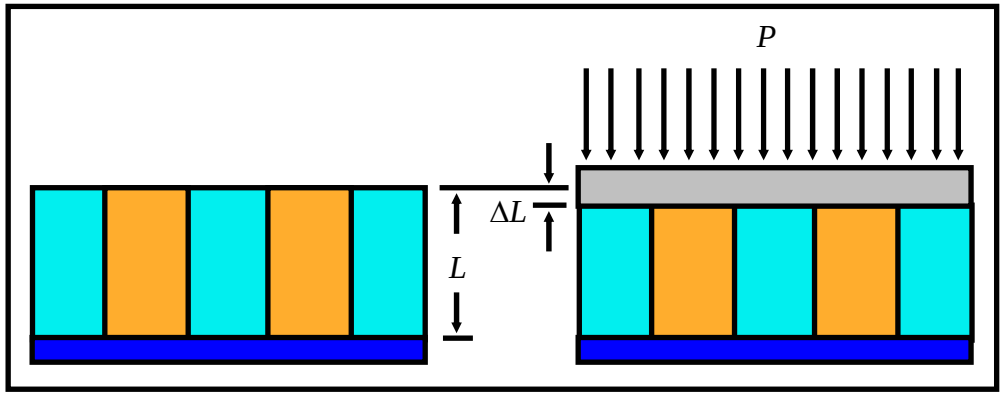
Lower Modulus ILD → Higher Stresses in Cu

- **Higher modulus dielectrics like SiO_2 are able to bear a substantial part of applied loads**
- **As modulus decreases, the interconnects are forced into the role of primary support structure**
- **Loads can be induced by**
  - CMP
  - CTE mismatch of materials
  - Wirebonding
  - Probing

Metal Deformation in CMP

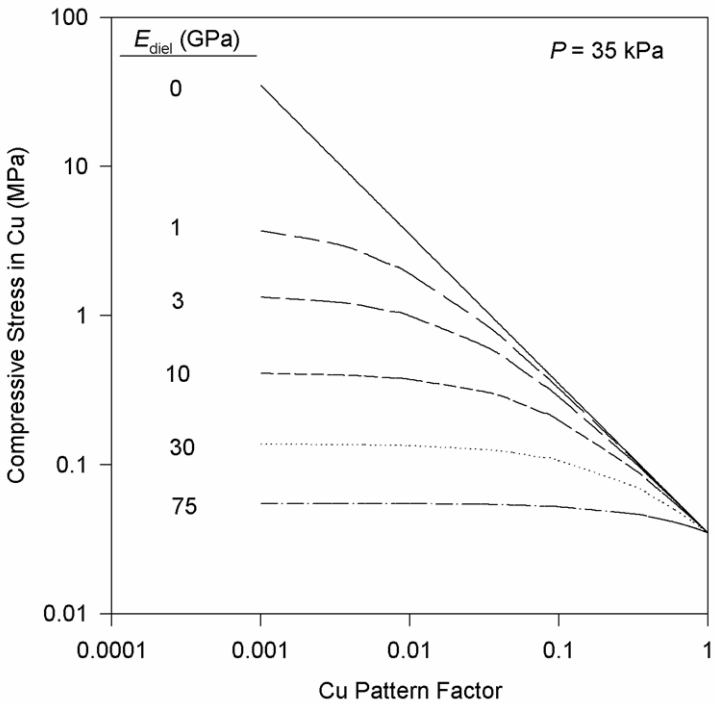
- Simplistic model:
  - ignore liner, hardmask, lateral strain
  - rigid substrate & pad
  - uniform pressure *P*
  - parallel loading
- Rule of mixture:
  - $E_{\text{eff}} = pE_{\text{Cu}} + (1\text{-}p)E_{\text{diel}}$ (p = Cu pattern factor)
- Assume uniform strain

$\varepsilon = \Delta L/L = \sigma_{\text{Cu}}/E_{\text{Cu}} = P/E_{\text{eff}}$



$$\sigma_{\text{Cu}} = P\left(\frac{E_{\text{Cu}}}{pE_{\text{Cu}} + (1-p)E_{\text{diel}}}\right)$$

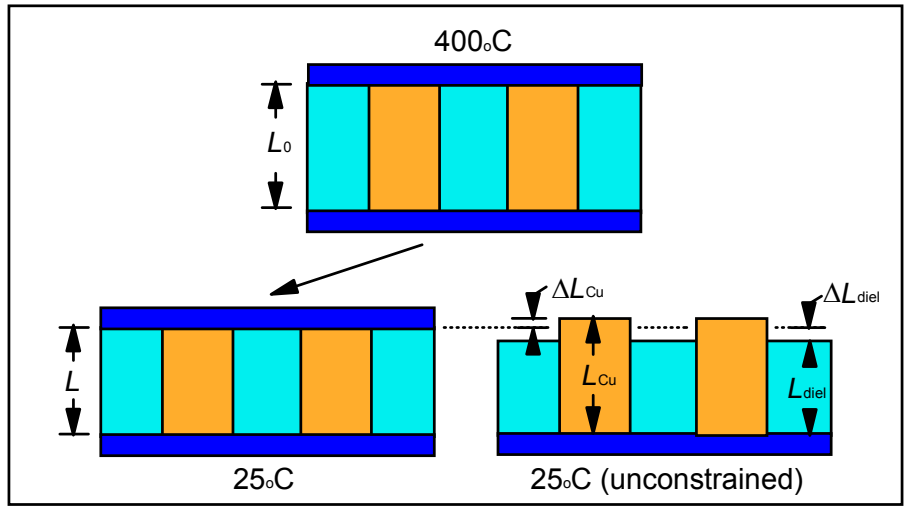
Metal Deformation in CMP (cont.)



- Assume
  - E_{Cu} = 118 GPa
  - P = 35 kPa (5 psi)
- Induced stresses in Cu are predicted to be ~ 1->10 MPa, at low Cu pattern factor, assuming E_{diel} = 3 GPa
- Although this stress is small, yield onset is nevertheless possible for favorably oriented crystals

Metal Deformation from CTE Mismatch

- Simplistic model:
  - ignore liner, hardmask, lateral strain, plastic deformation
  - parallel loading
  - rigid cap & substrate
  - assume zero stress at cap dep temperature (400°C)
- Strain determined by delta from unconstrained thickness at low temp (25°C)
- Final thickness *L* and stresses determined by balance of forces

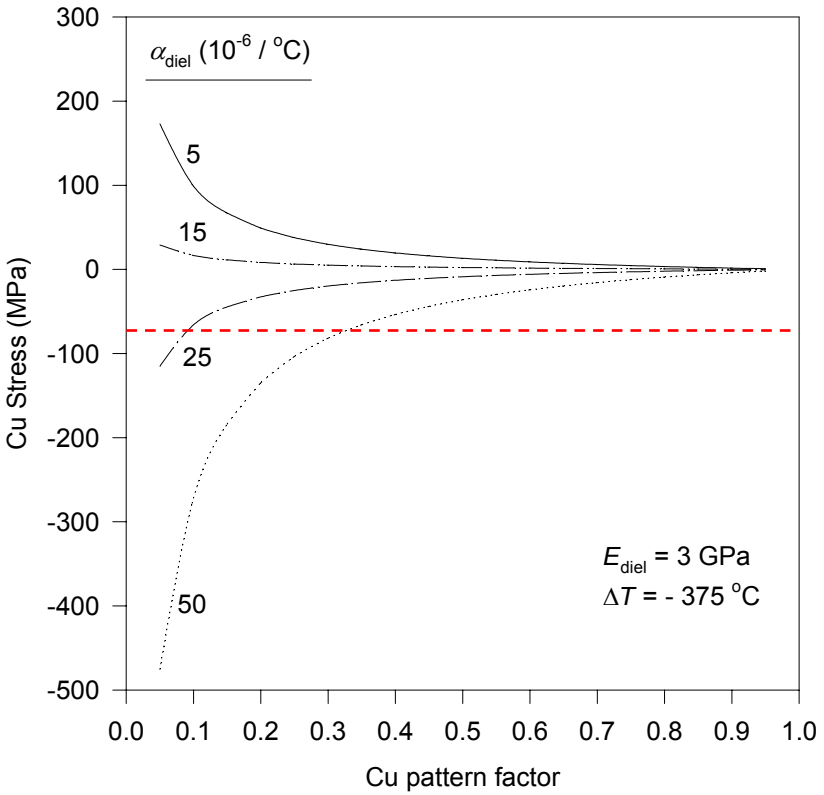


$$\sigma_{Cu} \approx \frac{(1-p)E_{Cu}E_{diel}(\alpha_{diel}-\alpha_{Cu})\Delta T}{pE_{Cu}+(1-p)E_{diel}}$$

p = pattern factor

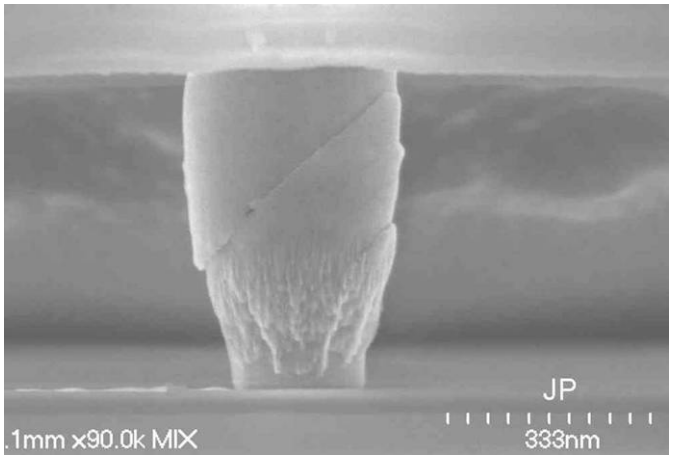
α = coefficient of thermal expansion

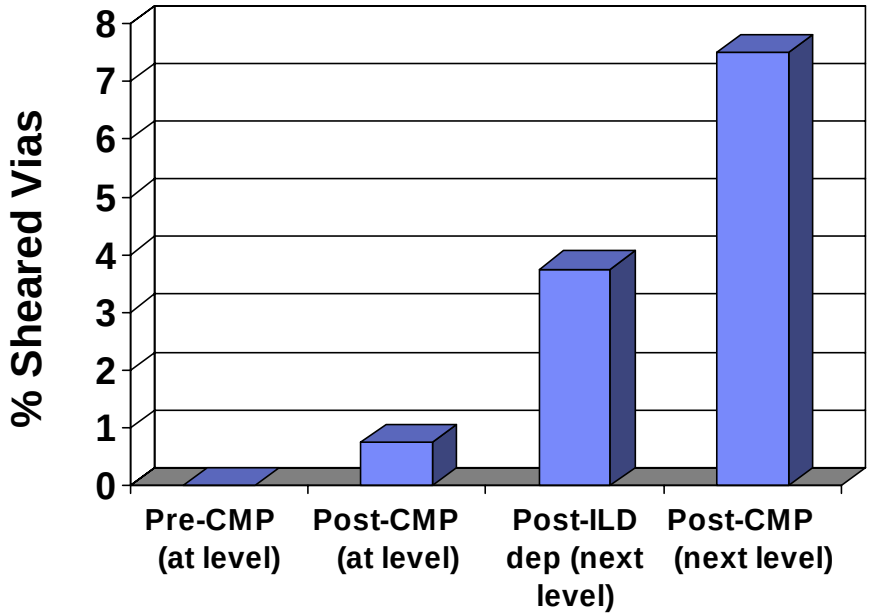
Metal Deformation from CTE Mismatch (cont.)



- Assume
  - α_{Cu} = 17x10^{-6} / °C
  - E_{diel} = 3 GPa
  - ΔT = - 375 °C
- For high thermal expansion films, compressive stresses far in excess of Cu yield stress (~70 MPa) are predicted for even moderate pattern factors
- Isolated vias expected to be especially susceptible to deformation, as observed

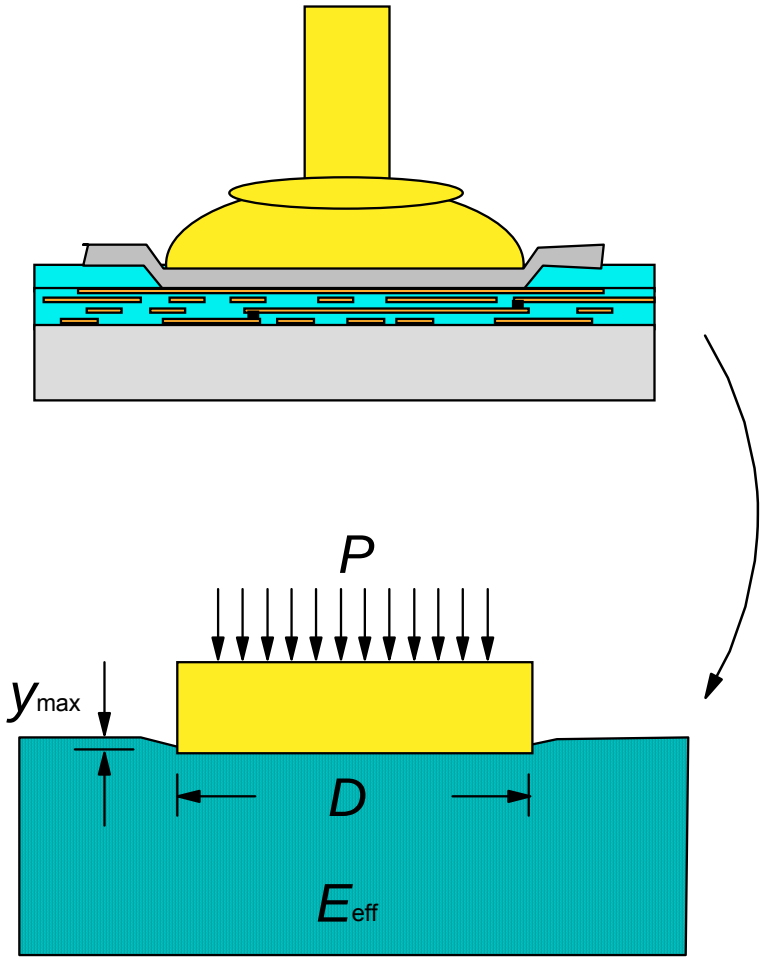
Isolated Via Shear on (111) Cu Slip Plane





- Sheared vias observed after CMP
- Large increase post ILD dep driven by CTE mismatch between Cu and low K
- Defects in isolated via stacks are associated with TC fails (R. Filippi et al., IRPS ’04)
- Shear not observed in nested via stacks

Deformations Induced by Wirebonding



Simplistic, order-of-magnitude estimates:

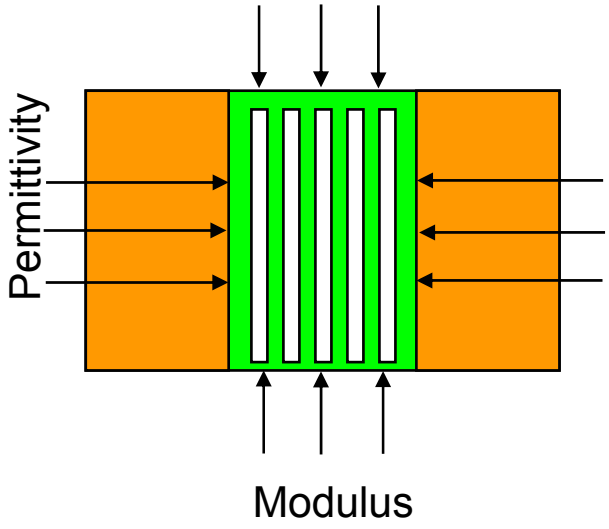
- For 200 mN bond force and D = 50 μm, the load P is ~ 100 MPa
  - on the order of compressive strengths of low K films
- Maximum deformation

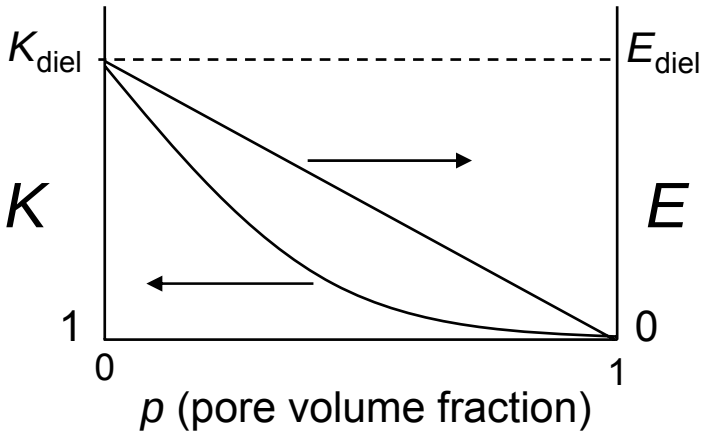
$$y_{\max} = \frac{PD(1-\nu^2)}{E_{eff}}$$

is ~ 0.5 μm for E_{eff} = 10 GPa

- Maximum shear stress (~P/3) at depth d = 0.32D (~15 μm)
  - low-K pullout not unexpected
  - reinforcement needed

Structure and Scaling





- **Ordered porosity can give an optimal combination of mechanical properties and capacitance**
  - During processing, mechanical properties are most important in the direction perpendicular to the wafer
  - During operation, dielectric properties are most important in directions parallel to the wafer surface
- **Example: vertical pores**
  - Modulus rule of mixture

$$E \approx (1-p)E_{diel}$$

  - Permittivity rule of mixture

$$K^{-1} \approx (1-p)K_{diel}^{-1} + p$$

K decreases faster than *E*

Summary

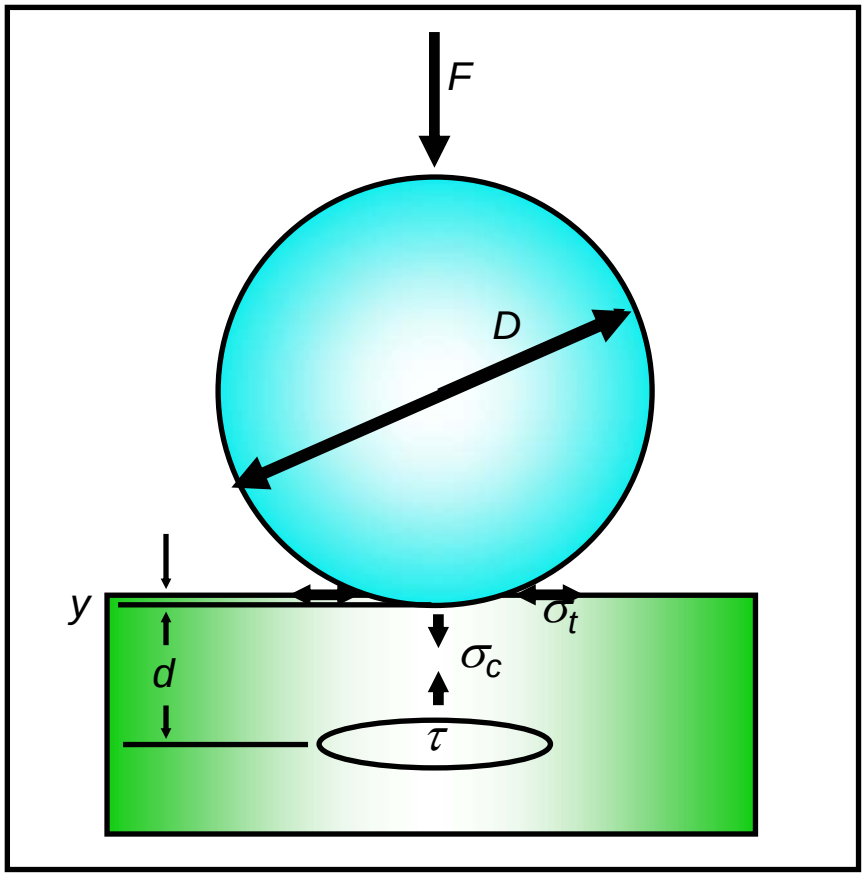
- Lower K implies lower density, modulus, hardness, and strength
- The relatively open structure of Low K materials allows easier transport of moisture and poisoning agents (e.g. amines) as well as greater susceptibility to plasma damage
- Hardmasks – sacrificial, if not permanent – are generally required for integration of Low K
- CMP is especially challenging for Low K - processes need to scale and performance is sensitive to chemical environment and layout, in addition to material properties
- As dielectric modulus decreases, Cu features increasingly bear applied loads and become susceptible to deformation
- Novel structures, e.g. ordered porosity, can achieve improved performance with smaller reductions in effective modulus

Acknowledgements

- **T. Dalton**
- **B. Engel**
- **J. Petrus**
- **E. Levine**

Appendix

Hertzian Contact Stress Model



For a perfectly rigid sphere impinging on a film of modulus E_{film} and Poisson ratio ν_{film}:

- penetration depth

$$y = 1.040\, D \left[C_E \frac{F}{D^2} \right]^{2/3}$$

- maximum compressive stress

$$\sigma_c = 0.918 \left[C_E^{-2} \frac{F}{D^2} \right]^{1/3}$$

where

$$C_E = \frac{1 - \nu_{film}^2}{E_{film}}$$

Induced stresses scale ~ 2/3 power of modulus

Scaling of Strength with Modulus

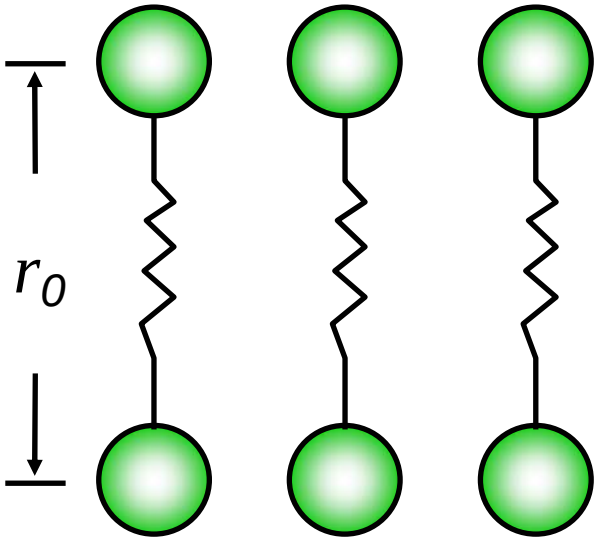
- **Griffith theory**

$$\sigma_f \propto \sqrt{\frac{E\gamma}{c}}$$

σ_f = fracture strength
E = modulus
γ = surface energy
c = flaw size

- **Surface energy is expected to scale with modulus**
  - less bonds to pull ↔ less bonds to break
- **Strength will scale with some effective power of *E***
  - relate γ to *E* through bond density n_B to find scaling law

Spring Model



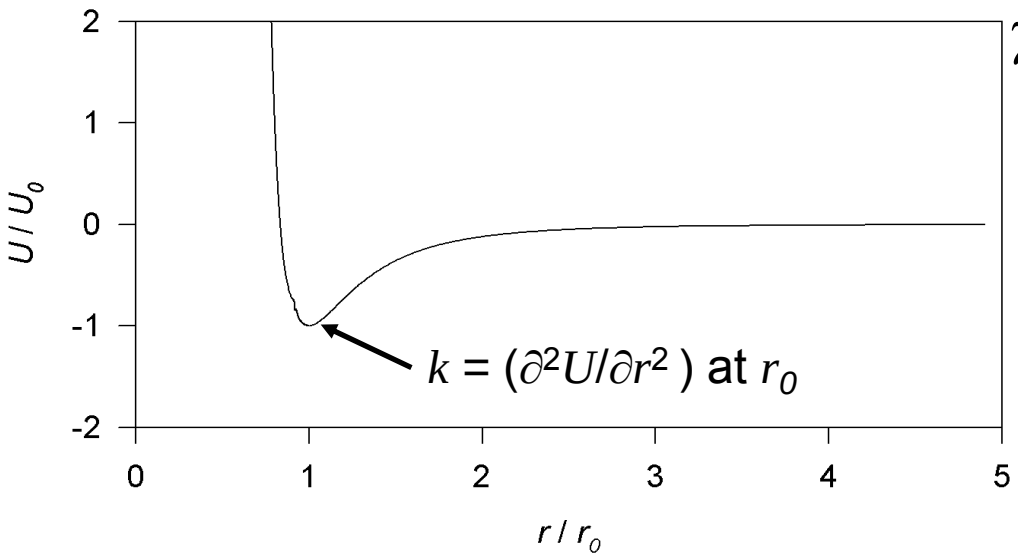
- Potential energy well U_0 at $r = r_0$
- Spring constant k per bond ($E \sim k$)
- n_B bonds per unit volume

$$\gamma = \tfrac{1}{2}\, U_0\, n_B^{2/3}$$

$$E = r_0^2\, n_B\, (\partial^2 U/\partial r^2)$$

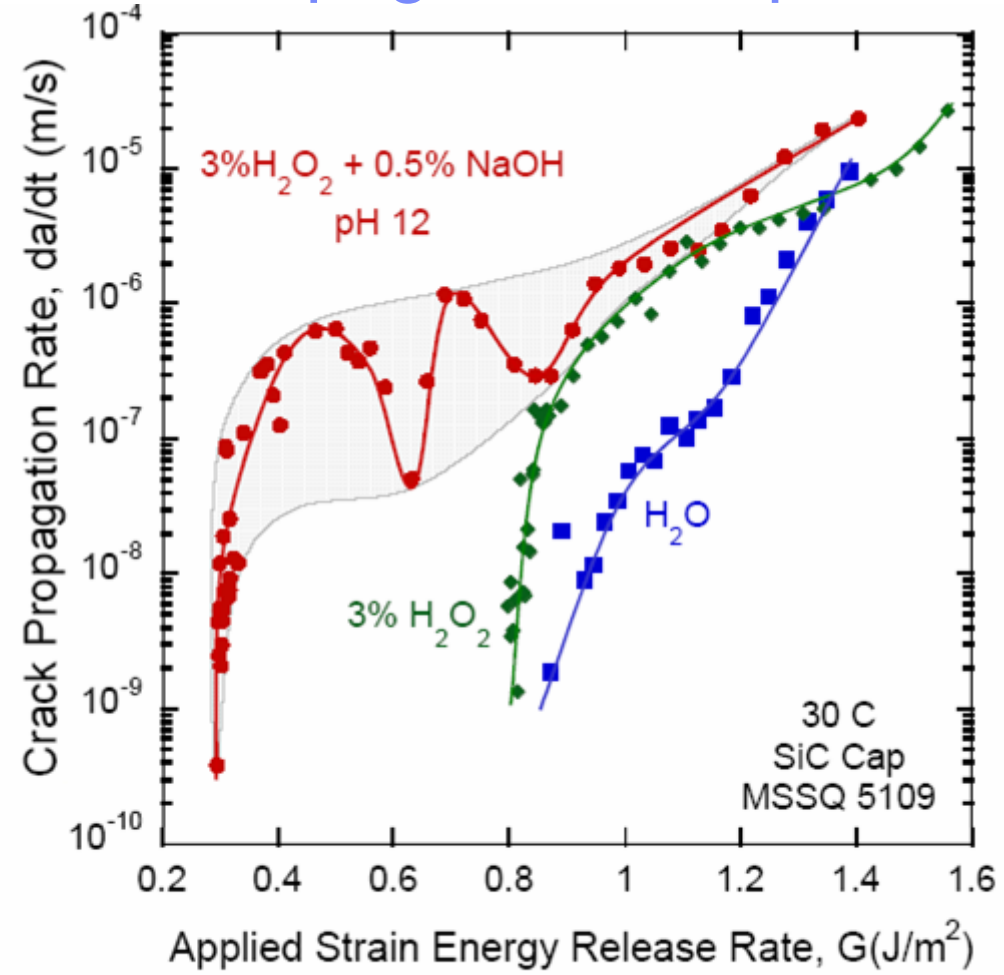
$$\gamma = \tfrac{1}{2}\left[\left(\frac{r_0^2}{U_0}\right)\left(\frac{\partial^2 U}{\partial r^2}\right)\right]^{-2/3} U_0^{1/3}\, E^{2/3}$$

$$\sigma_f \sim E^{5/6}$$



Fracture strength scales ~ as the 5/6 power of modulus

Crack Propagation in Aqueous Environments



The corrosion of MSSQ in H_2O_2 + NaOH solutions allows cracking to extend to extremely low values of G.

E. Guyer and R. Dauskardt (IITC 2004)

- Crack extension force

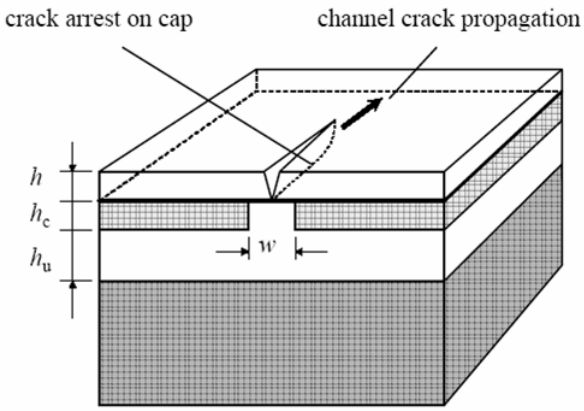
$$G = \sigma^2 h / E_o$$

(soft film of thickness h, stress σ, and plane strain modulus E_o over a stiff substrate)

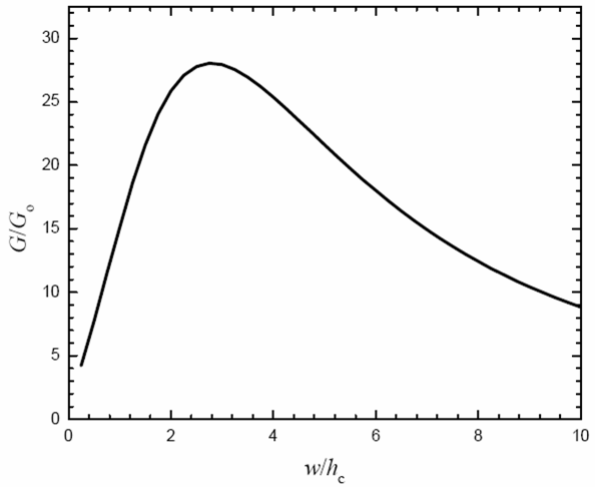
- Critical threshold for cracking depends on solution chemistry through the surface energy, γ

$$G_c = 2\gamma$$

Cracking: Influence of Underlying Pattern

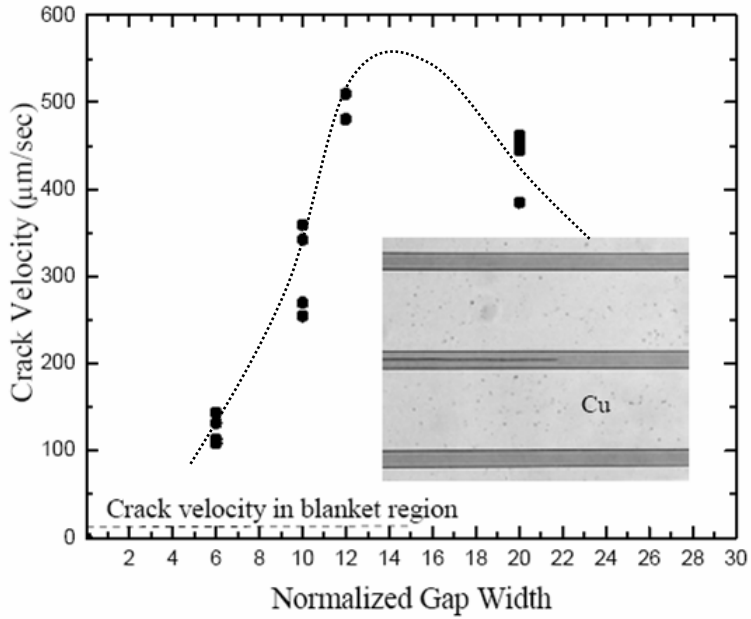


Multi-layer structure of underlying patterned metal and dielectric layers with a channeling crack in the overlayer.



Energy release rate versus the gap width between metal pad

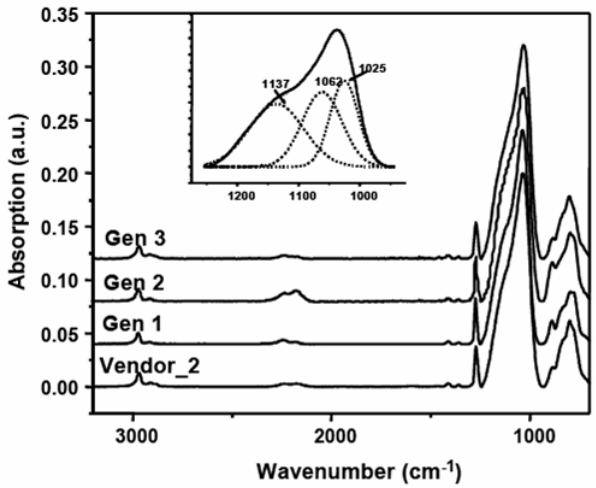
Blanket film data underestimate the actual risk of cracking



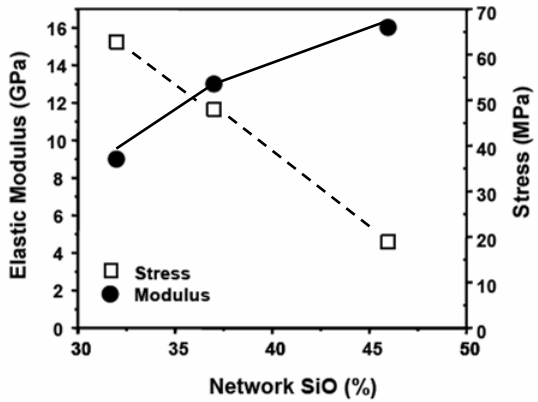
Crack velocity measured at various gap widths. The insert shows a channeling crack in a 3 μm thick dielectric overlayer induced by the presence of a gap between two wide copper plates.

X. Liu et al. (IITC 2004)

Dielectric Deposition: Material Optimization of SiCOH Films

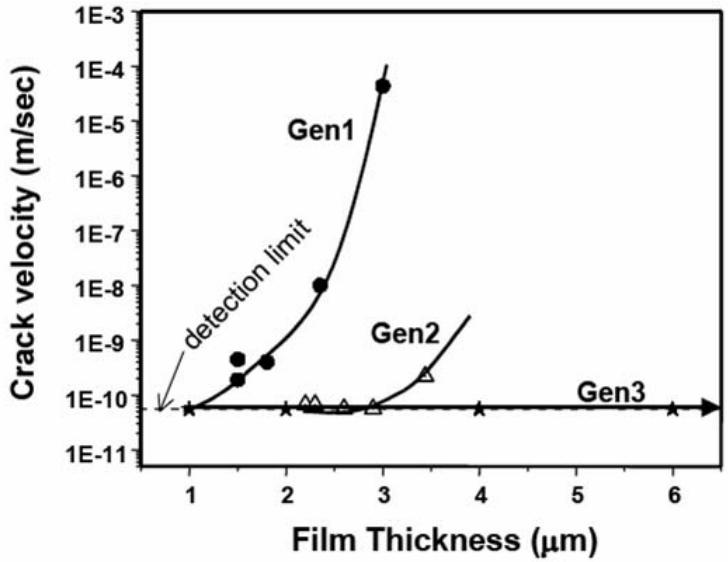


FTIR spectra of four SiCOH films made from



Elastic modulus and stress of SiCOH films vs. fraction of network oxide.

Increasing network vs. cage SiO reduces stress and increases modulus, reducing the driving force for crack propagation



Crack development velocity at 100% humidity

A. Grill et al. (IITC 2004)

