Nanowires of four epitaxial hexagonal silicides grown on Si(001)

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Epitaxial self-assembled silicide nanowires can be grown on Si (001) if the magnitude of the lattice mismatch between epilayer and substrate is large along one crystal axis and small along the perpendicular axis. This phenomenon is illustrated with four examples: $ScSi_2$, $ErSi_2$, $DySi_2$, and $GdSi_2$, which have lattice mismatches of −4.6%, 6.3%, 7.6%, and 8.9%, respectively, along one of the Si ⟨110⟩ directions and mismatches of 0.8%, −1.6%, −0.1%, and 0.8%, respectively, along the perpendicular Si⟨110⟩ direction. The resulting self-assembled nanowires have widths and heights in the range of 3–11 and 0.2–3 nm, depending on the lattice mismatches. The average lengths of the nanowires are in the range 150–450 nm, and are determined primarily by kinetic issues. The epitaxial growth of silicide nanowires should prove interesting to those studying quasi-one-dimensional systems. © *2002 American Institute of Physics.* [DOI: 10.1063/1.1428807]

I. INTRODUCTION

In recent years, tremendous interest has been generated in the fabrication of nanoscale wires.[1] When wire width and height become comparable to characteristic lengths (e.g., electronic wavelength or magnetic domain width), new physical properties are expected that may lead to a new generation of electronic, optoelectronic, and magnetic devices.[2,3] To realize these new properties, the width and height of the wires usually need to be in the single-digit-nanometer scale or even less.[2,3] This regime is very difficult to reach with lithographic methods, particularly when macroscopic amounts are to be fabricated. Natural self-assembly methods become the method of choice, and various techniques have been used to grow quasi-one-dimensional structures on Si, including Ge wires on Si(001),[4] CaF_2 wires on Si(111),[5] In and Ga wires on Si(001),[6] Bi wires on Si(001),[7] PtSi wires on Si(001),[8] Ge wires on Si(113),[9] and Dy and Ho silicide wires on Si(001).[10,11] Each of these linear structures depends on some type of symmetry-breaking phenomenon at the substrate surface to encourage one-dimensional growth along a preferred direction, which can be step edges on vicinal substrates,[4,5] the preferential capture of adatoms onto an oriented string of dangling bonds at a surface,[6,7] or asymmetric strains induced by lattice mismatches between epitaxial materials and substrates.[8–11]

In general, an atomically flat two-dimensional epitaxial layer can be grown when the lattice constant of the epilayer matches that of the substrate on which it is grown. When there is a significant lattice-mismatch (>2%) between epilayer and substrate, the lattice mismatch will limit the lateral growth. For a system with symmetrical lattice mismatch, e.g., Ge on Si(001) and InAs on GaAs(001), the strain energy in the deposited film can be relaxed by the creation of islands (or dots) of the epitaxial material.[12] Based on these observations, we proposed a strategy for the intentional epitaxial growth of nanowires; choose an epilayer that is closely lattice matched to the substrate along one major crystallographic axis but has a significant lattice mismatch along the perpendicular axis.[13] In principle, this should allow the unrestricted growth of the epitaxial crystal in the first direction but limit the width in the other. The asymmetrical linear growth was first observed in Dy silicides grown Si(001), although the asymmetric lattice mismatch between the Dy silicide and Si(001) were not realized as the reason to cause the asymmetric growth.[10] By applying this principle to the $ErSi_2$/Si(001) system, which has perpendicular lattice mismatches of 6.3% and −1.6%, we have observed self-assembled $ErSi_2$ nanowires with widths of a few nanometers and lengths of a few hundred nanometers. The formation of similar nanowires have also been reported in Dy and Ho silicides grown on the Si(001) surface.[11] In order to extend this principle to different systems and to control the sizes of nanowires by an appropriate choice of the large and small lattice mismatches, we have reviewed the crystal structures and binary phase diagrams of all the compounds listed in Refs. 14 and 15. Those stable compounds that satisfy the requirements for forming nanowires on Si(001) are shown in Fig. 1. All but two of the compounds ($ScSi_2$ and YSi_2) are rare earth "disilicides," and all have the hexagonal AlB_{2-x} crystal structure except for $TmSi_{2-x}$, which has the orthorhombic BCr structure. Detailed thermodynamic and structural studies have determined that these silicides are usually silicon deficient by ~3%–20%.[16–18] Thin silicide films with the AlB_2 structure grown on Si(001) usually have their $(1\bar{1}00)$ plane parallel to the Si(001) plane, and their [0001] axis along one of the Si⟨110⟩ axes in the silicide/Si interface.[19–21]

Thin films of these disilicides display a wide range of interesting electronic properties. Those that have been measured are metallic conductors with resistivities in the range 10^{-5}–10^{-4} Ω cm[21–23] and form contacts to *n*-type (*p*-type) silicon with a very low (high) Schottky barrier.[22,24] They have been proposed for applications in metal-base transis-

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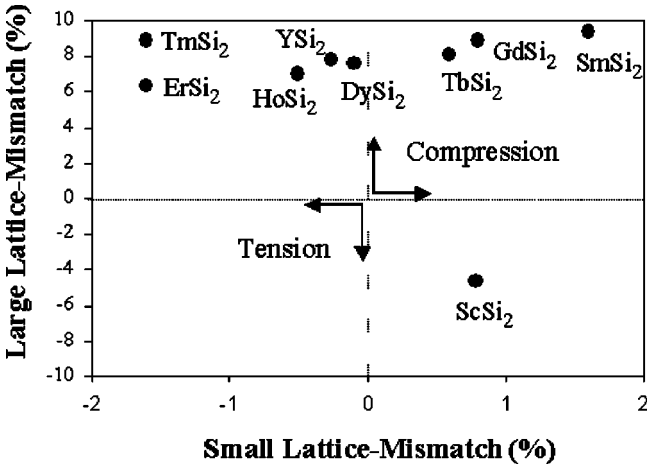

FIG. 1. Diagram showing lattice mismatches of silicides that have a large absolute value lattice mismatch between 4% and 10% and a small lattice mismatch within ±2%, with respect to Si(001) along two perpendicular $\langle 110\rangle_{Si}$ directions.

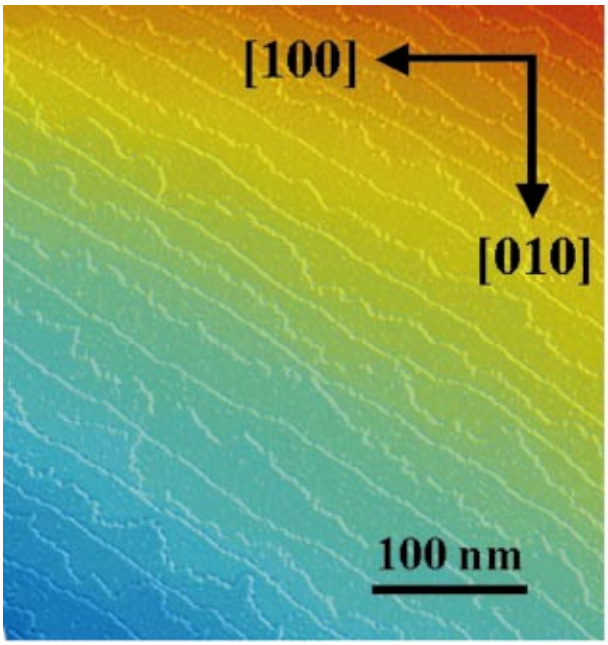

FIG. 2. (Color) STM topograph (400 nm×400 nm) showing a clean Si(001) surface. The substrate slopes downward from top right to bottom left with terraces of different heights (in the order of red, green, blue). The single atomic steps primarily oriented along the $[\bar{2}10]$ direction.

tors, tunable infrared detectors, and ohmic contacts in conventional microelectronics. Reducing the silicides from bulk or thin film form to one-dimensional nanowires should provide a fascinating field of study for new physical properties, and may have important implications for nanoscale technology. Here we report on the growth and structural characterization of four different silicides that form self-assembled nanowires on Si(001): $ScSi_2$, $ErSi_2$, $DySi_2$, and $GdSi_2$, which have large lattice mismatches (−4.6%, 6.3%, 7.6%, and 8.9%, respectively) along one of the $\langle 110\rangle_{Si}$ directions and much smaller lattice mismatches (0.8%, −1.6%, −0.1%, and 0.8%, respectively) along the perpendicular $\langle 110\rangle_{Si}$ direction. We chose these four silicides to represent the various magnitudes and signs of lattice mismatch evident in Fig. 1, as well as their interesting physical properties.[21–24] This work is a first step toward rational epitaxial nanowire fabrication and structure modification for future systematic measurements of physical properties correlated to structure.

II. EXPERIMENTAL PROCEDURE

In our experiments, device quality "flat" Si(001) substrates were prepared by heating to 1200 °C for about 20 seconds in an ultrahigh vacuum (UHV) chamber with a pressure $<1\times10^{-9}$ Torr. Prior to deposition, the surface structures of the substrates were investigated *in situ* with an Omicron scanning tunneling microscope (STM) with a pressure $<2\times10^{-10}$ Torr to examine the nature of the steps on the starting surface and to ensure they were clean. Scandium, erbium, dysprosium, and gadolinium were then deposited on the substrates with an *in situ* electron-beam evaporator with the thickness monitored by an internal flux meter that was calibrated *ex situ* by Rutherford backscattering spectrometry. The substrate temperatures during depositions ranged from room temperature to 620 °C. The deposition times ranged from a few seconds to 7 min, yielding coverages of the rare-earth elements on Si(001) up to ~0.5 monolayer (ML). After a deposition, the samples were annealed at temperatures ranging from 600 to 800 °C for a few minutes to ensure that all the deposited metal had reacted with silicon. The surfaces of the samples and the silicide nanowire structures were then investigated again with the STM.

III. EXPERIMENTAL RESULTS

Figure 2 is a typical STM image of a clean and annealed Si(001) substrate before deposition. The well-known "2×1" reconstructed surface structure can be observed on Si(001) terraces between single atomic steps. As measured from the STM images, the average terrace widths along $[110]_{Si}$ and $[1\bar{1}0]_{Si}$ were 57.8 and 21.3 nm, respectively, implying that the normal direction of the surface of the Si substrate used in our experiments was misoriented from $[001]_{Si}$ toward $[120]_{Si}$ by ~0.4°.

The final state of the nanowires was influenced by their growth conditions, such as deposition and annealing temperature, deposition rate, coverage of deposited atoms, and annealing time. The physical properties of Sc, Er, Dy, and Gd are similar (e.g., their melting points are 1539, 1522, 1409, and 1314 °C, respectively), and the experimentally determined growth conditions for producing dislocation-free nanowires are also very close. The optimum substrate temperature and time for defect-free nanowire growth were ~575–620 °C and ~2–5 min, respectively. When the annealing temperature and/or time exceeded these ranges, dislocations were introduced into the silicide crystals to relieve the lattice-mismatch strain, leading to the coarsening and fragmentation of the nanowires.[25] When the annealing temperature and/or time fell below the optimum ranges, the reaction between the deposited metal and Si substrate was incomplete, and the nanowires remained in their early stages of growth. The amount of deposited metal was usually ~0.05–

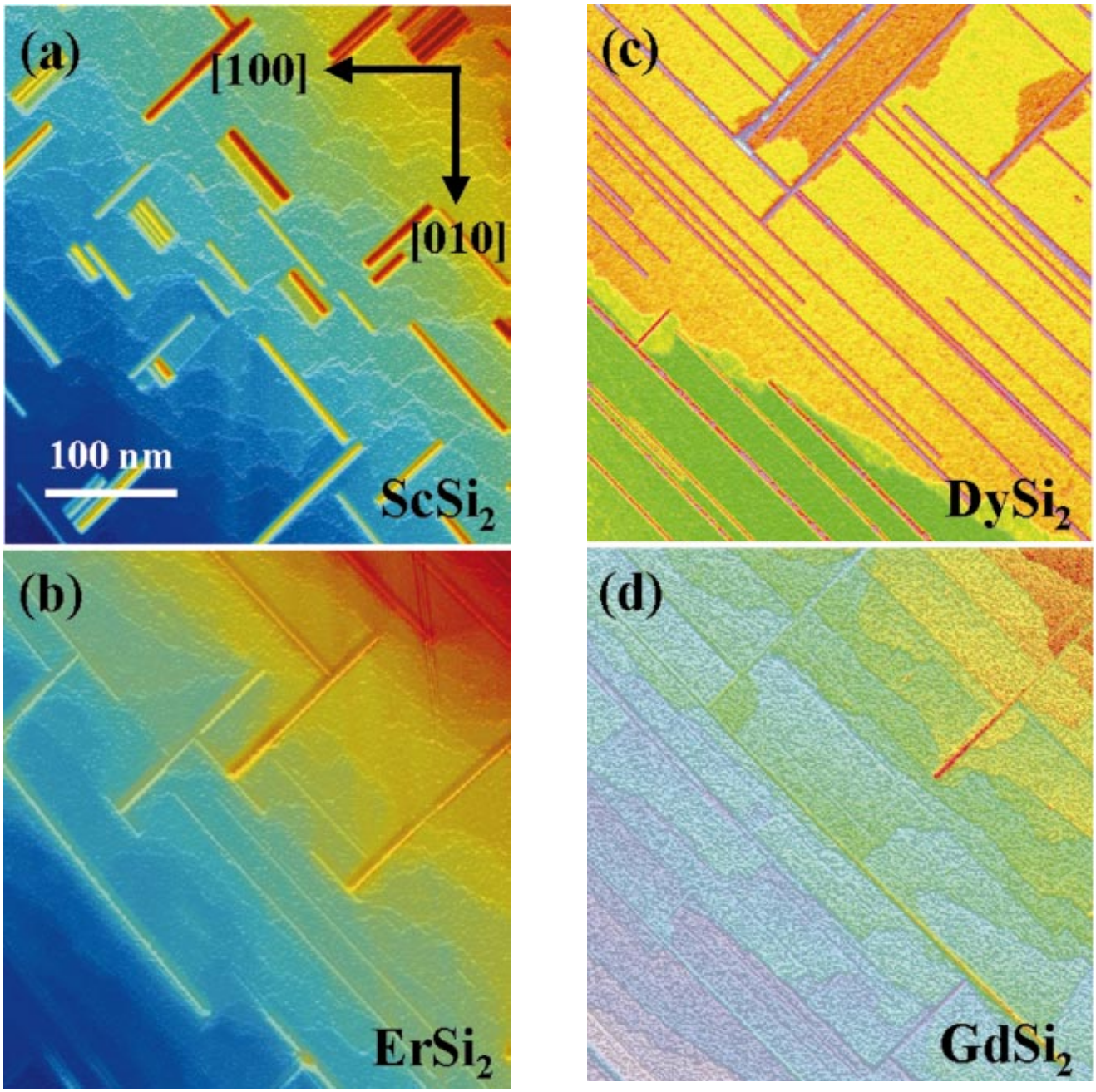

FIG. 3. (Color) STM topographs (400 nm×400 nm) showing (a) $ScSi_2$, (b) $ErSi_2$, (c) $DySi_2$, and (d) $GdSi_2$ nanowires grown on Si(001) surface shown in Fig. 2. The substrate slopes downward from top right to bottom left with terraces of different heights (in the order of red, green, blue) and are often separated by single atomic steps, but many step bunches can be observed near the ends of the nanowires.

0.5 ML. When the coverage fell below this range, only randomly distributed atomic clusters were formed; when the coverage exceeded this range, coarsening and intersection of the nanowires resulted in the formation of silicide meshes or even continuous thin films. The detailed kinetic study of $ErSi_2$ nanowires under various growth conditions has been presented elsewhere.[25] Here we focus on how the structures of different silicide nanowires depend on lattice mismatch under their optimum growth conditions.

Typical STM images of $ScSi_2$, $ErSi_2$ $DySi_2$, and $GdSi_2$ nanowires grown on ''flat'' Si(001) substrates typical of Fig. 2 are shown in Figs. 3(a)–3(d), respectively. For these samples, the metals were deposited on Si substrates at 600 °C for 2 min, yielding coverages of ~0.35 ML Sc, ~0.20 ML Er, ~0.25 ML Dy, and ~0.28 ML Gd. After the deposition, the samples were then annealed at 600 °C for 2 more min. Nanowires aligned along one of the two perpendicular $\langle 110 \rangle_{Si}$ directions can be observed on all four samples. The wires are straight and do not follow or terminate at single Si atomic steps, but rather the steps form a zig–zag pattern with significant step bunching that locally follows the nanowires.

The widths and heights of the different silicide nanowires varied significantly because of their different lattice mismatches with respect to the Si substrate. The average dimensions of the $ScSi_2$, $ErSi_2$, $DySi_2$, and $GdSi_2$ nanowires shown in Fig. 3 were measured from STM images with

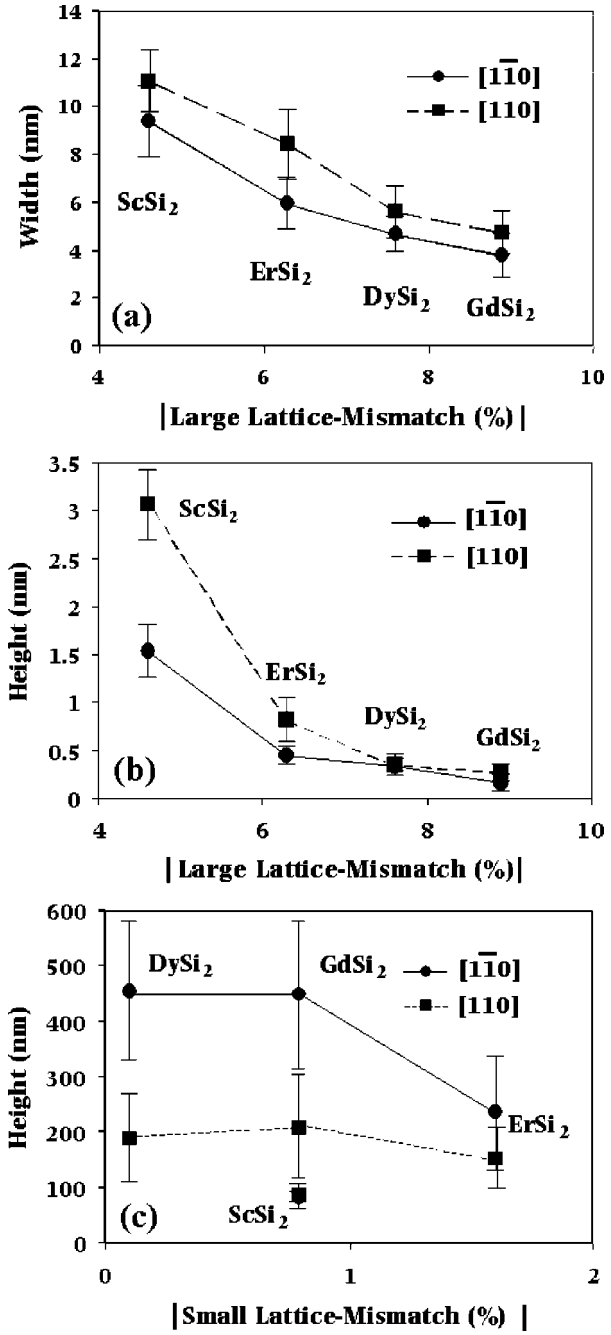

FIG. 4. (a) Average widths vs large lattice mismatches, (b) average heights vs large lattice mismatches, and (c) average lengths vs small lattice mismatches, respectively, of $ScSi_2$, $ErSi_2$, $DySi_2$, and $GdSi_2$ nanowires along $[110]_{Si}$ and $[1\bar{1}0]_{Si}$ directions, respectively. The variation ranges of the nanowire sizes are shown by error bars, which represent standard deviations ($\pm\sigma$) of the data.

higher magnification, and are shown as a function of the appropriate lattice mismatch in Fig. 4. As shown in Figs. 4(a) and 4(b), the average widths and heights of the nanowires decreased monotonically as the absolute values of the lattice mismatches along the width direction increases. However, there was no simple relation between the average lengths of the nanowires and the lattice mismatches along the length direction, as shown in Fig. 4(c).

High-resolution STM images of $ScSi_2$, $ErSi_2$, $DySi_2$, and $GdSi_2$ nanowires are shown in Fig. 5. The lattice spacings on all the nanowire surfaces along their length directions agree with the value of the atomic spacing along $\langle 110\rangle_{Si}$ directions on the Si(001) surface, 0.384 nm, within the measurement uncertainties. The observed periodic structures on the top surfaces of the nanowires agree well with a "$2\times n$" reconstruction of a slightly distorted silicide surface, where n varies for the different silicides, and thus the silicide lattices appear to be elastically strained to fit the Si substrate in the width direction. No dislocations were observed in the STM images of the nanowires grown under the growth conditions specified above. The top and the edges of the nanowires are usually atomically smooth except for occasional point defects (mainly vacancies). The lattice mismatch also influenced the shape of the nanowires. As shown in Fig. 5(a), the $ScSi_2$ nanowires usually have a trapezoidal cross section with sidewall slopes in the range 15°–21°. For the silicides in compression, the nanowires have larger width to height ratios with a $(1\bar{1}00)$ plane defining the top surface, but their shape does change with increasing lattice mismatch. The $ScSi_2$, $ErSi_2$, and $DySi_2$ nanowires always grew on the top of a Si terrace, but some sections of $GdSi_2$ nanowires grew into a Si terrace and appeared to be slightly below the level of the surrounding Si as detected by STM [Fig. 5(d)].

Figure 6 displays the wide variety of $GdSi_2$ nanowire environments, which provide some clues for the nanowire growth. Some atoms were observed to align into atomic strings, as labeled A1–A4, which may be the nuclei for $GdSi_2$ nanowires. The strings were single or double atomic rows with lengths less than 15 nm. They were distributed randomly along the two perpendicular $\langle 110\rangle_{Si}$ directions on the Si terraces (A1 and A2) or at Si step edges (A3 and A4). The nanowires themselves were always oriented along one of the two perpendicular $\langle 110\rangle_{Si}$ directions and based on a single terrace. They could grow entirely on the top of a Si terrace (e.g., the nanowire B1). When the end of a growing nanowire approached a Si step, it did not change direction to follow the original Si step edge, but rather the step conformed to the nanowire (e.g., the Si step along the nanowire C1) and/or retreated from the advancing nanowires (Si steps at the end of the nanowires C3 and C4). Such step/nanowire interactions were also observed for $ScSi_2$, $ErSi_2$, and $DySi_2$ (see Fig. 3). However, $GdSi_2$ nanowires were unique in that when some approached Si steps, they could cut into the higher Si terrace and form sections of $GdSi_2$ nanowire embedded within the terraces (e.g., nanowires C1–C4). In this case, the apparent height sensed by STM of the nanowire was lower than the surrounding Si.

III. DISCUSSION

The size and shape of the self-assembled nanowires is strongly influenced by their asymmetric lattice mismatches with respect to the Si lattice. All the silicides studied here have the AlB_2 hexagonal crystal structure.[14–21] Based on the known crystallographic orientation of silicide thin films with respect to a Si(001) substrate and the interfacial structures proposed in Ref. 13, the relative orientations of the bulk atomic structures of the silicide and Si crystals are illustrated in Fig. 7. $ScSi_2$, $ErSi_2$, $DySi_2$, and $GdSi_2$, have large lattice

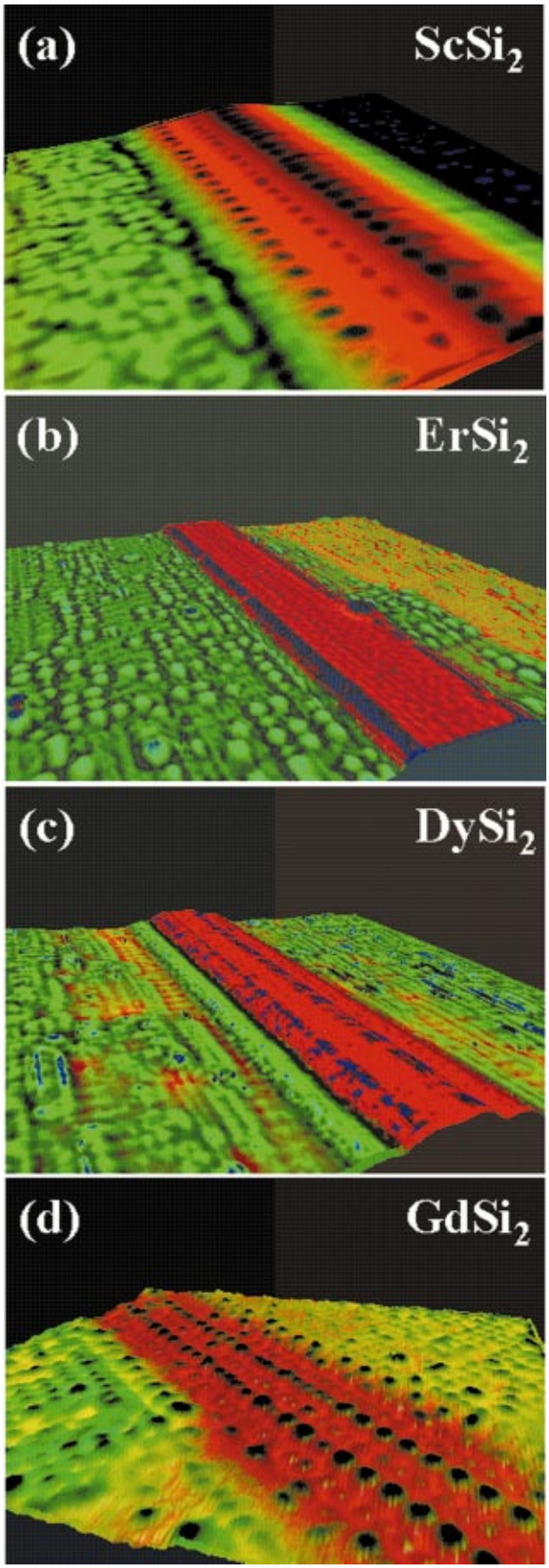

FIG. 5. (Color) High-resolution STM topographs showing sections of (a) a $ScSi_2$ nanowire (width: 13.05 nm, height: 1.79 nm), (b) an $ErSi_2$ nanowire (width: 4.69 nm, height: 0.70 nm), (c) a $DySi_2$ nanowire (width: 4.83 nm, height: 0.56 nm), (d) a $GdSi_2$ nanowire (width: 3.27 nm, height: −0.05 nm, below the Si terrace), as determined by STM, which responds to both geometrical and electronic structure differences.

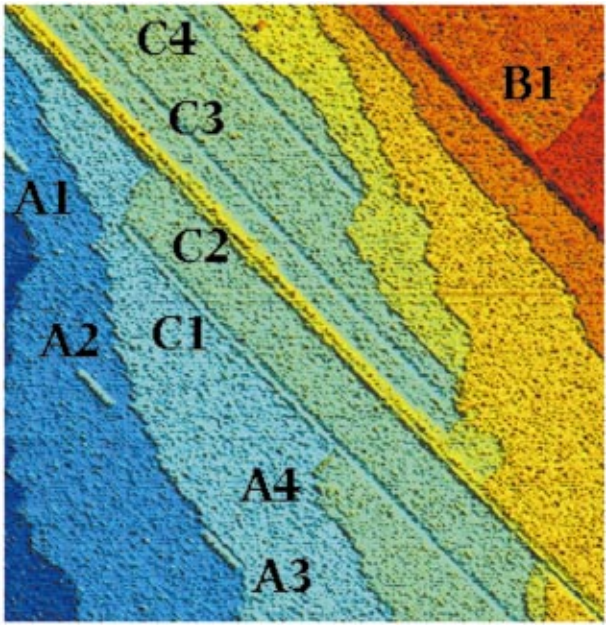

FIG. 6. (Color) STM topograph (200 nm×200 nm) showing $GdSi_2$ nanowires grown on Si(001). The substrate slopes downward from top right to bottom left (in the order of red, green, blue) with Si terraces of different heights separated by single atomic steps. The short silicide atomic strings are marked by A1–A4. The nanowire B1 is on the top of a Si terrace. The top left sections of the nanowires C1 and C2 are on the top of the lower Si terraces, while the bottom right sections impinge into Si terraces. The sections of nanowires C3 and C4 shown here are completely incorporated within their Si terraces.

mismatches (−4.6%, 6.3%, 7.6%, and 8.9%, respectively) along $[0001]_{\text{silicide}}$ and one of the $\langle 110\rangle_{\text{Si}}$ directions and much smaller lattice mismatches (0.8%, −1.6%, −0.1%, and 0.8%, respectively) along the perpendicular $[11\bar{2}0]_{\text{silicide}}$ and $\langle 110\rangle_{\text{Si}}$ directions. To minimize the strain energy, the silicide crystals grow preferentially along the $[11\bar{2}0]_{\text{silicide}}$ direction, leading to the formation of elongated silicide wires.

The tendency for the asymmetric growth increases with the large lattice mismatch along the width ($[0001]_{\text{silicide}}$) direction increasing in the order of $ScSi_2$, $ErSi_2$, $DySi_2$, and $GdSi_2$, resulting in the widths and heights of the nanowires

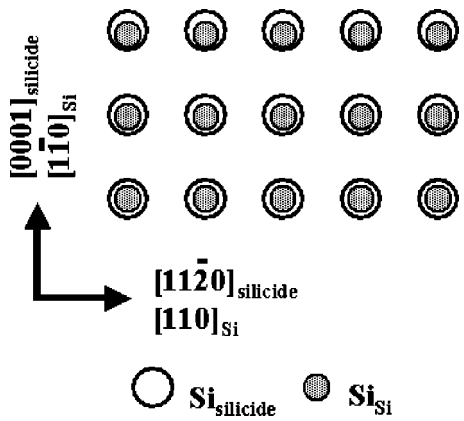

FIG. 7. Schematic diagram illustrating the projected relative positions of Si atoms in a silicide with an AlB_2 structure and in an unreconstructed Si(001) surface (not drawn to scale). At an actual interface, the silicide atoms locating next to the interface will be strained.

decrease monotonically with increasing absolute value of the large lattice mismatch along the width ($[0001]_{silicide}$) direction (see Fig. 4). Since strain energy is proportional to the square of the lattice mismatch, one might naively expect the length to width aspect ratio of the nanowires to vary with the square of ratio of the large to the small lattice mismatch for each silicide. However, there is no such correlation, and Fig. 4(c) shows that there is not a strong relationship between small lattice mismatch and average nanowire length. In fact, $ScSi_2$ appears to lie well outside the behavior of the other silicides when considering nanowire length, which may be related to the fact that this silicide is in tension rather than compression in the width direction.

Although it is energetically favorable to form silicide nanowires by the reaction between deposited metal adatoms and Si atoms on the substrate, kinetically this reaction must break Si–Si bonds at the substrate surface. High temperatures and/or long annealing times can ensure complete reaction of the metal, but dislocations will be introduced into the silicide crystals to relieve the lattice mismatch strain. The introduction of dislocations into the epitaxial nanocrystals relieves the asymmetric lattice mismatch, resulting in coarsening and/or fragmentation of the nanowires. Since, the optimum temperature window for dislocation-free nanowire growth is relatively low, 575–620 °C, the most likely source of Si atoms to react with the deposited metal is step edges, because of the lower number of Si–Si bonds.[13,25] The arrangement of the nanowires and Si steps after growth indicates that when the leading end of a growing nanowire approaches a Si step, the step retreats from the advancing nanowire. The original Si steps are deformed to conform to the nanowires, which creates a ''snowplow'' effect, causing successive step edges to bunch up ahead of the nanowire (see Figs. 3 and 6). The average terrace widths on the Si(001) substrate before deposition along $[110]_{Si}$ and $[1\bar{1}0]_{Si}$ were 57.8 and 21.3 nm, respectively, and all the steps were one atom high (see Fig. 2). The average lengths of the nanowires along $[110]_{Si}$ and $[1\bar{1}0]_{Si}$ [see Fig. 4(c)] were significantly longer (except for $ScSi_2$, which were only slightly longer) than the original terrace widths along $[110]_{Si}$ and $[1\bar{1}0]_{Si}$, respectively, which demonstrates that the growth of the nanowires cannot be limited by a single Si atomic step. The growth of the nanowires is either terminated by intersecting a perpendicular nanowire or by reaching a step bunch that is too large to dissociate. The $GdSi_2$ nanowires only have average heights of 0.16 and 0.26 nm along $[110]_{Si}$ and $[1\bar{1}0]_{Si}$, respectively (as measured from the nanowires and/or nanowire sections grown on the top of the Si terraces). During the growth, they can advance into a higher Si terrace [see Figs. 5(d) and 6], since the consumption of local Si atoms at the leading end of a growing $GdSi_2$ nanowire within its width can supply enough Si atoms for its growth. This phenomenon was not observed in $ScSi_2$, $ErSi_2$, and $DySi_2$ nanowires, which are thicker and therefore need to detach more Si atoms from the nearby Si step edges for their growth.

IV. SUMMARY

$ScSi_2$, $ErSi_2$, $DySi_2$, and $GdSi_2$ have appropriate asymmetric lattice mismatches with respect to Si(001) substrates to form self-assembled epitaxial nanowires. The lattice mismatches along the width direction of the $ScSi_2$, $ErSi_2$, $DySi_2$, and $GdSi_2$ nanowires increased in this order, and the average widths and heights of the nanowires decreased in this order. The silicides shown in Fig. 1 provide a wide range of lattice mismatches, and alloys between them should provide the ability to fine tune the lattice mismatches to obtain desired nanowire widths. The lengths of the nanowires are determined largely by kinetic issues, which must be studied further to extend wire length. These epitaxial nanowires may provide interesting systems for the study of the electronic properties of one-dimensional systems.

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