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Nanoscale molecular-switch crossbar circuits

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Abstract

Molecular electronics offer an alternative pathway to construct nanoscale circuits in which the critical dimension is naturally associated with molecular sizes. We describe the fabrication and testing of nanoscale molecular-electronic circuits that comprise a molecular monolayer of [2]rotaxanes sandwiched between metal nanowires to form an 8×8 crossbar within a 1 μm^2 area. The resistance at each cross point of the crossbar can be switched reversibly. By using each cross point as an active memory cell, crossbar circuits were operated as rewritable, nonvolatile memory with a density of 6.4 Gbits cm^{-2}. By setting the resistances at specific cross points, two 4×4 subarrays of the crossbar were configured to be a nanoscale demultiplexer and multiplexer that were used to read memory bits in a third subarray.

In order to realize functional nano-electronic circuits, researchers need to solve three problems: invent a nanoscale device that switches an electric current on or off; build a nanoscale circuit that controllably links very large numbers of these devices with each other and with external systems in order to perform memory and/or logic functions; and design an architecture that allows the circuits to communicate with other systems and operate independently of their lower-level details. At the device level, researchers in molecular electronics have achieved significant progress recently, demonstrating tunnelling junctions [1, 2], devices with negative differential resistance [3], electrically configurable switches [4–6] and transistors made from a single carbon nanotube [7, 8] or a single molecule [9, 10]. At the circuit level, devices have been connected together to separately perform basic memory [4, 5, 11] and logic [4, 6, 11–14] functions. Architectural issues are still in the early stages, but designs suitable for nano-electronic circuits have been discussed and patented [15–17].

To satisfy all three of the above requirements, we have proposed nanoscale circuits based on a configurable crossbar architecture to connect molecular switches [15–17] in a two-dimensional grid (as shown schematically in figure 1(a)). A crossbar has several advantages. First, the wire dimensions can be scaled continuously down to molecular sizes, while the number of wires in the crossbar can be scaled up arbitrarily to form large-scale generic circuits that can be configured for memory and/or logic applications. Second, it requires only $2N$ communication wires to individually address 2^N nanowires with a demultiplexer [17], which allows the nano-circuit to communicate efficiently with external circuits and systems, for example, CMOS. Third, it is a reconfigurable architecture that can tolerate defective elements generated during the nanofabrication process [15]. Fourth, the simple physical structure of the crossbar makes nanoscale fabrication feasible and potentially inexpensive.

Imprint lithography is a new nanoscale processing technique that can produce sub-10 nm feature sizes with high throughput and low cost [18]. In addition, imprinting may also preclude damage to sensitive circuit components, including active molecules, in contrast to the high-energy electrons

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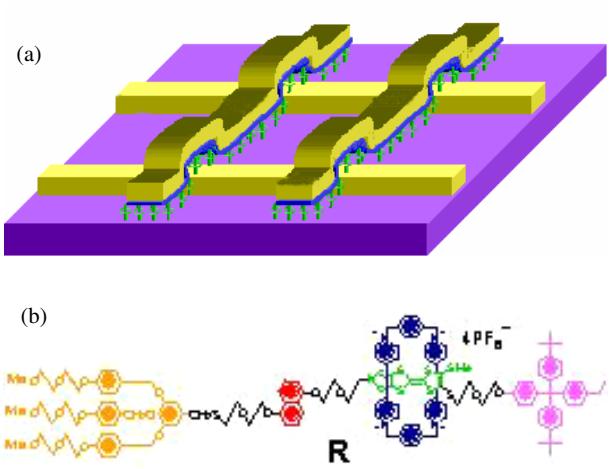

Figure 1. (a) Schematic representation of the crossbar circuit structure. A monolayer of the [2]rotaxane (green) is sandwiched between an array of Pt/Ti nanowires (gold, left–right) on the bottom and an array of Pt/Ti nanowires (gold, up–down) on the top. Before the fabrication of the top nanowires, the entire molecular monolayer is covered with a Ti protective layer, which is etched away anisotropically by using the top nanowires as an etch mask, leaving the Ti layer (blue) and molecules under the top Pt nanowires intact (details described in the appendix). (b) Molecular structure of the bistable [2]rotaxane **R**. The molecule has a hydrophobic (purple) and a hydrophilic (orange) stopper. The [2]rotaxane has cyclobis(paraquat-*p*-phenylene) (dark blue) as the ring component and the supporting counterions are hexafluorophosphate.

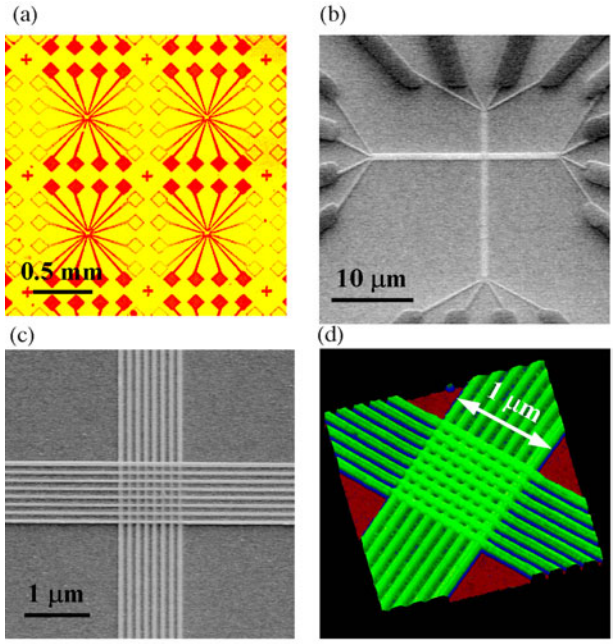

Figure 2. (a) An optical microscope image of an array of four out of 625 test circuits, showing that each has 16 contact pads with micron-scale connections leading to nanoscale circuits in the centre. (b) A SEM image showing two mutually perpendicular arrays of nanowires connected to their micron-scale connections; (c) a SEM image showing that the two sets of nanowires cross each other in the central area; (d) a 3D AFM image of the crossbar.

utilized in e-beam lithography. We have previously developed an inexpensive process to fabricate nanoscale devices and circuits utilizing imprint lithography [19, 20]. Individual molecular cross-point devices incorporating an amphiphilic bistable [2]rotaxane (figure 1(b)) sandwiched between two metal nanowires were shown to act as reversible, electrically toggled switches [20]. In this paper, we focus on nanoscale crossbar circuits comprising devices made from the same rotaxane molecules by the same process. We demonstrate how these many-device crossbars can be configured to be extremely high-density memory circuits, and then how they can be reconfigured to function as a demultiplexer to integrate memory and logic functions.

The crossbar circuits, shown schematically in figure 1(a), were fabricated by imprint lithography with the process outlined in the appendices and described in detail elsewhere [19, 20]. A monolayer of the [2]rotaxane molecules was sandwiched between bottom Ti(3 nm)/Pt(5 nm) and top Ti(11 nm)/Pt(5 nm) nanowires. The basic element in the circuit is the Pt/rotaxane/Ti junction formed at each cross point, that acts as a reversible and nonvolatile switch, and 64 such switches are connected to form a 8 × 8 crossbar circuit within a 1 μm^2 area. The structure of the amphiphilic bistable [2]rotaxane **R** that we have used in this work is shown in figure 1(b). The molecule consists of two mechanically interlocked components: a dumbbell encircled by a ring [21, 22]. The large stoppers—one hydrophobic and the other hydrophilic—at either end of the central shaft make the molecules amphiphilic, and also produce a large area per molecule in a monolayer film.

Optical microscope, scanning electron microscope (SEM) and atomic force microscope (AFM) images of representative crossbar circuits and their test structures are shown in figure 2. In order to achieve nanometre lateral resolution in the AFM image, a carbon nanotube tip (ProbeMax) was used. The nanowires have a measured width of ∼40 nm, which is consistent with the measured width of the nanowire templates on the imprint mould. The active device area at each cross point of the circuit was thus ∼1600 nm^2, corresponding to ∼1100R molecules sandwiched between the two electrodes as determined from the known density of the molecules on the surface of the Langmuir trough before they were transferred to the substrate.

The 8 × 8 crossbar circuits were first tested as 64-bit random access memories at room temperature under ambient conditions. During the test, all 16 nanowires in a circuit were electrically addressed simultaneously via their corresponding contact pads and a matching probe card on an Electroglas 1034X probe station. A computer-controlled switching matrix connected voltage sources to each nanowire and a current meter to a selected output nanowire. Figure 3(a) is a schematic diagram showing the test configuration for the writing and reading modes of the memory (see details in the appendices). In order to write one bit at a cross point (e.g. (1, A) in figure 3(a)), the corresponding row and column of the crossbar were selected by applying a voltage pulse of amplitude V on the top nanowire (row A in figure 3(a)) and grounding the bottom nanowire (column 1 in figure 3(a)). Ideally, to prevent accidental writing of other bits, a voltage pulse of amplitude $V' = V/2$ should be applied to all other rows and columns simultaneously (see the appendices for details of the actual measurements performed). Initially a voltage pulse with a duration of 0.5 s and an amplitude V of 3.5 V was applied

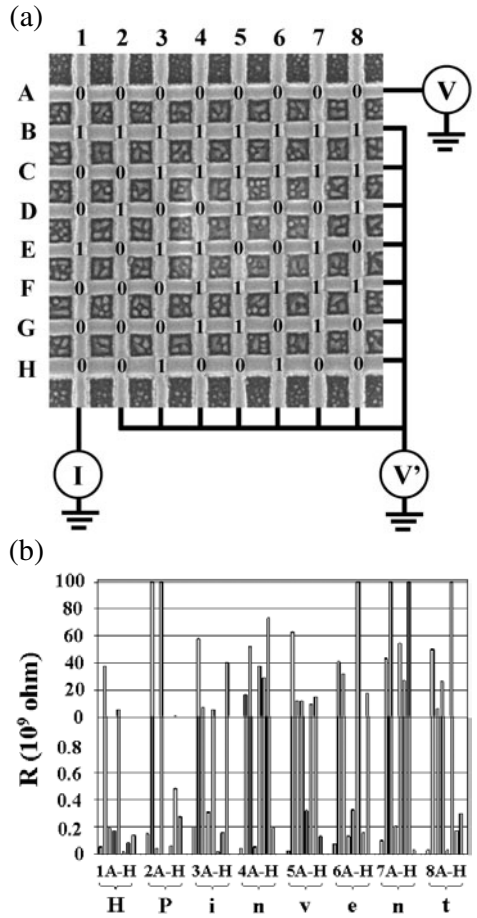

Figure 3. The crossbar as a 64-bit random access memory. (a) The ideal 'write' and 'read' modes for the memory. To write a bit, V is increased in increments of 0.5 from 3.5 V until the bit is written or V reaches 7 V, while keeping $V' = V/2$ (in our actual circuit, the vertical nanowires were floating); to read a bit, $V = 0.5$, and $V' = 0$. (b) Resistance at each cross point in the circuit after one particular set of bits was written into a defect-free crossbar. The resistances of the cross points representing '0' states, which ranged between 10^6 and 5×10^8 Ω, are shown in the bottom half of the plot; the resistances of the cross points representing '1' states, which are $>4 \times 10^9$ Ω, are shown in the top half of the diagram. The bit state at each cross point is indicated by a '0' or '1' in figure 3(a). Each column corresponds to a standard ASCII character, and the bits stored in the memory represent the characters 'HPinvent'.

to reduce the resistance of a cross point below 5×10^8 Ω, as measured at 0.5 V. If not, the voltage of the writing pulse was increased in 0.5 V increments until the bit was successfully written (resistance $<5 \times 10^8$ Ω) or the voltage reached 7.0 V, at which time the bit was declared defective. To read the memory, a bias voltage $V = 0.5$ V was applied to the selected row, and all of the other rows and columns were grounded ($V' = 0$). The resistance of the bit to be read could be determined uniquely by only measuring the current flowing to ground via the selected column.

From our previous study of single-cross-point devices fabricated with the same molecules and the same method [6, 20], we learned that the devices showed a sharp transition from a high-resistance to a low-resistance state when a positive voltage (sign convention defined in figure 3(a), top wire with respect to bottom wire) above a threshold voltage was applied, and vice versa when a negative voltage was applied. The switching is not truly binary; rather the resistance of the junction can be tuned continuously within a certain range by applying voltage pulses of increasing magnitude. Statistically, ∼85% of the bits among the 24 tested 8×8 crossbar circuits showed switching properties. The rest of the bits were either 'shorted', with their resistances $<10^5$ Ω (comparable to the nanowire resistance), or 'open', with resistances $>10^9$ Ω that remained unchanged even after a high writing voltage (>7 V) was applied. The 'open' devices included some with structural defects, such as broken nanowires as detected by post-measurement SEM. However, some unbroken devices as determined by SEM still had an 'open' electrical character, perhaps caused by a contact problem. When a particular bit was selected for writing, an unselected bit was written unintentionally in less than 10% of the trials. This 'half-select' problem will be greatly improved by using a switching matrix that can bias all unselected wires to $V/2$, by improved control over the voltage pulses, by better process control to improve the uniformity of the bits in an array, and by integration of devices with diode characteristics at the cross points. Out of the 24 crossbar circuits analysed, three had no catastrophic defects, nor did they display half-select problems.

After the first sharp transition to a smaller resistance, a cross point acted as a reversible, electrically toggled switch, e.g. a nonvolatile memory bit. A positive voltage ranging from 3.5 to 7 V would turn it 'on', and a negative voltage ranging from −3.5 to −7 V would switch it 'off'. A voltage bias $|V| < 3.5$ V applied to the devices did not change their resistance state. After the first switching event, the on/off resistance ratios ranged from ten to 10^4 for different cross points. The ratio typically decayed from ∼100 and gradually approached unity after a few to several hundred cycles for different devices. Only ∼50% of the bits could be erased (switching from a resistance $<5 \times 10^8$ to $>10^9$ Ω) after the first writing step, and this percentage decayed gradually in the rest of the writing cycles. Several circuits measured after an interval of 24 h retained the resistance of the states into which the bits had last been set, and previous experiments on single cross-point devices have shown retention times exceeding four months [6]

The results of writing and reading all the bits in a 'defect-free' 8×8 crossbar memory can be seen in figure 3(b). The actual value for the low-resistance state (0) and the high-resistance state (1) varied between 10^6–5×10^8 Ω and $>4 \times 10^9$ Ω, respectively. In fact, it was still easy in the case of this 8×8 crossbar to distinguish a low bit from a high bit, because the highest low bit ($\sim 5 \times 10^8$ Ω) was still much lower in resistance than the lowest high bit ($>4 \times 10^9$ Ω). As a demonstration, this 64-bit memory was used to store the word 'HPinvent' with standard ASCII characters (figure 3(b)).

The electrical testing for the 8×8 prototype memory was via the contact pads and micron-scale connections to all the nanowires. However, it is impractical to have direct connections to all the wires for actual circuits with a large number of nanowires. A necessary interface between a nanoscale memory and appropriate control circuitry is a multiplexer and demultiplexer [16], logic circuits that can use an address code to select and transmit signals from multiple input wires to a single output wire (or from a single input

Table 1. (a) Experimentally measured DC resistance values at the cross points in the top right decoder section shown in figure 4. The bold numbers represent the low resistance values at selected cross points. The resistance values beyond the measurement range of our instrument are indicated as ∞. Unit: MΩ. (b) Experimentally measured DC voltages on nanowires 5–7, respectively, under various combinations of V_a and V_b in the demultiplexer shown in figure 4. The bold numbers represent the DC voltages close to 0 V on the selected nanowires. Unit: V. (c) Experimentally measured AC voltages on nanowires 5–7 with the different combinations of the DC voltages V_a and V_b in the demultiplexer shown in figure 4. The bold numbers represent the high AC voltages on the selected nanowires. Unit: mV. The source AC voltage was 0.25 V peak to peak.

(a) R (MΩ)	5	6	7	8
A	**38**	7314	**45**	∞
B	∞	**96**	1124	**22**
C	**18**	**58**	∞	∞
D	∞	7578	**21**	**13**

(b) V_a, V_b	V_5	V_6	V_7	V_8
0, 0	0.92	0.58	0.42	**0.05**
0, 1	0.48	**0.04**	0.92	0.72
1, 0	0.62	0.95	**0.08**	0.48
1, 1	**0.03**	0.52	0.72	0.89

(c) V_a, V_b	V_5	V_6	V_7	V_8
0, 0	0.2	0.2	1.3	**16.5**
0, 1	1.0	**11.9**	0.1	0.2
1, 0	0.1	0.2	**14.8**	0.1
1, 1	**13.6**	0.2	0.3	0.5

Table 2. Experimentally measured resistance values at the cross points in the memory section shown in figure 4. Unit: MΩ. Experimentally measured AC at the corresponding cross points selected by the de/multiplexer. Unit: pA. The bold numbers represent the resistance and current values at the cross points in the '0' state. The resistance values beyond the measurement range of our instrument are indicated as ∞. Unit: MΩ.

R (MΩ)	5	6	7	8
E	**36**	**163**	8706	∞
F	**171**	3062	**29**	∞
$\tilde{I}$ (pA)	5	6	7	8
E	**473**	**72**	10	9
F	**151**	7	**365**	9

wire to one of several output wires). The scaling advantage of a demultiplexer/multiplexer is that it only requires N pairs of address wires to select and control $2N$ nanowires, e.g. ten pairs of address wires can in principle control 1024 nanowires, and thus only 20 pairs of address wires might be required to completely address a 1 Mbit crossbar memory.

To demonstrate a demultiplexer/multiplexer functionality integrated with memory in a single crossbar, we configured a defect-free 8 × 8 crossbar into a 4 × 4 crossbar memory and two 4 × 4 decoders for the demultiplexer/multiplexers by setting the resistances at specific cross points (table 1(a)), one to control the horizontal wires (E, F, G and H) and the other to control the vertical wires (5, 6, 7 and 8) in the memory (figure 4). Note that this choice was arbitrary; we

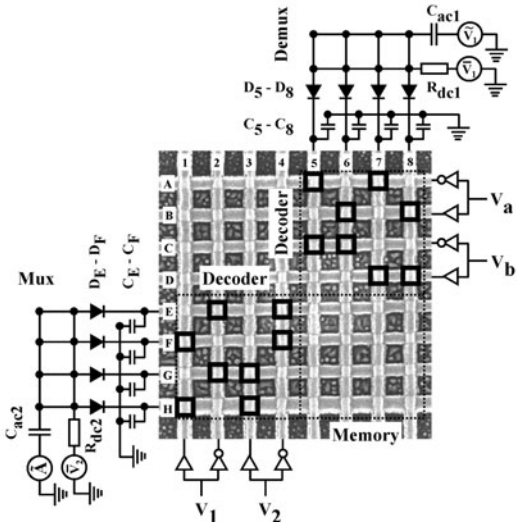

Figure 4. The crossbar as a combination of a 4 × 4 demultiplexer (top right), a 4 × 4 memory (bottom right) and a 4 × 4 multiplexer (bottom left). The black squares in the de/multiplexer sections show the positions of the low-resistance cross points, and the rest of the cross points have a high resistance. The nanowires A–D (1–4) are used as addressing wires with their voltages being set externally by V_a and V_b (V_1 and V_2) through 'identity' and 'not' gates, which in turn determine the DC voltages on nanowires 5–8 (E–H). The external circuit on the top right (bottom left) functions as part of the demultiplexer (multiplexer) to selectively apply (detect) an AC signal on one and only one of the nanowires among 5–8 (E–H) to 'read' the resistance at the cross point of the two selected nanowires. In the circuit, $\tilde{V}_1 = 0.25$ V (100 Hz), $\bar{V}_1$, $\bar{V}_2 = 1.0$ V, C_{ac1}, $C_{ac2} = 1$ μF, R_{dc1}, $R_{dc2} = 50$ MΩ, $C_{5-8} = 0.5$ nF and $C_{E-F} = 100$ pF. V_a, V_b, V_1 and V_2 are set to 0.0 or 2.0 V. $\tilde{\mathbf{A}}$ represents an AC meter.

could have chosen any 4 × 4 quadrant to be the memory, with the adjacent quadrants becoming the decoders. When V_a and V_b (or V_1 and V_2) were set with different input combinations, the potentials on nanowires 5, 6, 7 and 8 (or E, F, G and H) reflected the input code (see details in the appendices). As built, the DC resistor-logic decoders suffer from a narrow operating range (table 1(b)). To effectively widen the gap between the high and low states, we designed external circuits that connect the decoders with diodes and capacitors to form a functional demultiplexer (top right in figure 4) and a multiplexer (bottom left). The demultiplexer applied an AC voltage selectively on one and only one of the nanowires among 5, 6, 7 and 8 (table 1(c)), and the multiplexer selected the AC flowing through one and only one of the nanowires among E, F, G and H; the AC meter ($\tilde{\mathbf{A}}$ in figure 4) detected the AC flowing through the corresponding cross point between the two nanowires selected by the demultiplexer and multiplexer. When V_1, V_2, V_a and V_b were set with certain input combinations, the current flowing through a specific cross point was measured and thus its resistance determined.

After the demultiplexer and multiplexer had been assembled and tested, the external circuits were disconnected from the nanoscale crossbar. The resistances at arbitrarily selected cross points in the 4 × 4 memory section shown in figure 4 were switched and tested using the direct reading and writing procedure described previously, with an example shown in table 2(a). The nanoscale circuit was then

reconnected with the external circuits for the demultiplexer and multiplexer. By changing the combinations of voltages V_a, V_b, V_1 and V_2, the resistances in a 2×4 submatrix of the memory could be read, and the results are shown in table 2(b). For cross points with measured DC resistances smaller than 500 MΩ (corresponding to the '0' state), the corresponding AC was larger than 50 pA; for the cross points with resistances larger than 1 GΩ (corresponding to the '1' state), the corresponding currents were less than 10 pA. There was a clear threshold for the current readout to distinguish between 0 and 1 states.

When we tried to extend the measurements beyond the 2×4 submatrix, we could not identify a clear threshold because of the large variations of the resistances at the cross points in the demultiplexer/multiplexer and the memory. This situation could have been dealt with in this demonstration by utilizing different diodes and capacitors for the different nanowires, but since this would be difficult to implement in an actual CMOS interface, we did not perform this demonstration. The best way to scale up the memory will be to improve the resistance uniformity of the cross points. This can be done by developing a better electronic 'writing' circuit to control the voltage pulses, better processes for the circuit fabrication, and integration of devices with rectifying electric character.

In summary, we have shown that nanoscale molecular crossbar circuits fabricated from a molecular monolayer of [2]rotaxane can function as ultra-high-density memory, and demonstrated demultiplexer/multiplexer logic integrated with memory.

Acknowledgments

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Appendix. Methods

A.1. Imprint lithography

The imprinting mould was fabricated on a silicon substrate using combined electron beam and optical lithography, followed by reactive ion etching (RIE) to define the features. The Si surface was patterned and etched to leave raised mesas ∼80 nm above the etched surface of the mould. Each mould had several hundred such circuit patterns laid out in a geometrical array, to enable a large number of circuits to be fabricated with one imprinting step. To form the circuit electrodes, a liquid-phase mixture of 8 wt% poly-benzyl methacrylate in benzyl methacrylate monomer solution was spin-coated onto a 100 nm thick SiO_2 layer on a silicon substrate. The mould was then pressed onto the coated substrate with a homogeneous pressure of 500 psi, which was then heated to 80 °C to cross-link the monomer/polymer layer and transfer the pattern from the mould into the solid polymer layer before detaching the mould from the polymer. After imprinting, oxygen RIE was used to remove ∼10 nm of residual polymer at the bottom of the imprinted trenches, and expose the SiO_2 surface. Then, 5 nm titanium (Ti) and 10 nm platinum (Pt) metal layers were sequentially evaporated onto the substrate. A final acetone lift-off process removed the unpatterned field to define the Ti/Pt nanowires and their micron-scale connections to the contact pads.

A.2. Circuit fabrication

A molecular monolayer of the [2]rotaxane **R** (figure 1(b)) was deposited over the entire substrate, including imprinted bottom metal electrodes, using the Langmuir–Blodgett (LB) method. During LB film deposition the aqueous subphase was maintained at pH ∼8.5 by the addition of tris(hydroxymethyl)aminomethane, to typical concentrations of 10^{-4} M, at 21 °C. Fabrication of the top electrodes began with the blanket evaporation of a 7.5 nm Ti protective layer. This metal layer minimized subsequent disruption of the molecular monolayer, enabling further organic resist and solvent processing. The Ti layer also functioned as a direct electrical contact to the molecules. Patterned top electrodes of 5 nm Ti and then 10 nm Pt were next fabricated with the same imprinting process described above, using the same mould. For the top electrodes, the imprinting mould was oriented perpendicular to the bottom electrodes and aligned to ensure that the top and bottom nanowires crossed. Finally, RIE with CF_4 and O_2 (4:1) gases at a pressure of 40 mTorr and a power of 200 W was used to remove the blanket Ti protective layer anisotropically down to the SiO_2 layer, but selectively leave the Pt electrodes intact. The molecules and Ti layer under the Pt top electrode were protected. After RIE, the crossbar circuits with the molecular monolayer sandwiched between the metal nanowires remained (figure 1(a)).

A.3. Write and read modes for memory

In order to write one bit at a cross point (e.g. (1, A) in figure 3(a)), the corresponding row and column of the crossbar were selected by applying a bias voltage V on the top nanowire (row A in figure 3(a)) and grounding the bottom nanowire (column 1 in figure 3(a)). However, to prevent any other bits from being accidentally written, the bias voltage on all the other rows and columns should be set at an intermediate voltage, $V' = V/2$. Thus, none of the cross points at the intersections of rows (B–H) and columns (2–8) not selected for the write operation would have a bias voltage across them and they could not be written. All of the cross points on the selected row (A) and column (1) that were not intentionally being written would have only half the writing voltage bias across them, and as long as the switch molecules have a sharp and sufficiently reproducible writing threshold, there should be no accidentally written bits. In our actual test, our switching matrix did not have enough connections to set all the unselected rows and columns to $V/2$, so only the rows were biased and the columns were allowed to float.

A different electronic configuration was required to read the memory. In this case, a bias voltage (much smaller than the voltage used to write the bit) was applied across the row and column of the bit to be read (e.g. row A and column 1 for reading cross point (1, A) in figure 3(a)), but all of the other rows and columns were grounded. Although current might flow through all of the other cross points on the selected row (A), the resistance of the bit to be read could be determined

uniquely by measuring only the current flowing to ground via the selected column (1).

Although the qualitative behaviour of the switching was the same, the threshold switching voltages varied significantly from device to device and even for a single device when switched many times. To avoid large state variations and in order to make a clear distinction between binary 0 and 1 states in the memory, we used the following scheme for writing the memory. As fabricated, the bit resistances in a circuit were usually very high, $>10^9$ Ω as measured at 0.5 V. In the writing mode, the application of a voltage pulse with a duration of 0.5 s and an amplitude of 3.5 V was usually sufficient to cause an irreversible sharp transition to a smaller resistance. If the resistance was reduced below 5×10^8 Ω as read at 0.5 V in a subsequent read step, the writing procedure on this bit was complete. However, if the resistance was still larger than 5×10^8 Ω, higher voltage pulses with an increment of 0.5 V were applied to the bit until the resistance as read at 0.5 V fell below 5×10^8 Ω or the voltage reached a 7 V upper limit, at which point the bit was labelled defective. This upper limit was selected to prevent any other bits in the array from being accidentally written, since some of other cross points could be biased to 3.5 V, which is close to the writing threshold. Since any voltage bias $|V| < 0.5$ V applied to cross points did not change their resistance state, and the I–V characteristic measured in the range ±0.5 V showed an ohmic response, a bias of 0.5 V was used for the read mode.

A.4. Demultiplexer/multiplexer for memory

In the decoder sections shown in figure 4, the cross points indicated by black squares in figure 4 were set to low resistances, and the rest of the cross points remained at high resistance values, which are listed in table 1(a). The A, B, C and D inputs in figure 4 were used as the address wires for the demultiplexer controlling the vertical nanowires in the memory. For example, when V_A and V_B were set at low voltages, the nanowires A, B, C and D were set to high (1.0 V), low (0.0 V), high and low voltages, respectively, through the 'identity' and 'not' gates connected to them via external circuitry. The actual potentials on the vertical nanowires 5, 6, 7 and 8 were measured to be 0.92, 0.58, 0.42 and 0.05 V, respectively, as listed in table 1(b). Vertical nanowire 5 had a potential of approximately 1.0 V, since it was connected through the low-resistance cross points (5, A) and (5, C) with nanowires A and C, which were both set to 1.0 V. Nanowire 8 had a potential approximately 0.0 V, since it was connected through the low-resistance cross points (8, B) and (8, D) with nanowires B and D, which were both set to 0.0 V. Nanowires 6 and 7 both had intermediate potentials, since they were connected through low-resistance cross points with input voltages that were set to 0.0 and 1.0 V. When V_a, V_b were set with different input combinations, the potentials on nanowires 5, 6, 7 and 8 reflected the input code appropriately (see table 1(b)).

A multiplexer or demultiplexer needs to select one and only one nanowire under each combination of inputs from the addressing wires, which in an actual circuit would be connected directly to CMOS and would most likely be fabricated using conventional processing techniques. The median voltages between low and high levels that occur with a DC resistor-logic decoder reduce the operating range and make it difficult to distinguish between a '1' and a '0' in the memory, especially since two levels of such logic are involved (the decoders for the demultiplexer and multiplexer). To solve this problem, we designed an external circuit with diodes and capacitors connected to the nanowires to create AC voltage/current dividers between the diodes and capacitors (see figure 4).

In an actual memory, this could be part of the conventional electronics used to control the circuit, or could even be built into the nanoscale circuitry with appropriate components. In the demultiplexer as shown in the top right section in figure 4, when a DC voltage V_d is applied across a diode, the small-signal AC resistance of the diode becomes $\tilde{R} = \tilde{R}_0 \exp[-V_d/(nkT)]$, where $\tilde{R}_0$ is the small-signal AC resistance at $V_d = 0$, and n, k and T are the emission coefficient of the diode, the Boltzmann constant and the operating temperature, respectively. The DC voltage across each diode V_d in the circuit is determined by the difference between a DC reference voltage $\bar{\boldsymbol{V}}_{\mathbf{1}}$ as marked in figure 4 and the DC voltage on the corresponding nanowire. For a particular nanowire set at a DC voltage close to zero by the addressing voltages V_a and V_b, the DC voltage across its corresponding diode V_d was approximately equal to $\bar{\boldsymbol{V}}_{\mathbf{1}}$. In this case the AC impedance for that diode $\tilde{R} \sim \tilde{R}_0 \exp[-\bar{\boldsymbol{V}}_{\mathbf{1}}/(nkT)]$ was significantly *smaller* than that for the AC impedance of its corresponding capacitor connected to the nanowire (one of C_5–C_8 in figure 4). Thus, the AC voltage on the selected nanowire was close to the AC voltage source $\tilde{\boldsymbol{V}}_{\mathbf{1}}$ shown in figure 4. The rest of the nanowires were set with DC voltages larger than zero by the addressing voltages V_a and V_b (see table 2(b)). The DC voltages V_d across their corresponding diodes were significantly smaller than $\bar{V}_1$, and the AC impedances for those diodes $\tilde{R}$ were significantly larger than $\tilde{R}_0 \exp[-\bar{\boldsymbol{V}}_{\mathbf{1}}/(nkT)]$ and the AC impedances of their corresponding capacitors. The AC voltages divided on those nanowires will be closely equal to zero.

The AC voltages measured on nanowires 5–8 are listed in table 1(c) (the truth table for this demultiplexer) for the four input combinations of V_a and V_b. The AC voltages displayed a much larger separation between the high and low states than the DC voltages, since the AC voltages depend exponentially on the difference of their DC biases. By optimizing the diodes and capacitors in the circuit appropriately, the demultiplexer can be improved significantly. The same principle was used to form a multiplexer by combining a DC decoder with AC dividers made of diodes and capacitors as shown in the bottom left section in figure 4. The addressing voltages V_1 and V_2 set the DC voltages on one of the nanowires (E–H) close to zero and the rest of them higher than zero. The AC impedances of the diodes (D_E–D_F) connected with the nanowires with zero (non-zero) DC voltages were significantly lower (higher) than the AC impedances of the corresponding capacitors (C_E–C_F). The AC flowing through the memory section on the nanowire connected to the diode with low AC impedance passed through the diode and was measured by the AC meter $\tilde{\boldsymbol{A}}$ as shown in figure 4. The AC on the nanowires connected with the diodes with high AC impedance was shunted to ground by the capacitors. When V_1 and V_2 were set with different input combinations, the current from the single nanowire with near DC bias of 0.0 V was measured by the current meter $\tilde{\mathbf{A}}$.

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