

Optical Lithography has been tremendously successful in mass production. It enjoys economies of scale that lower the cost of production as the volume increases, but half of all chip designs produce fewer than about 600 wafers total. The cost of production of those designs is much higher and dominated by the cost of the reticle, which is becoming more expensive as the critical dimensions shrink.

The low volume ASIC and SOC segment of the IC industry is not well served by current lithography techniques or R&D cartels and that has motivated a search for maskless lithographies, such as e-beam direct write. However, as Dan Hutcheson of VLSI Research points out, the writing speed has to be enormous to compete even with the high prices of current low-volume DUV lithography. In particular, to achieve 1 wph throughput, an e-beam system must write data at  $>2.5 \times 10^9$  pixels per second, much faster than current tools, and even then, production would be economically viable only for chips with production runs less than  $\sim 200$  wafers. JEOL and other vendors continue to sell tools into that market, but most such applications are expected to be taken over by field programmable gate arrays and other larger volume parts that can be made on scanning steppers with  $>100$ wph throughput. To be economically viable for part of the mainstream ASIC and MPU market, the production rate must be 10-20 wph, which is the target for electron projection lithography.

Micronic Laser Systems has proposed a maskless optical lithography system that prints 1,000,000 pixels at a time. However, the spatial light modulator used by Micronic is a MEMS device that can only run at about 1 kHz. The data transfer rate is thus  $< 10^9$  pixels/second, too slow by about a factor of 100 to be economically viable. However, fast maskless lithography can produce photomasks more economically than today even if it is too expensive for wafer production.

It is urgently important to lower the costs of advanced reticles, especially for the low-volume industry segment where reticle costs dominate everything, including design. Several ideas have been proposed. My favorite is Phase Phirst! where alternating aperture phase-shift masks are produced on ready-to-write pre-patterned substrates, with one patterning step. The cost and turn-around for 100nm generation PSMs made this way would be comparable to today's 250nm COG reticles. The problem is that all the designs would have to be compatible with a small number of pre-patterned phase-step arrays, and that is not the case today. Only by standardizing those arrays can defect-free substrates be mass produced. However, the designers are hesitant to undertake the required revision of existing legacy designs in spite of the fact that the device physics and production constraints of sub-130nm technology require it.

Optical lithography will continue to be preferred for large volume lithography. The future, however, may be in very specialized consumer devices with short production cycles and low cost. Producing the chips going into those things may require something new!