Microstructural Characterization of Copper Interconnects

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The data presented here were collected in collaboration with:

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Matt Herrick, Cindy Simpson, Stacye Thrasher, Greg Braeckelmann, Stewart Rose and Hisao Kawasaki
(Digital DNA Laboratories, Motorola, Austin, TX)

Larry Zhao (no longer with AMD)

Richard Ortega and Delrose Winter
(AMIA Laboratories-Rigaku)

Outline

- Why Characterize Microstructure?
- Microstructure characterization methods utilized in this study to quantify in-laid Cu lines.
  - Grain size
  - Texture
  - Mechanical stress
- Application of these methods to understand the evolution of microstructure during thermal cycling.
- Summary and Conclusions

Why Microstructure?

- Cu is the interconnect metal for high-speed logic technologies.
- Much of the published microstructural characterization has been done on blanket films but Cu is fabricated with dual inlaid technology.
- The inlaid fabrication method affects the grain growth and microstructure of the Cu.
  - Grain growth is affected by the confinement of the sidewalls.
  - Sidewall-nucleated grains are observed.
  - Mechanical stress is affected by the inlaid fabrication methodology.
  - Electroplating introduces new variables to understand.
  - EM performance is affected by grain orientation, grain size, stress.

    P. Besser et al., Proceedings of the IEEE IEDM 2000 Meeting.
- This work was undertaken to characterize and understand the microstructure of Cu in inlaid Cu lines.

What aspects of microstructure are important and how are they measured?

AMD

☆Grain size

- TEM costly
- EBSD time-intensive
- FIB/SEM A lot of work, but the ***Best way***

❖Crystallographic orientation

- XRD cheap, non-destructive. ***Best way.***
  gives average grain orientation through thickness.
- EBSD complicated, cannot be done through passivation.

➢Stress

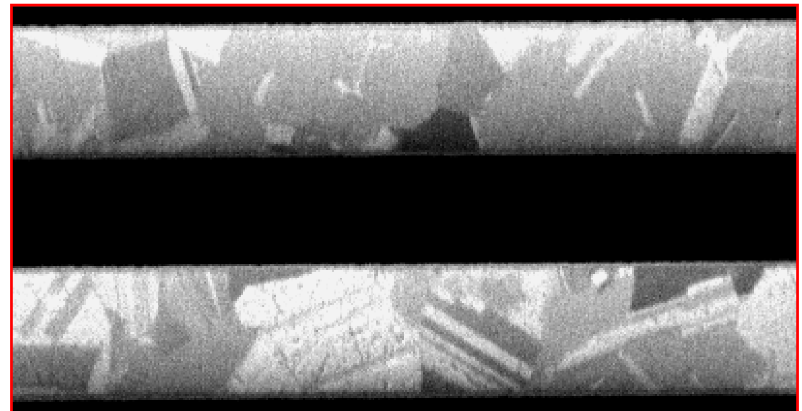
- Curvature easy, convenient. Not for lines. ***Great for films.***
- XRD direct measurements for lines. ***Best way.***

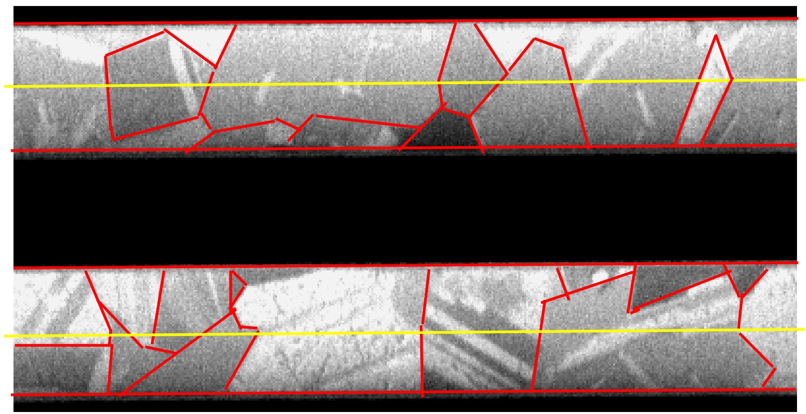
Sample Description

- A test chip was processed through an abbreviated version of a old dual inlaid Cu flow.
  - Oxide ILD, 4500Å deep trenches with nearly vertical sidewalls
  - Refractory barrier, Cu seed, Electroplated Cu
  - SiNx capping layer + oxide was deposited on some samples
- Linewidths of 0.35, 0.5, 0.7 and 1.06 μm wide (at the top).
- Samples annealed at three temperatures- low, medium, high
- Samples annealed post-CMP and pre-CMP
- Grain size, stress and texture were measured with and without capping layers on the lines.
- Blanket films were also created, with identical thermal histories.

Grain size measurement in Cu lines *

- FIB images taken of the lines after the ILD is stripped show the grain boundaries and twins.
- Grain size is determined using the mean grain length in the center of the trench, along trench direction.
- Twins (coherent interfaces) are not considered grain boundaries.
- 150-200 grains are measured per grain distribution (per linewidth).
- Equivalence between TEM and FIB/SEM has been shown.





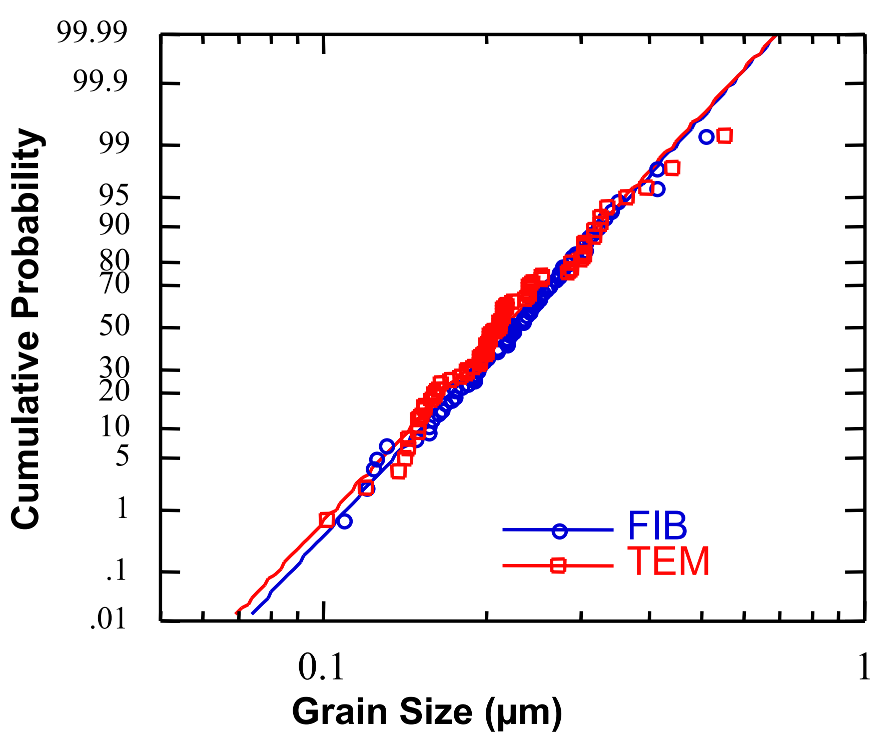
*** Method first applied to damascene lines by Besser, Sanchez and Field, *Adv. Metall. and Interconnect Systems for ULSI Applications in 1996, MRS Symposium Proceedings* (1997).**

Grain size determination in lines

The grain size distribution in lines is determined with this method: median grain size, standard deviation attained.

Grain size distribution is log-normal.
Grain size is a function of linewidth.

FIB/TEM equivalence



- 0.42 µm wide lines
- For this work, about 70 grains were measured for each distribution.
- The grain size distributions from TEM and FIB are equivalent.
- FIB can be used for grain size distributions in lines.

Data courtesy of Martin Gall, Motorola

Grain size measurements in lines

Low vs. High Temp PP Anneal

The grain size distribution and median grain size increase dramatically with increasing anneal temperature.

P.R. Besser et al., Journal of Electronic Materials (April, 2001)

Grain growth with ILD deposition

Low Temp PP Anneal- with and without passivation.

△ 1.06 µm lines
□ 0.7 µm lines
○ 0.35 µm lines
▲ Passivated 1.06 µm lines
■ Passivated 0.7 µm lines
◆ Passivated 0.35 µm lines

Cummulative Probability: 99.999, 99.5, 95, 70, 40, 10, 1, .01, .0001

Grain Size (µm): 0.01, 0.10, 1.00, 10.00

If the anneal temperature is low, then significant grain growth occurs **during** ILD deposition.

P.R. Besser et al., Journal of Electronic Materials (April, 2001)

Grain size measurements in lines

Medium Temp PP Anneal- with and without passivation.

Passivated 1.06 µm lines
Passivated 0.7 µm lines
Passivated 0.35 µm lines
1.06 µm lines
0.7 µm lines
0.35 µm lines

Cummulative Probability: 99.999, 99.5, 95, 70, 40, 10, 1, .01, .0001

Grain Size (µm): 0.01, 0.10, 1.00, 10.00

If the anneal temperature is equal to or greater than the ILD deposition temperature, then the grain growth during ILD deposition is insignificant.

P.R. Besser et al., Journal of Electronic Materials (April, 2001)

Effect of Barrier Layer on Grain Size

Cumulative Probability

99.999
99.5
95
70
40
10
1
.01
.0001

Barrier 3

Barrier 2

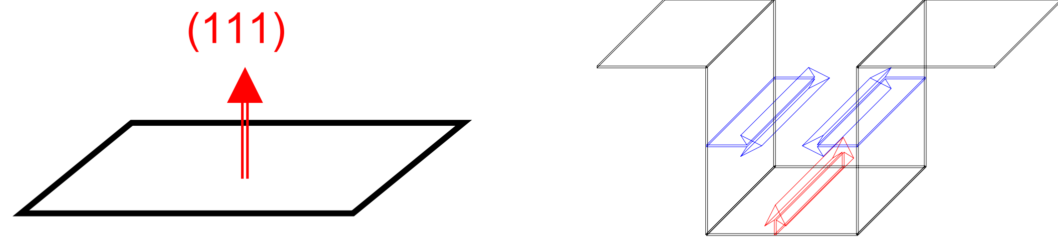
0.01
0.10
1.00
10.00

Grain Size (μm)

Grain size of Cu in the trench is independent of refractory barrier type.

Texture of damascene-fabricated Cu lines is complicated

- Al grains nucleate and grow on a planar oxide or barrier surface.
  - Al grains have a strong (111) texture.
  - A strong Al (111) texture is preferred for optimal EM performance.

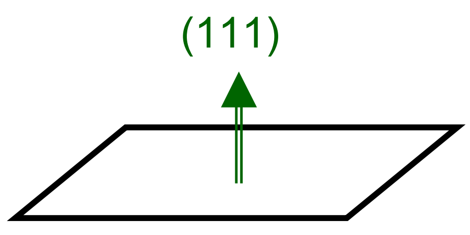


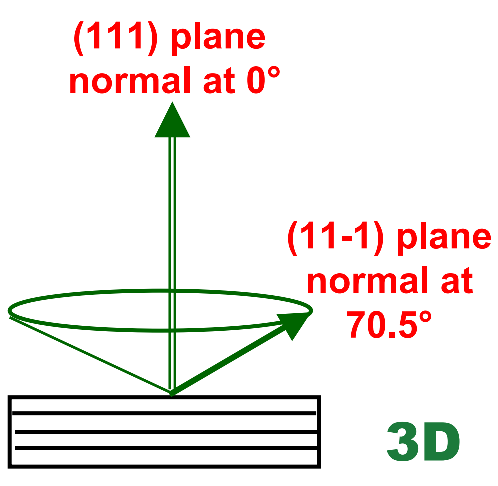
- Cu grains nucleate and grow from the sidewall and the trench bottom.
  - Cu (111) texture from bottom and sidewall.
  - Non-symmetric pole figure and linewidth dependence expected.
  - Cu can have other texture components such as (511), (200).

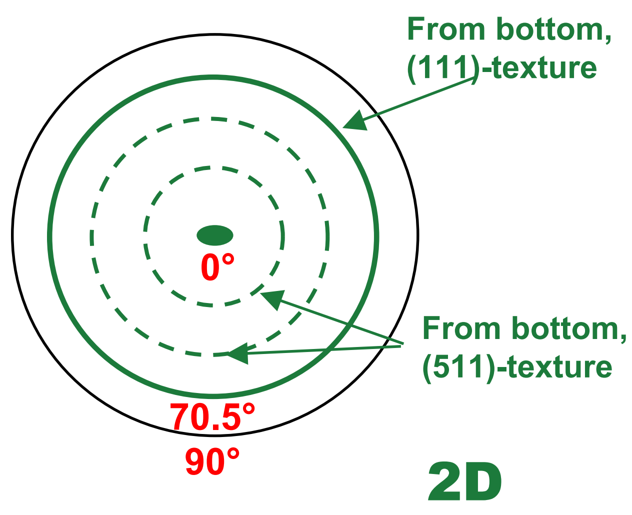
Pole figures for films and lines.

The sample is tilted/rotated to measure the entire population of a particular family of crystallographic planes, relative to the surface normal. XRD was used for this work. XRD can be measured through a passivation layer and samples the entire film thickness.

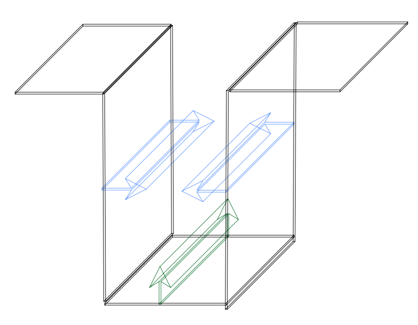
films



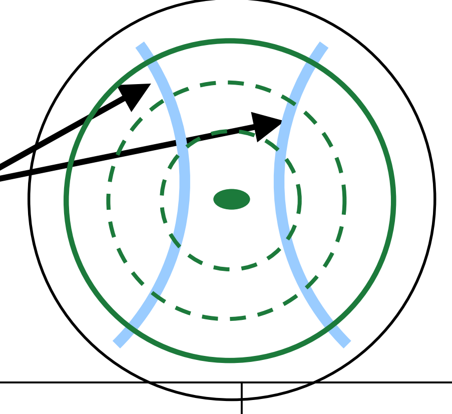




lines

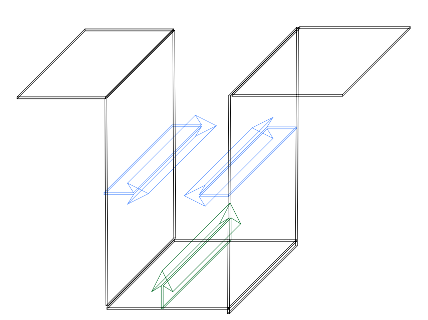


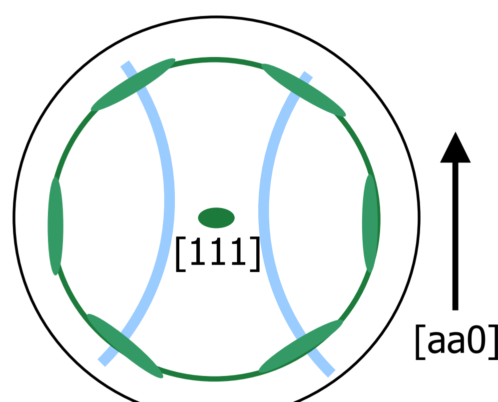
For lines, the grains nucleate at the trench bottom as well as the sidewall. The (11-1) from the sidewall leads to an additional peak on the (111) pole figure for in-laid lines.



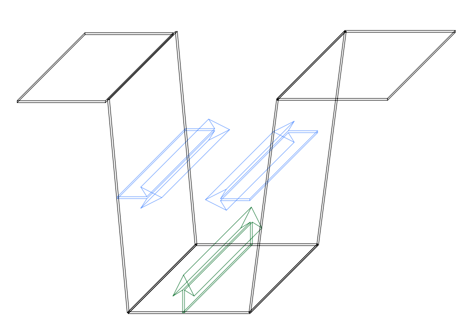
Schematic drawing of pole figures for lines.

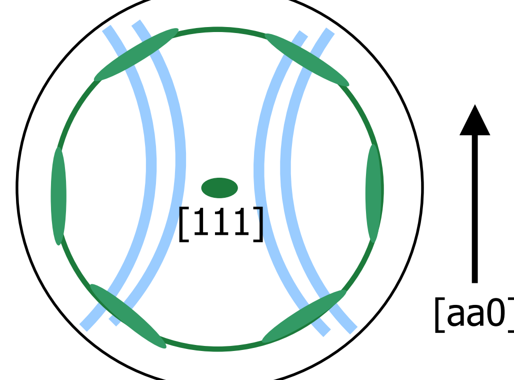
Vertical Sidewall.
Preferred in-plane (111).





85° tilt





Non-vertical sidewall.
Preferred in-plane (111).
(111) grains nucleated on sidewall lead to multiple peaks in the (111) pole plot. Peak separation is twice the sidewall angle.

P.R. Besser et al., Journal of Electronic Materials (April, 2001)

(111) Pole Figures for Cu Lines vs. Linewidth

NARROW LINES

Narrow lines have a larger sidewall contribution.

.35 MICRON

.50 MICRON

.70 MICRON

1.0 MICRON

(111) from sidewall

WIDE LINES

FILM

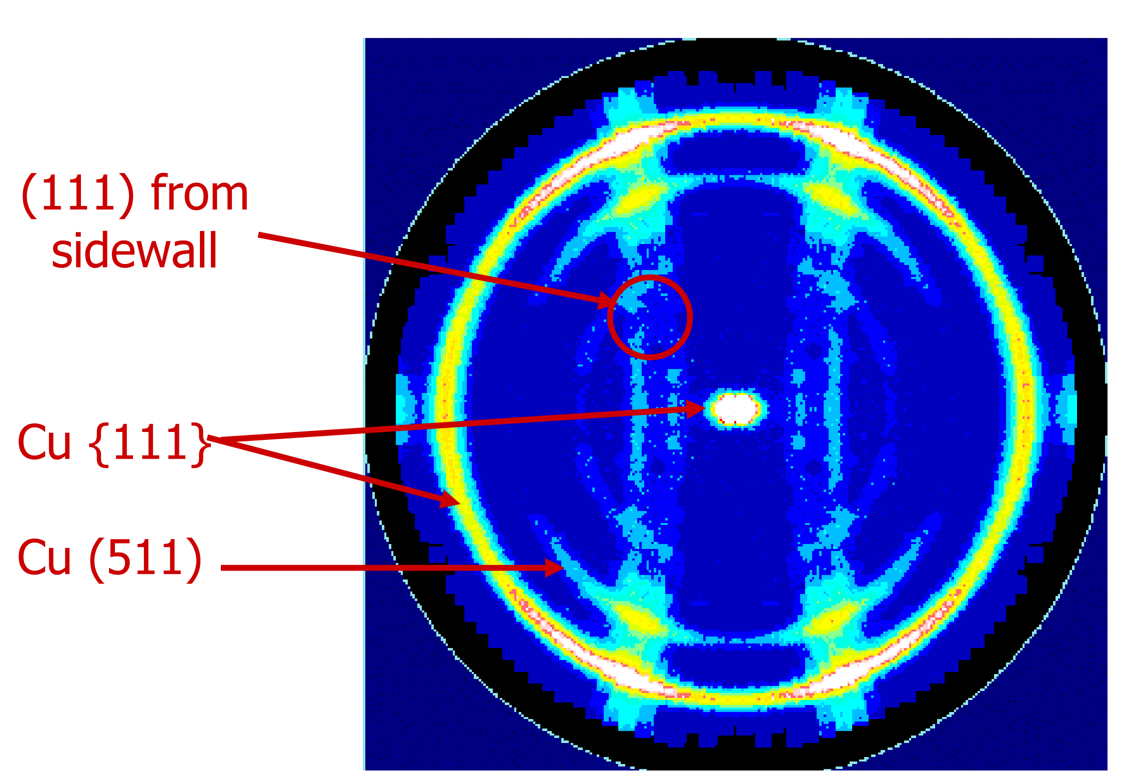
Cu (111)

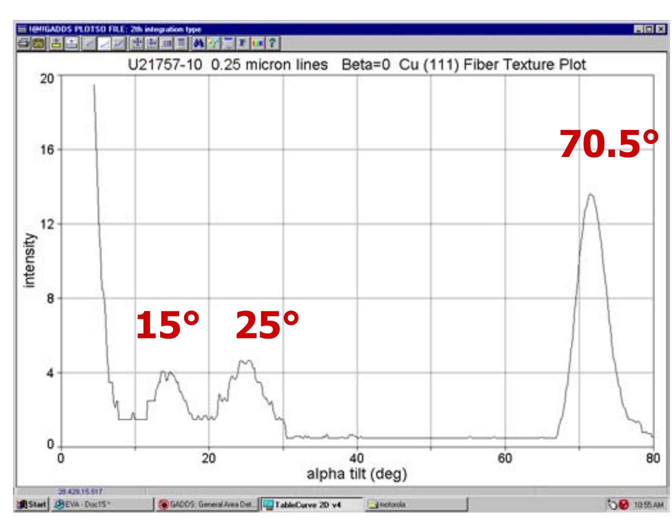
Cu (511)

Cu (11-1)

P.R. Besser et al., Journal of Electronic Materials (April, 2001)

(111) Pole Figure- 0.35μm Cu Lines, Low Temp anneal.



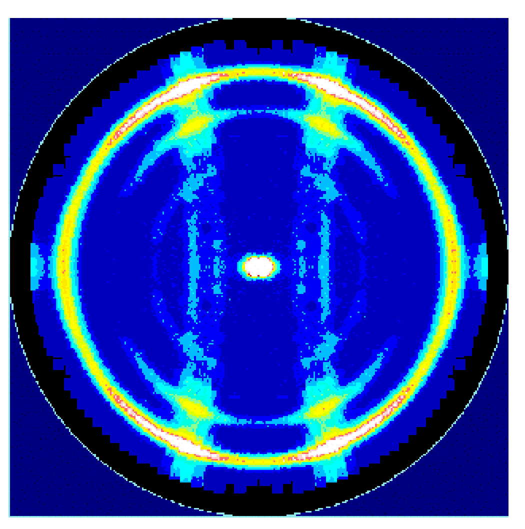


Cu lines have a strong (111) texture and (511) twins.
The (111) grains have a preferred in-plane texture: [aa0] along sidewall.
(111) sidewall-nucleated grains are visible. Twins have a preferred orientation.
The entire pole figure must be collected to quantify the orientation. θ-2θ scans are useless.

P.R. Besser et al., Journal of Electronic Materials (April, 2001)

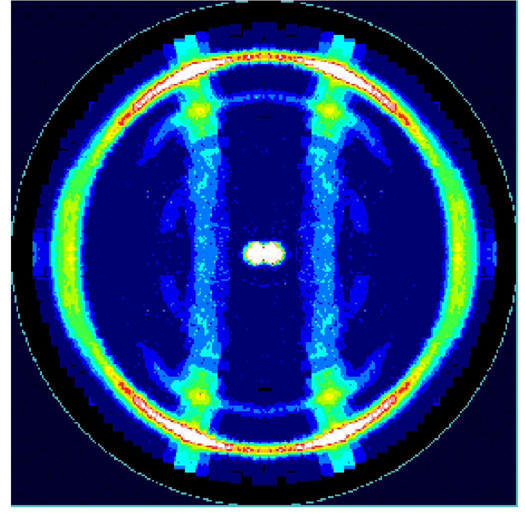
(111) Pole Figure of 0.35µm Cu Lines

Low Temp,
post-plate anneal



High Temp,
post-plate anneal

Low Temp,
post-CMP anneal

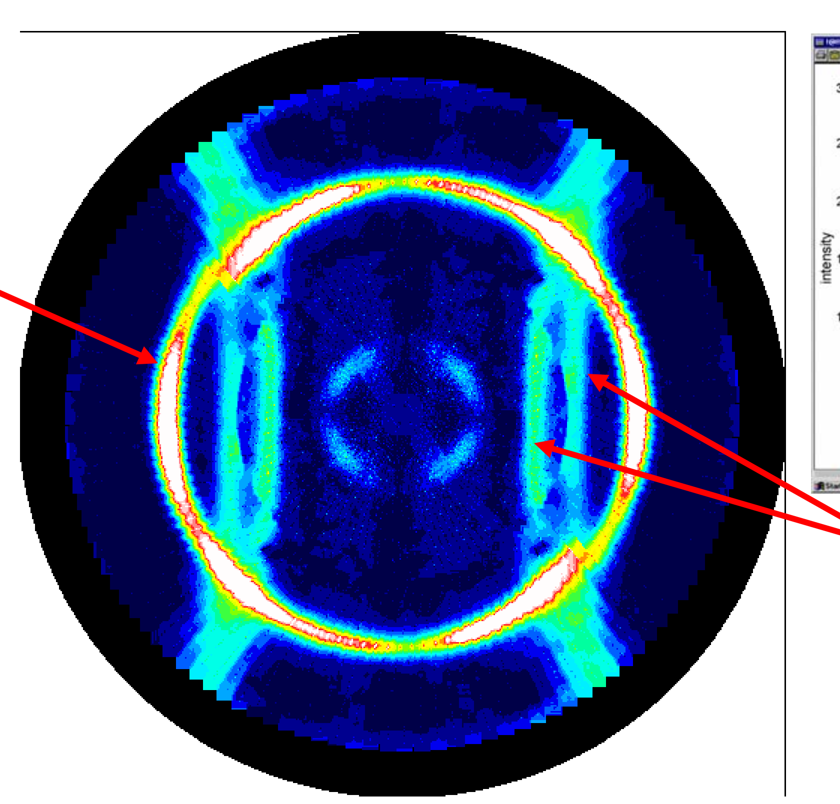


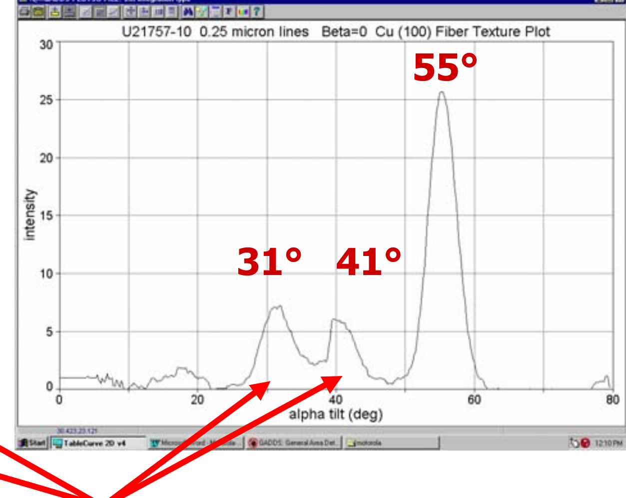
Cu line pole figures are similar, independent of when the anneal is performed. Grain growth is independent of when the anneal was performed.

P.R. Besser et al., Journal of Electronic Materials (April, 2001)

(100) Pole Figure of 0.35µm Cu Lines, Low Temp anneal.

(111) grains from trench bottom have a preferred in-plane orientation and show the 3-fold symmetry. Peak occurs at 55°.



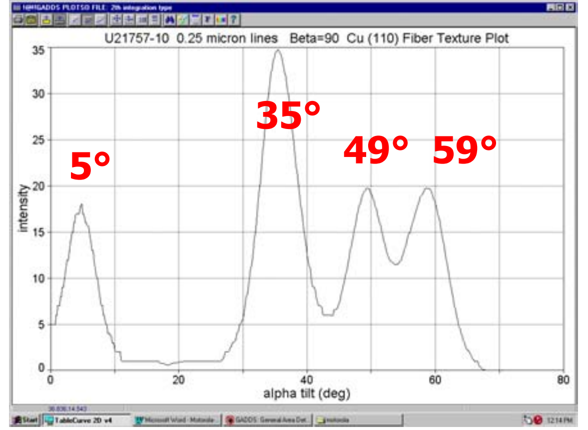


(111) grains from sidewall should give a peak at ~35°. Peaks at 31 and 41° from the 5° sidewall angle.

No (100) grains.
The (111) grains have a preferred in-plane texture.
(111) sidewall-nucleated grains are visible.

P.R. Besser et al., Journal of Electronic Materials (April, 2001)

(110) Pole Figure of 0.35µm Cu Lines, Low Temp anneal.



(111)

(111) grains from trench bottom have a preferred in-plane orientation.

(111) grains from sidewall should give peaks at 0 and 55°. Peaks at 5, 49 and 59° arise from the 5° sidewall angle. Peaks have a preferred in-plane orientation with the [aa0] parallel to the trench bottom.

No (110) grains.

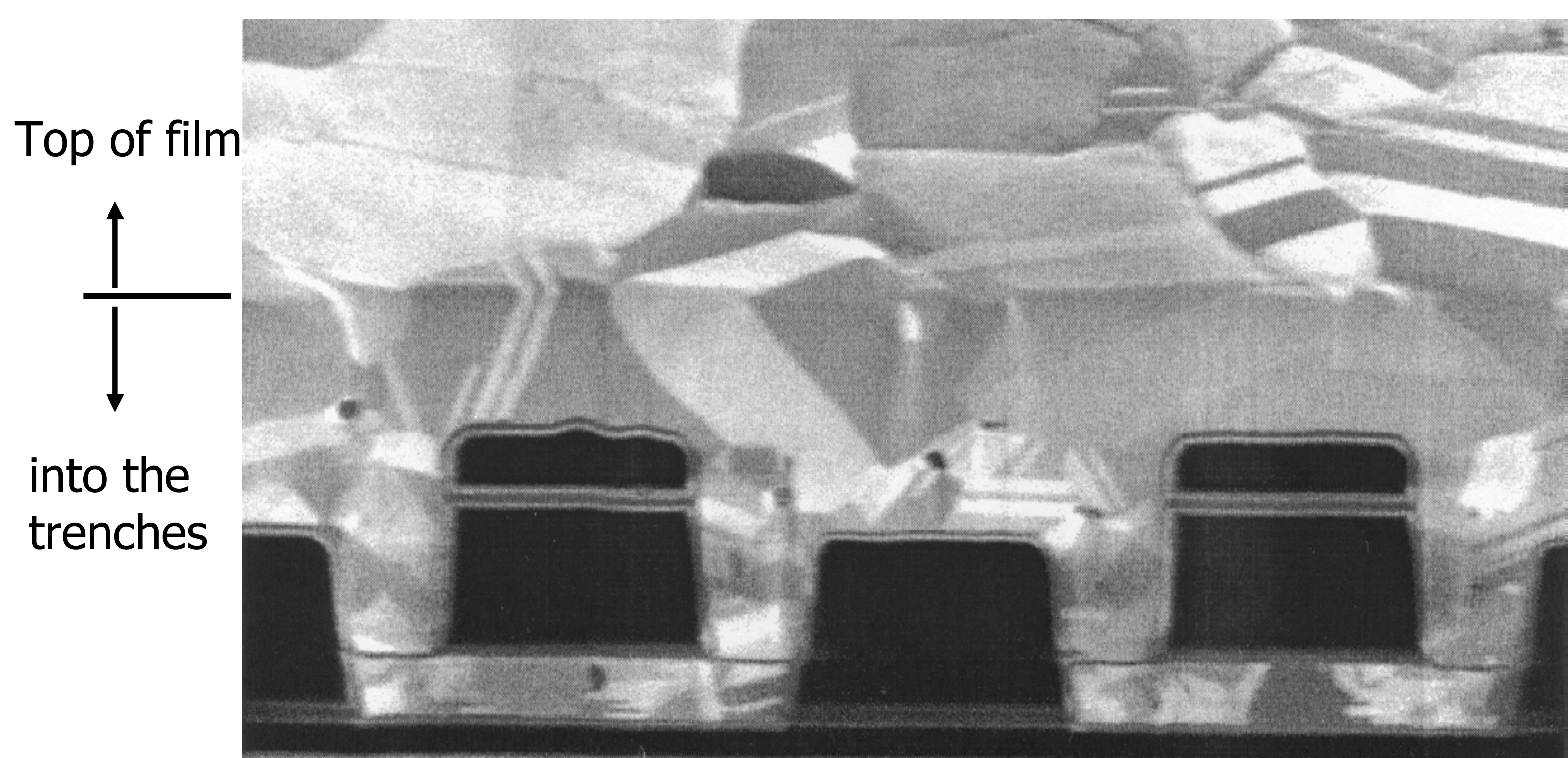
The (111) grains have a preferred in-plane texture: [aa0] along sidewall.
(111) sidewall-nucleated grains are visible.

P.R. Besser et al., Journal of Electronic Materials (April, 2001)

Does Texture and grain size of blanket films matter?

- These results differ from others-
  - Lucent (Lingk et al.) and U. of Michigan (Sanchez et al.) find relatively weak texture in their inlaid Cu lines-
    - *Appl. Phys. Lett.* 74(5) 1999. *J. Appl. Phys.* 84(10) 5547 (1998)
  - Also, new grain growth initiates initiates at the top corner of the trench.
  - Grains extend from the overburden into the trench for **WIDE** lines.
- The current work on **0.35μm lines** observes:
  - Crystallographic texture is strong (111).
  - Texture and therefore, grain growth, is independent of when the anneal is performed (post CMP or post plating).
  - Texture on the field is not necessarily representative of texture in the trench.
  - The (111) grains have a preferred orientation relative to the sidewall to surface energy. *(Sanchez and Besser, IITC (1998)).*
- Differences are attributed to differences in processing and linewidth.
  - Plating additives, chemistry, seed layer, barrier type, waveform, etc.
  - Thermal history is different as well.

Grain growth in field is not necessarily correlated with grain growth in trenches

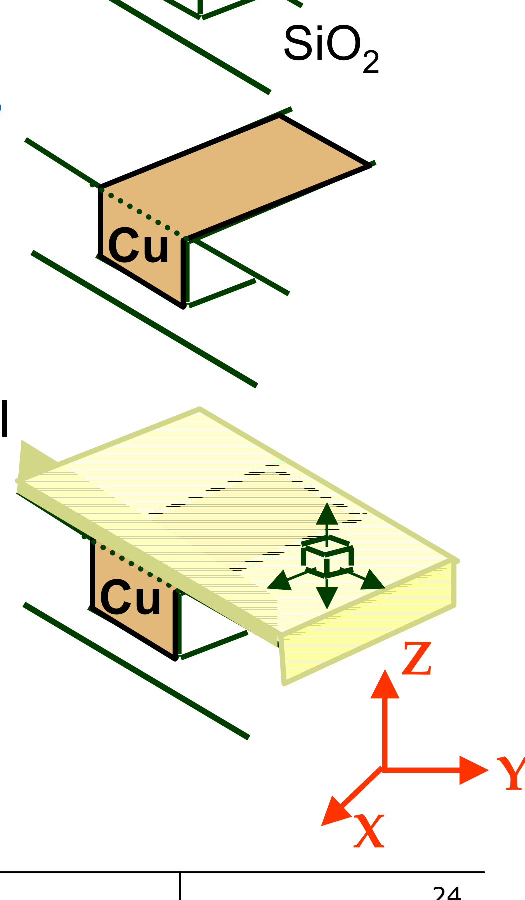


FIB image is tilted at 52°

P.R. Besser et al., Journal of Electronic Materials (April, 2001)

Development of stress in RIE and damascene lines

- Mechanical stresses and their determination are well understood in inlaid Cu lines-
  - *Rick Vinci did the first work, with lift-off Cu lines.*
  - *Besser, Stress-Induced Phenomena in Metallization, AIP Conf. Proc. **491**, pp. 229-239 (1999).*
  - *Besser et al., MRS Symp. Proc.**563** (1999).*
  - *Kasthurirangan et al., Stress-Induced Phenomena in Metallization, AIP Conf. Proc. **491**, p. 304 (1999).*
- Mechanical stresses arise from a difference in thermal expansion between the Cu and the substrate and dielectrics. $CTE_{Cu} >> CTE_{Si}$
- The stresses in Cu lines are smaller than that in Al lines of the same aspect ratio.
- Inlaid fabrication alters the stress state.
- The stresses at RT are hydrostatic and tensile. Stresses are linear with temperature.
- How does the stress state change with annealing conditions?



A novel stress measurement technique

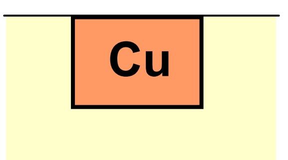
AMD

- **Developed by AMD and AMIA Labs (The Woodlands, TX).**
- **Diffractometer**
  - **Texture can be measured on lines and films.**
  - **Small spot size achieved with capillary optics (60 µm). 2D detector.**
  - **Goniometer is an X-Y-Z motion stage with a Fiber optic camera.**
- **Cu**
  - **Has anisotropic elastic properties. Texture is important.**
  - **(422) is a desirable reflection for stress measurement. Different interplanar spacing of Cu means that accessing (422) requires changing wavelengths.**
  - **For this work, Cu K-β radiation was used to access to the (422).**
- **Stress can be measured on the 0.25, 0.18, 0.13 µm lines!**
  - **Dzero determined on a blanket film**
  - **Strain is measured on the lines in the X, Y, and Z directions.**
- **For details of the stress measurement method, see**

  Besser, *5th Int'l Workshop on Stress-Induced Phenomena*, AIP Press 491 (1999).
  Besser, Joo, Winter, Ngo, and Ortega, *MRS Symp. Proceedings* Vol. 563 (1999).

Stress data- Unpassivated Lines

- Mechanical stress was measured on 0.35 μm lines, 4.5kÅ deep.
- NO ILD on lines.
- All stress values are in MPa. X is along the length, Y along the width and Z along the height of the line.



Anneal Temperature	X	Y	Z	Hydrostatic
Post-plating, Low Temp	113	60	42	72
Post-plating, High Temp	375	357	142	291

- Stress is dependent upon the post-plating anneal temperature.
- Stress is hydrostatic, even though the lines are unpassivated.

P.R. Besser et al., Journal of Electronic Materials (April, 2001)

Stress data- Passivated lines

Anneal Temperature	X	Y	Z	Hydrostatic
Post-plating , low temp	307	162	55	175
Post-plating, medium temp.	399	235	156	263
Post-plating, medium +40°	458	289	194	314
Post-plating, high temp.	618	470	228	439

- Mechanical stress was measured on 0.35 µm lines, 4.5kÅ deep.
- Samples had the same passivating ILD.
- All stress values are in MPa. X is along the length, Y along the width and Z along the height of the line.
- Mechanical stress increases with anneal temperature.

Z
X
Y
Cu

P.R. Besser et al., Journal of Electronic Materials (April, 2001)

Stress results

- Mechanical stress is a linear function of post-plating anneal temp.
- Increasing the anneal temperature increases the RT stress level.

Stress at Room Temp. (MPa)

700
600
500
400
300
200
100
0

X
Y
Z
H

LOW MEDIUM HIGH

Anneal Temperature

Z
X
Y
Cu

P.R. Besser et al., Journal of Electronic Materials (April, 2001)

Stress Correlation to Grain Size

Median Grain Size (µm)

0.6
0.5
0.4
0.3
0.2
0.1
0

High T
Med T
Low T

0 100 200 300 400 500

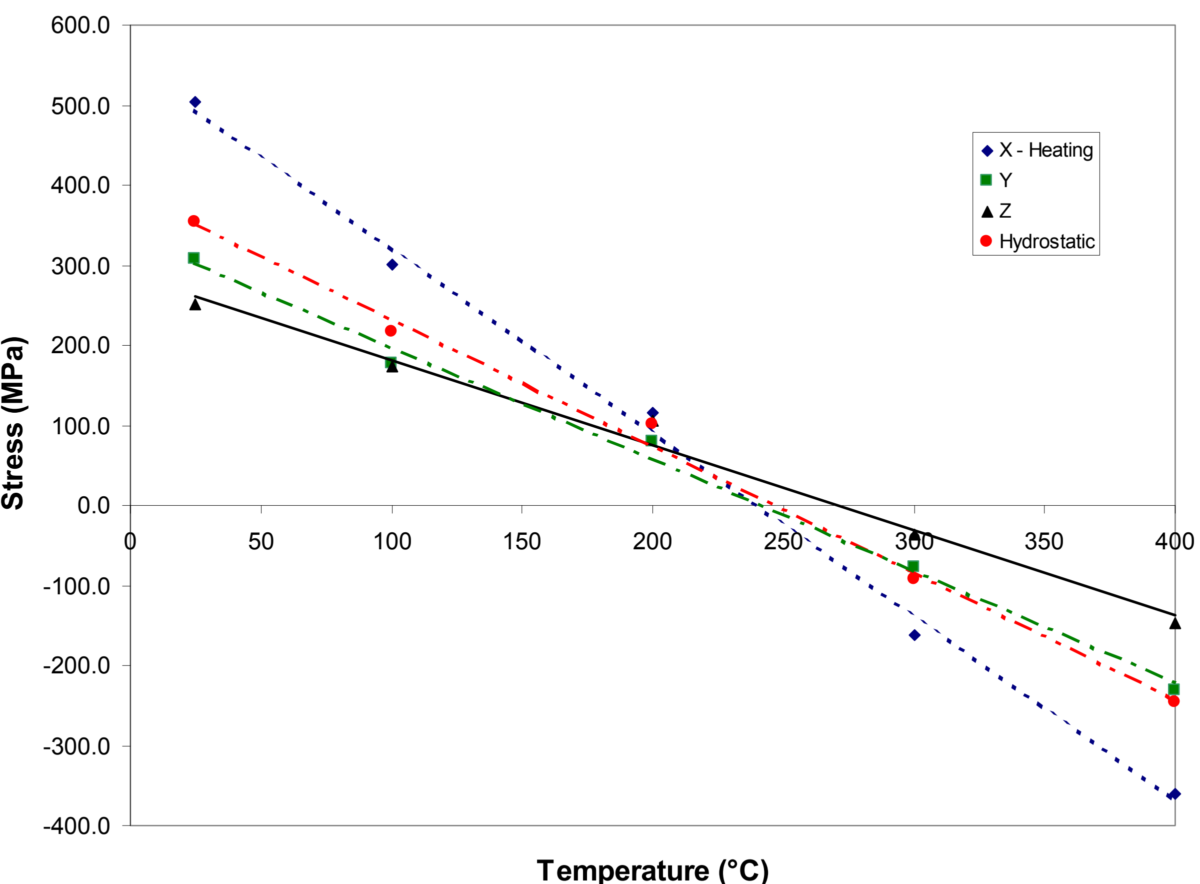
Hydrostatic Stress (MPa)

- Grain boundaries are an incoherent interface with a volume associated with them and can allow stress relaxation. Increasing the grain size reduces the grain boundary volume and increase the stress state.

P.R. Besser et al., Journal of Electronic Materials (April, 2001)

Mechanical stress in passivated Cu lines during heating- AMD samples

AMD



Besser et al., MRS Symp. Proc. Vol. 563 (1999).

What are the implications of this work?

AMD

- **Processing**
  - Microstructure is strongly influenced by processing and integration.
  - Many parameters affect microstructure: barrier type, ILD type and thermal history, BEOL anneals, Cu seed layer thickness and deposition conditions, Cu plating conditions, etc.
  - Increasing anneal time and temperature increases grain size, but also increases stress. High stress levels are not desired for ULK materials. A balance is needed that depends on your integration and material choices.
  - High stress may drive hillocking and extrusions during processing.
- **Electrical testing and Reliability**
  - Microstructure is a function of linewidth.
    - Grain size is bamboo for wide lines.
    - Stress depends on the anneal temperature and grain size.

    } **Not true for Al**
  - Stress migration is tested at 250-350C, as is EM. Your lines may be in compression at these temperatures, depending on your integration and materials. Voiding would not be expected at these temperatures.
  - Electromigration (next page)

Microstructure Conclusions

- Microstructural characterization methods for in-laid Cu lines have been developed.
  - Grain Size (FIB/SEM), Texture (XRD), and Stress (XRD)
  - These methods have been applied to characterize the microstructure of inlaid Cu lines as a function of thermal history.

- <u>Grain Size</u>
  - The mean intercept method was used. Equivalence of TEM and FIB methods was shown.
  - Increasing the anneal temperature or time increases the median grain size of the Cu of the in-laid Cu lines.
  - Significant grain growth is observed during the ILD deposition, if the anneal temperature is lower than the ILD deposition temperature.

Microstructure Conclusions

- Texture
  - The in-laid Cu lines in this study have ***very*** strong (111) fiber texture with a negligible random contribution. (511) or twins are observed.
  - Preferred in-plane orientation of the (111) grains is observed: trench bottom-nucleated (111) oriented prefer a [aa0] sidewall.
  - Texture is independent of anneal (pre or post CMP).
  - Sidewall-nucleated (111) grains are present, independent of anneal conditions and are 5° tilted, following the angle of the trench sidewall. Sidewall grains tend to have [aa0] along trench bottom.
  - For this set of processing conditions (chemistry, waveform, tools, seed and barrier), texture in the field and lines are independent.
- Stress
  - Mechanical stress level in narrow lines is a linear function of the post-plating anneal temperature. This differs from Al, where stress is a function of the ILD deposition temperature.
  - Stress is linearly related to the grain size of the Cu in the trenches.

Electromigration implications

- The effective diffusivity under EM testing is the sum of all diffusivities.

$$D_{eff} = D_b + D_{gb}\left(\frac{\delta_{gb}}{d}\right) + D_{Cu/b}\delta_{Cu/b}\left(\frac{2}{w}+\frac{1}{h}\right) + D_{Cu/N}\left(\frac{\delta_{Cu/N}}{h}\right) + D_s\left(\frac{\delta_{seam} l_{seam}}{h \times w}\right)$$

Bulk | **Grain boundaries** | **Cu/barrier interface** | **Cu/SiNx interface** | **Seam**

- *The fastest diffusion path will dominate the total diffusivity.*
- In general,
  - D_b is negligible for T< .5T_m
  - D_s is zero with good processing.
  - $D_{Cu/b}$ and $D_{Cu/N}$ are believed to be dominant diffusion paths.
  - $D_{Cu/b}$, D_{gb} and $D_{Cu/N}$ are a strong function of the materials.
  - Texture and processing will affect D_{gb}.

Reproduced from J. Appl. Phys. 85(5) 2583 (1999).

Effective Cu Diffusivity

- The effective diffusivity under EM is given by:

$$D_{eff} = D_{gb}\left(\frac{\delta_{gb}}{d}\right) + D_{Cu/b}\delta_{Cu/b}\left(\frac{2}{w} + \frac{1}{h}\right) + D_{Cu/N}\left(\frac{\delta_{Cu/N}}{h}\right)$$

Grain boundaries | **Cu/barrier interface** | **Cu/SiNx interface**

- **Linewidth-**
  - Contribution along barrier is linewidth dependent. Contribution along grain boundaries depends on linewidth also.
- **Barrier-**
  - Changes in barrier affect $D_{Cu/b}$ and contribution along grain boundaries.
- **Annealing Temperature-**
  - Changes in annealing temperature should only affect contribution along grain boundaries

Reproduced from J. Appl. Phys. 85(5) 2583 (1999).

Linewidth dependence of Cu EM

w = 0.36um
w = 1.0 um
w = 2 um
% cumulative probability
1
10
40
70
95
10
100
Failure time (Arb units)

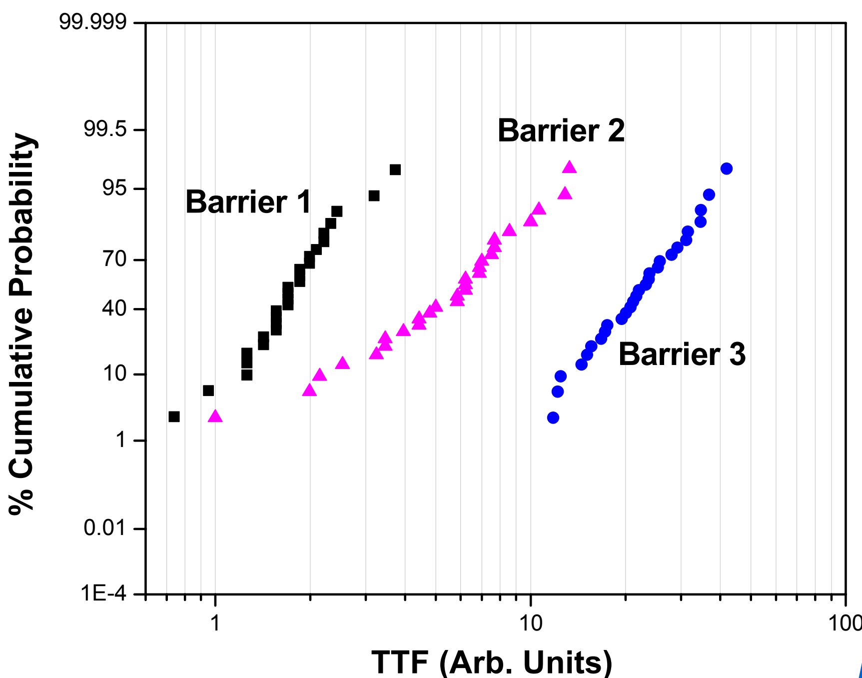
Time to 50% Failure (Arb. Units)
0
50
100
150
200
250
0
0.5
1
1.5
2
2.5
Line width (µm)

- Decreasing the linewidth reduces the MTTF.
- Grain size reduces with decreased linewidth but is bamboo at all linewidths. Texture changes as well.
- The contribution along the barrier is linewidth dependent.
- Dominant diffusion mechanism is along the barrier.

Besser et al., IEEE IEDM 2000 Conference (2000)

Effect of Barrier Type on Cu EM

Barrier Type	Median grain size	Texture results	MTTF (arb. Units)	Activation energy
1	Not Measured	Strong <111>	X	X
2	X	Strong <111>	3 X	X
3	X	<111>	12 X	1.2 X



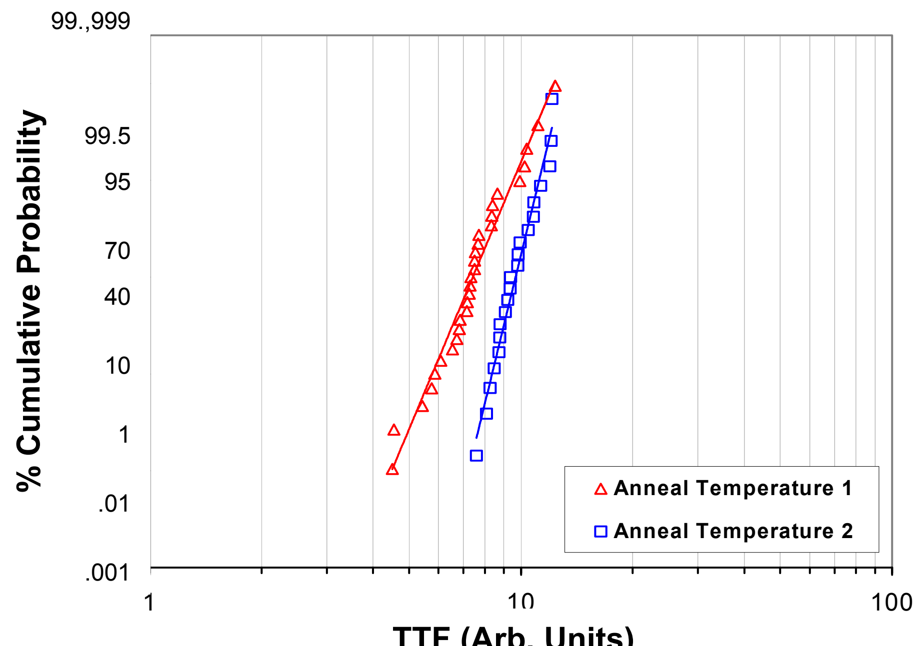
Changing the barrier type did not significantly alter the grain size or crystallographic texture of the Cu in the trenches.

The MTTF and Activation Energy did improve significantly, reflecting changes in $\mathbf{D_{Cu/b}}$.

Besser et al., IEEE IEDM 2000 Conference (2000)

Effect of Anneal Temperature on Cu EM

Anneal Temperature	Median grain size	Texture results	MTTF (arb. Units)	Normalized activation energy
T1	X	Strong <111>	7.2	X
T2	1.3X	Strong <111>	9.5	1.2X



T2 > T1

Increasing the anneal temperature increases the grain size in the trench by 30%, but does not alter the texture.

The MTTF and Activation Energy increase, reflecting the change in D_{gb}.

Besser et al., IEEE IEDM 2000 Conference (2000)

Conclusions

- Methods for quantifying microstructure of inlaid Cu lines (Grain Size, Texture, and Stress) have been presented. The quantification must be performed on lines (rather than films).
- Optimizing the reliability of Cu interconnects requires understanding how changes in processing and materials affect the microstructure of the inlaid Cu lines.
- EM testing has been performed on dual inlaid Cu varying-
  - Barrier type- Microstructure was unchanged (for these experiments) but reliability is strongly dependent on diffusion along the barrier.
  - Linewidth- Grain size and texture change with linewidth as does surface area to volume ratio for the barrier. Dominant diffusion path believed to be barrier.
  - Annealing temperature- Increasing the anneal temperature increases the median grain size of the in-laid Cu lines and increases reliability.
- Microstructure improvements are a secondary reliability improvement method to materials, process and integration improvements.

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