

# Ultra-Low k Spin-on Polymer; Benefits, Challenges and Solutions for Damascene Integration

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✱ Ensemble\* Dielectric Solutions Development Team

✱ porous SiLK\* Dielectric Development Team

✱ SiLK\* Semiconductor Dielectric Development Team

✱ SFM Application Lab Team

# ITRS 2001 - Dielectric needs

<i>Year of Production</i>	<i>2001</i>	<i>2004</i>	<i>2007</i>	<i>2010</i>
<i>DRAM 1/2 PITCH (nm)</i>	130	90	65	45
Interlevel metal insulator - effective dielectric constant (k)	3.0 - 3.6	2.6 - 3.1	2.3 - 2.7	2.1 - 2.4
Interlevel metal insulator (minimum expected) - bulk dielectric constant (k)	< 2.7	< 2.4	<2.1	< 1.9

- K-effective is the goal !
  - ⇒ ILD material selection and integration choice is open
- Most companies will use the same low k ILD material for 2 technology generations but achieve a lower k-effective with a different integration scheme for the second generation.
- Different low k materials can potentially leapfrog each other at successive technology generations

# Low k Spin-on Polymers

✱Benzocyclobutene	$k = 2.7$
✱Fluorinated Polyimide	$k = 2.5 - 2.9 *$
✱Perfluorocyclobutane	$k = 2.4$
✱Polyarylene	$k = 2.8$
✱Polybenzoxazole	$k = 2.6 - 2.9 *$
✱Polynorbornene	$k = 2.5$
✱Polyphenylene	$k = 2.6$

\* anisotropic materials exist in these polymer families

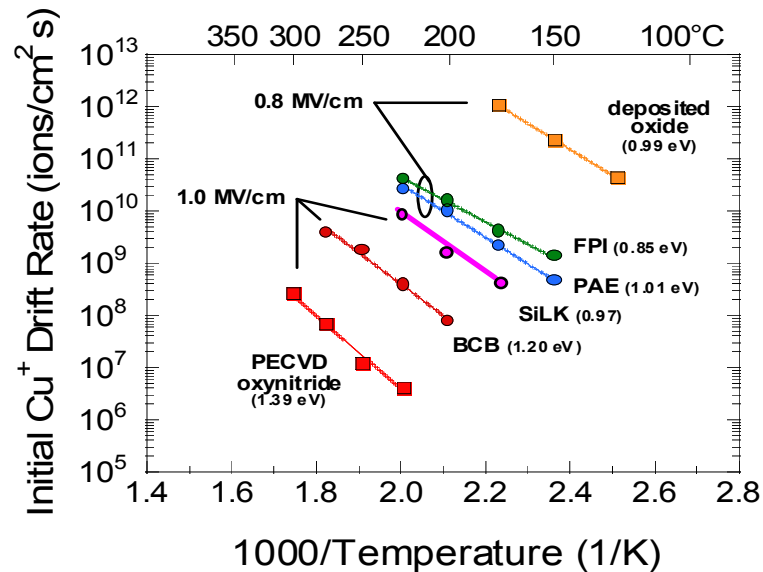
## SiLK Semiconductor Dielectric Properties

Thermal Stability @ 450 °C	< 1% / hr weight loss
Glass Transition	> 490 °C
Dielectric Constant @ 1 MHz	2.6 (isotropic)
Refractive Index @ 633 nm	1.62
Moisture Uptake (25 °C / 85% RH)	< 0.24 % (wt)
Expansion Coefficient	62 ppm / °C (50-150 °C)
Film Stress @ 25 °C	60 MPa (tensile)
Thermal Conductivity	0.23 W / mK @ 125 °C
Voltage Breakdown	> 4 MV/cm
Hardness (indentation)	0.29 GPa
Modulus (indentation)	3.6 MPa
Toughness	0.62 MPa m <sup>1/2</sup>
Strength (tensile)	93 MPa

This does not look like Oxide !

## Low k Spin-on Polymer Material Property Benefits

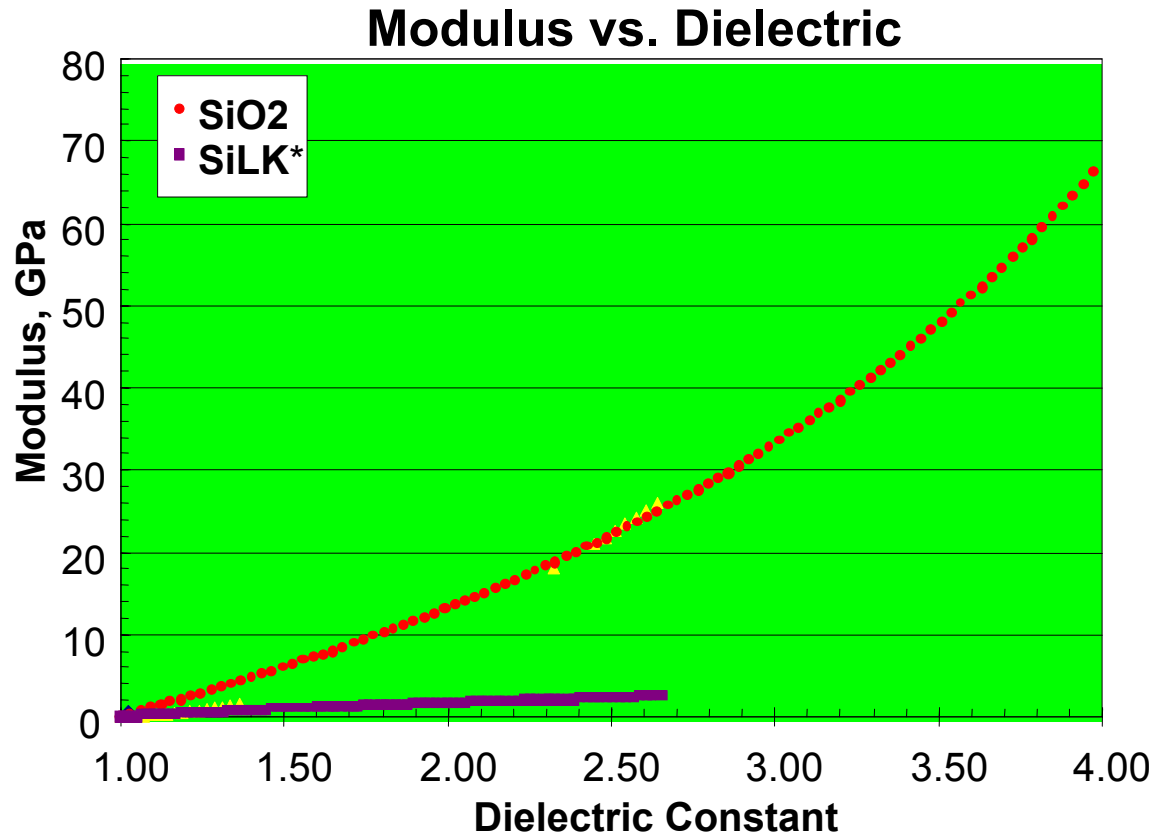
### Initial $\text{Cu}^+$ Drift Rates



Ref: Loke *et al.*, "Copper Drift in Low-*K* Polymer Dielectrics for ULSI Metallization," presented at the 1998 Symposium on VLSI Technology (Honolulu, HI), June 9, 1998.

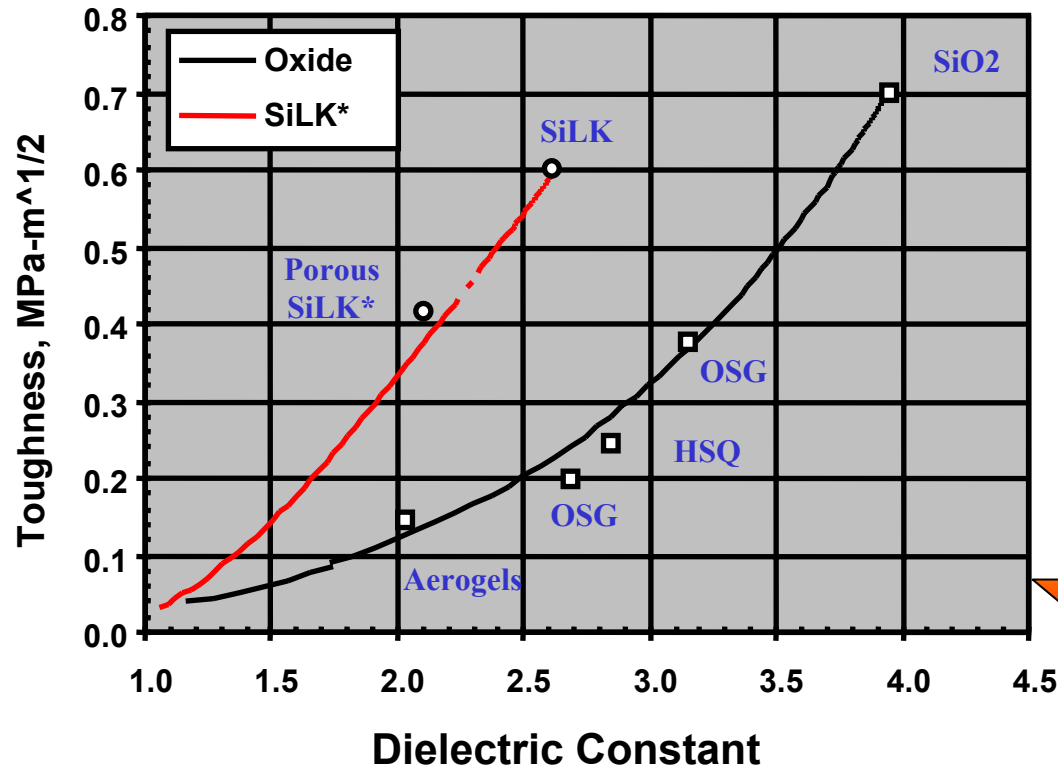
- Low k Spin-on Polymers have Cu drift rates approaching SiN and are more than 10<sup>4</sup> times lower than oxide or oxide based (OSG) ILD materials

## Low k Spin-on Polymer Material Property Challenges



- Modulus and hardness will decrease for all materials when voids (air) is introduced
- At  $k < 2.6$ , all ILD materials will have a modulus significantly less than the metal conductor (Cu)

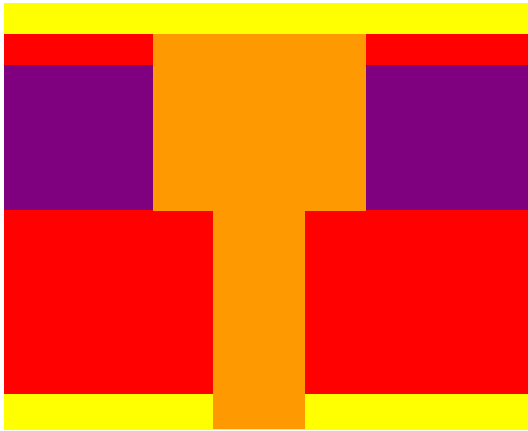
## Low k Spin-on Polymer Material Property Solutions Fracture Toughness



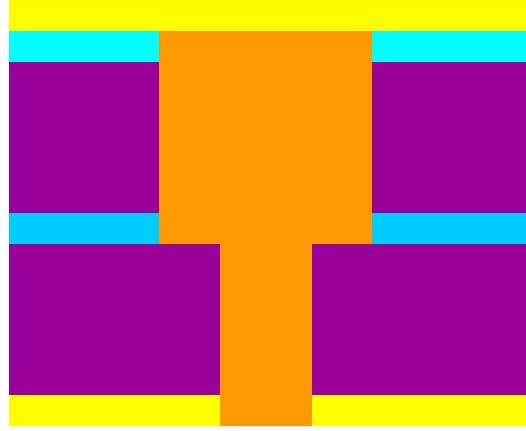
Increasing  
CMP & Packaging  
concerns

- Toughness determines CMP survivability not hardness or modulus for polymers.
- Polymers have almost the same toughness as oxide and are significantly tougher than OSG materials at equivalent k values

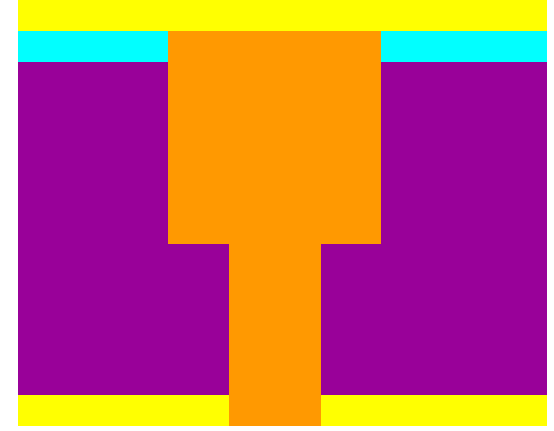
## Low k Spin-on Polymer Integration Processes



Hybrid ILD  
Integration



Buried Etch Stop  
Integration

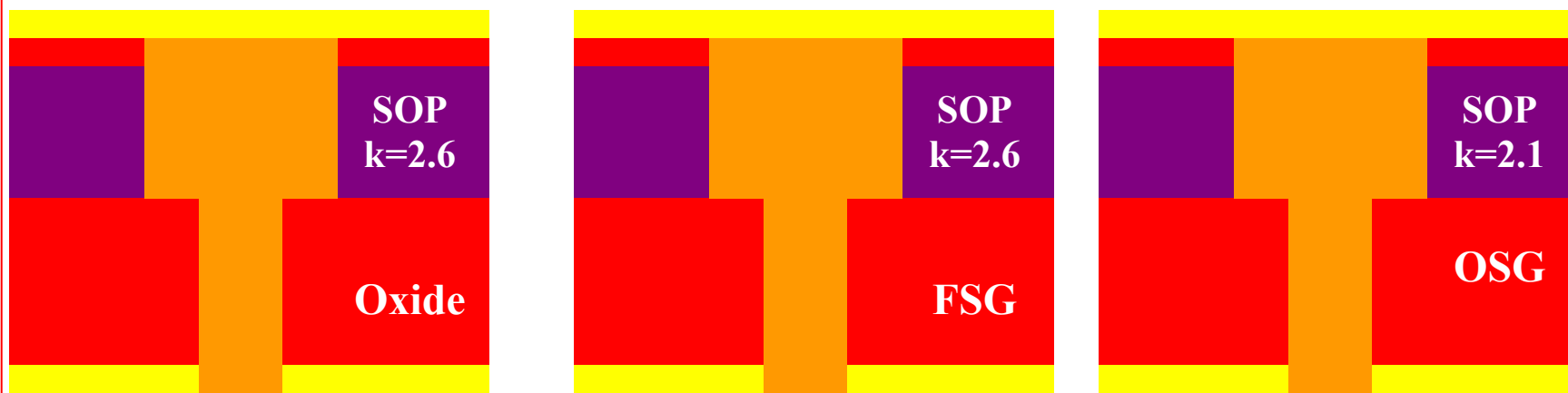


Timed Etch  
Integration



- Extendible K-effective roadmap
- Leveraged development knowledge through multiple technology generations
- CoO reduction roadmap

## Low k Spin-on Polymer Hybrid Integration Processes



Oxide  
Hybrid ILD  
Integration

FSG  
Hybrid ILD  
Integration

OSG  
Hybrid ILD  
Integration



- Extendible K-effective roadmap
- Leveraged development knowledge through multiple technology generations
- Multiple Low k strategy entry points

## Low k Spin-on Polymer Integration Modules

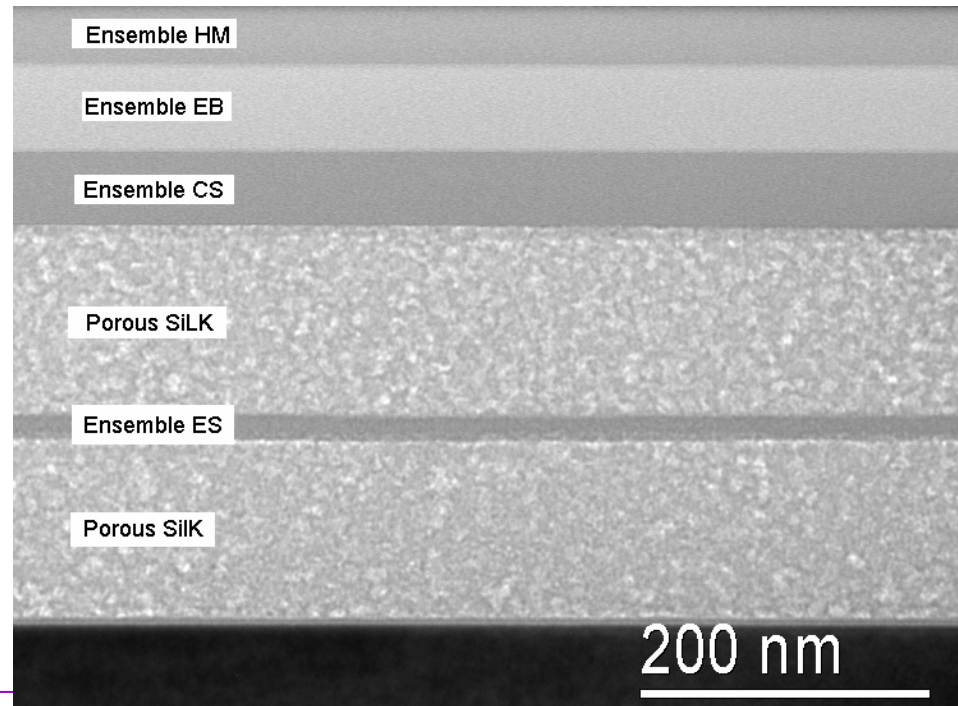
### Challenge

Availability of integrated all spin-on dielectric stack

### Solution

All dielectric layers deposited sequentially with a single final cure per interconnect layer !

Dielectric Dep.
Lithography
Etch
Clean
Metal Barrier
CMP
Packaging
Reliability
Extendibility



## Low k Spin-on Polymer Integration Modules

Dielectric Dep.
Lithography
Etch
Clean
Metal Barrier
CMP
Packaging
Reliability
Extendibility

### Challenge

Compatibility with 248nm, 193nm, ... photoresist

### Solution

Most low k spin-on polymer materials do not contain any amine (NH) structures nor are they prone to amine absorption during etch and clean processing !

## Low k Spin-on Polymer Integration Modules

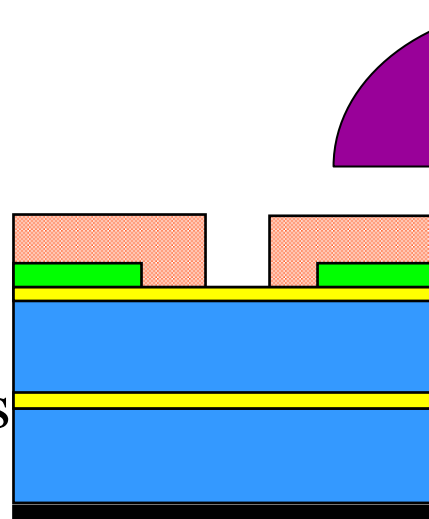
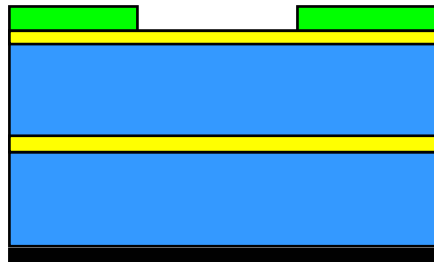
### Challenge

Availability of a photoresist rework process

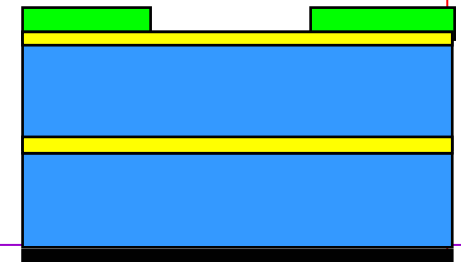
### Solution

Dual Hard mask integration scheme !

Dielectric Dep.
Lithography
Etch
Clean
Metal Barrier
CMP
Packaging
Reliability
Extendibility



Standard  
Ash  
Process



- Bottom hardmask protects polymer during ash
- Top hardmask is removed during CMP to lower k-effective

## Low k Spin-on Polymer Integration Modules

### Challenge

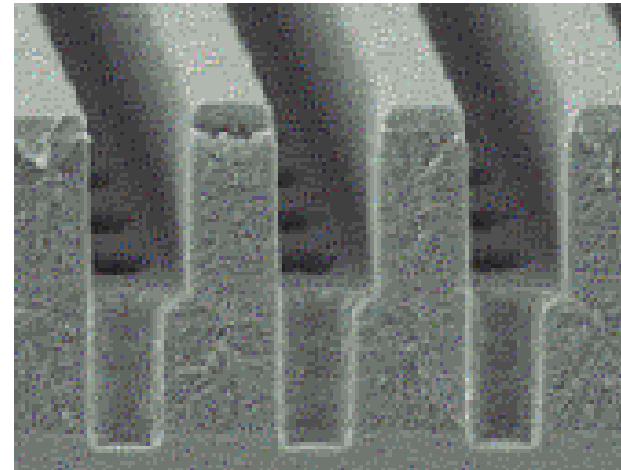
Etch of high aspect structures in damascene integration

### Solution

Dual Hard mask materials offer an etch selectivity of greater than 20:1 !

Dielectric Dep.
Lithography
Etch
Clean
Metal Barrier
CMP
Packaging
Reliability
Extendibility

- Both “timed etch” and “buried etch stop” integration schemes have been demonstrated

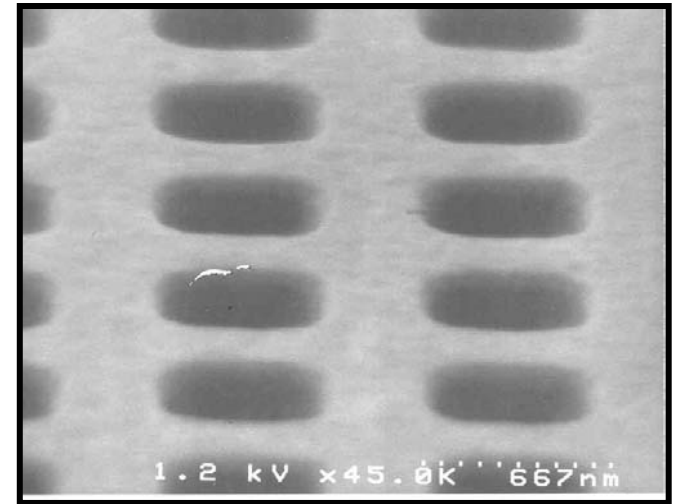
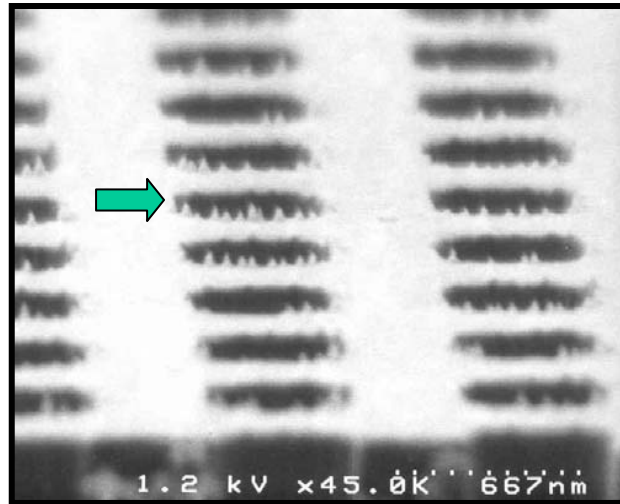


Courtesy of Tokyo Electron, Ltd.



## Porous SiLK

Before wet clean processing    After wet clean processing



- Depending on the etch chemistry
- Post etch clean removes this material prior to metallization
- Cleaning similar to dense SiLK

Dielectric Dep.

Lithography

Etch

Clean

Metal Barrier

CMP

Packaging

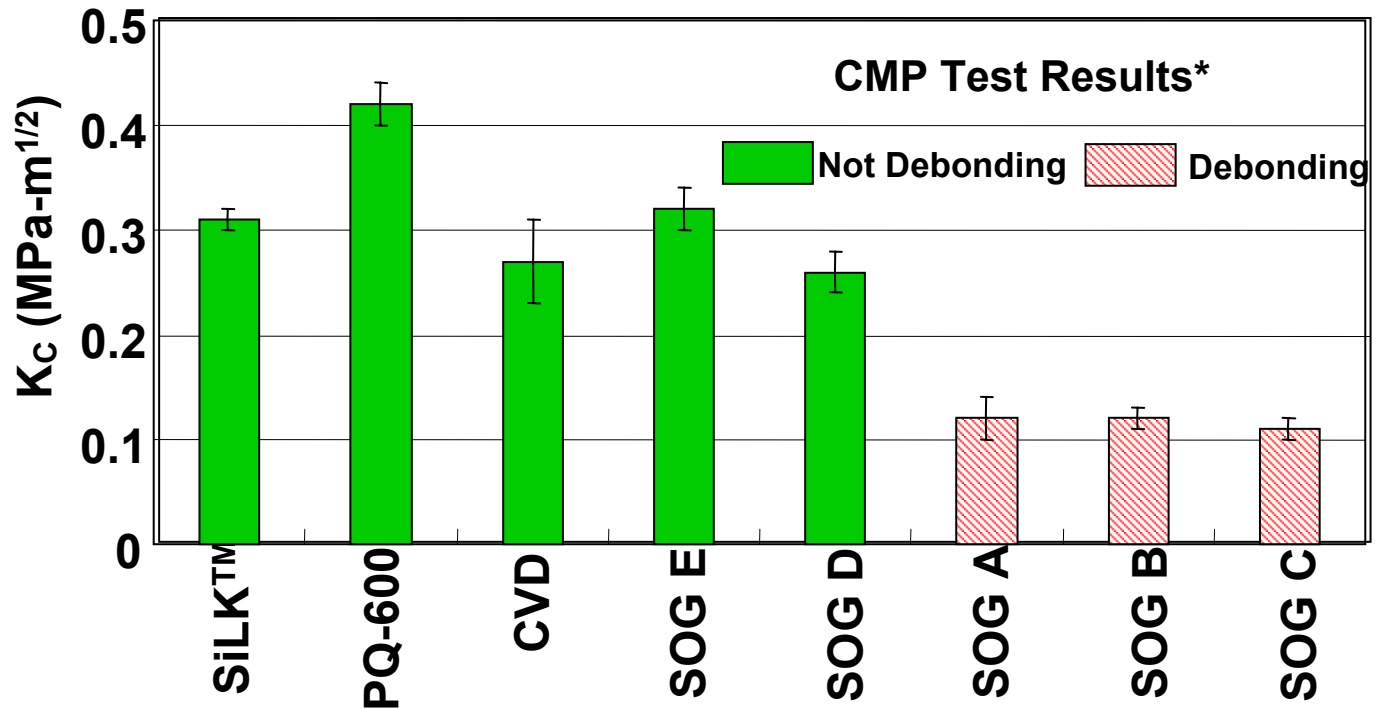
Reliability

Extendibility

## Low-k Materials in CMP

*Minimum Toughness/Adhesion Threshold to survive CMP*

Dielectric Dep.
Lithography
Etch
Clean
Metal Barrier
<b>CMP</b>
Packaging
Reliability
Extendibility

*Ohta et. al., JAPS Sept. 2000*

Dielectric Dep.

Lithography

Etch

Clean

Metal Barrier

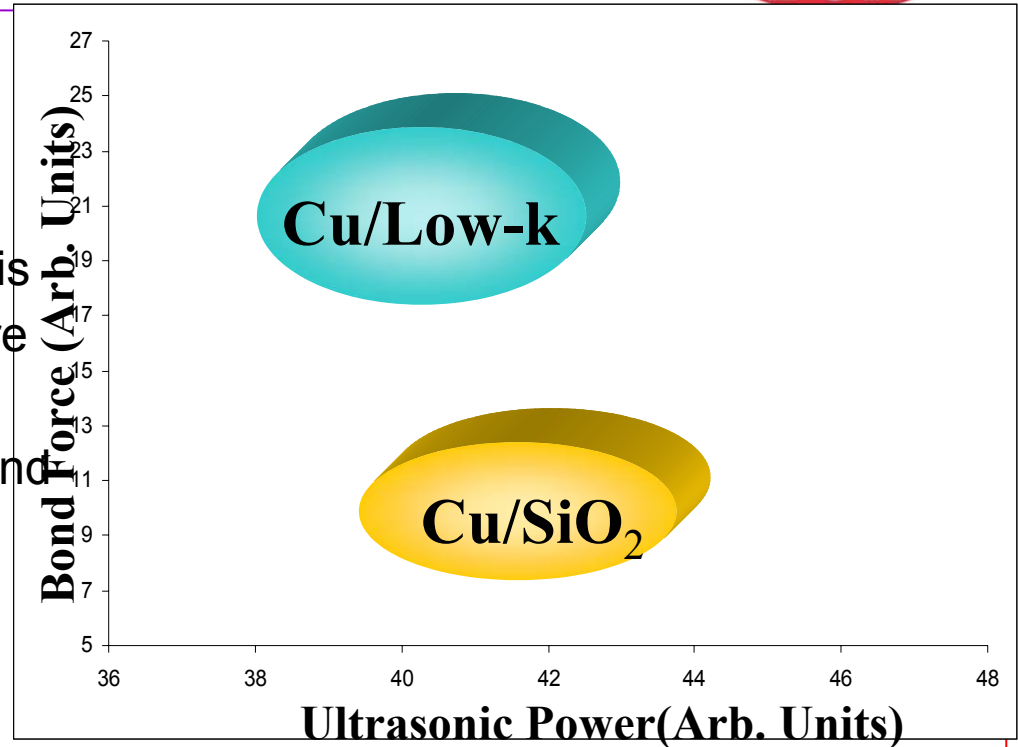
CMP

Packaging

Reliability

Extendibility

- Higher Bond force is necessary to ensure intimate contact between the wire and bond pad.

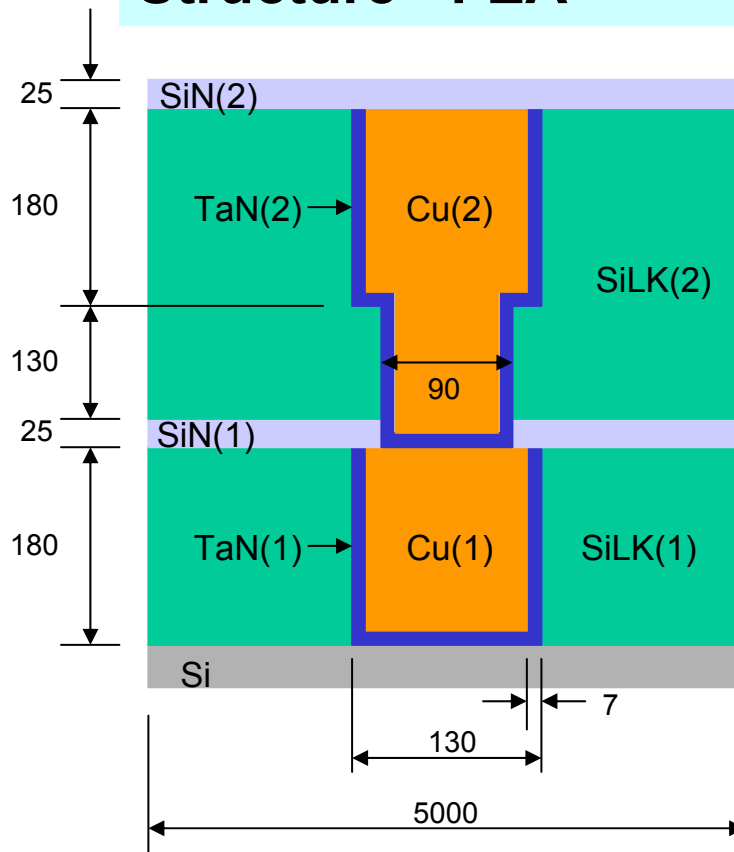


- Inter metallic coverage and ball shear value was observed slightly less due to less efficient energy transfer to the wire/pad interface.
- With careful optimization of bond process parameter or wire bond pad design, good bond with tensile failure on the bond wire at the neck during wire pull can be achieved

# Sequential Processing Modeling

Dielectric Dep.
Lithography
Etch
Clean
Metal Barrier
CMP
Packaging
Reliability
Extendibility

## Stacked Via Structure - FEA



### Simulation Steps

- step 1: SiLK(1) cured at 400C
- step 2: Cool down to 20C
- step 3: Heat up to 350C
- step 4: Numerical CMP of TaN(1)
- step 5: TaN(1) deposition
- step 6: Cool down to 100C
- step 7: Numerical CMP of Cu(1)
- step 8: Cu(1) plating
- step 9: Heat up to 350C
- step 10: SiN(1) deposition
- step 11: Heat up to 400C
- step 12: SiLK(2) cured at 400C
- step 13: Cool down to 20C
- step 14: Heat up to 350C
- step 15: Numerical CMP of TaN(2)
- step 16: TaN(2) deposition
- step 17: Cool down to 100C
- step 18: Numerical CMP of Cu(2)
- step 19: Cu(2) plating
- step 20: Heat up to 350C
- step 21: SiN(2) deposition
- step 22: Cool down to 20C

## Stress of Stacked Via Structure

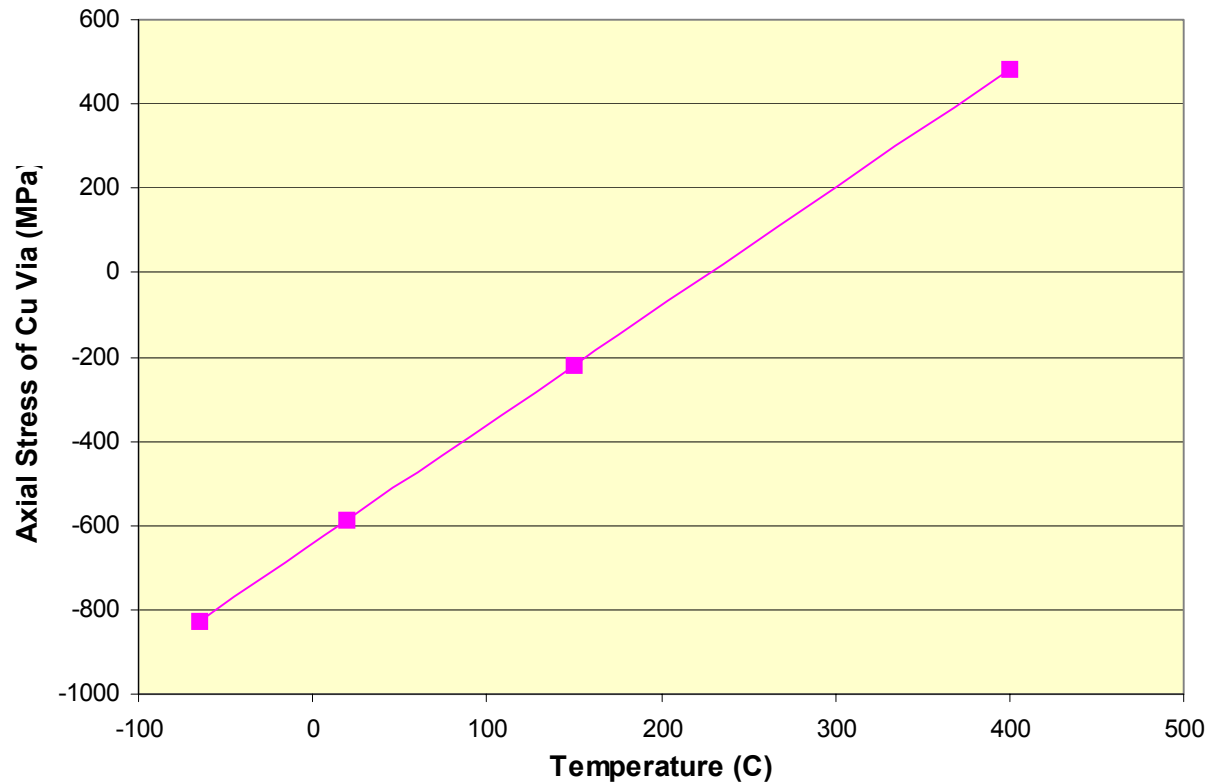
### • Simulation Steps

- step 1: SiLK(1) cured at 400C
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- step 5: TaN(1) deposition
- step 6: Cool down to 100C
- step 7: CMP of Cu(1)
- step 8: Cu(1) plating
- step 9: Heat up to 350C
- step 10: SiN(1) deposition
- step 11: Heat up to 400C
- step 12: SiLK(2) cured at 400C
- step 13: Cool down to 20C
- step 14: Heat up to 350C
- step 15: CMP of TaN(2)
- step 16: TaN(2) deposition
- step 17: Cool down to 100C
- step 18: CMP of Cu(2)
- step 19: Cu(2) plating
- step 20: Heat up to 350C
- step 21: SiN(2) deposition
- step 22: Cool down to 20C



# Stress during Thermal Cycle

After Step 22



Dielectric Dep.

Lithography

Etch

Clean

Metal Barrier

CMP

Packaging

Reliability

Extendibility

## Low k Spin-on Polymer Integration Modules

Dielectric Dep.

Lithography

Etch

Clean

Metal Barrier

CMP

Packaging

Reliability

Extendibility

✱ Extendibility is the key to maintaining pace with the ITRS and the IC Industry

✱ Leveraging 70-80% of the process knowledge from the previous technology node is as important as high utilization of the existing tool set

## Low k Spin-on Polymer Extendability Microstructure Challenges

Dielectric Dep.
Lithography
Etch
Clean
Metal Barrier
CMP
Packaging
Reliability
Extendability

### Small Pore Size

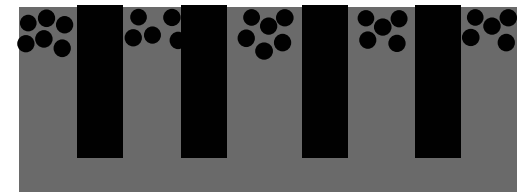


...protection from  
electrical shorts

*and*



### Uniform Distribution

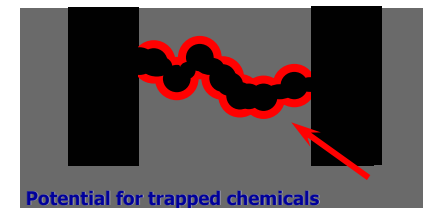


...mechanical integrity,  
dielectric performance

*and*



### Closed Pore System

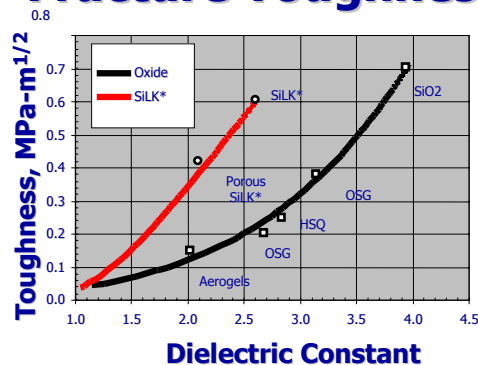


...protection from  
trapped mat'ls, device  
yield

*and*



### Fracture Toughness



## Low k Spin-on Polymer Extendibility

# Templated Pore Solution

"one poragen yields one pore"

Poragen  $\Rightarrow$  Pre-formed nano-particles

Inherent advantages:

- doesn't rely on nucleation and growth
- less process dependent

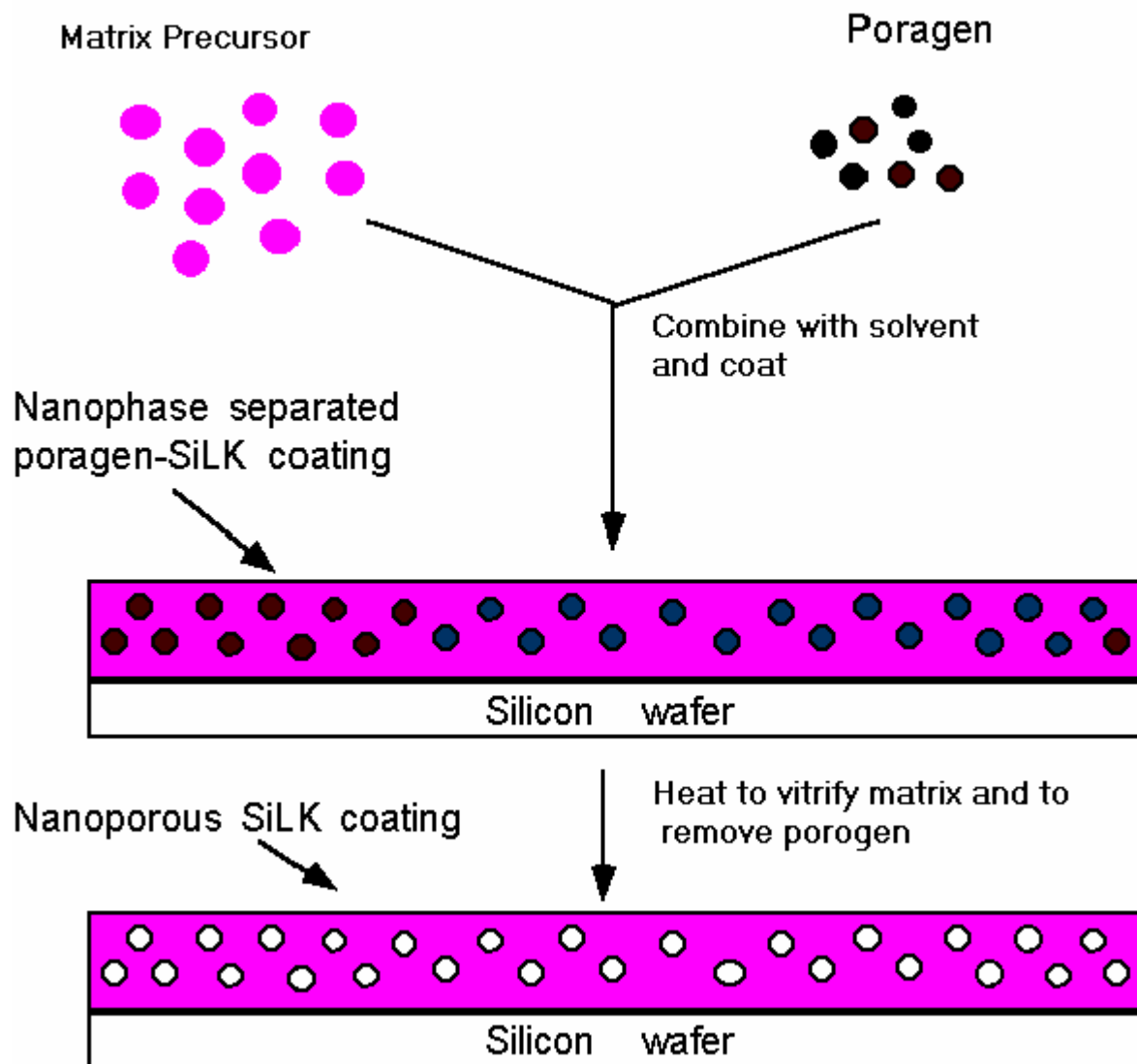
Technical challenges:

- < 10 nm size is a new frontier
- particles must be isolated
- requires a metal free process

Dielectric Dep.
Lithography
Etch
Clean
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CMP
Packaging
Reliability
Extendibility

## Low k Spin-on Polymer Extendibility

Dielectric Dep.
Lithography
Etch
Clean
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Packaging
Reliability
Extendibility



## Low k Spin-on Polymer Extendibility

### Porous SiLK Evolution: V1 $\Rightarrow$ porous SiLK

Dielectric Dep.

Lithography

Etch

Clean

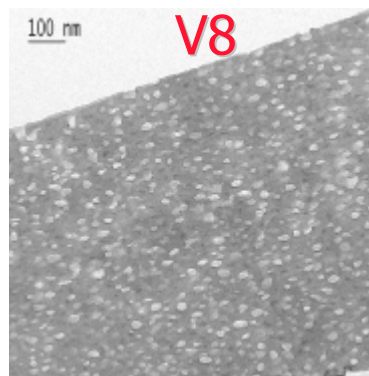
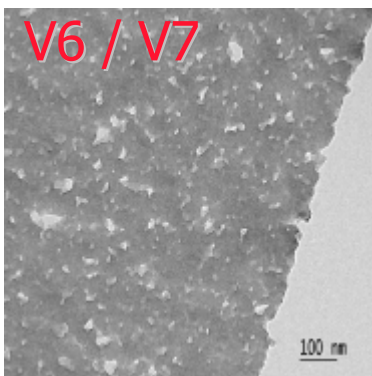
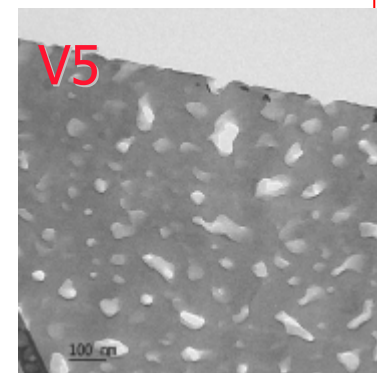
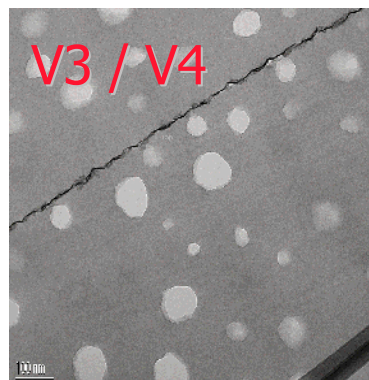
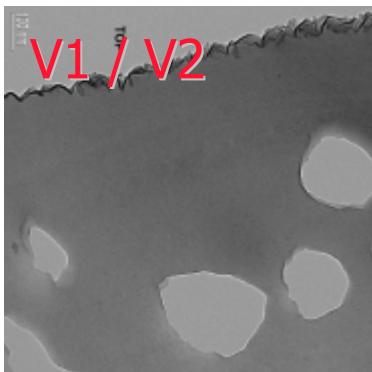
Metal Barrier

CMP

Packaging

Reliability

Extendibility



## Low k Spin-on Polymer Extendibility

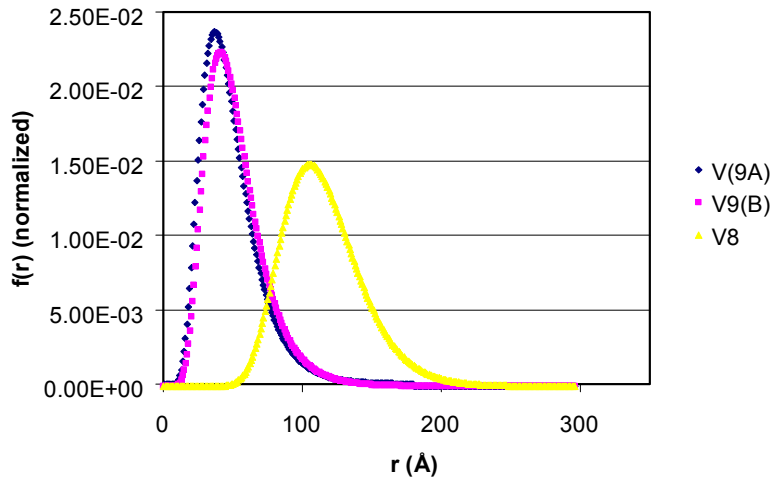
Dielectric Dep.
Lithography
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Extendibility

	SiLK	V7	V8	Porous SiLK
K	2.65	2.35	2.20	2.10
D <sub>avg</sub> (nm)	NA	25	16	< 10
Modulus (GPa @ 1 um)	3.6	2.8	2.7	2.8
Hardness (GPa @ 1 um)	0.27	0.17	0.16	0.15
CTE	62	62	62	~ 62
Toughness / Adhesion (Mpa-m <sup>0.5</sup> )	> 0.35	> 0.35	> 0.35	> 0.35
Process Temperature (°C)	400 – 450	430	430	400

- Extendible material that leverages processing knowledge

## Low k Spin-on Polymer Extendability

Log-Normal Distributions for Porous SiLK™



Dielectric Dep.

Lithography

Etch

Clean

Metal Barrier

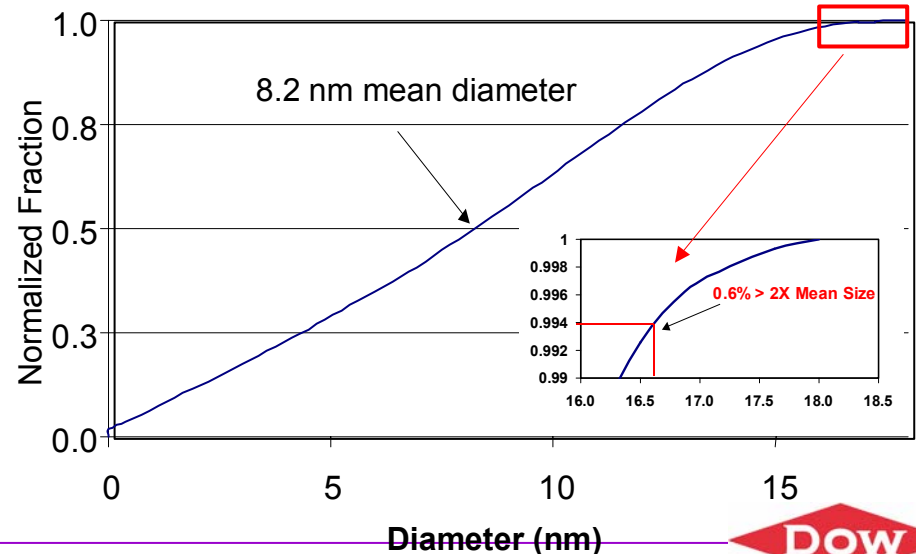
CMP

Packaging

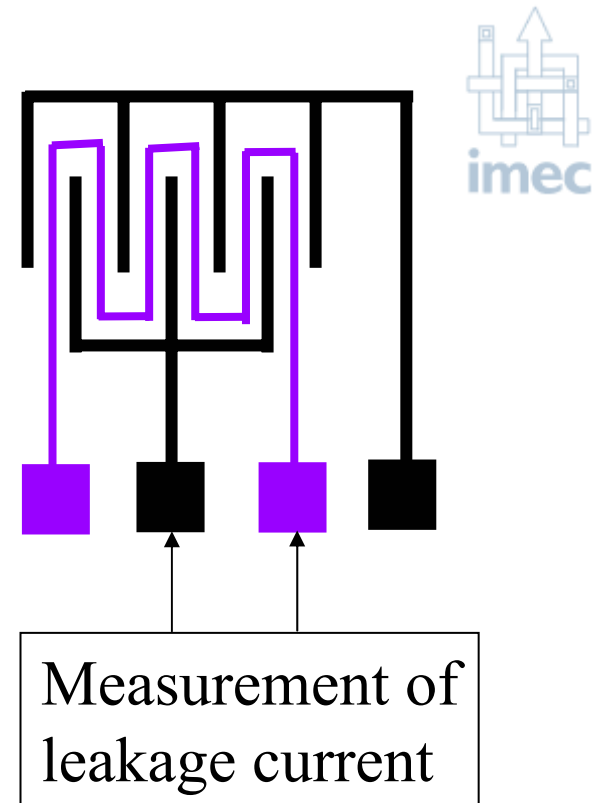
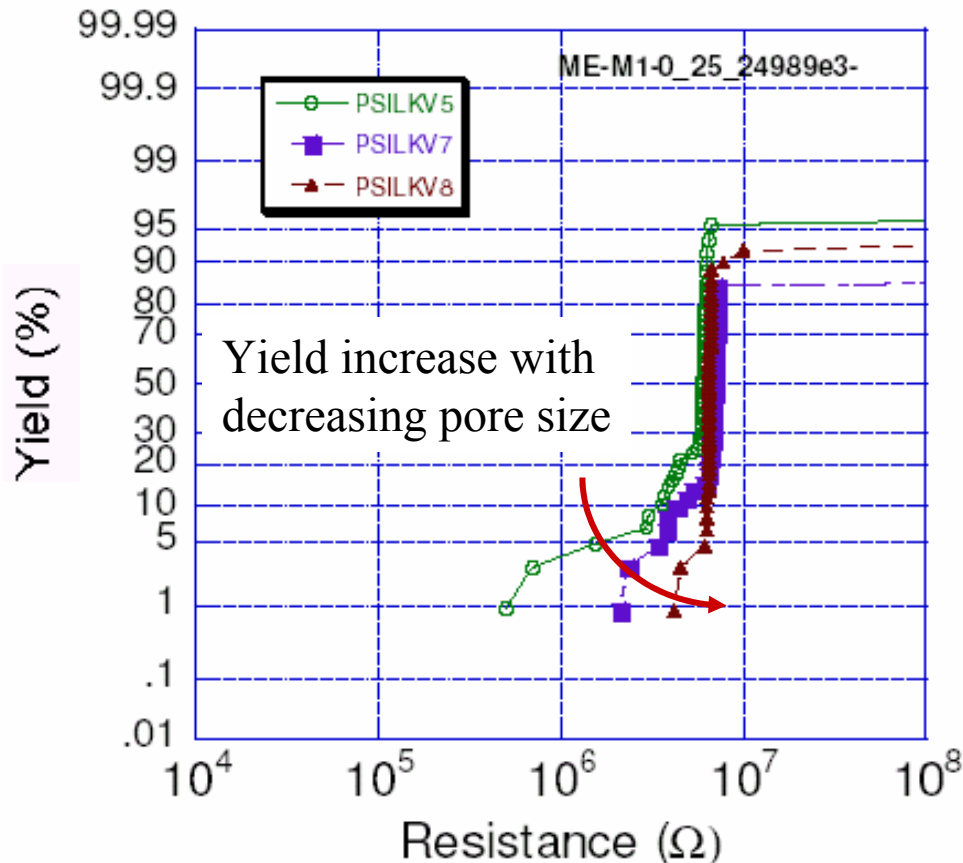
Reliability

Extendability

- Continual reduction in pore size (closed) and pore size distribution
- Good barrier metal integrity



# Pore Size Impact on Yield



→ 25 m meander line required to observe electrical differences (50 m effective length)

# Summary

## Challenges for Low k Spin-on Polymers

✱ Polymer mechanical properties are not like oxide and will require different integration and design mindset

## Benefits of Low k Spin-on Polymers (SiLK)

- ✱ Chemistry is unchanged since the mid 1990's
- ✱ Compatible with all existing process modules and tools
- ✱ Extendible versions, lower dielectric constant ( $k=2.1$ ), are already available
- ✱ Existing materials meet ITRS targets for  $k$  and  $k$ -effective through 45nm technology
- ✱ Have passed full reliability qualification at 130nm and 90nm
- ✱ In manufacturing at 130nm already