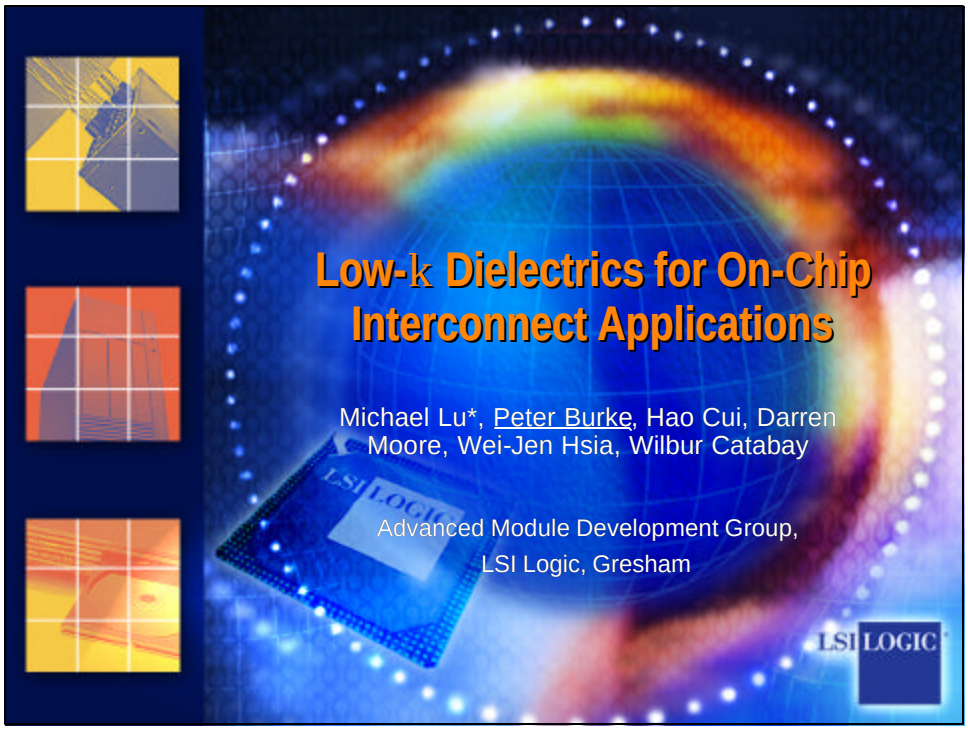


Acknowledgement

- Advanced Process Module Development Group, LSI Logic, Gresham.
- Process Integration Group, Santa Clara R&D, LSI Logic.
- Process Transfer Group, Gresham, LSI Logic
- Gresham Manufacturing Group, LSI Logic

Outline

- LSI Low-k Roadmap and History
- Why we need low-κ dielectrics for on-chip interconnect?
- How to achieve low dielectric constant?
- low-κ material choice and their properties.
- Process Integration Challenges.
- Summary

low-κ dielectric: a dielectric material which has a dielectric constant lower than that of silicon dioxide, and can be served as an insulator between metal wires in IC interconnect.

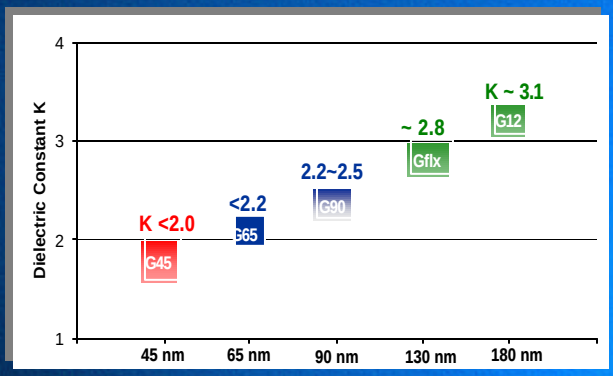
IRTS Roadmap for Lowk Dielectrics

Technology Node	250 nm	180 nm	130nm	90nm	65nm
# of metal layer	5-6	6-7	7-8	8-9	9-10
Local wiring pitch (nm)	650	460	320	180	130
1997					
effective dielectric constant	3.0-4.1	2.5-3.0	1.5-2.0	1.5-2.0	<1.5
IRTS1999					
effective dielectric constant		3.5 - 4	2.7-3.5	1.6 - 2.2	<1.5
IRTS2001					
bulk dielectric constant		3 - 4	<2.7	<2.4	<2.1
effective dielectric constant		3.5 - 4	3.0-3.6	2.6-3.1	2.3-2.7
LSI Roadmap					
bulk dielectric constant	4	3.1	<2.8	<2.2	<2.0
effective dielectric constant	4	3.3	<3	<2.5	<2.2

The original lowk roadmap is very aggressive, but the industry proved to be more conservative due to integration challenges.

LSI Logic Low-k Roadmap

LSI Logic believe that low-k dielectric is the performance driver for the BEOL interconnect, and is aggressively pursuing low-k material solutions that meets our technology requirements.



LSI Low-k History

- LSI: first Semiconductor user of OSG (k< 3.3) low-k materials in large volume production.
  - G12, 0.18 µm node, Trikon Flow-fill lowk.
- Foundry compatible FSG process for 0.18 µm technology: CMOS18
- Gflx 0.13µm node: Cu/Low-k BEOL
  - Dual Damascene, with k-value < 3.0
- Demonstrated single level Copper with ULK 2.2
- Demonstrated in-house k ~ 2.0 PECVD

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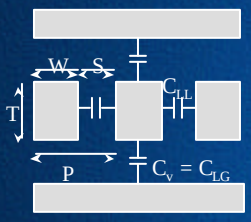
Motivation - Why we need low-k dielectrics?

Reduce parasitic BEOL capacitance

- To reduce the interconnect time delay (RC)
- To reduce the power consumption
- To minimize the cross-talking

Reduce RC delay *(skipped)*



$$RC = 2r k e_0 (4L^2/P^2 + L^2/T^2)$$

RC could be reduced by:
1. **Reduce metal resistivity. (r)**
2. **Reduce dielectric constant (k)**
3. **Optimize BEOL architecture (L, P, T)**

Current BEOL Architecture Trend

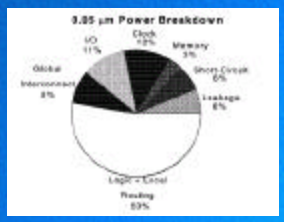
- Ideally, If L, P and T scale at same rate, the RC delay will be kept constant, as device feature size shrinks.
- But in reality, L does not scale at same rate as other backend parameter. As chip size increases, L increases accordingly, which makes RC increases dramatically as we move into deep-sub-micron technology node.

Reduce chip power consumption *(skipped)*

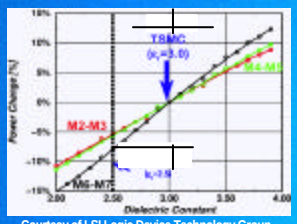
- Majority of chip power is consumed by transistor dynamic transition activities, which is proportional to

$$P \propto \alpha N C_L V^2 f$$

(α : transistor transition activity factor, N: total number of transistor, C: load capacitor, V: supply voltage, f: operation frequency)



- Total power consumption increases dramatically as device speed improves ($f\uparrow$) and chip density increases ($N\uparrow$).
- As device feature size reduces, interconnect capacitance becomes more and more dominant in total transistor capacitance load.

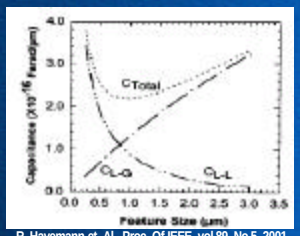


Courtesy of LSI Logic Device Technology Group

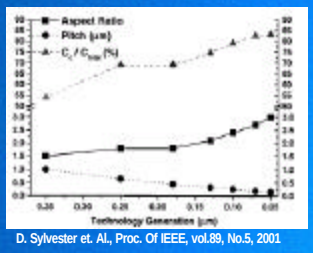
- Reducing Interconnect capacitance will reduce the total power consumed by the chip.

Reduce Cross Talk *(skipped)*

- On-chip cross talk becomes a major issue in ULSI circuits as BEOL feature size continue to scale down.
  - Reducing line-to-line spacing, increasing aspect ratio, larger die size, and reduced noise margin due to supply voltage drop.
- Cross talk is proportional to the ratio of line-to-line coupling capacitance to total line capacitance



R. Havemann et. Al., Proc. Of IEEE, vol.89, No.5, 2001



D. Sylvester et. Al., Proc. Of IEEE, vol.89, No.5, 2001

- Reducing the dielectric constant of intra-metal dielectric will help reducing the cross talk.

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What is dielectric constant?

- The dielectric constant represents **the polarizability of the material upon an electric field**.

$$\frac{e-1}{e+2} = \frac{1}{3e_o}\sum N_j a_j$$

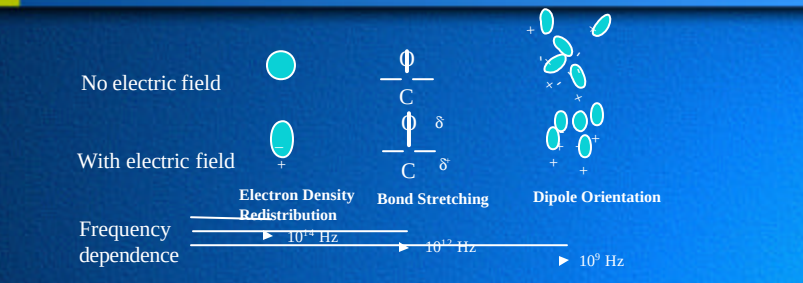
(where Nj is the total number of jth atom or molecules, and aj is the polarizability of that particular atoms or molecules.)

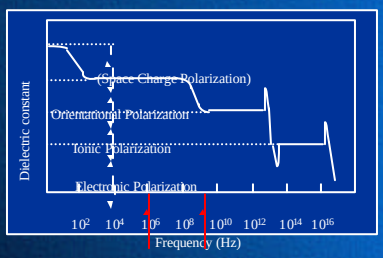
- Generally speaking, there are 3 polarization mechanism, which are additive.

$$\alpha = \alpha_{electronic} + \alpha_{atomic} + \alpha_{dipolar}$$

- To reduce dielectric constant, we need to reduce the $N\alpha_j$ product.

Frequency dependence of dielectric constant





- Dielectric constant decreases with increasing frequency.
- At optical frequency, $\varepsilon_\infty = \varepsilon_{electronic} = (n_{ref})^2$

General rules to reduce dielectric constant
(skipped)

- Minimize polarizability:
  - Avoid polar molecules such as carbonyl groups .

Group contribution to molar dielectric polarization P_{LL} in isotropic polymers

Group	P_{ll}	Group	P_{ll}
—CH_3	5.64		10
—CH_2—	4.65	—COO—	15
	3.62	—F	1.8
	2.58	—Cl	9.5
	25.5	—CF_2—	6.25
	25.0	—OH (alcohol)	6
—O—	5.2	—OH (phenol)	~20

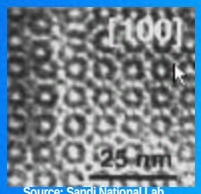
General rules to reduce dielectric constant

- Minimize polarizability
  - Use building elements with smaller electronic polarizability
    - Atoms with smaller atomic radius, such as F, C etc.
      - F-based low-κ dielectrics: FSG (fluorinated silicate glass), PTFE (Teflon).
      - C-based lowk dielectrics: OSG (organosilicate glasses), SiLK, etc.
    - Carbon-carbon double or triple bonds should be avoided because of the mobility of p electron.
      - The downside to avoid double bond is lower bond strength, which means lower stability, and weaker mechanical properties.

General rules to reduce dielectric constant

- Increase the free volume – reduce the total number of atoms and molecules (N) inside the material.
  - Microscopic level:
    - increase the bonding length, bonding orientation, for example: Si-O has bond length of 1.5097 Å, and Si-CH3 has 1.857 Å bond length.
    - discontinue the chain by inserting single bond atoms or groups into the backbone structure. For example, adding F or CH3 into SiO2 network.
  - Macroscopic level: adding porosity, such as Xerogel, Nanoform etc.
    - incorporation of a thermally degradable material (porogen) within a host thermosetting matrix.
    - "solvent-as-porogen": uses a high boiling point solvent as the porogen,

MesoELK



Source: Sandi National Lab

- LSI Low-k Roadmap and History
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Low-k Material Choices *(skipped)*

Material Catalog	k=4.1	k=3 - 4	k=2.5 - 3	k=2.0 - 2.5	Process	Vendor
Inorganic	SiO2	F-doped SiO2	Fox	XLK Nanoglass Silica xerogels, Silica aerogels	Spin on Spin on Spin on	Dow Corning Honeywell
Hybrid		Trikon Flowfill C-doped TEOS	Trikon Flowfill BD I Coral Trikon 2.8 Aurora 2.7 JSR LKD HOSP HSG ALCAP-S OCD	BD II Orion Aurora 2.4 JSR LKD AMAT ELK HOSP ELK HSG ALCAP-S OCL	CVD PECVD PECVD PECVD PECVD PECVD Spin on Spin on Spin on Spin on Spin on	Trikon AMAT NLVS Trikon ASMI Hitachi (IITC) JSR AMAT Honeywell Hitachi Asahi Chemical Tokyo Ohka
Organic			SILK FLARE PolyELK, MesoELK	Porous SILK FLARE ELK PTFE Polyimide nanofoams	Spin on Spin on Spin on Spin on Spin on	Dow Chemical Honeywell Schumacher W.L. Gore

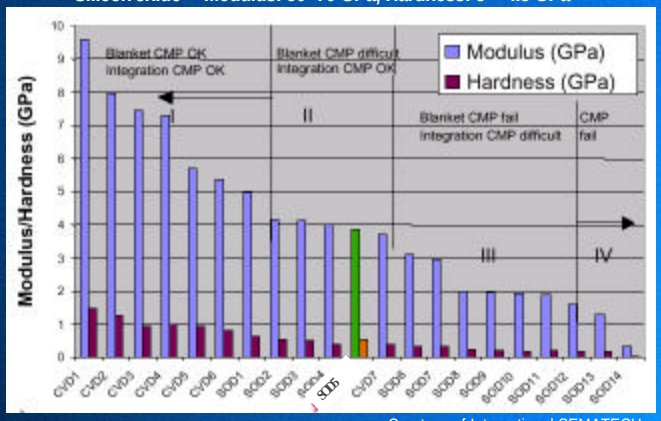
Desired Characteristic of Low-k Dielectrics

- It must exhibit adequate material properties (thermal, electrical, and mechanical)
- It must be able to work with the other materials of the interconnect structure (Cu, etc.)
- It must be compatible with the IC processes of cleaning, etch, CMP and thermal treatment.
- It must be available in high purity form, and lost cost.
- It must be able to operate reliably over the life of the product under the specified device operating conditions.

Low-k CMP

CMP performance depends strongly on the mechanical property of the low-k material

Silicon oxide -- Modulus: 50~70 GPa, Hardness: 3 ~ 4.5 GPa

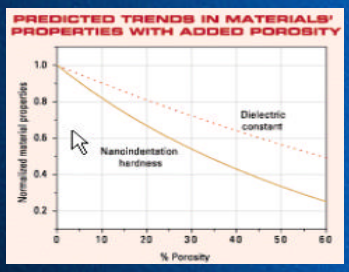


Courtesy of International SEMATECH

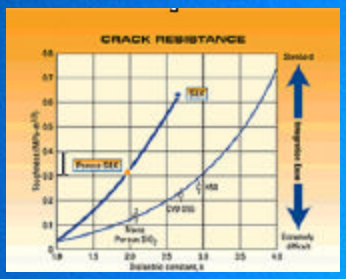
Low-k CMP

It is found that low-k mechanical properties degrade much faster as dielectric constant reduces, which makes integration of ultra-low-k material much more difficult.

Low-k hardness vs. film porosity



Low-k Toughness vs. dielectric constant



Desired Material Properties *(skipped)*

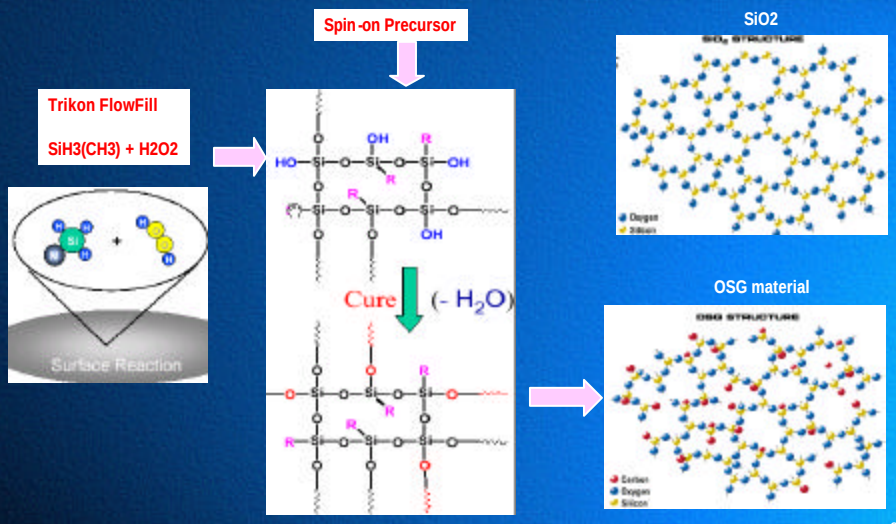
Elelctrical	
Dielectric constant	depend on technology node, <3.0 for 130nm node.
Dielectric constant stability	+ / - 0.1
Breakdown voltage	>2 MV/cm
Leakage current	<1E-10 A/cm2
Dissipation factor	<0.01
Charge trapping	low
Thermal	
Thermal stability	>425 ^{o}C
Thermal expansion coeffcient	-10 to 50 ppm/C
Thermal conductivity	>0.2
Glass temperature (Tg)	>400 ^{o}C
film shriekage after thermal cycling	<1%
Mechnical	
Adhesion (ILD/metal, ILD/ILD)	no peeling after CMP and thermal cycling
cracking limit	>2 micron
Stress	<1E9 dynes/cm2, tensile or compressive
Hardness	>1 Gpa
Modulus	>2 Gpa
Surface roughness	similar to SiO_2 or better
Chemical	
Moisture absorption	non-detectable change by weight, FTIR, TDS
Rsistance to Solvent (acid and base)	non-detectable change by weight, FTIR, TDS
Corrosion to Al, Cu	No
Pore size	small and uniform

Low-k Material: 3.0 <k < 4.0

- It is the 1st generation of low-κ material which is implemented into IC production at 0.25 μm , 0.18 μm technology node.
- Most popular candidates.
  - FSG (fluorosilicated glass):
    - It can be produced by doping F into oxide film thru conventional CVD process (PECVD or HDP):

      $SiH4 + SiF + O2 \rightarrow (SiO_2)_x(SiO_3F_2)_{1-x}$
    - K = 3.5~3.8, for a F concentration up to 5%. Film becomes less stable if F concentration further increases.
    - It is the 1st material industry adopt for low -k application although the capacitance reduction is not significant.
  - Trikon Flowfill lowk:
    - It is a methyl-silsesquioxane (MSQ) film which is produced by CVD reaction of methylsilane and hydrogen peroxide.
    - It has a dielectric constant between 2.8 – 3.5 depending on the process conditions.
    - It has an unique property to flow on substrate surface which makes it a perfect candidate for gap-fill application

OSG material structure



Low-k Material: 2.5 < k < 3.0

- This generation of low-κ material is targeted for 0.13 μm technology node.
- More candidates available in this category, but it seems that CVD prepared OSG materials are winning the battle in this κ range.
  - Spin-on organics:
    - SiLK (k = 2.6), BCB (k=2.65), fluoro-polyimide (k = 2.6 – 2.9).
    - Most of materials have adhesion problem and weak mechanical property
  - CVD deposited organosilicate glass (OSG):
    - AMAT Black Diamond (k=2.9), Novellus Coral (k=2.8), ASM Aurora 2.7 (k = 2.7), Trikon 2.8 (k=2.8).
    - They are formed by CVD method using precursors that contain methyl-group such as methyl-silane, tri-methylsilane etc.
  - Spin-on OSG film:
    - HOSP (hybrid-organo-siloxane polymer, k=2.5),
    - JSR LKD 2.9 version (MSQ, k = 2.9)

CVD deposited OSG *(skipped)*

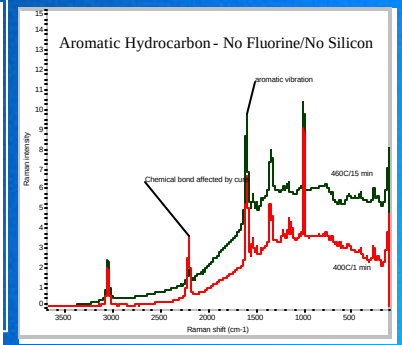
- It becomes the preferred choice of low-κ dielectric by many foundries and IDMs at 0.13 μm and 90nm nodes.
- Films from different suppliers are all very similar in terms of film composition and dielectric constant value.

Film Property	Lowk#1	Lowk#2	Lowk#3
Dielectric Constant	2.6-2.7	2.7-2.8	2.8-2.9
composition % - Si:O:C:H	19:32:13:36	20:32:14:34	18:30:14:38
Refractive Index	1.39	1.42	1.41
residue Stress (dynes/cm2)-tensile	~ 5E8	~ 3E8	~5E8
Stress Hysteresis (dynes/cm2), to 500ºC	5.7E+07	9.5E+07	2.0E+07
Thermal Stability, TDS	>500 ºC	>500 ºC	>500 ºC
Breakdown Voltage (MV/cm)	> 3	> 3	>3
Leakage Current @ 1MV/cm (A/cm2)	1.52E-10	1.53E-10	<1E-9
Film Density	1.3-1.4	1.3-1.4	1.3-1.4
Surface Roughness (Rms, Å)	8.6	8.4	6.2
Hardness (GPa)	0.2	0.9	1.4
Elastic Modulus (GPa)	2	6	8.9
Cracking Limit (um)	~1	~ 1	~ 3
Adhesion, KAPP (Mpa-m1/2) (dual damacene)	0.31	0.25	0.32
Thermal Expansion Coeff. (ppm/ºC)*	36.5	NA	21.4
Thermal Conductivity *	0.29	NA	0.37

SiLK *(skipped)*

- SiLK is a material Dow Chemical developed for low-κ application. It becomes famous since IBM announced implementation of this material into their 0.13 μm production.

Thermal stability @ 450C	< 1% wt loss at 450C
Glass Transition	>490C
k-value @ 1MHz	2.6
Refractive index @ 633 nm	1.6278 out-of-plane
Moisture uptake at 80%RH	<0.24wt%
CTE	62 ppm/C (50-150C)
Film stress at RT	60 MPa (tensile)
Toughness	0.62 MPa m ½
Thermal conductivity	0.23 W/mK @ 125C
Breakdown voltage	>4MV/cm
Interline leakage current	<50pA at 1MV/cm
Modulus, indentation	3.6(3)GPa
Hardness, indentation	0.29(8)GPa
Tensile Strength	93(3.5)MPa
Elongation to break	12(1.5)%



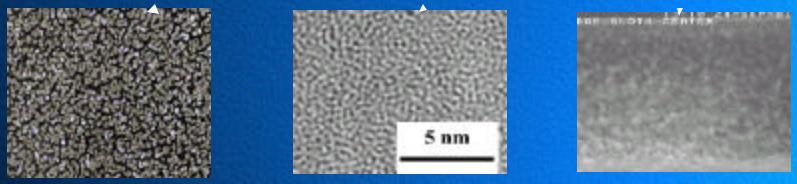
- Film is able to be extended to k<2.2 by adding porosity into SiLK (p-SiLK)

Ultra-low-k Material: k < 2.3

- Originally target for 0.13 μm generation, it has been delayed to 90 nm node, or more possibly, to 65nm technology node.
- Although there are many low-κ materials available which meet the κ requirement, no clear winner has appeared yet due to tremendous integration challenges.
  - CVD deposited porous OSG material:
    - Trikon Orion film (κ = 2.2),
  - Spin-on nanoporous silica-based material
    - Pure silica xerogel material with κ tunable between 1.3 – 2.5: Nanoglass from Allied Signal.
    - Porous HSQ film: XLK (k = 2.2) from Dow Corning
    - Porous MSQ film: JSR LKD5109 (κ = 2.2).
  - Organic material:
    - Non-porous organic: PTFE (Teflon, κ= 1.9), and Parylene-AF4 (κ=2.25).
    - Porous organics: p-SiLK (κ= 2.2)
  - Air-Gap: k → 1.

Ultra-lowk material properties

	XLK	JSR LKD	Trikon Orion
dielectric constant	2..0-2.2	2.3	2.0 - 2.2
Density (g/cm3)	1.03	1.03	1.04
average pore size (nm)	<3	~2	~2.5
Hardness (Gpa)	0.3	0.5	>0.7
Modulus (Gpa)	2~3	4	6.5
CTE (ppm)	30	14	NA



For ultra-lowk materials, more or less there are porosity being added in the film

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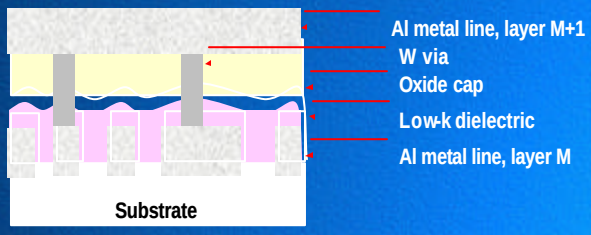
No matter which material is selected, they are all fundamentally flawed in some major characteristic. Therefore, the criterion of low-k material selection for IC manufacturers is not purely technical; the question usually becomes which material shortcomings are we going to choose to integrate around.

V. Ku, "Low-k integration Challenges," What's Up from SEMI, June 27, 2000

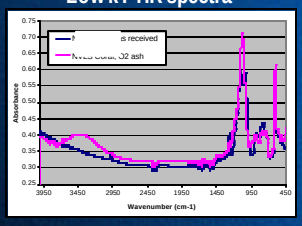
Al Subtractive Process



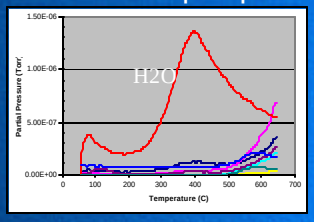
Plasma Susceptibility

- Lowk film is very sensitive to the plasma exposure, and could easily be damaged if these etch/ash process are not optimized. As the result, film property will change:
  - Dielectric constant will increase
  - Via profile will change (bowing etc.)
  - Film will degas which will cause poison via
  - Film will delaminate from the substrate

Low-k FTIR spectra

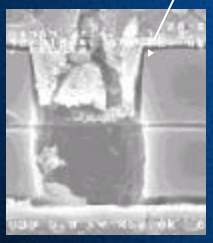


Low-k thermal desorption spectrum



Poison Via

Poisoned via

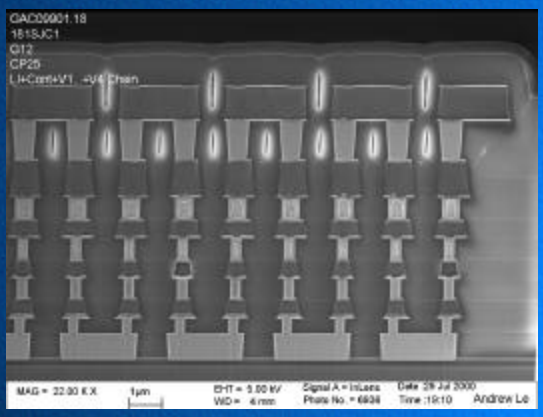


Good Via

After via open, barrier metal (Ti/TiN, Ta/TaN) could not be deposited onto lowk sidewall, therefore W plug would not be formed inside via around lowk region, causing open via circuit. The root cause of this problem is degassing from low-k film, which could be caused by:

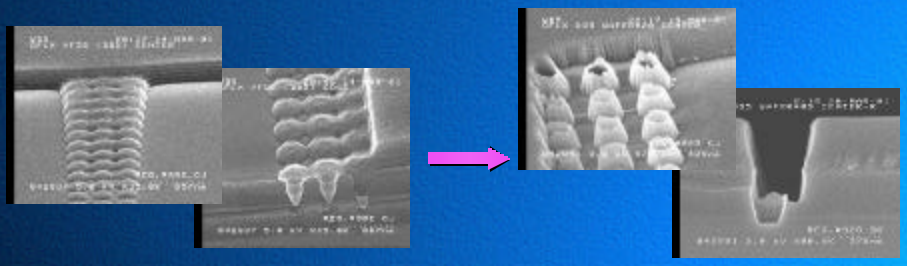
1. unstable low-k film at elevated temperature.
2. low-k film is damaged by via formation process (etch, ash, clean etc.) and absorbs moisture and process gases.
3. low-k film is porous and absorbs moisture.

LSI G12 BEOL – Al/Lowk (k<3.3)



Copper Dual D. Resist Poisoning

248 nm and 193 nm photoresist are very sensitive to contamination by trace quantities of amines or other bases, therefore low-k dielectrics contain such amines will easily poison the resist and interrupt the photo catalytic chain of reaction.



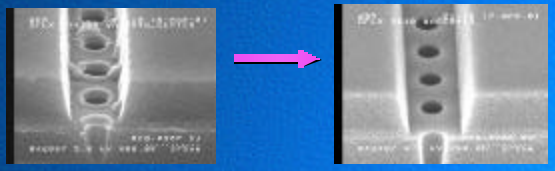
When resist poisoning happens, a portion of resist could not be developed and is left inside or around via holes.

As the result, Fencing is formed after trench etch.

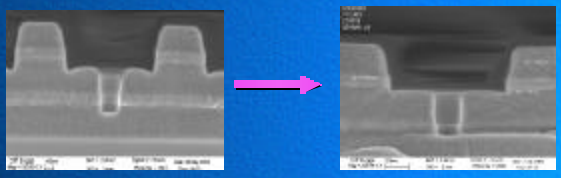
Dual-Damascene Etch *(skipped)*

- In dual-damascene process, the film stack could be very complicated (Organic BARC, Inorganic DARC, low-k, dielectric barrier film, middle etch stop, etc.). Low-k etch selectivity is one key requirement for etch to construct dual-damascene structure.

Fence Formation

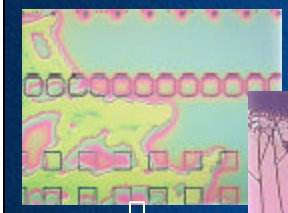


Micro-trenching



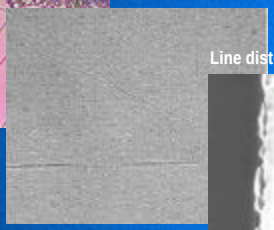
Low-k CMP induced defects

Low-k delamination

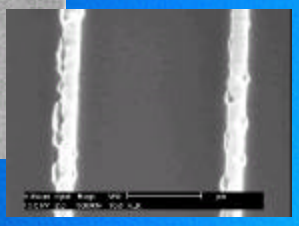


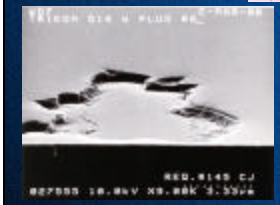
Low-k cracking

Low-K surface scratches



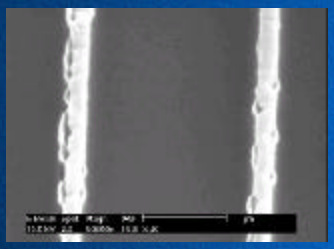
Line distortion due to softness of Low-k



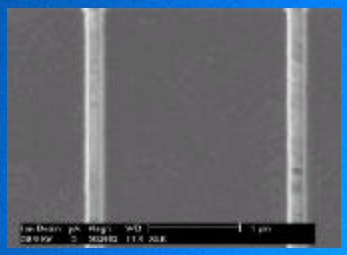


Alternative to polish Cu

- As we add more porosity into low-k material to reduce dielectric constant, eventually alternatives to polish Cu are needed to compromise the weak mechanical strength of ultra-lowk film (k <2.2)



CMP only

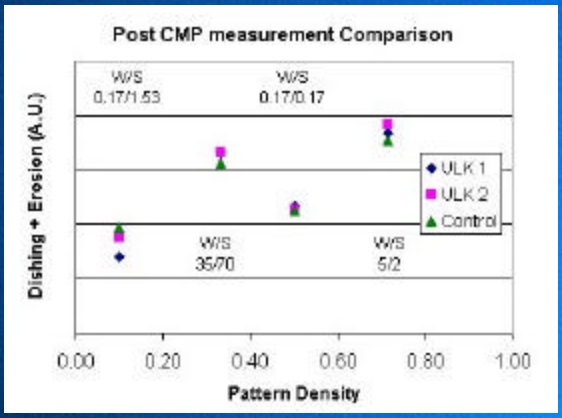


CMP followed by stress-free polishing

Courtesy of ACM Research, California

2.2 k Copper Results

- In-house have been able to modify CMP conditions, and successfully polish copper using 2.2k films (SD, see 2001 IITC).



Summary

- As technology advances into deep sub-micron region, Low-κ dielectrics is required to reduce the BEOL parasitic capacitance.
- Low-k material can by synthesized by minimizing the polarizability of the elements and adding porosity into the film.
- Although there are many low-k material available for evaluation, none of them is as perfect as silicon oxide. Compromise has to be made in process integration to be able to successfully integrate it into BEOL.
- LSI has embraced low-k material since its 0.18 μm technology node, and is one of the industry leader driving the lowk solutions for IC production.

References

- S. Wolf, "Silicon Processing for the VLSI Era, Vol.4", Chpt.14 – Lowk Dielectrics.
- J. Golden, "Designing porous low-k dielectrics", Semiconductor International 5/2001.
- R. Havemann, "High-performance Interconnects: an integration overview", Proc of the IEEE, vol 89/5/2001.