# Thermal Stress and Reliability Characterization of Cu Interconnects

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# Cu Interconnects Reliability

## IITC'02 Summary for EM/SM Issue

| No. | Category | Author Information | | | Device | Process | Summary/Comment |
|---|---|---|---|---|---|---|---|
| | | First | Last | Affiliation | | | |
| 7.5 | EM | A. Fischer | F. Ungar | Infineon | DLM ASTM Std Via EM (Via/Trench = 0.28um/0.4umWx400umL) | USG-TaN(Ta)-Cu-SiN | Bimodal TTF distribution=early branch via-voiding+late branch trench-voiding<br>Upstream-stressed via; ealry mode(n=1.1, Ea=0.86eV), late mode(n=1.6, Ea=0.83eV). Optimal M2 barrier eliminated early branch, and achieved monomodal by trench-voiding<br>Dow nstream-stressed vias; ealry mode(n=1.1, Ea=0.9eV), late mode(n=1.5, Ea=0.9eV). Optimal M2 barrier pre-clean eliminated early branch, and achieved monomodal by trench-voiding |
| 13.4 | SM | A. Glasow | A. Fischer | Infineon | DLM (M1 Trench/Via/M2 Trench = 0.28umWx100umL/0.28um/0.28umWx4umL) | USG-Cu-W-Al-SiN | Bimodal TTF distribution=early branch w hole metal line voiding(mode1 Ea=1.4eV; Cu grain boundaries)+late branch Cu/SiN interface voiding(mode2 Ea=0.9eV) at T > 225C. Monomodal mode 2 distribution at T < 225C. |
| | | | | | | USG-Cu-SiN | Monomodal TTF distribution(Ea=1.2eV) at 225C < T < 275C. |
| | | | | | | | 4 steps for void formation; 1. Vacancy generation through thremal cycle. 2. Vacancy migration by stress gradient. 3. Vacancy accumulation. 4. Void formation |
| 7.4 | SM | N. Okada | N. Nakamura | NEC | DLM NEC Special SM (M1 Trench/Via/M2 Trench = 0.14umW/0.13um/20umWx20umL) | USG-TaN(Ta)-Cu-SiN | SM testing @ 150C/350C ~10days. OBIRCH for identifing via failure; >3.0umWx3.0umL M2 DD degraded via chain yield, but not w ith SD. SR-EXAFS for atomic bond structure; Cu-Cu distance continuously expand 2.2A(RT)~5.5A(350C), w hich could be related to SM failure |
| 10.5 | SM | T. Suzuki | H. Yagi | Fujitsu | DLM (Via/Trench = 0.22-0.27um/0.28-8umWx20umL) | FSG?-TaN-Cu | SR-XRD 3D stress measurement in micro-structure; Via z >> Trench z especially at trench > 1um. Pillars in trench increase trench z to match w ith via z, and resulted low er SM failure rate. |

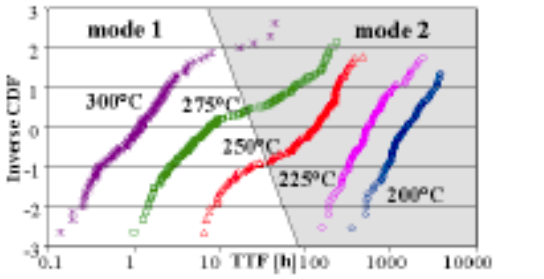


Fig.4
Failure distributions (ΔR/R=1%) obtained on samples of Cu-W-Al chains at different storage temperatures. A distinct bimodality is found for T>225°C. The early branch (mode 1) becomes more and more pronounced for higher temperatures.

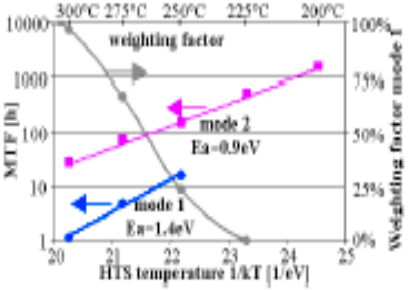


Fig.5
MTFs (left scale) determined on samples of Cu-W-Al chains for both modes suggest a larger activation energy Ea for mode 1. The percentage of failures belonging to mode 1 (right scale) increases with stress temperature but vanishes below 250°C.

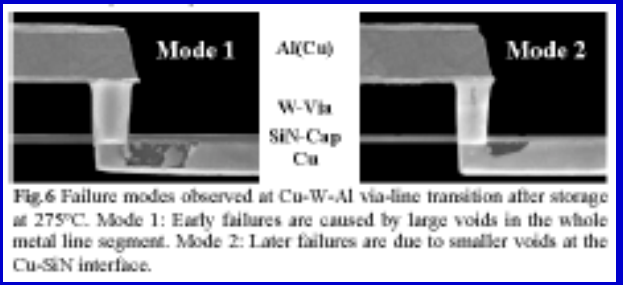


Fig.6 Failure modes observed at Cu-W-Al via-line transition after storage at 275°C. Mode 1: Early failures are caused by large voids in the whole metal line segment. Mode 2: Later failures are due to smaller voids at the Cu-SiN interface.

*Ref; A. Glasowet.al. (IITC'02)*

**EM; barrier/Cu interface dominant**

**SM; Cu grain boundary(early failure), Cu/SiN interface(late failure) dominant**

**⇨ Cu alloy for EM/SM early failure, and metal passivation for SM late failure**

# Cu Alloy Technology

## Literature Search - Cu Alloy for Interconnect

| Publication | Author Information | | | Material / Device | Process | Summary / Comments |
|---|---|---|---|---|---|---|
| | First | Last | Affiliation | | | |
| J. Appl. Phys. Jan'98 | L.Clevenger | J.Harper | IBM | **Cu-Sn** | Electron Beam Evaporation | Study of interdiffusion and phase formation in films of Sn/Cu. Complete intediffusion of Cu and Sn from a Sn/Cu bilayer 0.5-1.0mm thick requires annealing temperatures and times in excess of 350-400C for 30 min. Contamination of the copper surface by air |
| Proc. of IITC, June'01 | C.Wang | D.Erb | AMD | **Cu-Sn/Cu-In/Cu-Zr** | PVD Seed | 0.3~1.2 at.% Sn, In, Zr Cu alloy examined. Reduction of Cu agglomeration on TaN barrier observed, which suggests suppression of Cu mobility at Cu/barrier interface, thus reduces EM. Dopant redistribution rate; Sn>In>Zr. Cu resistivity increase per 1 at.% alloy element ($\mu$ohm-cm); In(1.1) < Sn(3.6) < Zr(18). 1KA CuSn(0.3 at.%) seed with 250C post ECP anneal improved EM 2X. |

- **Studied as dopant(at.%) for Cu EM**
  **Ti(0.48) > Ti (0.22) > Zr(0.14) > Be(10) > Mg(2) > Sn(0.53)**

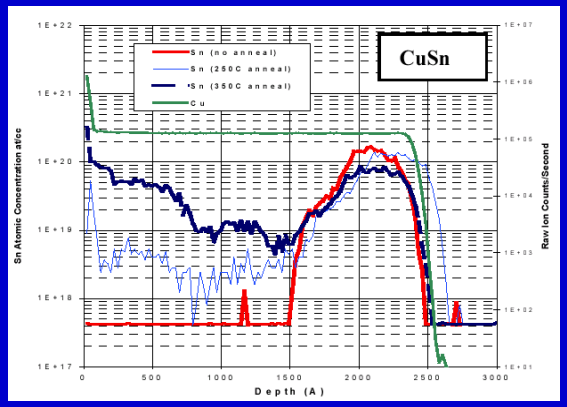


Figure 2: SIMS profiling of 2000Å Cu/ 500Å Cu (Sn, In or Zr)/ Ta/ oxide/Si film stacks, as deposited or annealed in UHV at 250-400°C for 5-60min.

*Ref; C.Wang et.al. (IITC'01)*

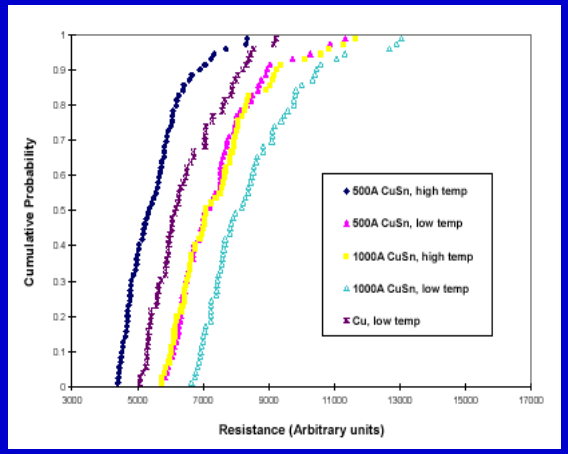


Figure 3: Metal-line resistance data of CuSn as functions of CuSn thickness (500Å or 1000Å) and anneal temperature.

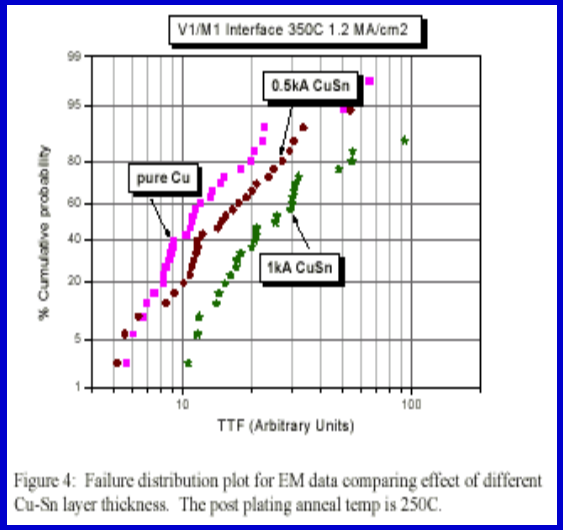


Figure 4: Failure distribution plot for EM data comparing effect of different Cu-Sn layer thickness. The post plating anneal temp is 250C.

**Advantage of Cu alloy; EM/SM improvement**

**Process technology of choice; PVD seed, electrolytic plating**

# Metal Passivation Technology

## Literature Search - Metal Passivation for Cu Interconnect

| Publication | Author Information | | | Material / Device | Process | Summary / Comments |
|---|---|---|---|---|---|---|
| | First | Last | Affiliation | | | |
| Proc. of IITC, June'01 | T.Saito | H.Yamaguchi | Hitachi | **W Selective** / Cu Interconnect | CVD | H2(pre) and HF(pre and post) treatment enhance selectivity and resulted short yield improvement. No yield degradation after 500hrs of BTS. ~10% **RC** delay improvement with 0.2μm 4 layer Cu/USG interconnect Bi-CMOS device by eliminating SiN cap layer. |
| Proc. of IITC, June'02 | T.Itabashi | H.Akahoshi | Hitachi | **CoWB Selective** / Cu Interconnect | Alkaline **(TMAH)** DMAB E-less | Simulation; 30% **RC** reduction at 0.2um w / metal cap. Co alloy plating w /o Pd activation (Rs increase) by DMAB. Alkaline free bath with TMAH. Prevent Cu diffusion up to 500C for 30min, while CoWP failed at 400C. |
| Proc. of IITC, June'02 | H.Kondo | N.Shimizu | Fujitsu | **ZrN** Blanket / Cu Interconnect | MOCVD | <20nm ZrN behaves as dielectric on USG and metal on Cu, self aligned cap. Resistivity estimated <200uohm-cm. ZrN capped Cu Rs stable with 450C 1hr anneal. WLR Line **EM**; ZrN Cap(Ea=0.74eV) > No ZrN Cap(Ea=0.71eV). TZBD; ZrN/USG(11.6MV/cm) > USG(7.4MV/cm). T |

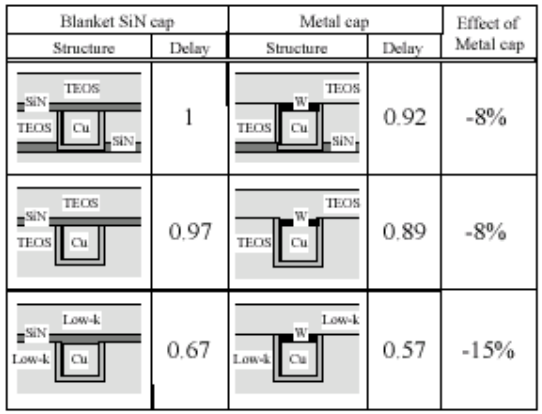


Fig.1. Comparison of the simulation results of the normalized delay time between various interconnect structures. Assumed k value of low-k material is 2.5.

*Ref; T.Saito et.al. (IITC'01)*

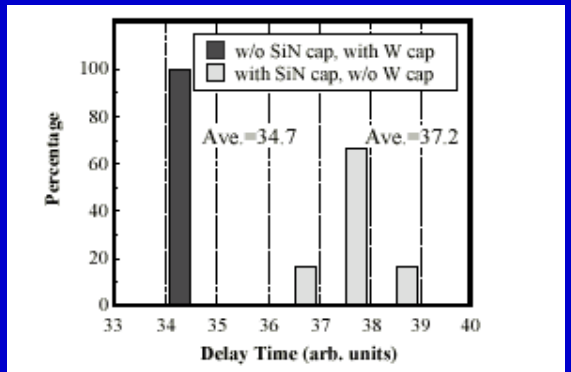


Fig.8(b). Comparison of the delay time using ring oscillator between the optimized W capping process and the control (w/o W cap). In case of W capping process, RC delay of wiring was reduced due to the absence of SiN capping layer.

*Ref; T.Saito et.al. (IITC'01)*

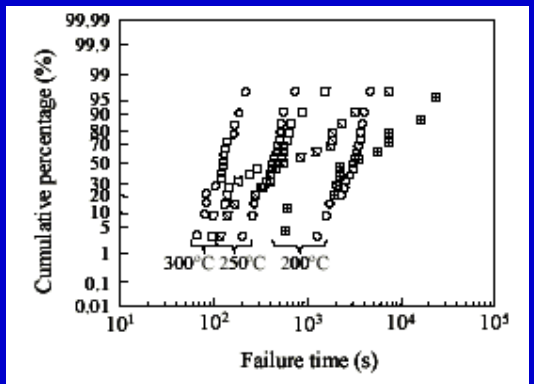


Fig. 5 Failure time distribution of WLR. ZrN capped interconnect(○) and non capped interconnect(□,⊡,⊞).

*Ref; H.Kudo et.al. (IITC'02)*

**Advantage of metal passivation; RC reduction, EM/SM improvement**

**Process technology of choice; CVD, MOCVD, electroless deposition**

# Approach for Cu Interconnects Reliability Improvement

## Summary

- Advantage of metal passivation; RC reduction, EM/SM improvement
- Process technology of choice; CVD, MOCVD, electroless plating
  - Selective CVD W; Well known technology. Confirmed Cu barrier properties, RC improvement, and SM performance. Concern for selectivity management
  - Selective electroless Co; Well studied technology in different industry. Confirmed Cu barrier properties, but no evidence for EM/SM improvement. Difficulty in managing selectivity with good control over feature size and dielectric material dependence
  - Blanket MOCVD ZrN; Interesting ZrN material characteristic. Confirmed Cu barrier properties and EM improvement, but no much advantage for RC reduction
  - ALD, PVD; No report
- Possible other electroless technology applications; Cu barrier, Cu seed repair, Cu direct plating, gate salicide(i.e. CoSi)

# Approach for Cu Interconnects Reliability Improvement

## Summary

- Advantage of Cu alloy; EM/SM improvement
- Process technology of choice; PVD seed, electrolytic plating
  - PVD seed; limitation of alloy element selection by thermal interdiffusion and redistribution controllability. Demonstrated CuSn feasibility for EM improvement.
  - Electrolytic plating; Well studied technology in different industry. Limitation of alloy element selection by coplatability due to reduction potential difference and thermal redistribuiton controllability. Difficulty in managing low alloy element concentration (<1 at.%) with practical plating chemical management and process tuning parameters. No evidence for for EM/SM improvement.
  - MOCVD, Ion implantation; No report
- Possible other alloy elements; Ag, Cd, Zn

# Thermal Stress and Reliability Characterization of Barriers for Cu Interconnects

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# Thermal Stress and Reliability Characterization of Barriers for Cu Interconnects

## Contents

- Maximizing Cu Interconnects Parametric Yield
  - Via Chain Yield Degradation by Cu De-Wetting
  - Cu De-Wetting Mechanism
  - Optimizing Post ECP Annealing for Cu De-Wetting
- Improving Cu Interconnects Thermal Stability
  - Cu Void Generation by Hot Storage Testing
  - Barrier Evaluation for Cu Void Generation Resistance
  - Cu Void Generation Mechanism
  - Barrier Evaluation for Device Applicability

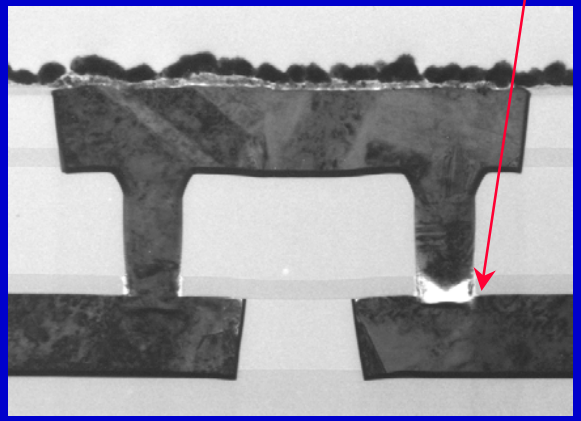
# Via Chain Yield Degradation by Post ECP Annealing

## Via Chain Yield vs. Post ECP Annealing Condition

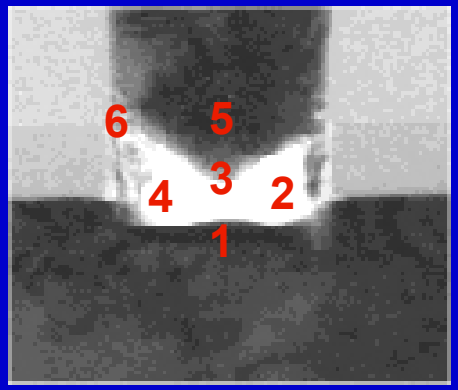
**ECP Cu 1.3μm/PVD Cu 150nm/PVD TaN 25nm on $SiO_2$/Si Substrate**

| Post ECP Annealing Condition | Furnace | | Hot Plate | No Annealing |
|---|---|---|---|---|
| | 350C, 30min | 250C, 30min | 350C, 2min | |
| 0.30um 400K Bordered | 13.3% | 26.7% | 16.7% | 100.0% |
| 0.28um 400K Bordered | 10.0% | 23.3% | 10.0% | 100.0% |
| 0.26um 400K Bordered | 6.7% | 10.0% | 3.3% | 93.3% |
| 0.24um 400K Bordered | 0.0% | 0.0% | 0.0% | 90.0% |
| 0.22um 400K Borderless | 0.0% | 6.7% | 0.0% | 86.7% |
| 0.22um 3M Bordered | 0.0% | 0.0% | 0.0% | 56.7% |
| 0.22um 3M Borderless | 0.0% | 0.0% | 0.0% | 40.0% |

**Voltage Contrast & TEM**



**EDX**



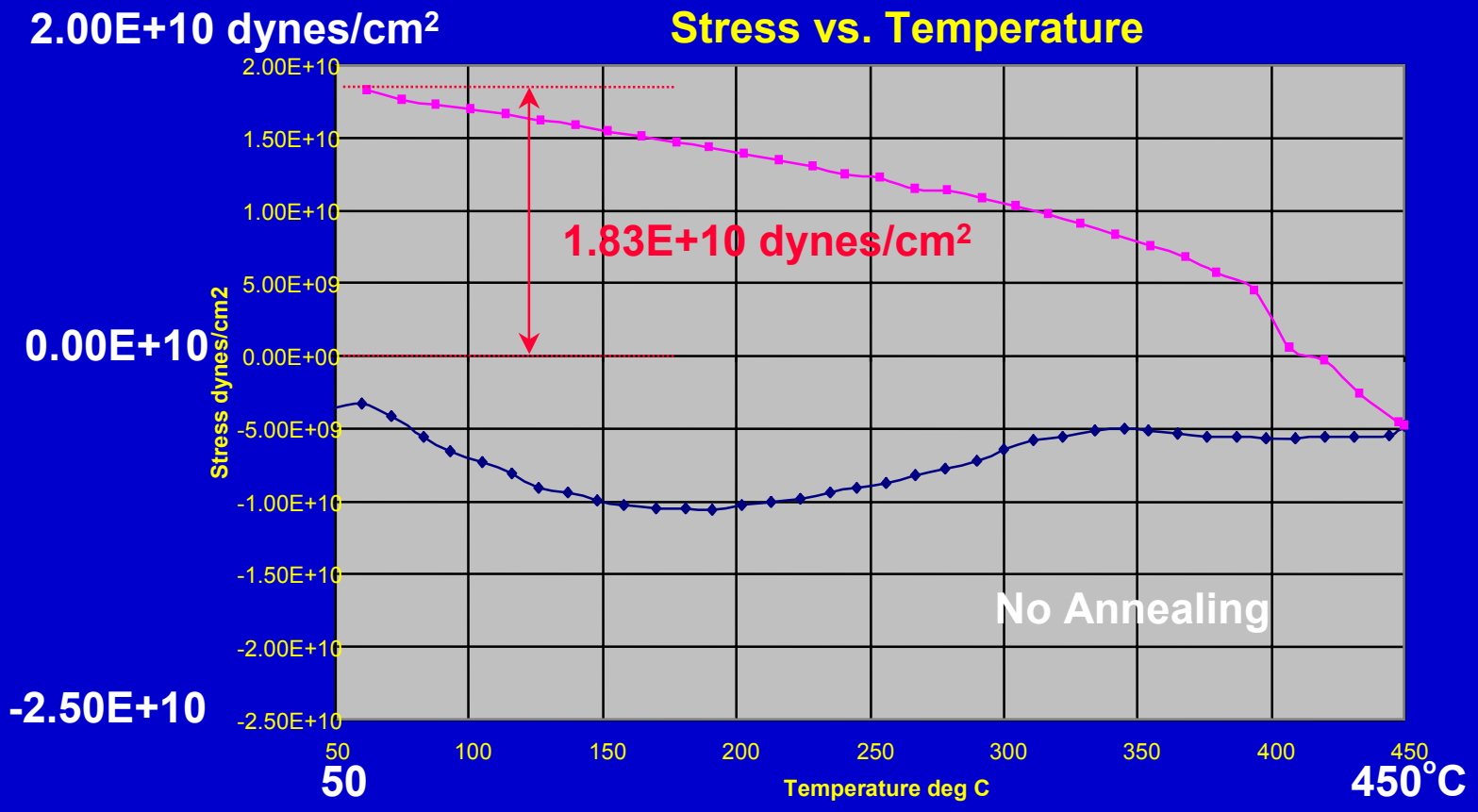

**1: Ta, Cu**
**2: Void**
**3: Ta, Cu**
**4: Void**
**5: Cu**
**6: Ta, Cu**

**Cu De-Wetting in 1/50K~100K Via Hole Resulted in 0% Via Chain Yield**

# Cu De-Wetting Mechanism in Via Hole

## ECP Cu Thermal Stress Hysteresis

**Blanket ECP Cu 1.3μm/PVD Cu 200nm/PVD TaN 25nm on $SiO_2$/Si Substrate**




**Un-Treated ECP Cu Showed High Tensile Cu/Barrier Residual Stress**

# Cu De-Wetting Mechanism in Via Hole - Cont'd

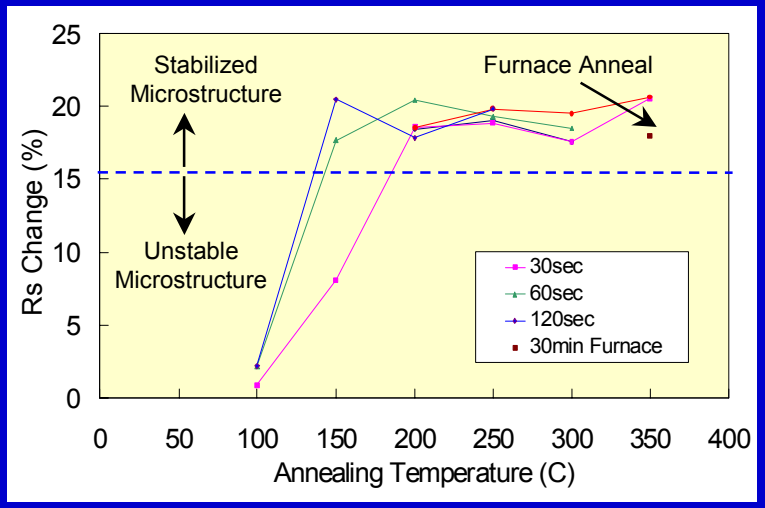
## Hypothesis

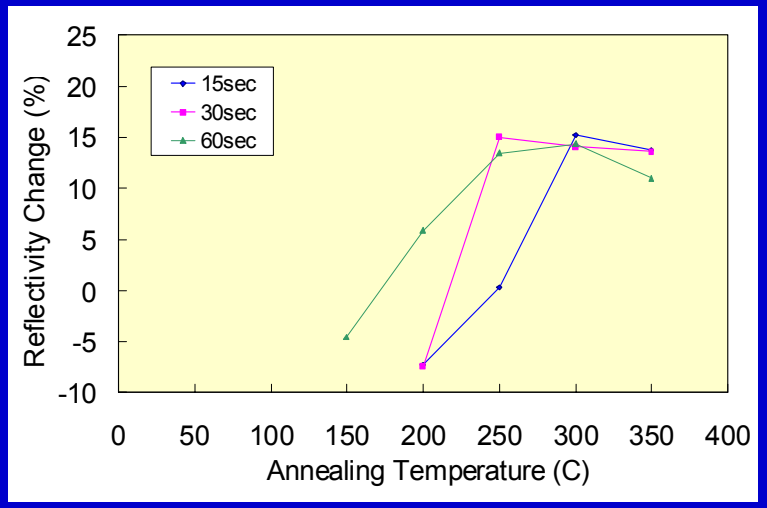
- Excessive Thermal Treatment of ECP Cu Results in Cu De-Wetting Due to High Cu/Barrier Residual Stress
- Insufficient Post ECP Annealing Does Not Eliminate Cu De-Wetting on Further Thermal Cycle
  i.e. Interlayer Dielectric Deposition/Curing
  Final Annealing/Sintering
- De-Wetting Can Be Minimized by Optimizing Post ECP Annealing Condition

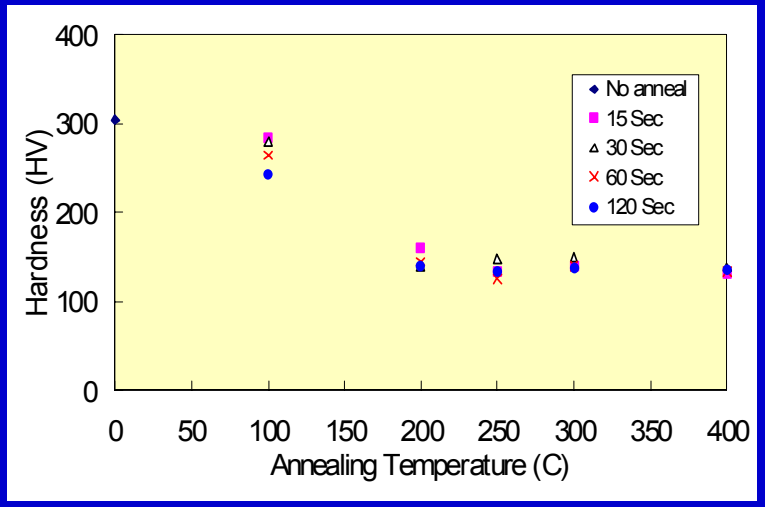
# Optimizing Post ECP Annealing Condition

## Minimal Thermal Treatment for ECP Cu Stabilization

**Blanket ECP Cu 1.0μm/PVD Cu 200nm/PVD TaN 25nm on $SiO_2$/Si Substrate**



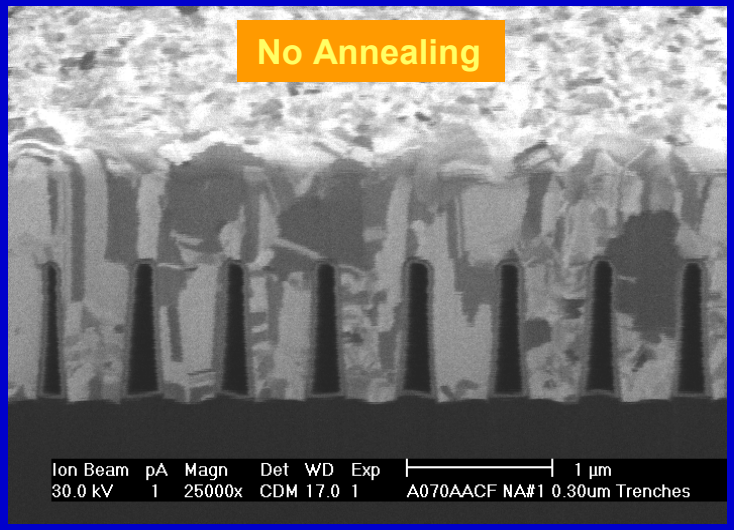

**250°C, 30sec Hot Plate Annealing Is Considered to be Minimum Thermal Treatment to Stabilize ECP Cu Film Properties**

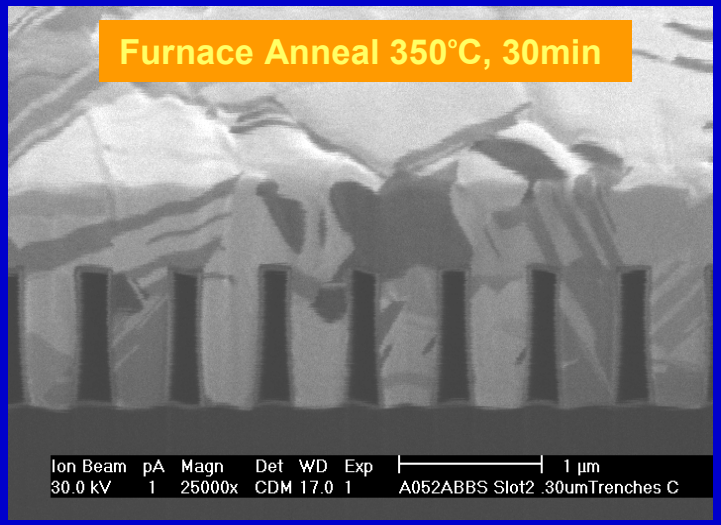
**Ref; M. Chen (AMAT)**

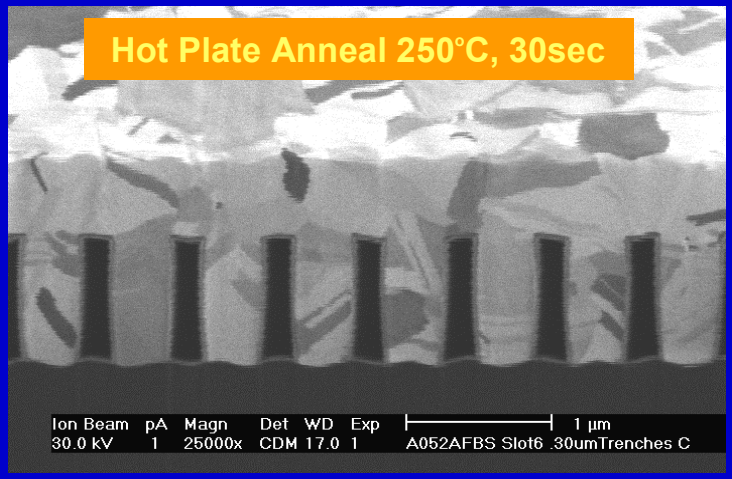
# Optimizing Post ECP Annealing Condition

## Minimal Thermal Treatment for ECP Cu Stabilization

**Blanket ECP Cu 1.0μm/PVD Cu 200nm/PVD TaN 25nm on $SiO_2$/Si Substrate**



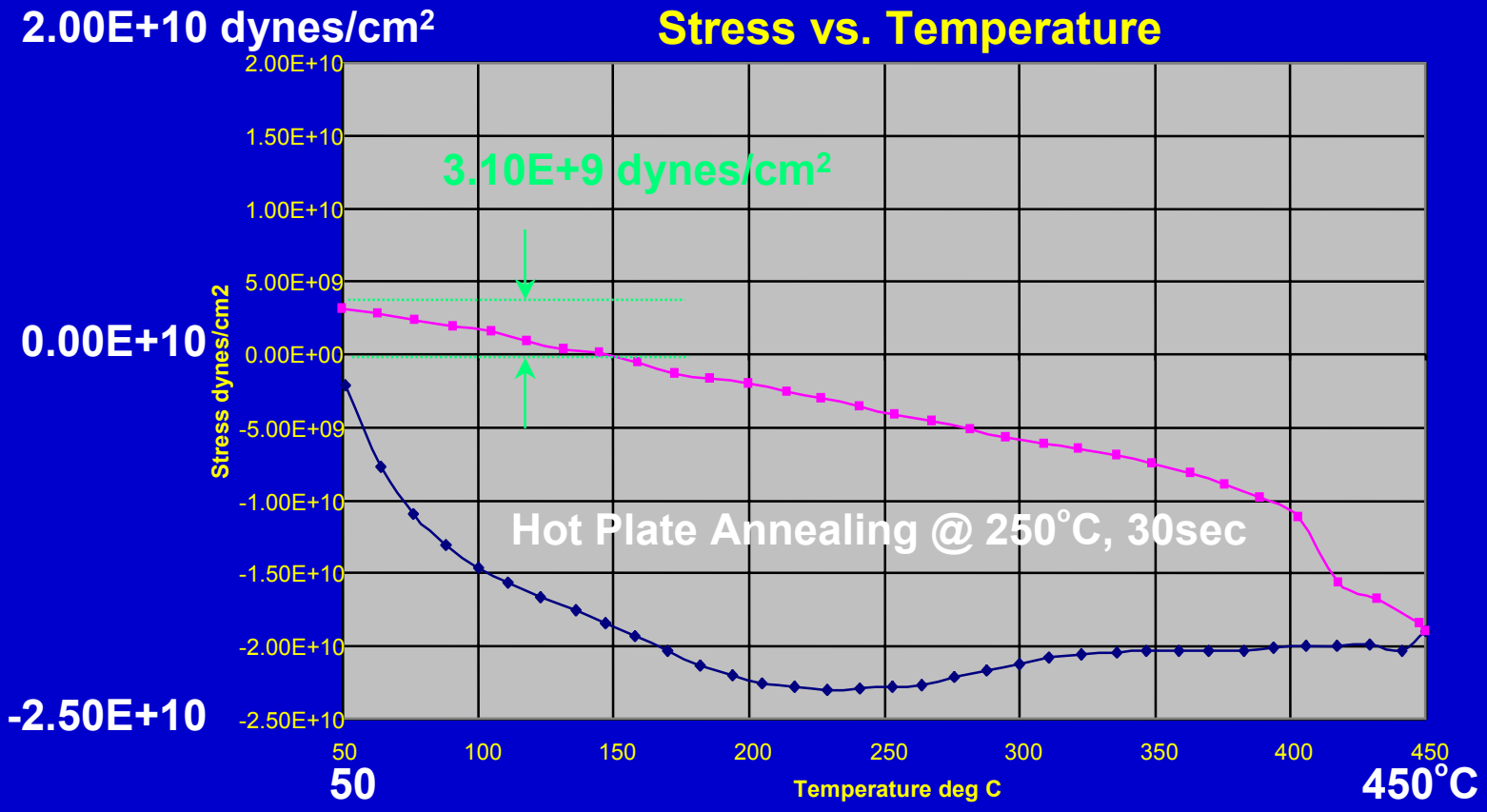

**250°C, 30sec Hot Plate Annealing Showed Equivalent ECP Cu Film Microstructure**

**Ref; M. Chen (AMAT)**

# Optimizing Post ECP Annealing Condition - Cont'd

## ECP Cu Thermal Stress Hysteresis

**Blanket ECP Cu 1.3μm/PVD Cu 200nm/PVD TaN 25nm on $SiO_2$/Si Substrate**




**Optimally Treated ECP Cu Showed Minimum Cu/Barrier Residual Stress**

# Optimizing Post ECP Annealing Condition - Cont'd

## Via Chain Yield vs. Post ECP Annealing Condition

**ECP Cu 1.3μm/PVD Cu 150nm/PVD TaN 25nm on $SiO_2$/Si Substrate**

| Post ECP Annealing Condition | Furnace | | Hot Plate | No Annealing | **Hot Plate** |
|---|---|---|---|---|---|
| | 350C, 30min | 250C, 30min | 350C, 2min | | **250C, 30sec** |
| 0.22um 400K Borderless | 0.0% | 6.7% | 0.0% | 86.7% | **100.0%** |
| 0.22um 3M Bordered | 0.0% | 0.0% | 0.0% | 56.7% | **70.0%** |
| 0.22um 3M Borderless | 0.0% | 0.0% | 0.0% | 40.0% | **80.0%** |

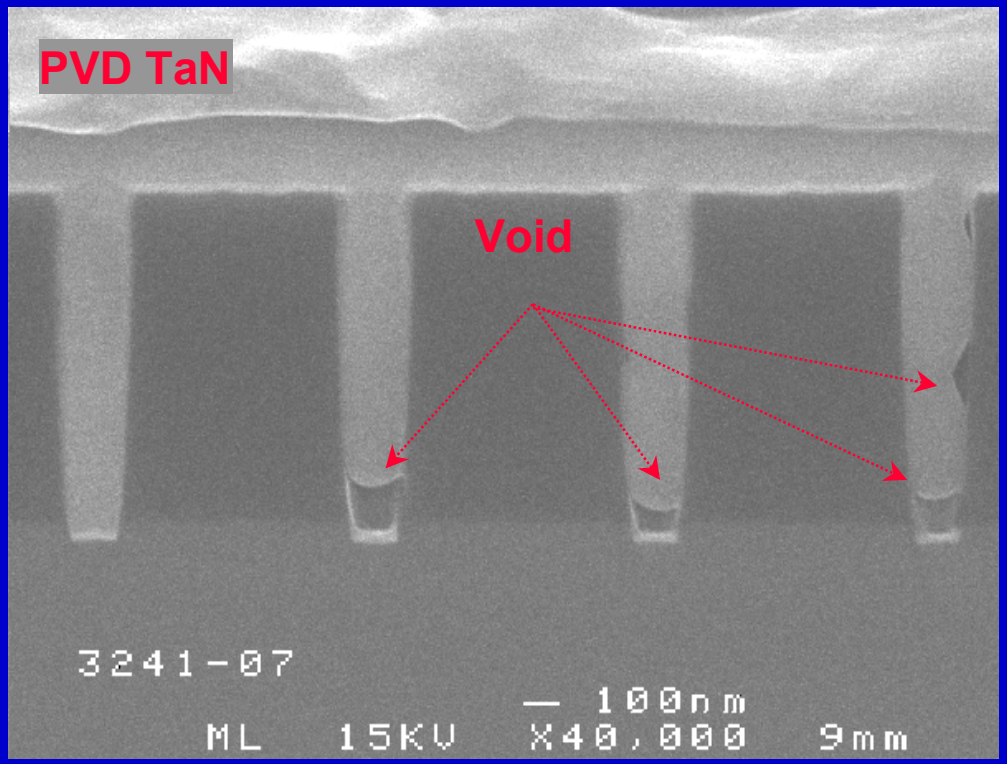
**Via Chain Yield Was Maximized with Optimum Post ECP Annealing Condition**

**(No Other Systematic Defects Observed for Yield Loss)**

# Cu Void Generation in Via Hole by Hot Storage Testing

## Cu Void Generation Observation

**ECP Cu 1.3μm/PVD Cu 150nm/ PVD TaN 25nm on 0.22μm Hole $SiO_2$/Si Substrate**
**Hot Plate Annealing @ 250°C, 30sec**



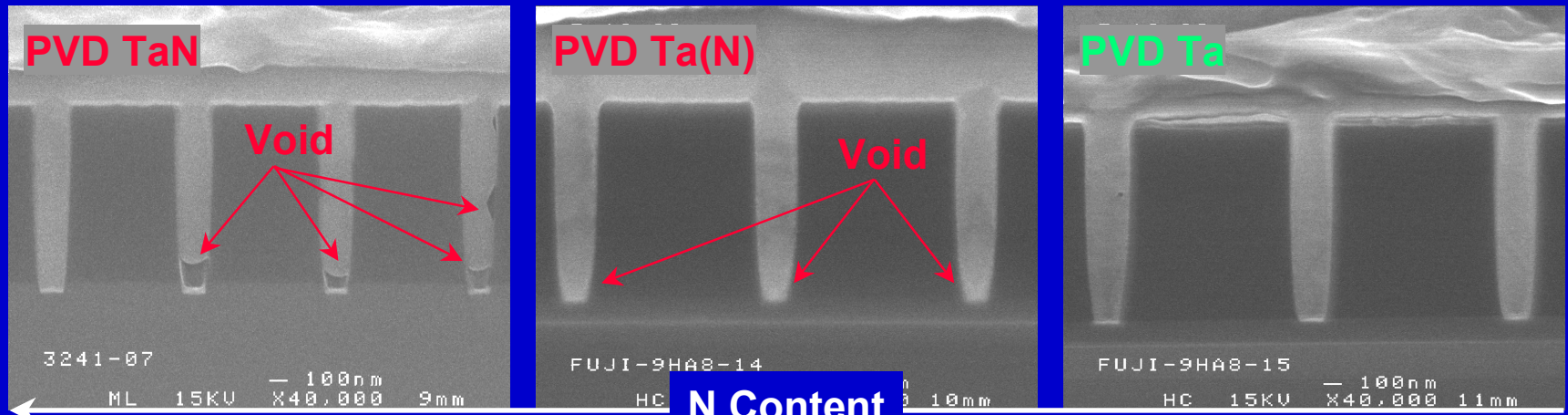

**Barrier/Seed**
⇩
**ECP**
⇩
**Hot Plate Anneal**
**(250°C, 30sec)**
⇩
**Cap Dielectric**
⇩
**Hot Storage**
**(120°C, 3weeks)**

**Cu Void Generation Observed by Hot Storage Testing**

# Evaluating Barriers for Hot Storage Testing Resistance

## Cu Void Generation vs. Barrier Material

**ECP Cu 1.3μm/PVD Cu 150nm/Barrier on 0.22μm Hole $SiO_2$/Si Substrate**
**Hot Plate Annealing @ 250°C, 30sec**



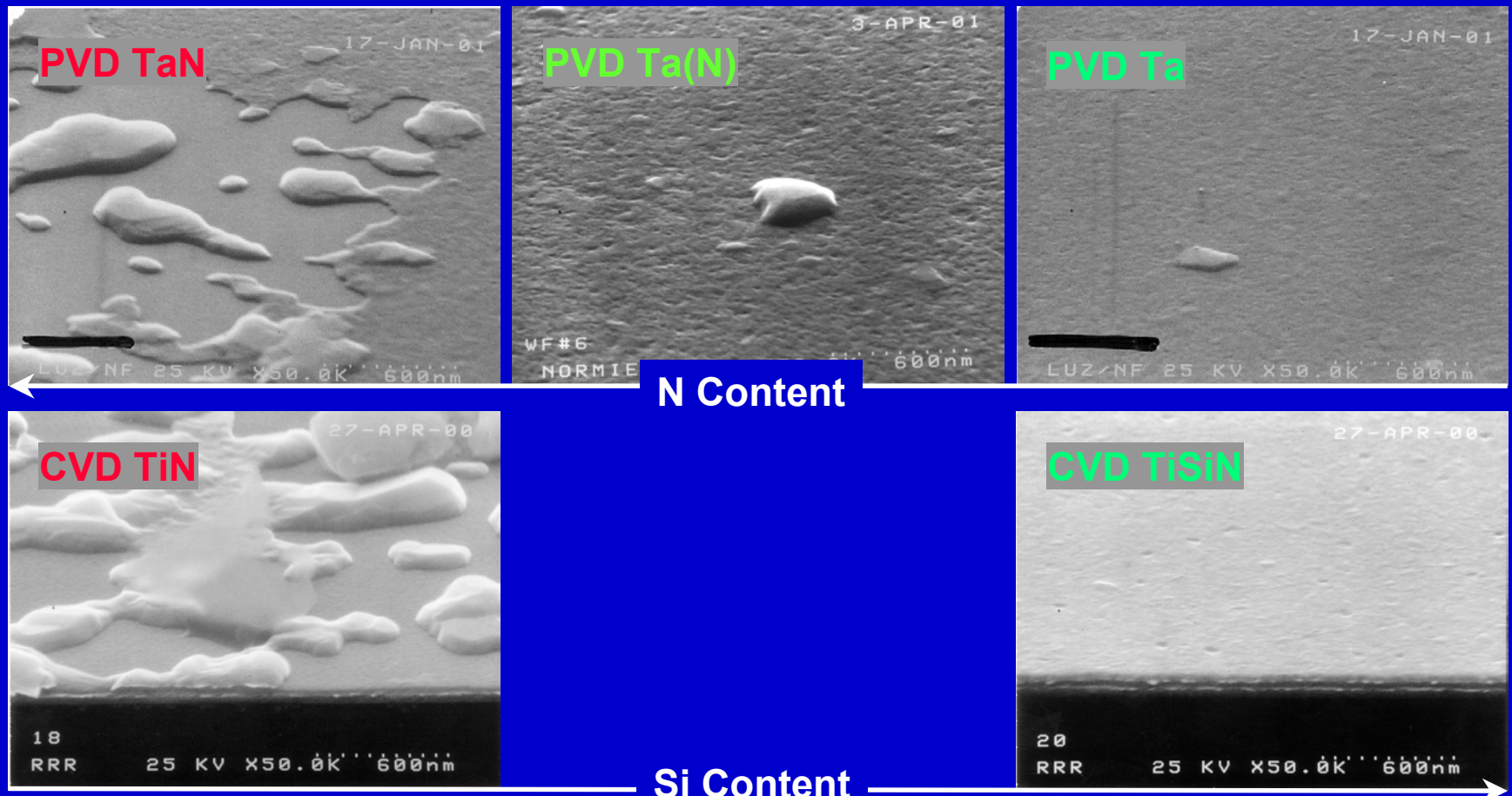


**Magnitude of Cu Void Generation Depends on Barrier Material**

# Cu Void Generation Mechanism in Via Hole

## Cu Wetting vs. Barrier Material

**Blanket PVD Cu 10-20nm/Barrier on $SiO_2$/Si Substrate**

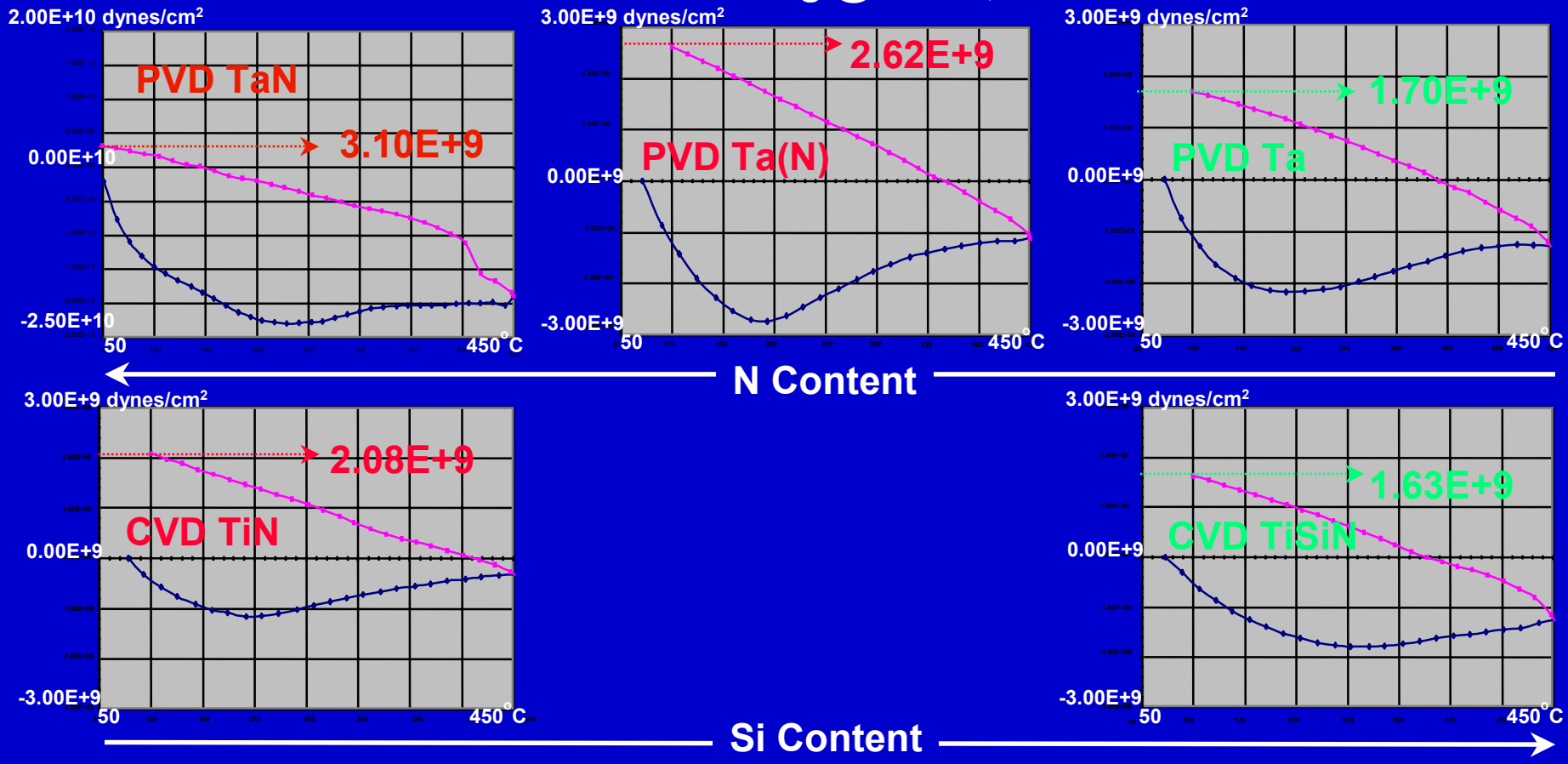



**Barrier with Good Cu Wetting Resulted in Good Cu Void Generation Resistance**

# Void Generation Mechanism in Via Hole - Cont'd

## Cu Stress Hysteresis vs. Barrier Material

**Blanket ECP Cu 1.3mm/PVD Cu 150nm/Barrier on $SiO_2$/Si Substrate**
**Hot Plate Annealing @ 250°C, 30sec**




**Barriers with Low Cu/Barrier Residual Stress Resulted in Good Cu Void Generation Resistance**

# Void Generation Mechanism in Via Hole - Cont'd

## Cu/Barrier Film Properties

| Barrier Material | PVD TaN | PVD Ta(N) | **PVD Ta** | CVD TiN | **CVD TiSiN** |
|---|---|---|---|---|---|
| Barrier Stress(dynes/cm2) | -3.E+10 | -3.E+10 | -3.E+10 | -5.E+09 | -5.E+09 |
| **Cu Wetting** | Bad | Good | Good | Bad | Good |
| **Cu/Barrier Stress Hysteresis (dynes/cm2)** | 3.10E+09 | 2.62E+09 | 1.70E+09 | 2.08E+09 | 1.63E+09 |
| **Cu Void Generation** | Void | Void | Good | Void | Good |

**PVD Ta and CVD TiSiN Provided Better Cu Void Generation Resistance**

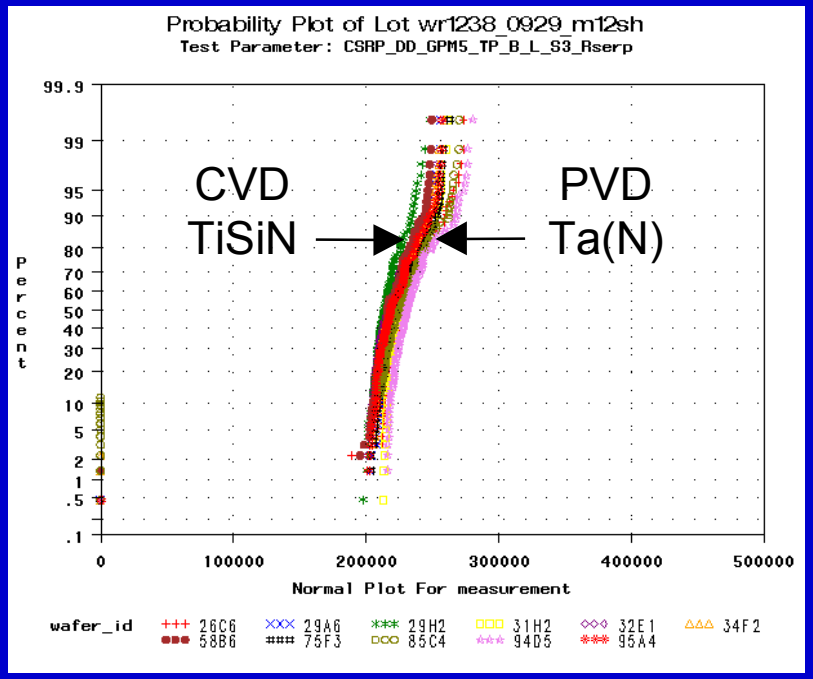
**Improvement of Cu Wetting and Cu/Barrier Residual Stress Lead to Cu Void Generation Suppression in Hot Storage Testing**

- **Cu/Barrier Interfacial Affinity**
- **Cu Bulk Structural Thermal Stability**

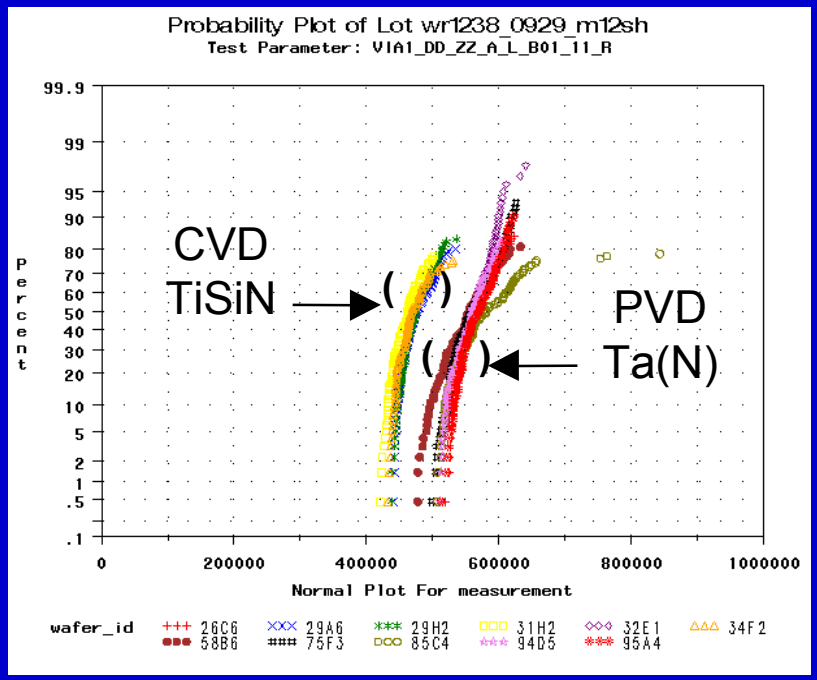
# Evaluating Barriers for Device Applicability

## Line and Via Resistance

**ECP Cu 1.3μm/PVD Cu 150nm/Barrier on $SiO_2$/Si Substrate**
**Hot Plate Annealing @ 250°C, 30sec**




**Line Resistance**
**(0.4μm L/S, 1.76m Long)**




**Via Resistance**
**(0.28μmϕ, 484k Vias)**

**CVD TiSiN Showed Comparable Line and Via Chain Yield with Reasonable Resistance to PVD Ta(N)**

# Evaluating Barriers for Device Applicability - Cont'd

## Line to Line BTS Testing

**0.24µm L/S @ 1.5MV/cm, 250°C**

**ECP Cu 1.3µm/PVD Cu 150nm/Barrier on FSG/Si Substrate**
**Hot Plate Annealing @ 250°C, 30sec**

| Barrier Material | PVD Ta(N) | CVD TiSiN |
|---|---|---|
| #Samples Passed/Tested | 20/20 | 20/20 |
| Test Time(Hr) | >320* | >320* |

*** Testing Aborted at 320 Hours**

**CVD TiSiN Showed Equivalent Barrier Performance to PVD Ta(N)**

# Thermal Stress and Reliability Characterization of Barriers for Cu Interconnects

## Summary

- Parametric yield loss of Cu interconnects correlated to Cu de-wetting at via bottom
- Cu void generation during hot storage caused Cu interconnects thermal integrity degradation
- Cu/Barrier residual stress as a factor in Cu de-wetting and Cu void generation
- Optimum post ECP annealing process reduced Cu de-wetting and recovered parametric yield of Cu interconnects
- Barrier material plays a key role in Cu interconnects thermal stability, and PVD Ta and CVD TiSiN barrier showed better thermal stress resistance