CONEXANT

# *Roadmap of SiGe BiCMOS technologies*

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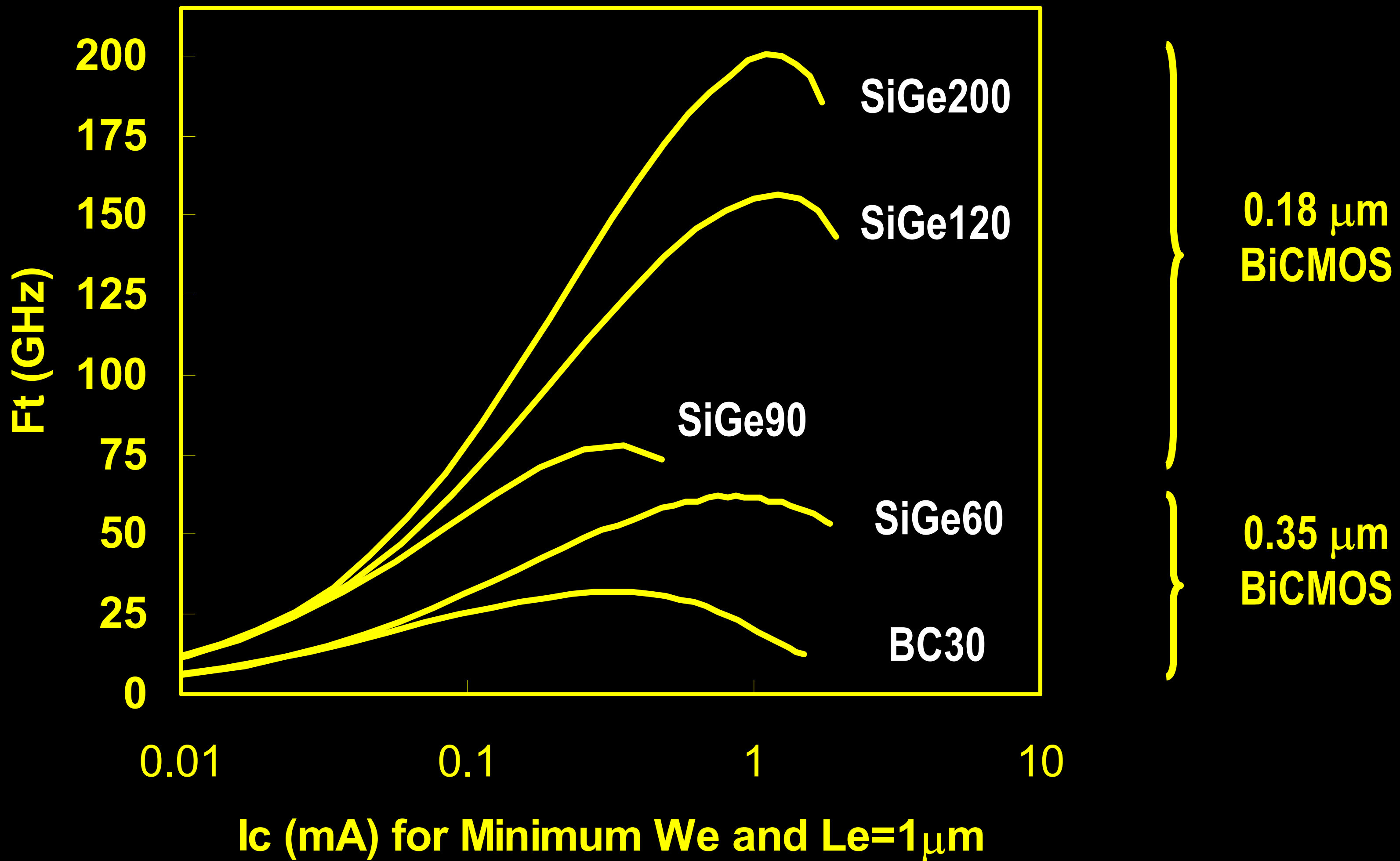
**Conexant Systems**

**April 17, 2002**

# BiCMOS Technology at Conexant

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# *Continued dominance of bipolar in RFIC*

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- **BJT/HBT higher performance than MOSFET**
  - MOS moving from MHz to GHz
  - BJT moving from 1-2 GHz to >200 GHz
- **Significantly lower cost than GaAs**
- **High-level integration complexity with BiCMOS technology at moderate cost penalty**

# SiGe RF big bang

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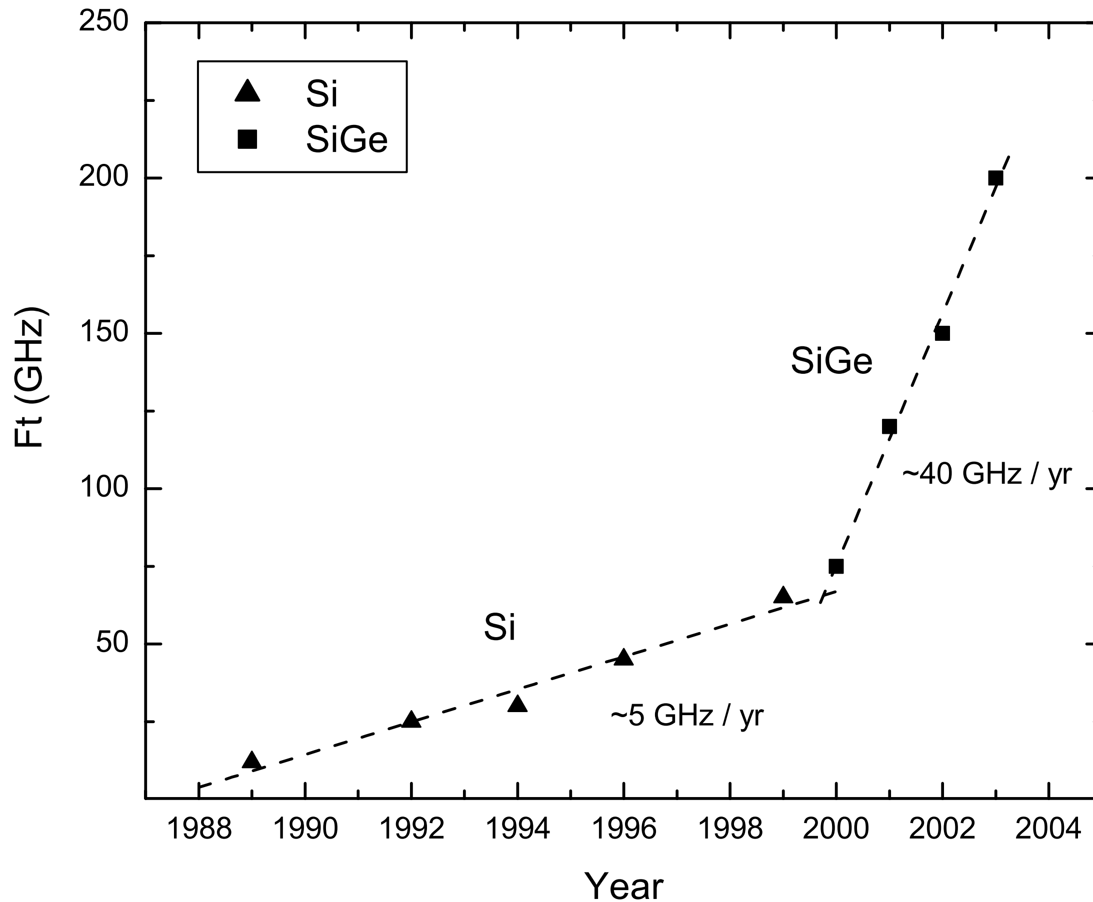


Exceptional technological progress in <5 yrs

SiGe BJT on 6x faster performance curve

# SiGe BiCMOS secures leading RFIC position

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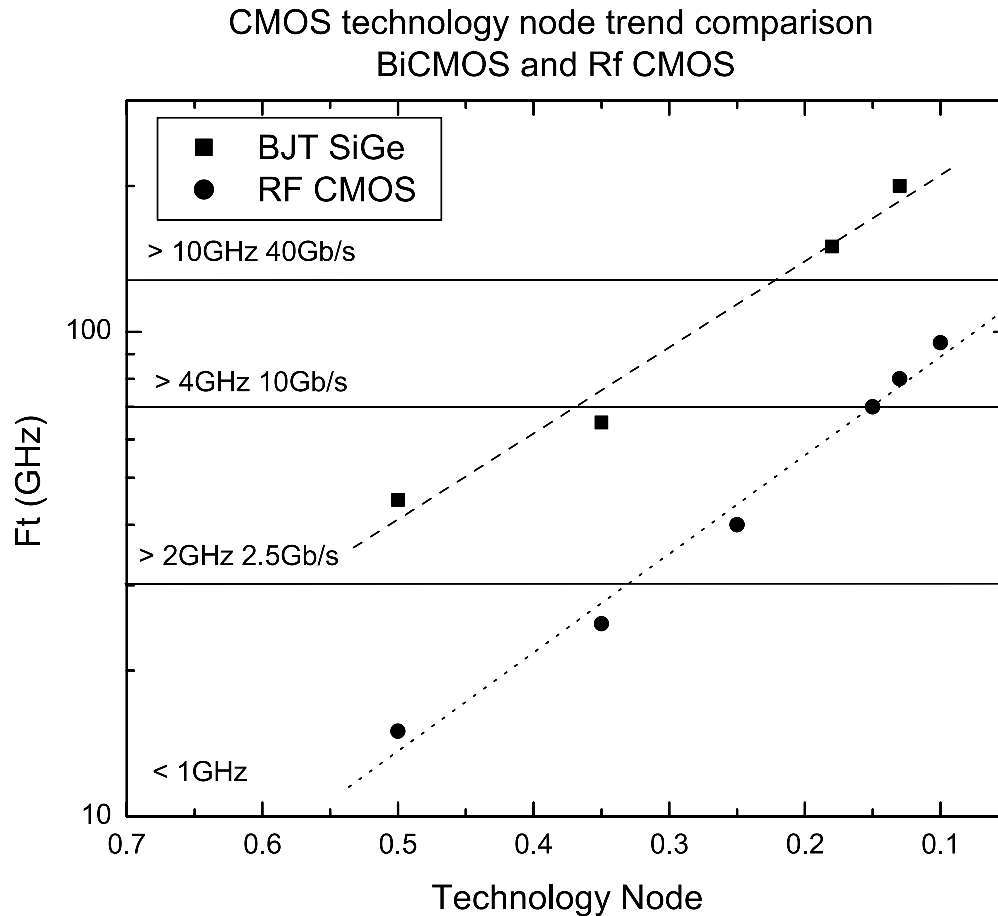


- CMOS and BJT technology advances along near-parallel paths
- SiGe maintains performance advantage ~2x over MOS at 0.10μm

# Technology cost comparisons

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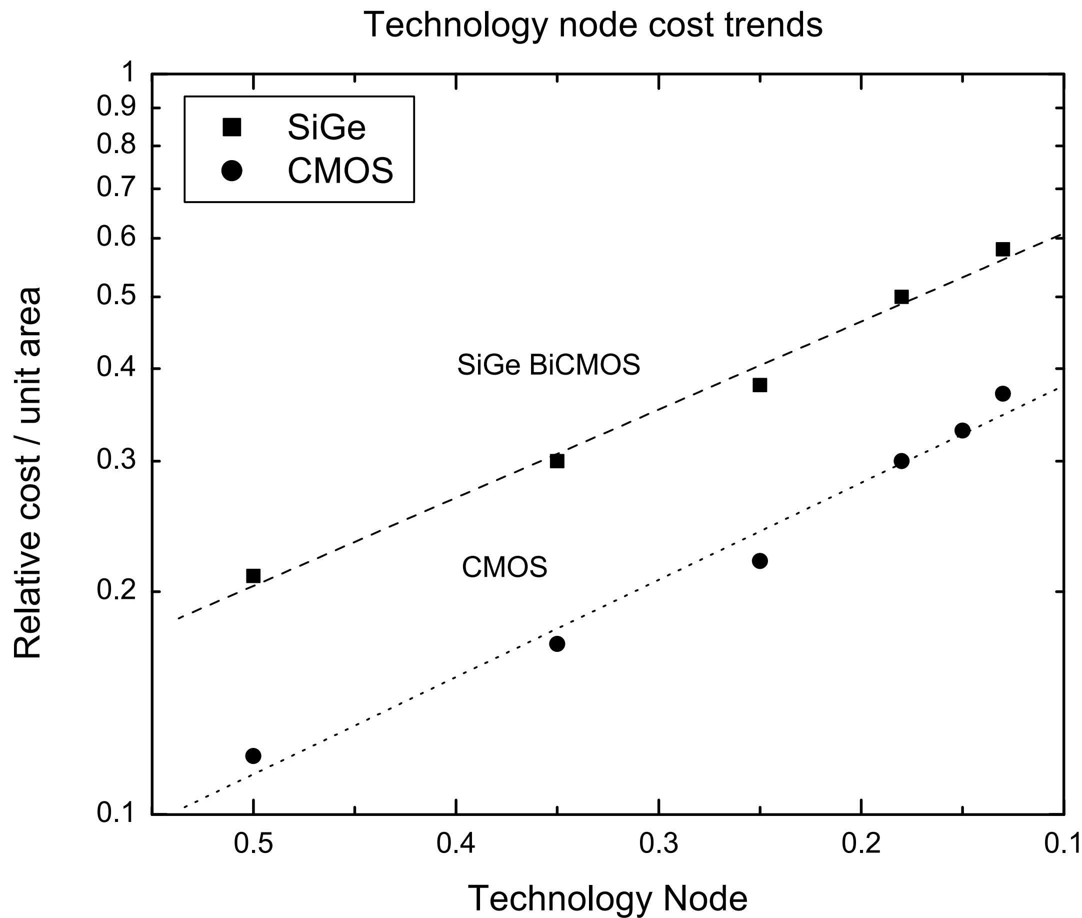


- Cost curves advance near-parallel
- BiCMOS has moderate cost penalty over CMOS at same technology node

# Performance-Cost comparisons

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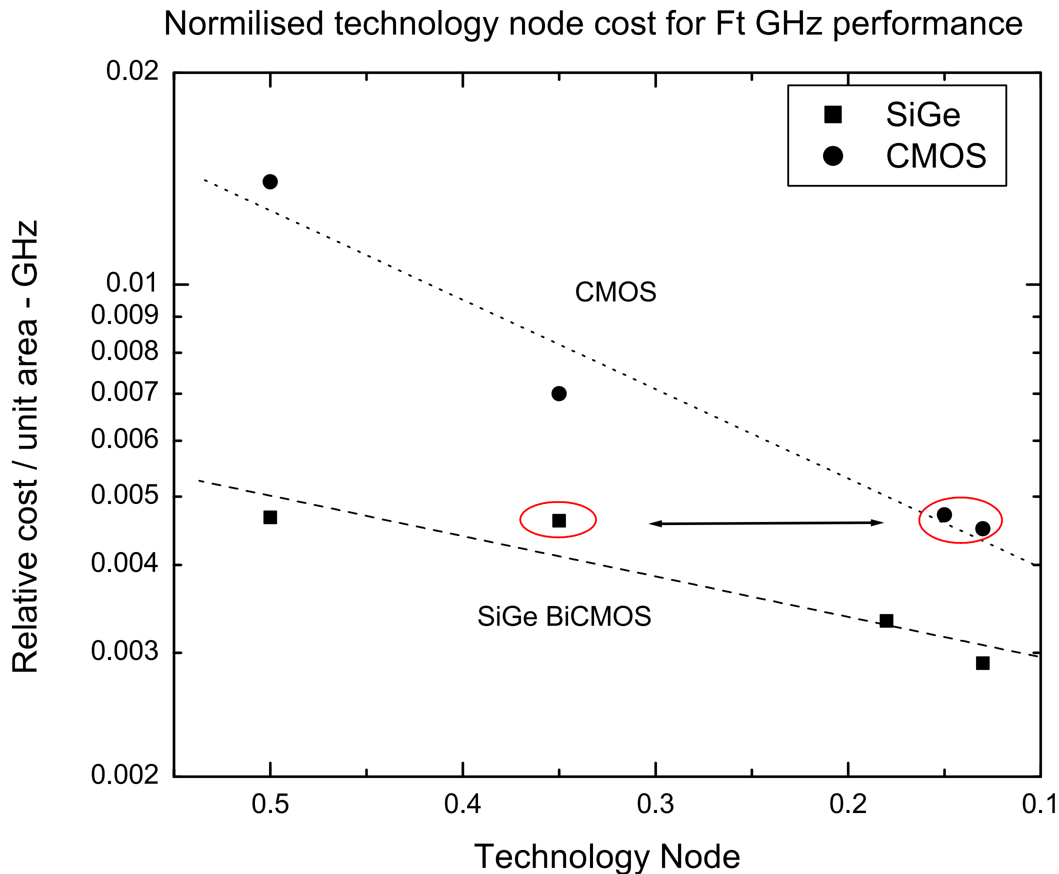


- Overall more performance at less cost
- skewed curves with advantage to BiCMOS beyond 0.10μm

# Wireless: 3G System Block Diagram

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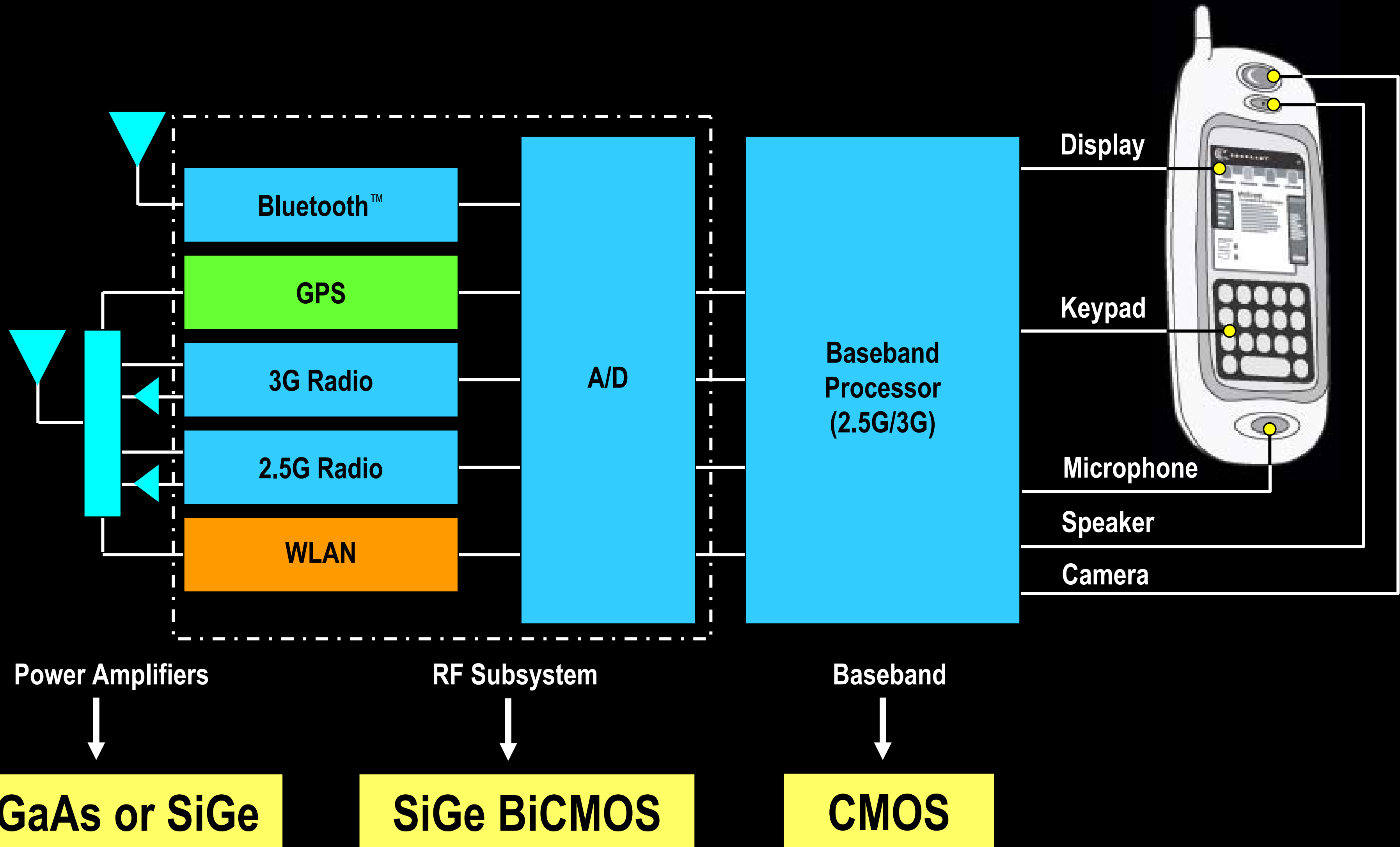

# Wireline: Optical Networking Block Diagram

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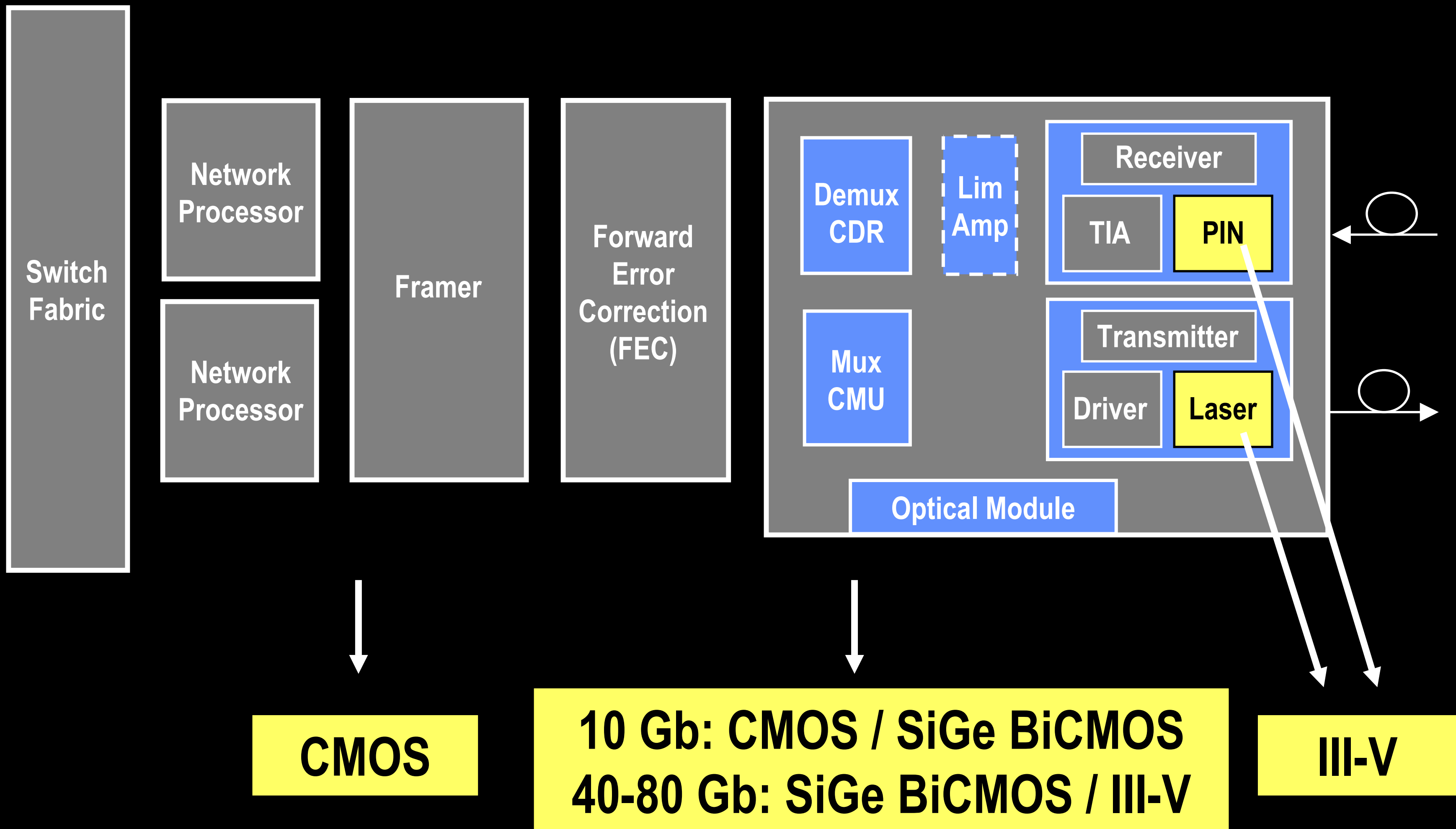

# Outline

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- Device Design for 200 GHz Ft and Fmax
- 0.18 μm SiGe BiCMOS Process Integration

# Device optimization parameters

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- **Aggressive vertical scaling to minimize diffusion component**
  - Band-gap engineering
  - Collector doping
  - Emitter resistance (Re)
  - Base width reduction (Wb)
- **Aggressive lateral scaling to minimize depletion terms**
  - Emitter width (We)
  - SA emitter

$$f_T = \frac{1}{2\pi\tau_{ec}} = \left\{ 2\pi \left[ R_e (C_{je} + C_{jc}) + \frac{kT}{qI_c}(C_{be} + C_{bc}) + R_c C_{bc} + \frac{W_b^2}{\eta D_b} + \frac{W_c}{2v_s} \right] \right\}^{-1}$$

Depletion terms

diffusion

$$f_{max} = \sqrt{\frac{f_T}{8\pi R_b C_{bc}}}$$

# Device Design for 200 GHz Ft and Fmax

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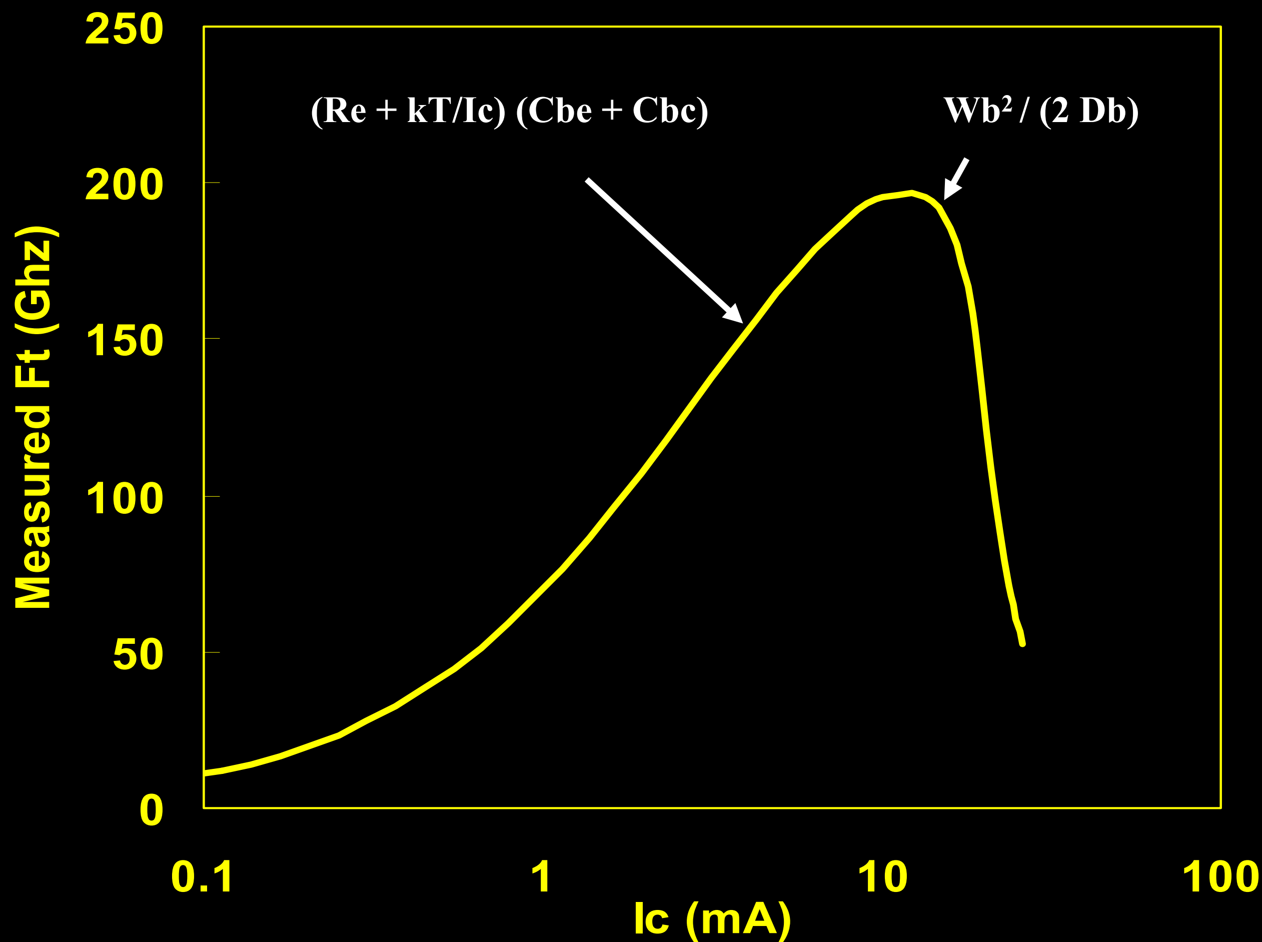

# *SiGe Collector Doping*

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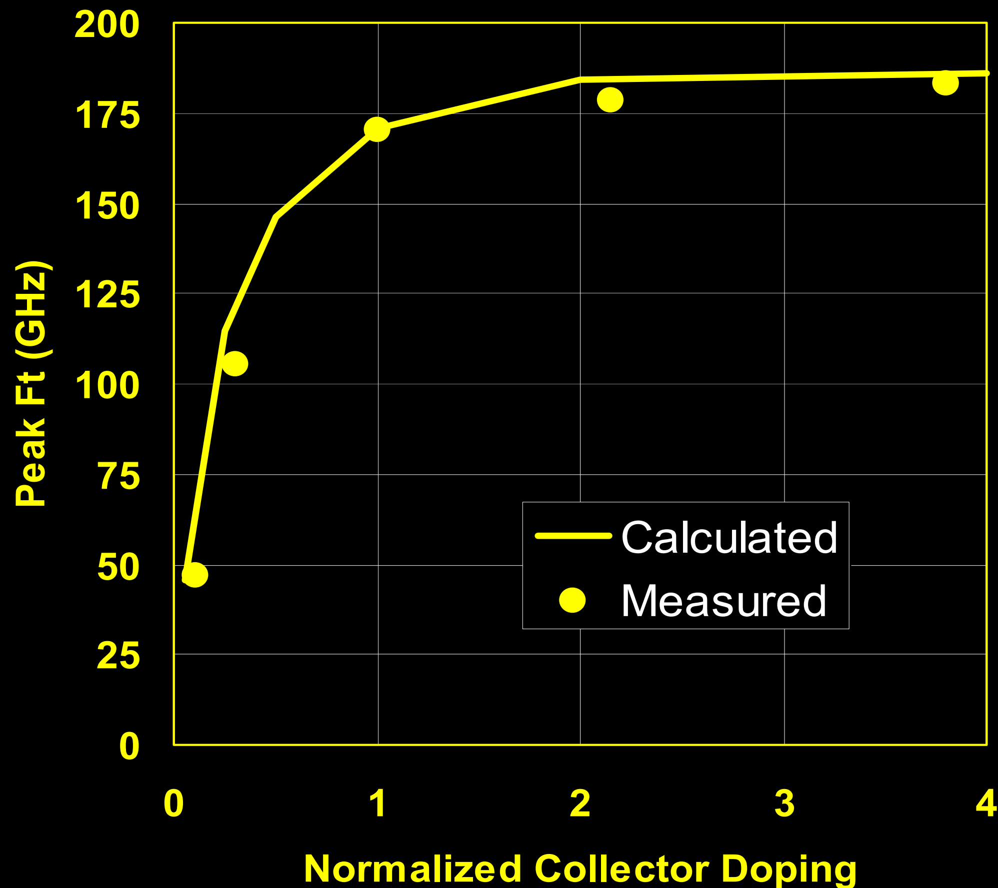
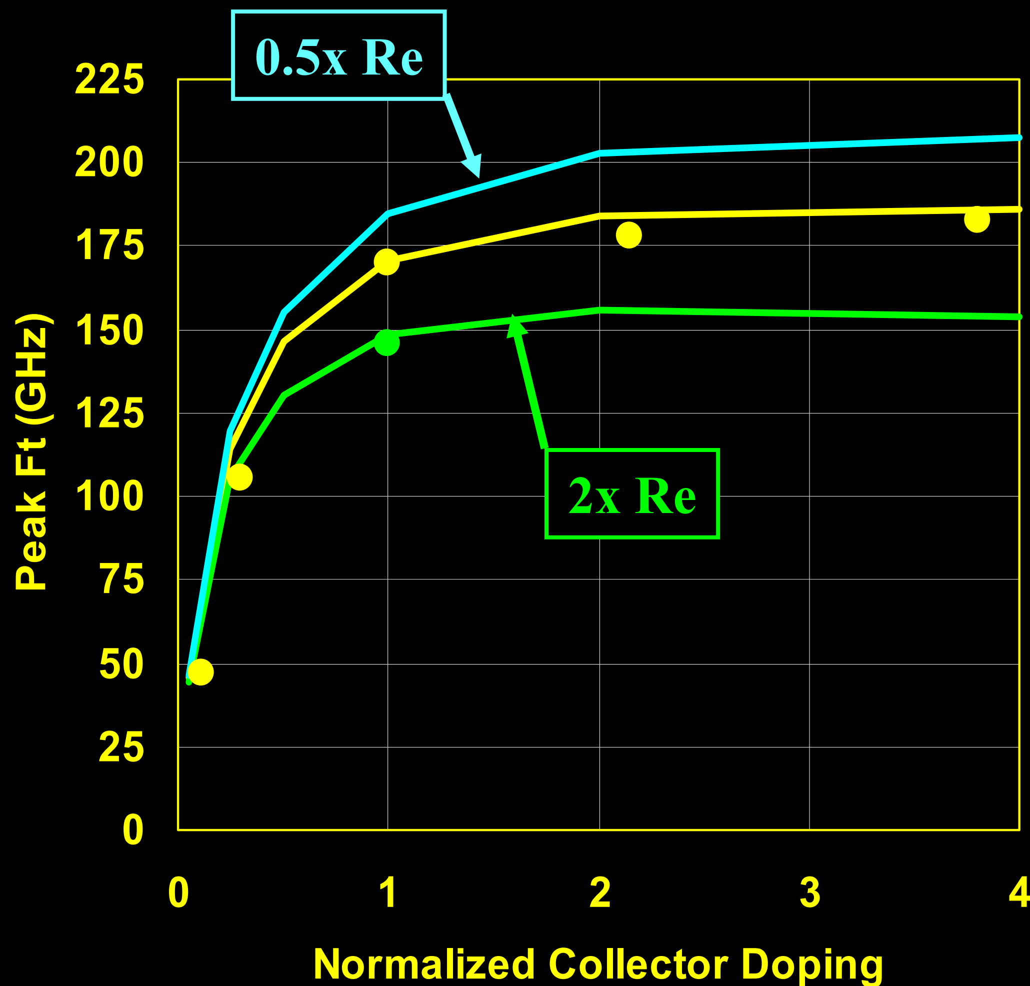
$$1/Ft \sim (Re + kT/Ic)(Cbe + Cbc) + Wb^2 / (2\ Db) + Wc/(2\ Vs) + Rc\ Cbc$$



# SiGe Emitter Resistance



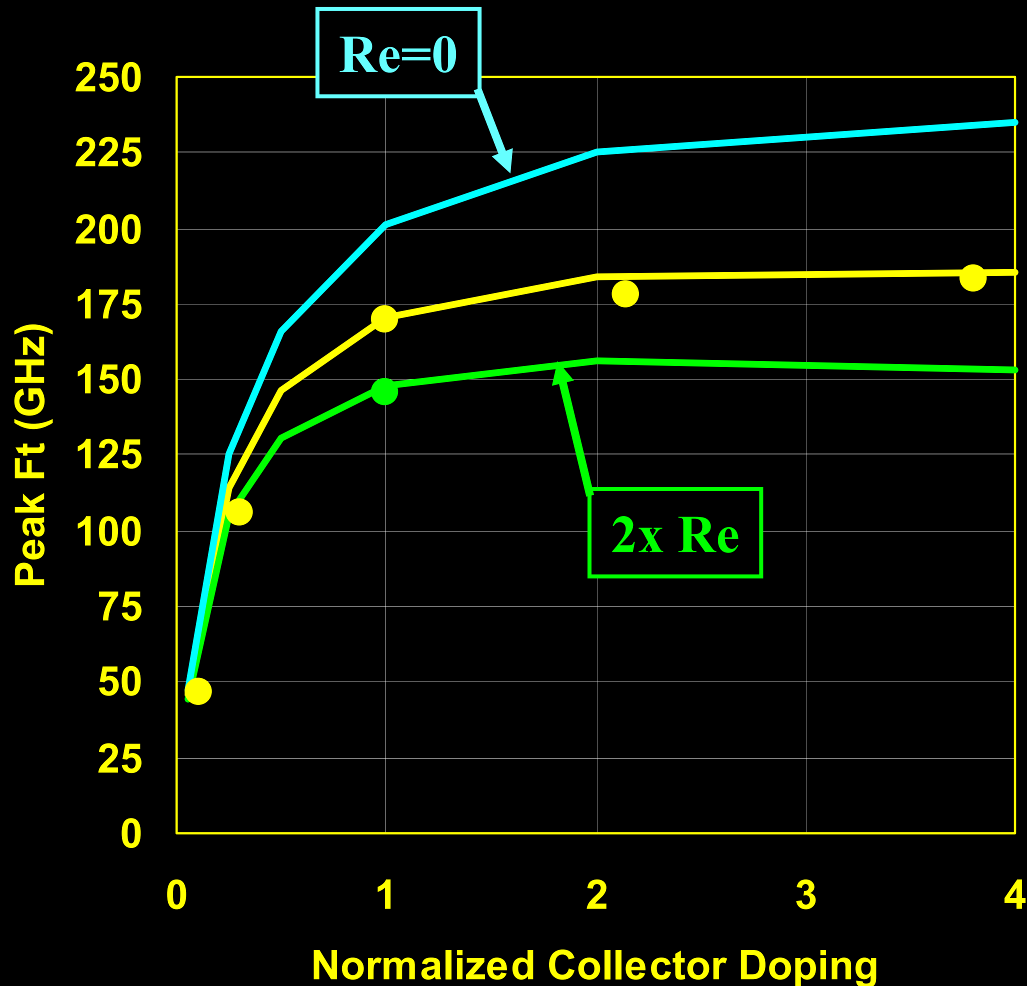
$$1/Ft \sim (Re + kT/Ic)(Cbe + Cbc) + Wb^2 / (2\, Db) + Wc/(2\, Vs) + Rc\, Cbc$$



# SiGe Emitter Resistance

CONEXANT

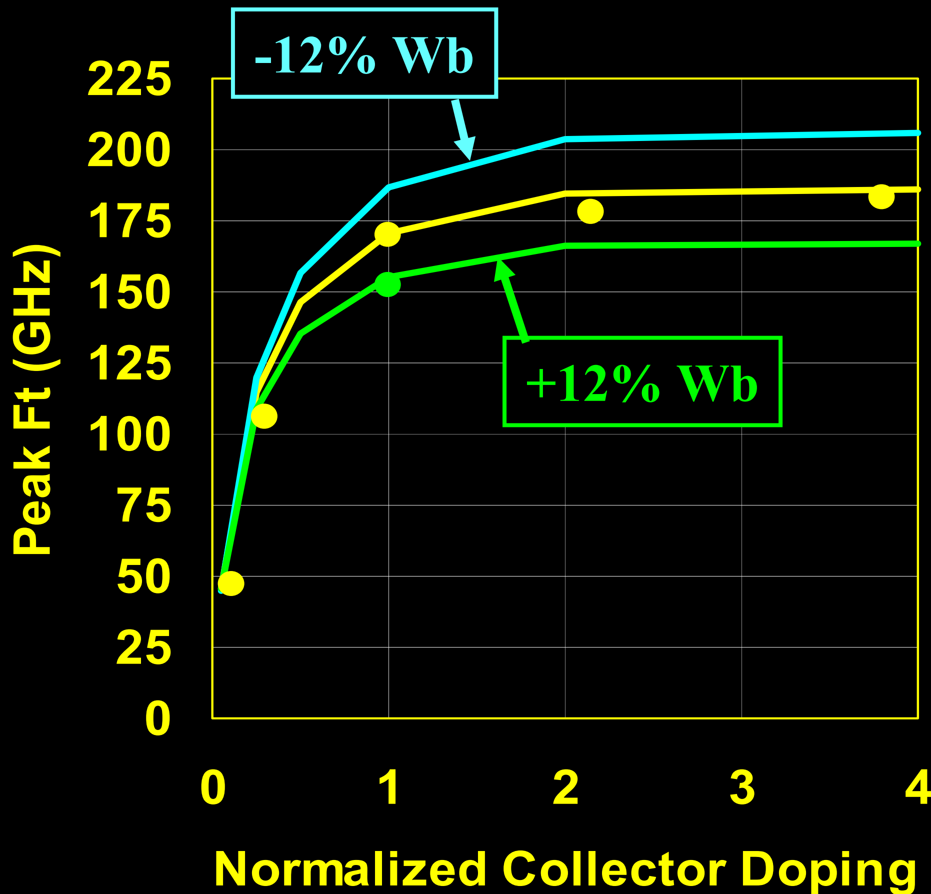
$$1/Ft \sim (Re + kT/Ic)(Cbe + Cbc) + Wb^2/(2\ Db) + Wc/(2\ Vs) + Rc\ Cbc$$



# SiGe Base Width



$$1/F_t \sim (R_e + kT/I_c)(C_{be} + C_{bc}) + W_b^2 / (2 D_b) + W_c/(2 V_s) + R_c C_{bc}$$




**Carbon Doping**

- \+ Reduces B diffusion
- — Degrades mobility
- — Increases Eg
- = Reduces Wb
- = Only small improvement in Ft

# Base narrowing for performance gain

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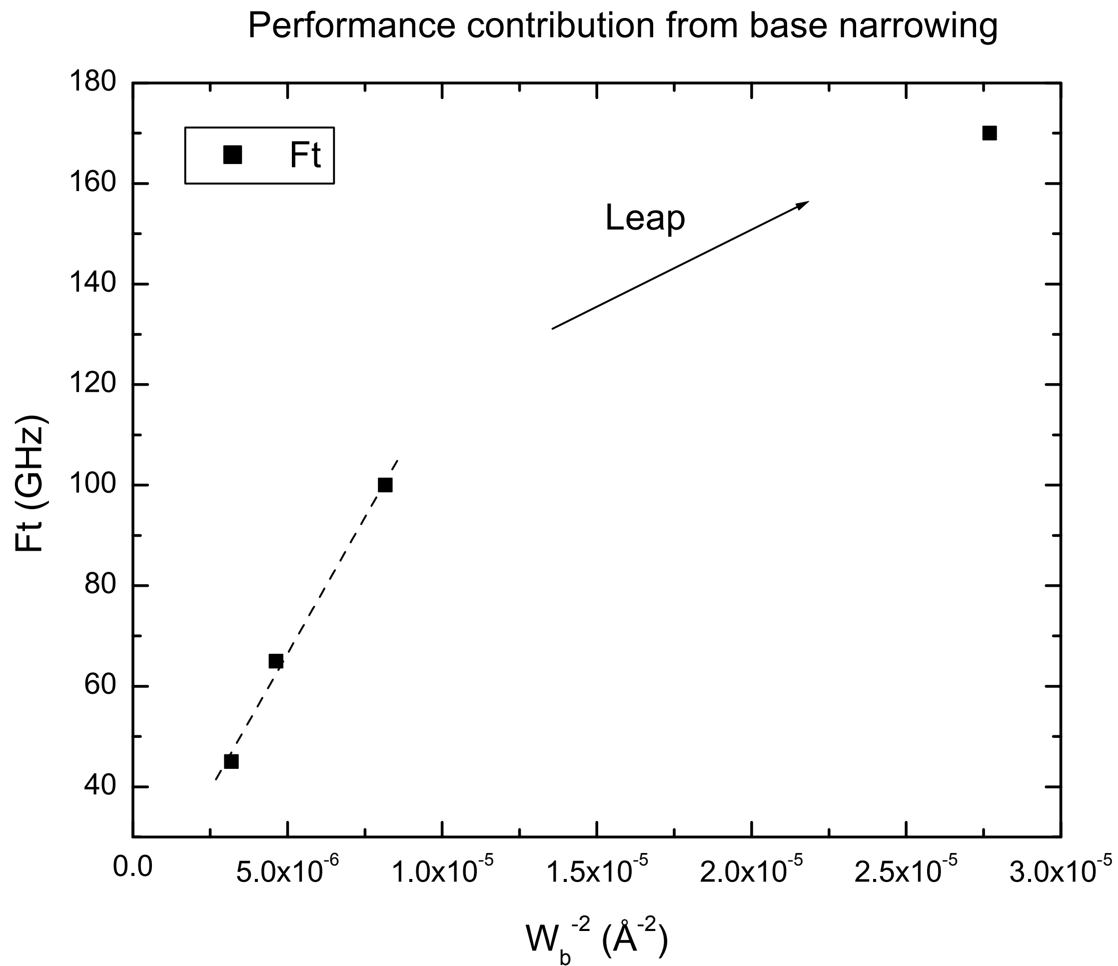

# SiGe Base Width

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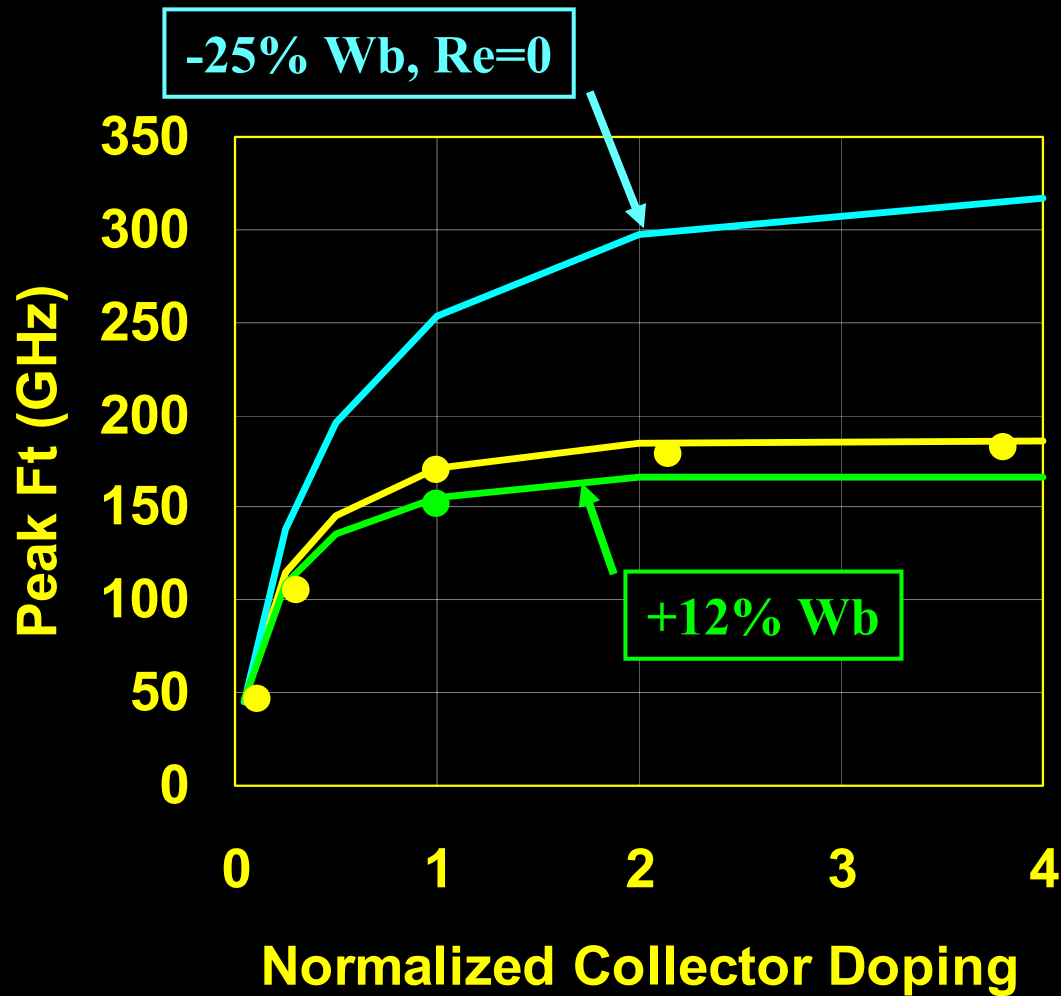

# Lateral Scaling

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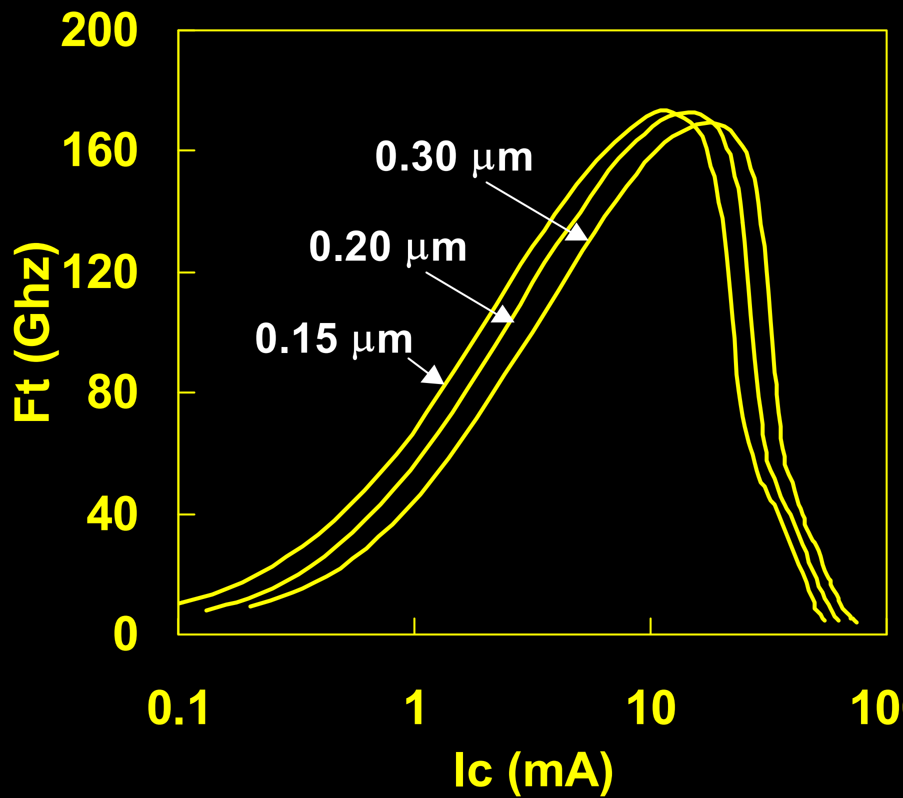
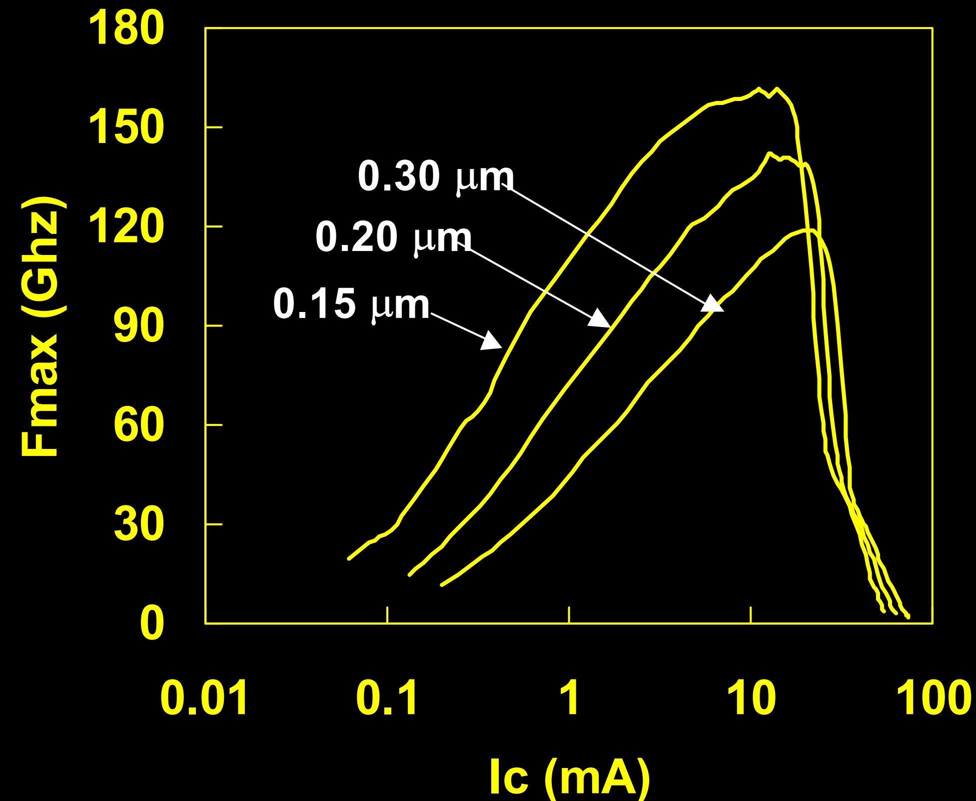
$$1/Ft \sim (Re + kT/Ic)(Cbe + Cbc) + Wb^2/(2\,Db) + Wc/(2\,Vs) + Rc\,Cbc$$

$$Fmax = (Ft/(8\pi\,Rb\,Cbc))^{1/2}$$




**Good scaling properties maintain Ft constant as We is reduced increasing Fmax**

# SiGe BiCMOS Landscape (Dec '01)

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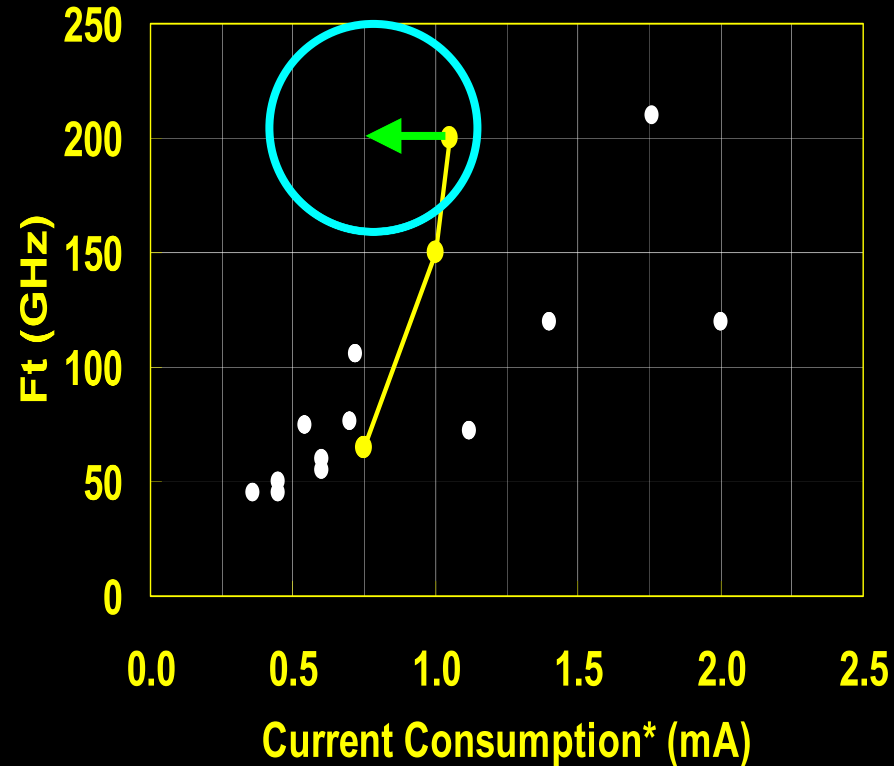


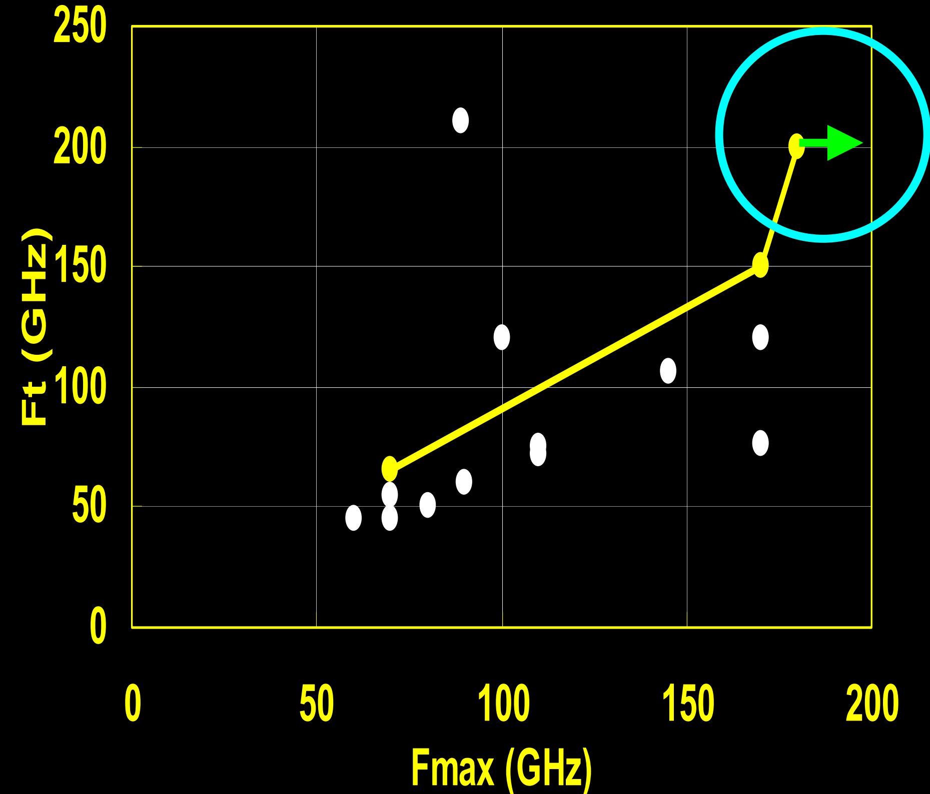


**200 GHz Ft/Fmax opens the door to 80 Gb applications in Silicon**

# *Outline*

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- **Device Design for 200 GHz Ft and Fmax**
- **0.18 μm SiGe BiCMOS Process Integration**

# 0.18 $\mu$m SiGe BiCMOS Process Integration

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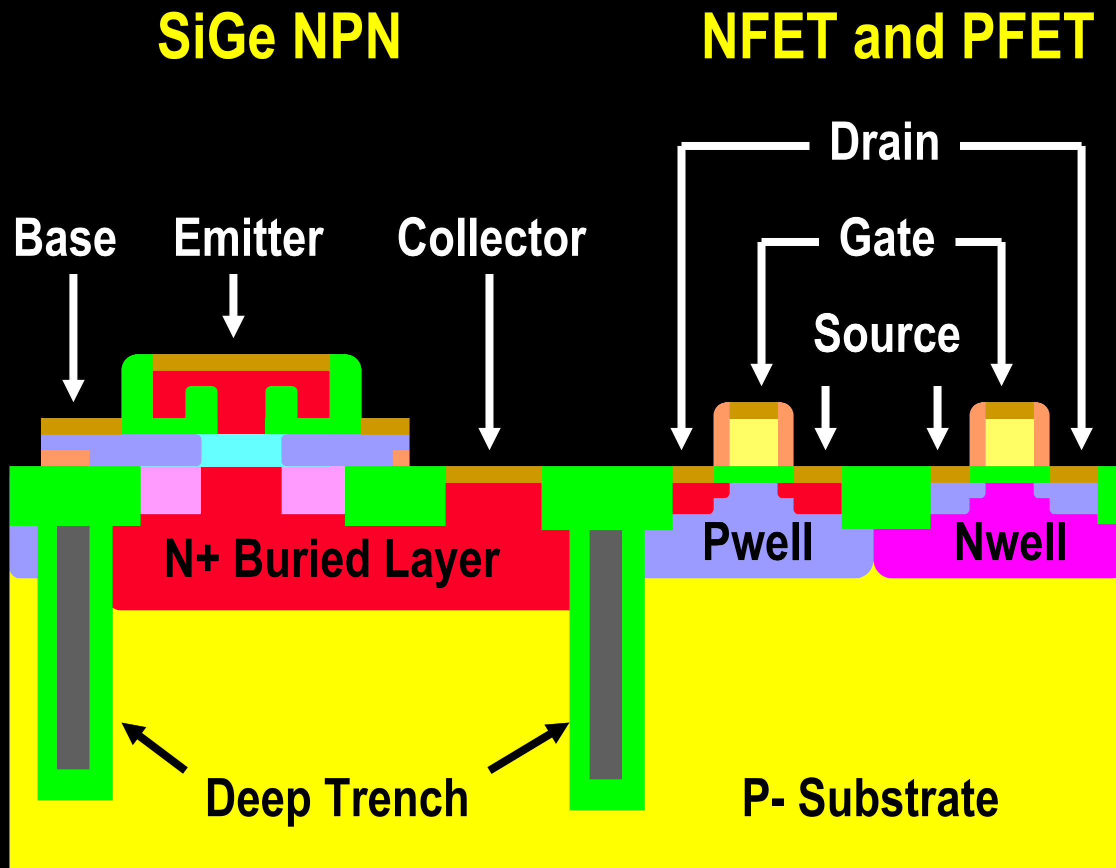

# SiGe BiCMOS: Buried Layer Integration

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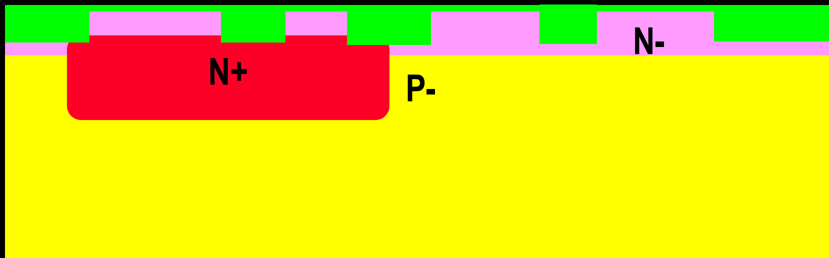
## Epi-Based

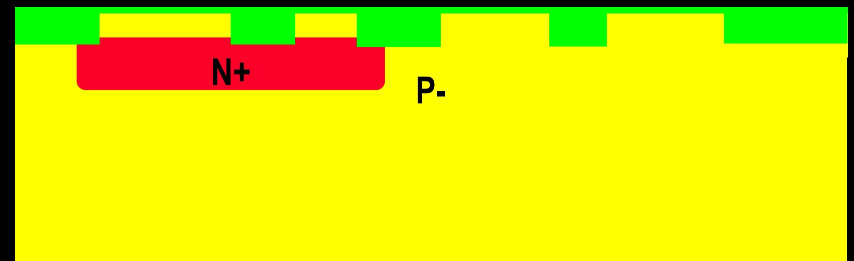
1. N+ Buried Layer Implant
2. Buried Layer Drive
3. N- Epitaxy




Lower Collector Resistance

## Epi-Less

1. High energy N+ Buried Layer Implant




Lower Cost

Lower Collector Substrate Capacitance

# SiGe BiCMOS: Isolation

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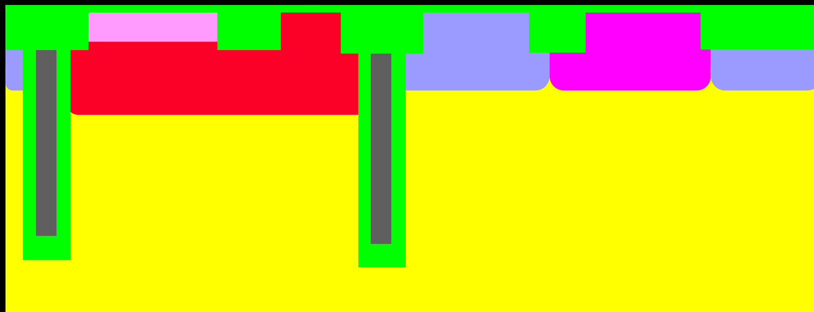
## Deep Trench

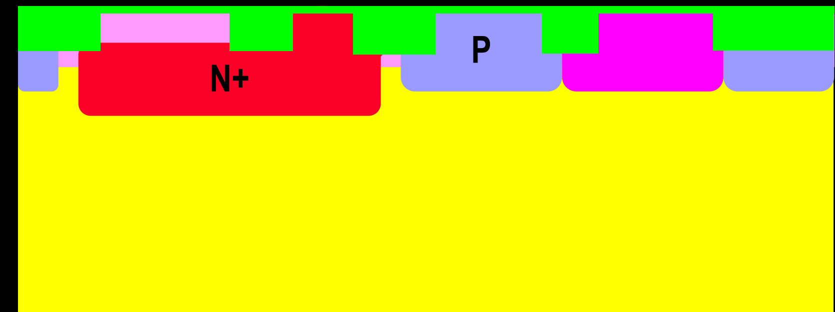
1. Deep Trench Etch
2. Deep Trench Oxide/Polysilicon Fill
3. N/Pwell Formation



4x Lower Collector-Substrate Capacitance

## Junction

- N/Pwell Formation




Lower Cost

# SiGe BiCMOS: Collector Implants

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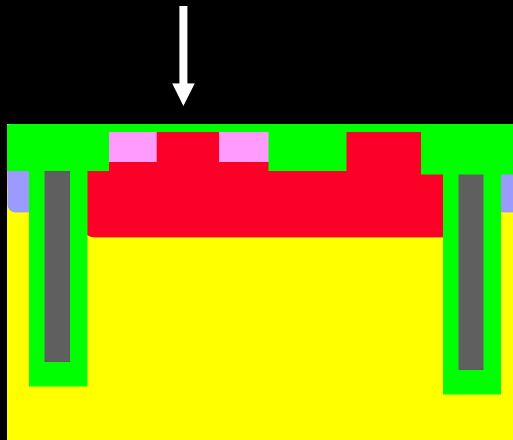
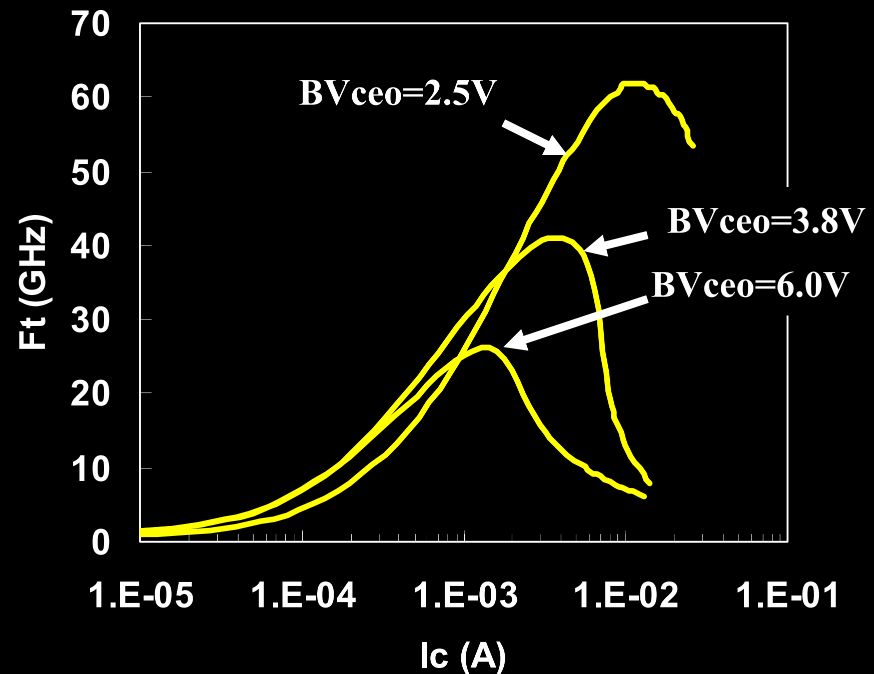
**Used to differentiate multiple NPNs on the same wafer**




**Tradeoff between Ft, Cbc, and breakdown becomes a design variable**

# SiGe BiCMOS: Gate Formation

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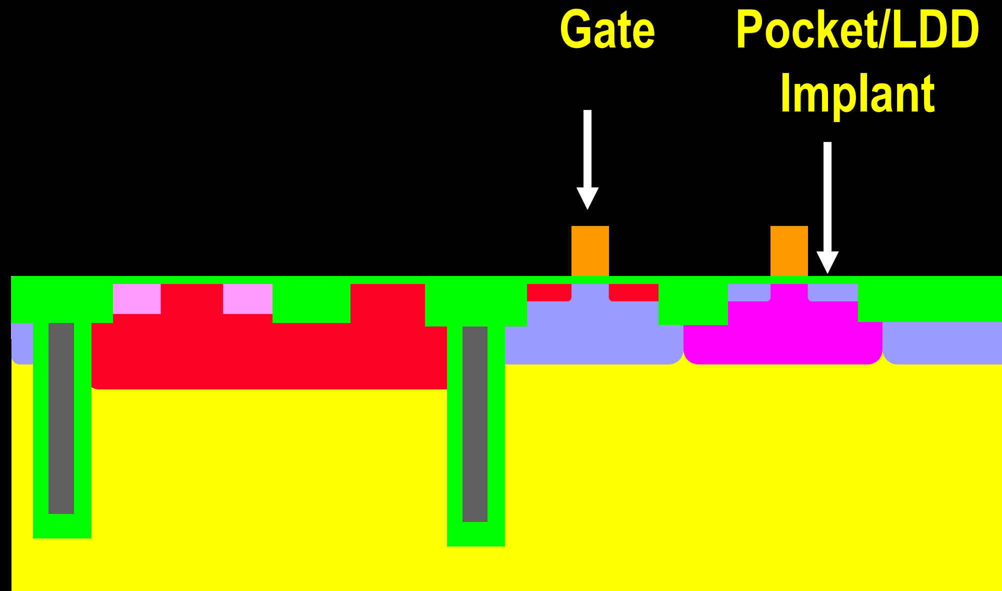


Gate formed prior to SiGe deposition to minimize thermal budget on NPN

# SiGe BiCMOS: Emitter-Base Integration

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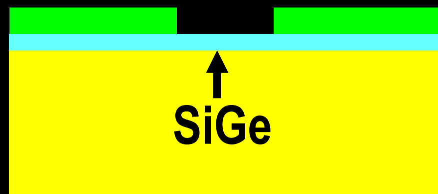
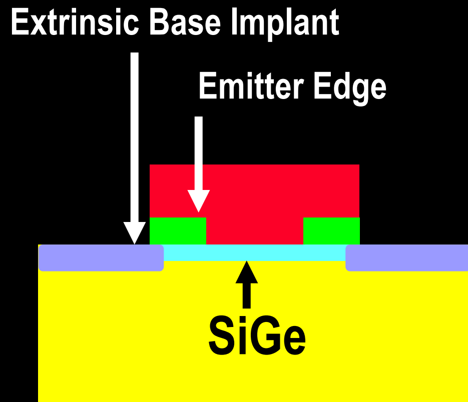
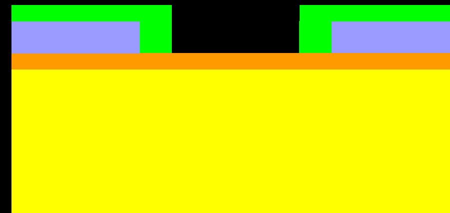
## QSA

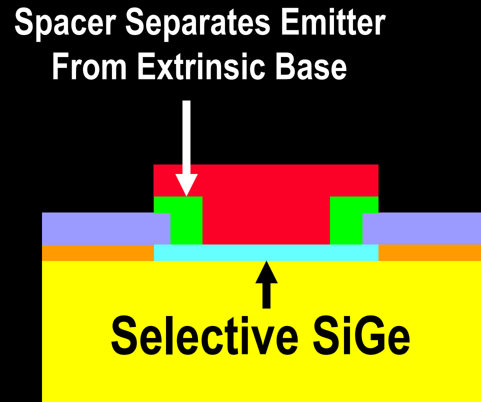



+ Lowest Cost
- High Rb

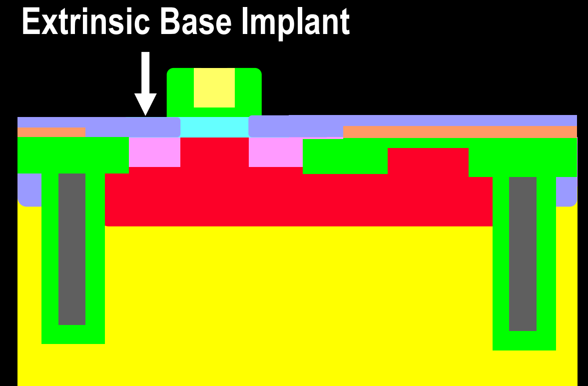
## Selective Epi

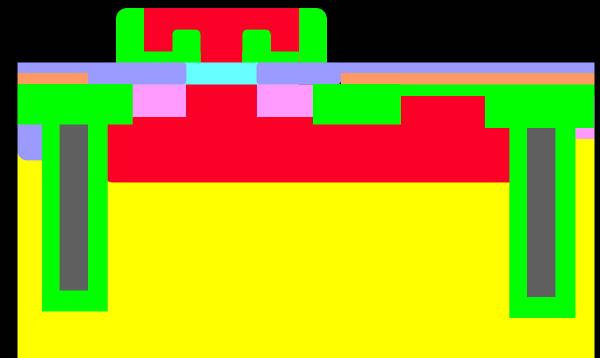





+ Easy "Plug-in" to Si NPN
+ Cjc self-aligned to emitter
- Requires selective SiGe

## Sacrificial Emitter



+ Lowest Rb
+ Best Scaling Properties

# SiGe BiCMOS: CMOS / Silicide

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Co Silicide

CMOS Spacers

S/D Implants

SRAM Cell

- NPN films completely removed from CMOS regions
- Silicide on all electrodes including emitter, base and collector

# *SiGe120 Cross-Section*

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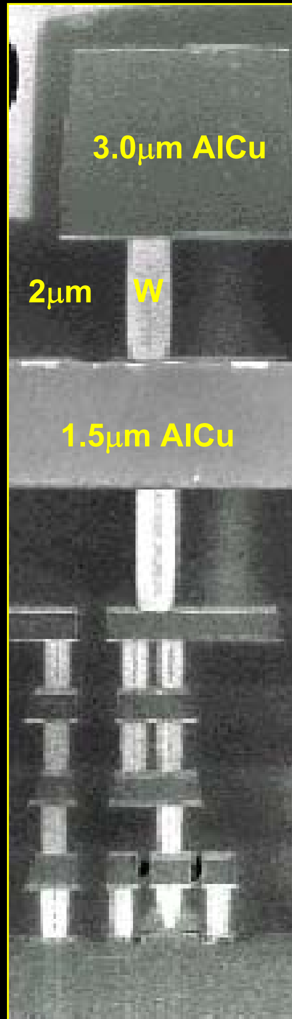
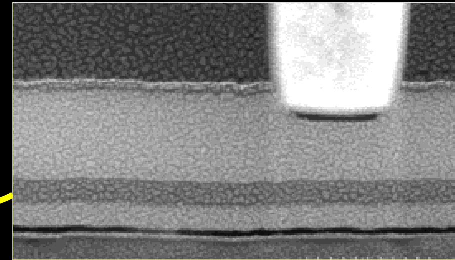
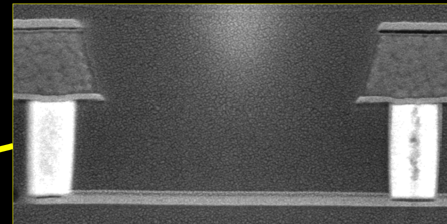
**6 Layers of Metal**



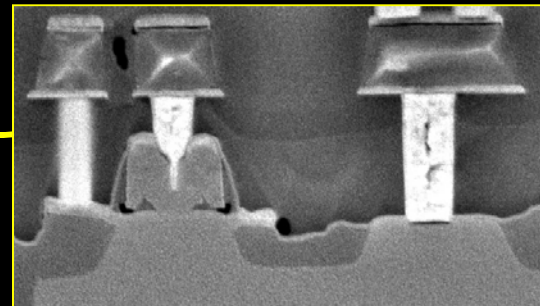

**1.5 fF/µm2 MIM Capacitor**



**25 Ω/sq Metal Resistor**



**NPN Transistor**



# Conclusions

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- The bipolar device has continued dominance in RFIC space for the foreseeable future
  - SiGe has opened a permanent gap in performance vs. CMOS
  - SiGe BiCMOS Cost / Area / GHz is competitive with that of deep-subμ CMOS
- Aggressive vertical and lateral scaling has so far enabled 200 Ft/Fmax
  - Advancement of vertical profile largely responsible for gains
  - Further device / process optimization en route to 300Ghz