Roadmap of SiGe BiCMOS technologies

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Continued dominance of bipolar in RFIC

- BJT/HBT higher performance than MOSFET
  - MOS moving from MHz to GHz
  - BJT moving from 1-2 GHz to >200 GHz

- Significantly lower cost than GaAs

- High-level integration complexity with BiCMOS technology at moderate cost penalty
Exceptional technological progress in <5 yrs
SiGe BJT on 6x faster performance curve
SiGe BiCMOS secures leading RFIC position

CMOS technology node trend comparison
BiCMOS and RF CMOS

- CMOS and BJT technology advances along near-parallel paths
- SiGe maintains performance advantage ~2x over MOS at 0.10 μm
Technology cost comparisons

- Cost curves advance near-parallel
- BiCMOS has moderate cost penalty over CMOS at same technology node
Performance-Cost comparisons

- Overall more performance at less cost
- Skewed curves with advantage to BiCMOS beyond 0.10\(\mu\)m
Wireless: 3G System Block Diagram

- Bluetooth™
- GPS
- 3G Radio
- 2.5G Radio
- WLAN

- A/D
- Baseband Processor (2.5G/3G)

- Power Amplifiers: GaAs or SiGe
- RF Subsystem: SiGe BiCMOS
- Baseband: CMOS

- Display
- Keypad
- Microphone
- Speaker
- Camera
**Wireline: Optical Networking Block Diagram**

Switch Fabric

Network Processor

Network Processor

Framer

Forward Error Correction (FEC)

Demux CDR

Lim Amp

Mux CMU

Optical Module

Receiver

TIA

PIN

Transmitter

Driver

Laser

10 Gb: CMOS / SiGe BiCMOS

40-80 Gb: SiGe BiCMOS / III-V

CMOS

III-V
Outline

- Device Design for 200 GHz $F_t$ and $F_{max}$
- 0.18 $\mu$m SiGe BiCMOS Process Integration
Device optimization parameters

- Aggressive vertical scaling to minimize diffusion component
  - Band-gap engineering
  - Collector doping
  - Emitter resistance (Re)
  - Base width reduction (Wb)
- Aggressive lateral scaling to minimize depletion terms
  - Emitter width (We)
  - SA emitter

\[
f_T = \frac{1}{2\pi \tau_{ec}} = \left\{ 2\pi \left[ R_e (C_{je} + C_{jc}) + \frac{kT}{qI_c} (C_{be} + C_{bc}) + R_c C_{bc} + \frac{W_b^2}{\eta D_b} + \frac{W_c}{2v_s} \right] \right\}^{-1}
\]

Depletion terms diffusion

\[
f_{\text{max}} = \sqrt{\frac{f_T}{8 \pi R_b C_{bc}}}
\]
Device Design for 200 GHz $F_t$ and $F_{max}$

\[
\frac{(R_e + kT/I_c) (C_{be} + C_{bc})}{Wb^2 / (2 \, Db)}
\]
SiGe Collector Doping

\[
\frac{1}{F_t} \sim (R_e + kT/I_c) \times (C_{be} + C_{bc}) + \frac{W_b^2}{2D_b} + \frac{W_c}{2V_s} + R_c \times C_{bc}
\]

![Graph showing the relationship between normalized collector doping and peak frequency response.](image)
SiGe Emitter Resistance

\[ \frac{1}{F_t} \sim (R_e + kT/I_c) (C_{be} + C_{bc}) + \frac{W_b^2}{2D_b} + \frac{W_c}{2V_s} + R_c C_{bc} \]
SiGe Emitter Resistance

\[
\frac{1}{Ft} \sim (R_e + kT/I_c) \left( C_{be} + C_{bc} \right) + \frac{W_b^2}{2D_b} + \frac{W_c}{2V_s} + R_c C_{bc}
\]

Re=0

Normalized Collector Doping

Peak Ft (GHz)

Normalized Collector Doping
SiGe Base Width

\[ 1/F_t \sim \left( R_e + kT/I_c \right) (C_{be} + C_{bc}) + \frac{W_b^2}{2D_b} + \frac{W_c}{2V_s} + R_c C_{bc} \]

Carbon Doping

- Reduces B diffusion
- Degrades mobility
- Increases \( E_g \)
- Reduces \( W_b \)
- Only small improvement in \( F_t \)
Base narrowing for performance gain

Performance contribution from base narrowing

\[ F_t (GHz) \]

\[ W_b^{-2} (\text{Å}^{-2}) \]
SiGe Base Width

Normalized Collector Doping

Peak $F_t$ (GHz)

-25% Wb, Re=0

+12% Wb

Normalized Collector Doping

0  1  2  3  4  5

0  50  100  150  200  250  300  350
Lateral Scaling

\[
\frac{1}{F_t} \sim (R_e + kT/I_c) (C_{be} + C_{bc}) + \frac{W_b^2}{(2D_b)} + \frac{W_c}{(2V_s)} + R_c C_{bc}
\]

\[
F_{\text{max}} = \left( \frac{F_t}{(8\pi R_b C_{bc})} \right)^{1/2}
\]

Good scaling properties maintain \( F_t \) constant as \( W_e \) is reduced increasing \( F_{\text{max}} \).
200 GHz $F_t/F_{max}$ opens the door to 80 Gb applications in Silicon

*Current required to reach peak $F_t$ for minimum $W_e$ and $L_e=1 \mu m$
• Device Design for 200 GHz Ft and Fmax

• 0.18 µm SiGe BiCMOS Process Integration
SiGe BiCMOS: Buried Layer Integration

Epi-Based
1. N+ Buried Layer Implant
2. Buried Layer Drive
3. N- Epitaxy

Lower Collector Resistance

Epi-Less
1. High energy N+ Buried Layer Implant

Lower Cost
Lower Collector Substrate Capacitance
SiGe BiCMOS: Isolation

Deep Trench

1. Deep Trench Etch
2. Deep Trench Oxide/Polysilicon Fill
3. N/Pwell Formation

4x Lower Collector-Substrate Capacitance

Lower Cost

Junction

- N/Pwell Formation
SiGe BiCMOS: Collector Implants

Used to differentiate multiple NPNs on the same wafer

Tradeoff between $F_t$, $C_{bc}$, and breakdown becomes a design variable
SiGe BiCMOS: Gate Formation

Gate formed prior to SiGe deposition to minimize thermal budget on NPN
**SiGe BiCMOS: Emitter-Base Integration**

**QSA**
- Lowest Cost
- High Rb

**Selective Epi**
- Easy “Plug-in” to Si NPN
- Cjc self-aligned to emitter
- Requires selective SiGe

**Sacrificial Emitter**
- Lowest Rb
- Best Scaling Properties

Extrinsic Base Implant
Spacer Separates Emitter From Extrinsic Base
SiGe BiCMOS: CMOS / Silicide

- NPN films completely removed from CMOS regions
- Silicide on all electrodes including emitter, base and collector
SiGe120 Cross-Section

6 Layers of Metal

1.5 fF/µm2 MIM Capacitor

25 Ω/sq Metal Resistor

NPN Transistor
Conclusions

• The bipolar device has continued dominance in RFIC space for the foreseeable future
  – SiGe has opened a permanent gap in performance vs. CMOS
  – SiGe BiCMOS Cost / Area / GHz is competitive with that of deep-subμ CMOS

• Aggressive vertical and lateral scaling has so far enabled 200 Ft/Fmax
  – Advancement of vertical profile largely responsible for gains
  – Further device / process optimization en route to 300Ghz