Properties and Applications of Strained Si/SiGe

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Applied Materials

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Outline of talk

- *Bandgap Engineering*
- *Strained Si - Growth*
- *Film Characterization - Strain, Defect density*
- *Device Structure, challenges*
- *Strained Si on SOI*
- *Conclusions*

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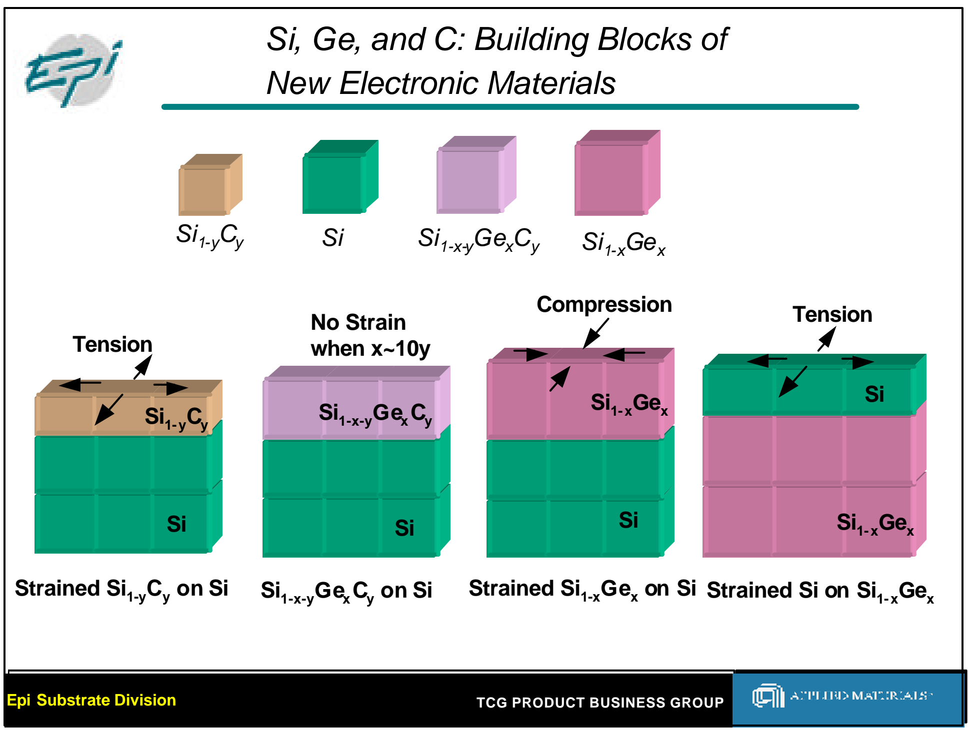
Si, Ge, and C: Building Blocks of New Electronic Materials
Si1-yCy
Si
Si1-x-yGexCy
Si1-xGex
Tension
No Strain when x~10y
Compression
Tension
Si1-yCy
Si
Si1-x-yGexCy
Si
Si1-xGex
Si
Si
Si1-xGex
Strained Si1-yCy on Si
Si1-x-yGexCy on Si
Strained Si1-xGex on Si
Strained Si on Si1-xGex
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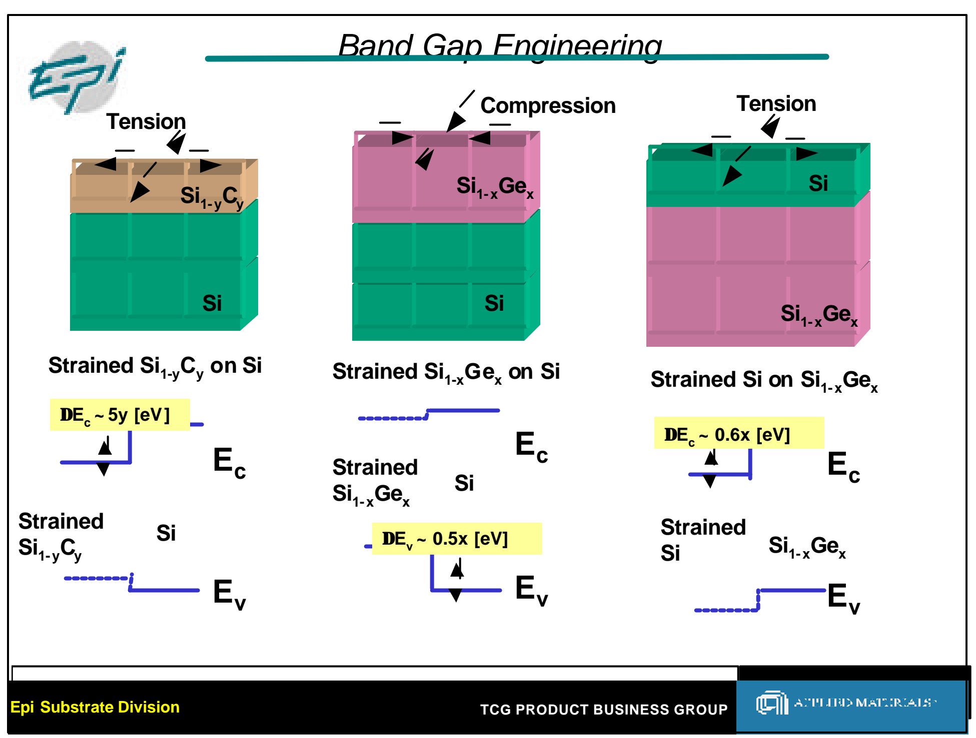
Band Gap Engineering
Tension
Compression
Tension
Si1-yCy
Si
Si1-xGex
Si
Si
Si1-xGex
Strained Si1-yCy on Si
Strained Si1-xGex on Si
Strained Si on Si1-xGex
DEc ~ 5y [eV]
Ec
Strained Si1-yCy
Si
Ev
Ec
Strained Si1-xGex
Si
DEv ~ 0.5x [eV]
Ev
DEc ~ 0.6x [eV]
Ec
Strained Si
Si1-xGex
Ev
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Applications for Low Temperature SiGe and SiGeC Epitaxy

Material	Application	Benefits	Status
$Si_{1-x}Ge_x$, $0<x<0.3$	Base of npn HBT	• Enhanced gain due to barrier for holes drifting from SiGe base to Si emitter • Enhanced frequency due to drift electrical field	Volume production
$Si_{1-x-y}Ge_xC_y$, $0<x<0.3$, $y<0.002$	Base of npn HBT	• Reduction of boron diffusion by carbon	R&D/ Pilot production
$Si_{1-x}Ge_x$, $0<x<0.3$	Elevated source/drain of MOSFET	• Reduced thinning of source/drain areas during silicidation (Ge can be used to increase growth rate)	R&D/ Pilot production
Strained Si on $Si_{1-x}Ge_x$, $0.2<x<0.5$	Channel of MOSFET	• Enhanced speed due to increase in mobility	R&D
SiC, $0<y<0.02$	Channel of MOSFET	• Enhanced speed due to increase in mobility	R&D
$Si_{1-y}C_y$, $0<y<0.02$	Base of npn HBT	• Enhanced gain due to barrier for electrons drifting from SiC base to Si emitter • Enhanced frequency due to drift electrical field	R&D
$Si_{1-x}Ge_x$, $x<0.1$	Waveguides	• Increased refractive index	R&D
$Si_{1-x}Ge_x$, $x>0.3$	Photodetectors	• Increased infrared light absorption	R&D

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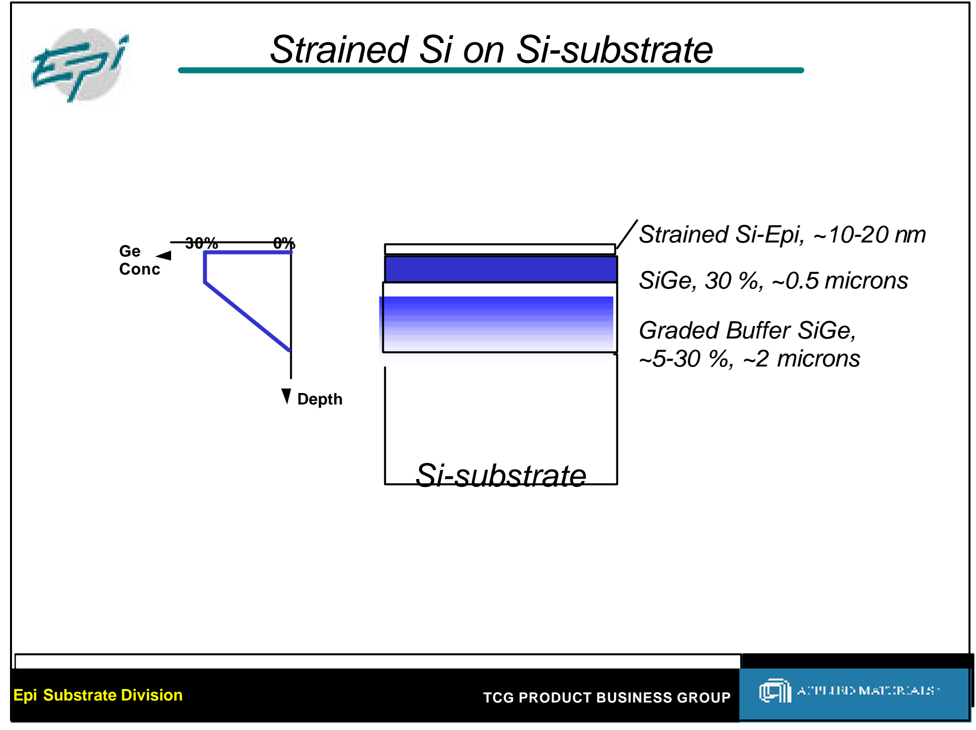


Why Strained Si?

Advantages:

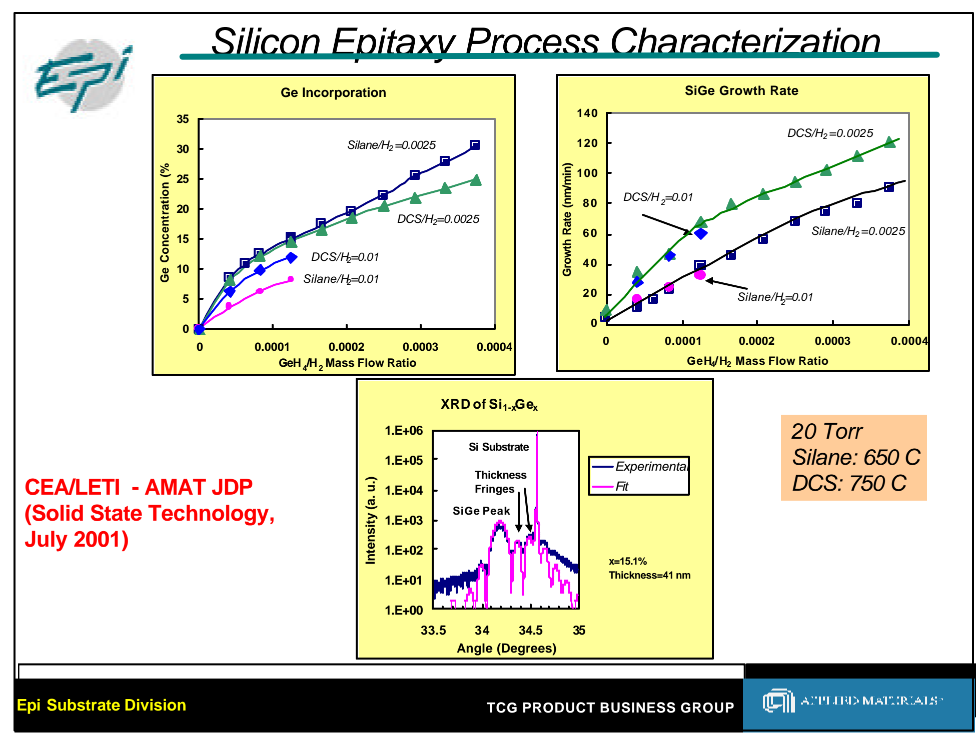
Bulk electron and hole mobility is enhanced in Strained Si:
For p-MOSFET, hole mobility increases for Ge content up to 30-40%, while for n-MOSFET, the electron mobility saturates at about 20% of Ge.

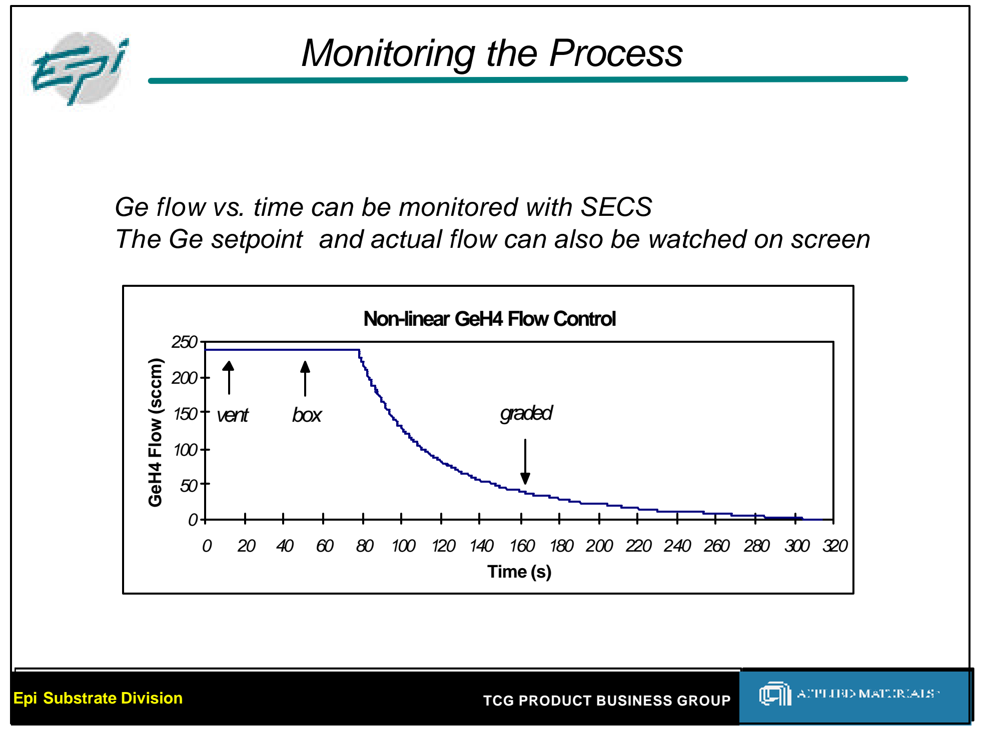
Reported Improvements:

- **Electron mobilities > 70 % on bulk Si NMOS is reported by IBM which translates into > 35% Id improvement (VLSI '01)**
- **Electron mobilities of > 50 % and hole mobilities 15-20 % on SOI is reported by IBM (VLSI '01)**
- **Electron mobilities of 1.7x on SOI is reported by Hoyt (IEEE El. Dev. Letr '01)**
- **Electron mobilities > 75 % on bulk Si is reported by Hoyt, Gibbons & Rim (IEEE Trans, '00)**

Key issues:

- **Gate Oxidation**
- **Device Isolation**
- **Self Heating**
- **Growth rate - cost**
- **Defect density at surface**
- **Process integration difficulties**




Monitoring the Process
Ge flow vs. time can be monitored with SECS
The Ge setpoint and actual flow can also be watched on screen
Non-linear GeH4 Flow Control
GeH4 Flow (sccm)
Time (s)
vent
box
graded
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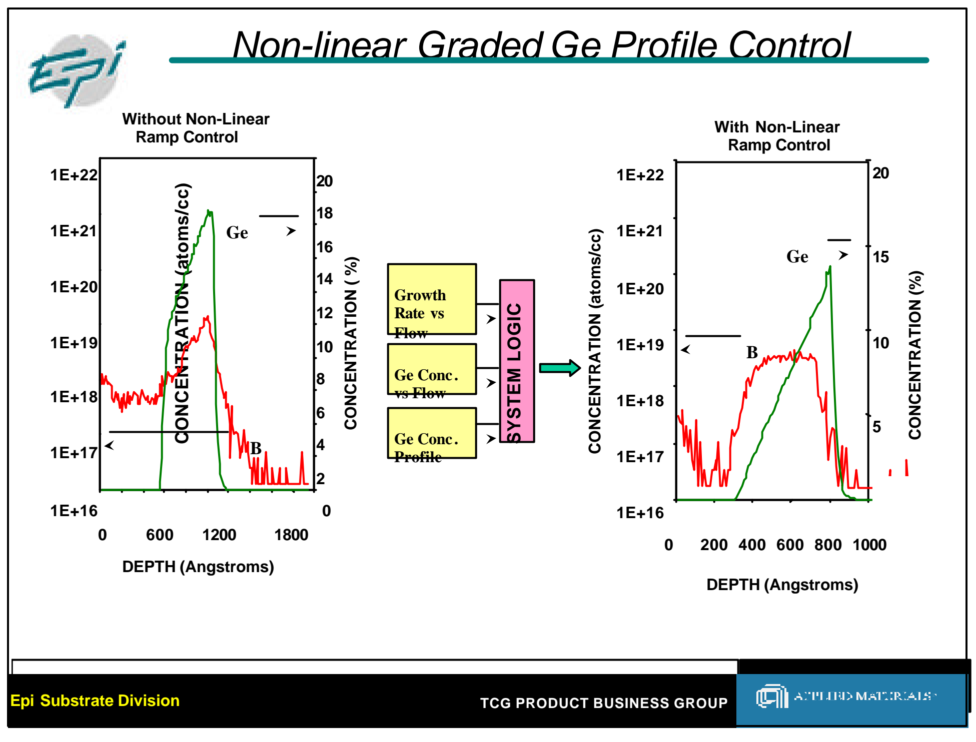
Non-linear Graded Ge Profile Control
Without Non-Linear Ramp Control
With Non-Linear Ramp Control
CONCENTRATION (atoms/cc)
CONCENTRATION (%)
CONCENTRATION (%)
DEPTH (Angstroms)
Ge
B
Growth Rate vs Flow
Ge Conc. vs Flow
Ge Conc. Profile
SYSTEM LOGIC
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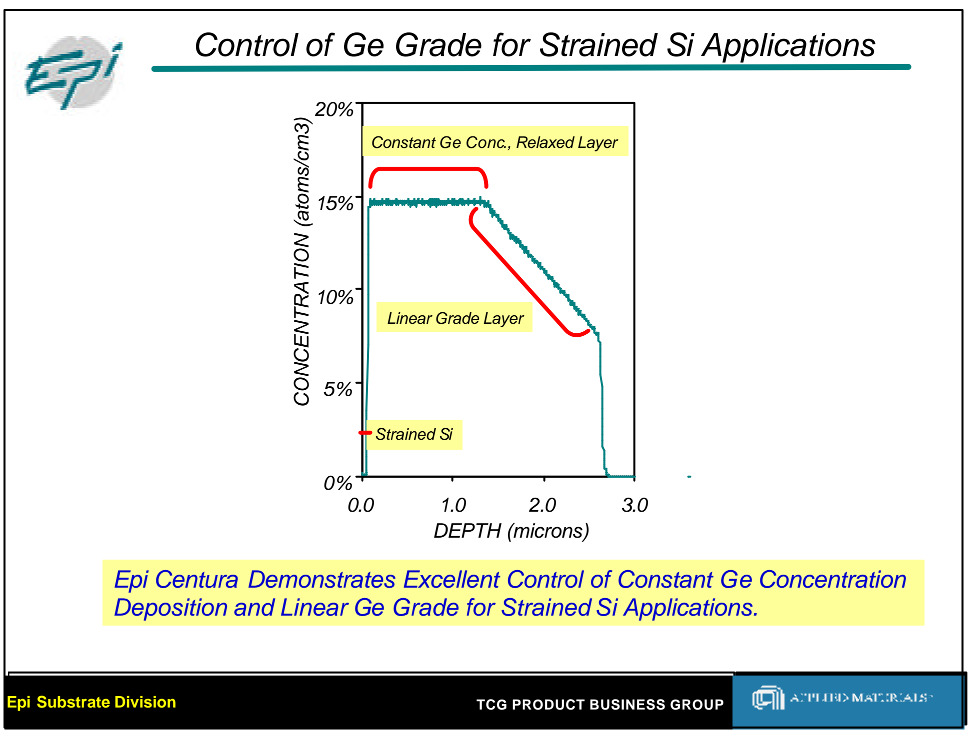
Control of Ge Grade for Strained Si Applications
20%
15%
10%
5%
0%
CONCENTRATION (atoms/cm3)
Constant Ge Conc., Relaxed Layer
Linear Grade Layer
Strained Si
0.0
1.0
2.0
3.0
DEPTH (microns)
Epi Centura Demonstrates Excellent Control of Constant Ge Concentration Deposition and Linear Ge Grade for Strained Si Applications.
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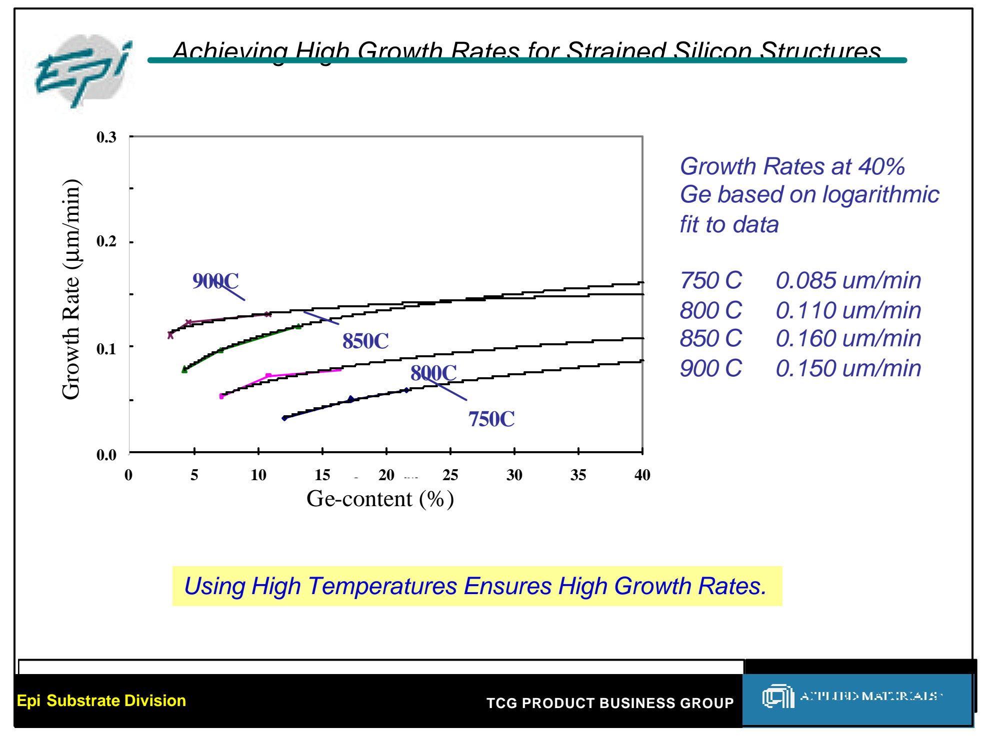
Achieving High Growth Rates for Strained Silicon Structures
Growth Rate (µm/min)
0.3
0.2
0.1
0.0
0
5
10
15
20
25
30
35
40
Ge-content (%)
900C
850C
800C
750C
Growth Rates at 40% Ge based on logarithmic fit to data
750 C 0.085 um/min
800 C 0.110 um/min
850 C 0.160 um/min
900 C 0.150 um/min
Using High Temperatures Ensures High Growth Rates.
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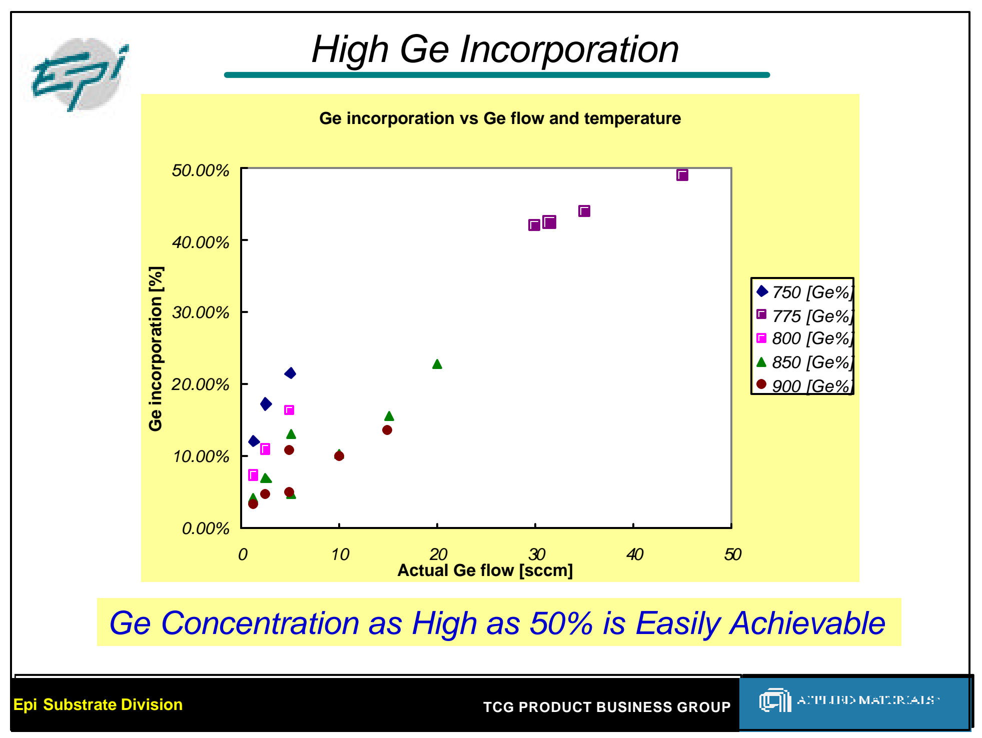
High Ge Incorporation
Ge incorporation vs Ge flow and temperature
Ge incorporation [%]
50.00%
40.00%
30.00%
20.00%
10.00%
0.00%
0
10
20
30
40
50
Actual Ge flow [sccm]
750 [Ge%]
775 [Ge%]
800 [Ge%]
850 [Ge%]
900 [Ge%]
Ge Concentration as High as 50% is Easily Achievable
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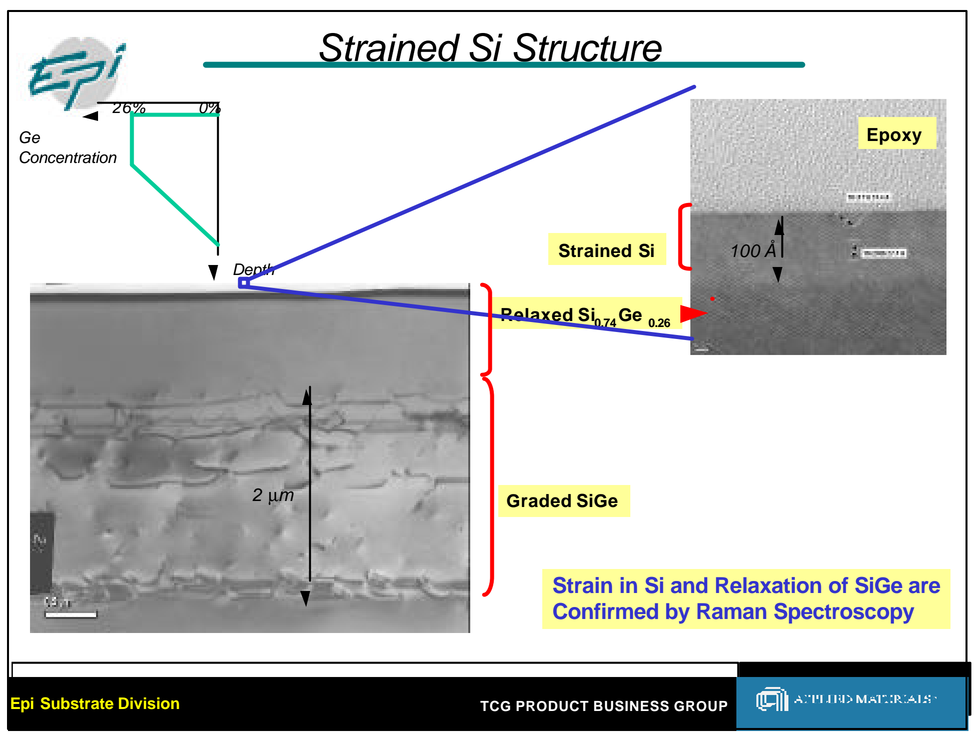
Strained Si Structure
26%
0%
Ge
Concentration
Depth
Epoxy
Strained Si
100 Å
Relaxed $Si_{0.74}Ge_{0.26}$
Graded SiGe
2 µm
Strain in Si and Relaxation of SiGe are
Confirmed by Raman Spectroscopy
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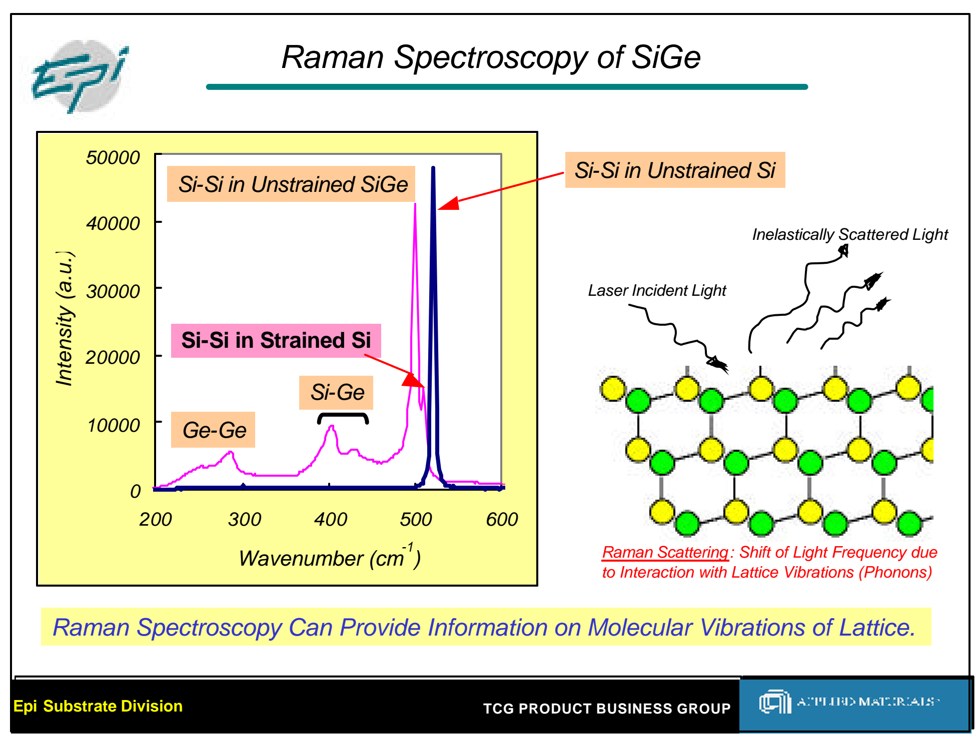

Raman Spectroscopy of SiGe
Si-Si in Unstrained SiGe
Si-Si in Unstrained Si
Si-Si in Strained Si
Si-Ge
Ge-Ge
Intensity (a.u.)
Wavenumber (cm-1)
Inelastically Scattered Light
Laser Incident Light
Raman Scattering: Shift of Light Frequency due to Interaction with Lattice Vibrations (Phonons)
Raman Spectroscopy Can Provide Information on Molecular Vibrations of Lattice.
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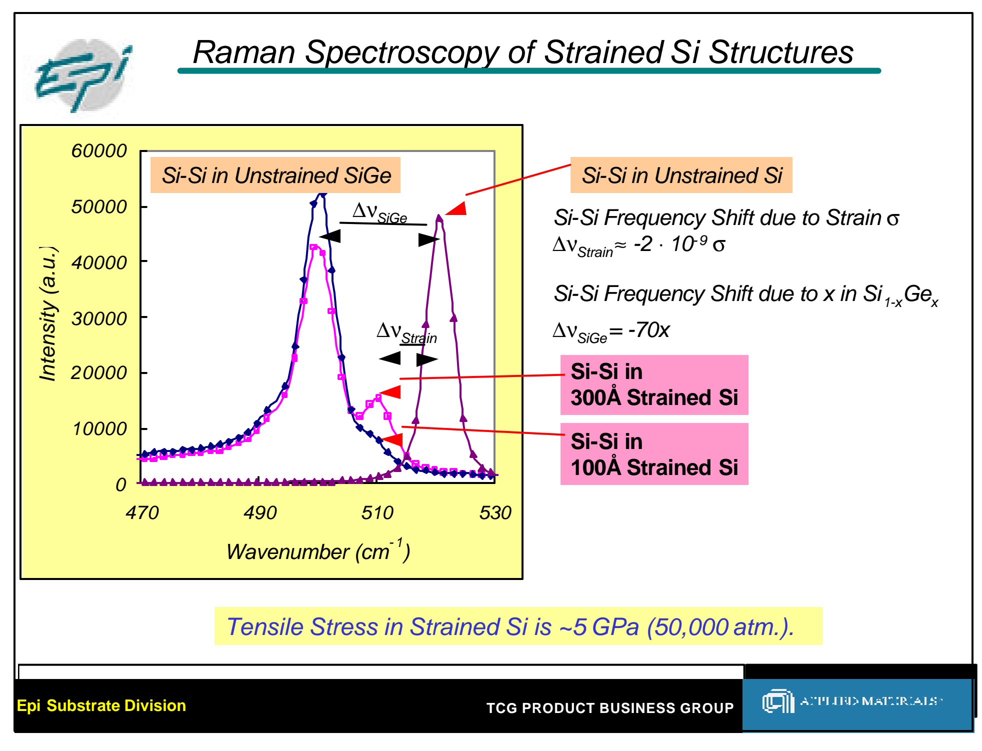

Raman Spectroscopy of Strained Si Structures
Si-Si in Unstrained SiGe
Si-Si in Unstrained Si
Si-Si Frequency Shift due to Strain σ
Δν Strain ≈ -2 · 10-9 σ
Si-Si Frequency Shift due to x in Si1-xGex
Δν SiGe = -70x
Si-Si in 300Å Strained Si
Si-Si in 100Å Strained Si
Intensity (a.u.)
Wavenumber (cm-1)
Tensile Stress in Strained Si is ~5 GPa (50,000 atm.).
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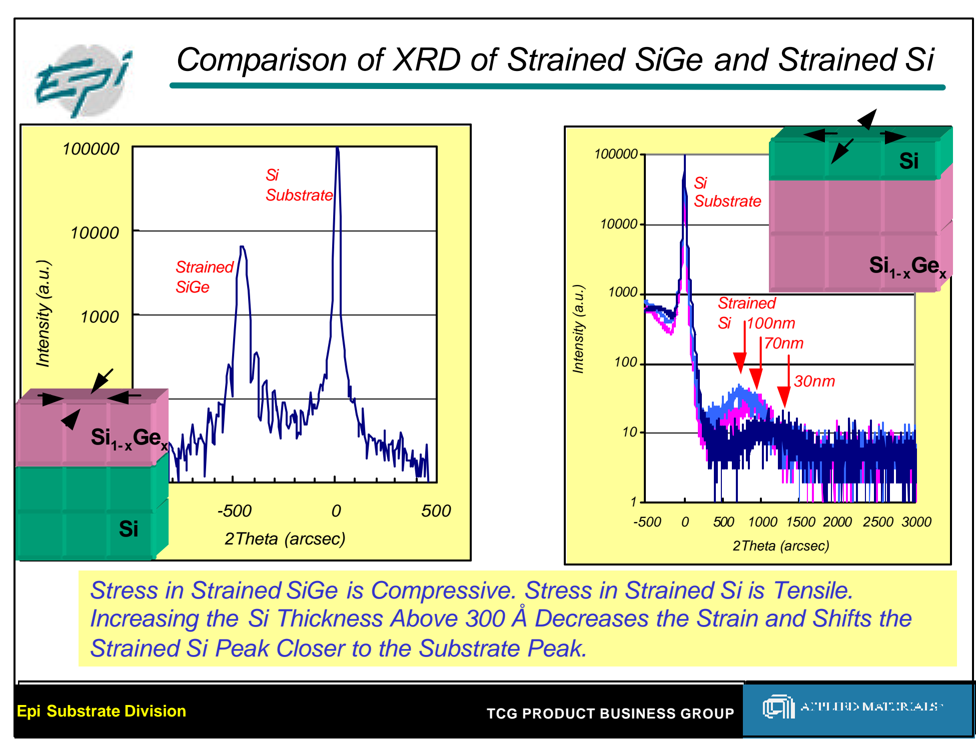

Comparison of XRD of Strained SiGe and Strained Si
100000
10000
1000
Intensity (a.u.)
Si Substrate
Strained SiGe
Si1-xGex
Si
-500
0
500
2Theta (arcsec)
100000
10000
1000
100
10
1
Intensity (a.u.)
Si Substrate
Strained Si
100nm
70nm
30nm
-500 0 500 1000 1500 2000 2500 3000
2Theta (arcsec)
Stress in Strained SiGe is Compressive. Stress in Strained Si is Tensile.
Increasing the Si Thickness Above 300 Å Decreases the Strain and Shifts the Strained Si Peak Closer to the Substrate Peak.
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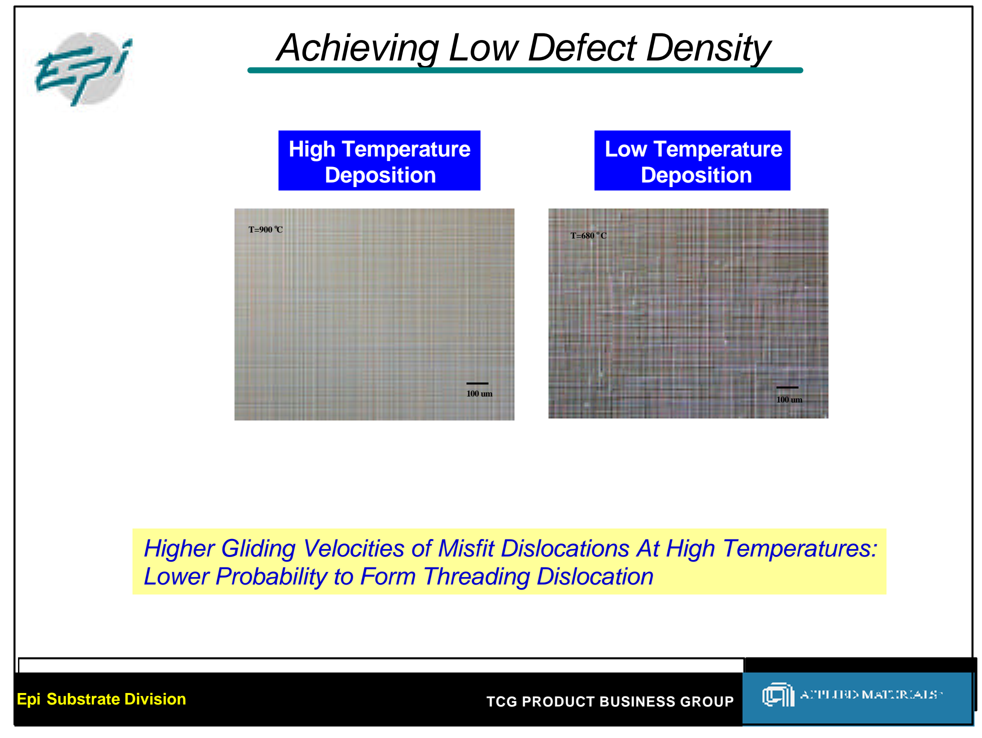

Achieving Low Defect Density
High Temperature Deposition
Low Temperature Deposition
Higher Gliding Velocities of Misfit Dislocations At High Temperatures:
Lower Probability to Form Threading Dislocation
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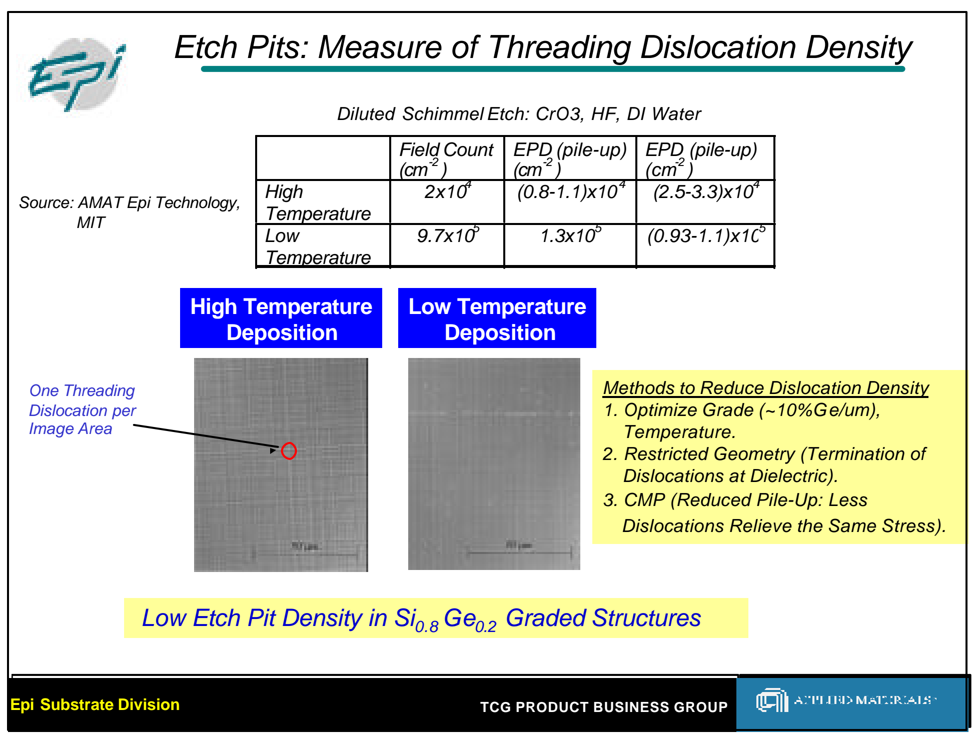
Etch Pits: Measure of Threading Dislocation Density
Diluted Schimmel Etch: CrO3, HF, DI Water
Source: AMAT Epi Technology, MIT

	Field Count (cm^{-2})	EPD (pile-up) (cm^{-2})	EPD (pile-up) (cm^{-2})
High Temperature	$2x10^4$	$(0.8-1.1)x10^4$	$(2.5-3.3)x10^4$
Low Temperature	$9.7x10^5$	$1.3x10^5$	$(0.93-1.1)x10^5$

High Temperature Deposition
Low Temperature Deposition
One Threading Dislocation per Image Area
Methods to Reduce Dislocation Density
1. Optimize Grade (~10%Ge/um), Temperature.
2. Restricted Geometry (Termination of Dislocations at Dielectric).
3. CMP (Reduced Pile-Up: Less Dislocations Relieve the Same Stress).
Low Etch Pit Density in $Si_{0.8}Ge_{0.2}$ Graded Structures
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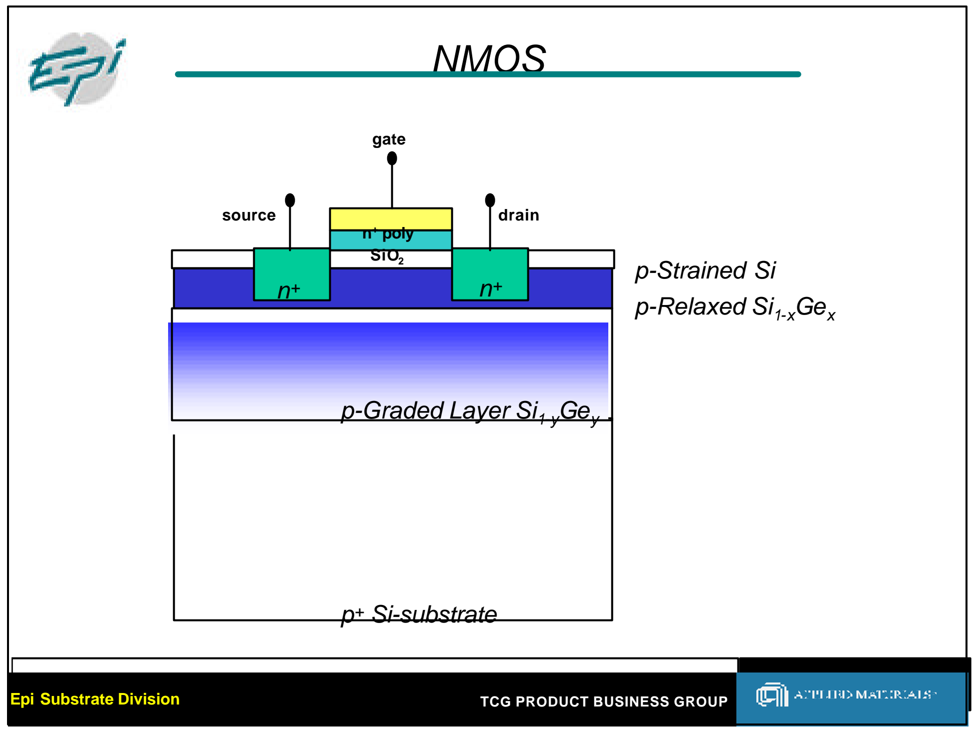
NMOS
gate
source
drain
n^+ poly
SiO_2
n+
n+
p-Strained Si
p-Relaxed $Si_{1-x}Ge_x$
p-Graded Layer $Si_{1-y}Ge_y$
p+ Si-substrate
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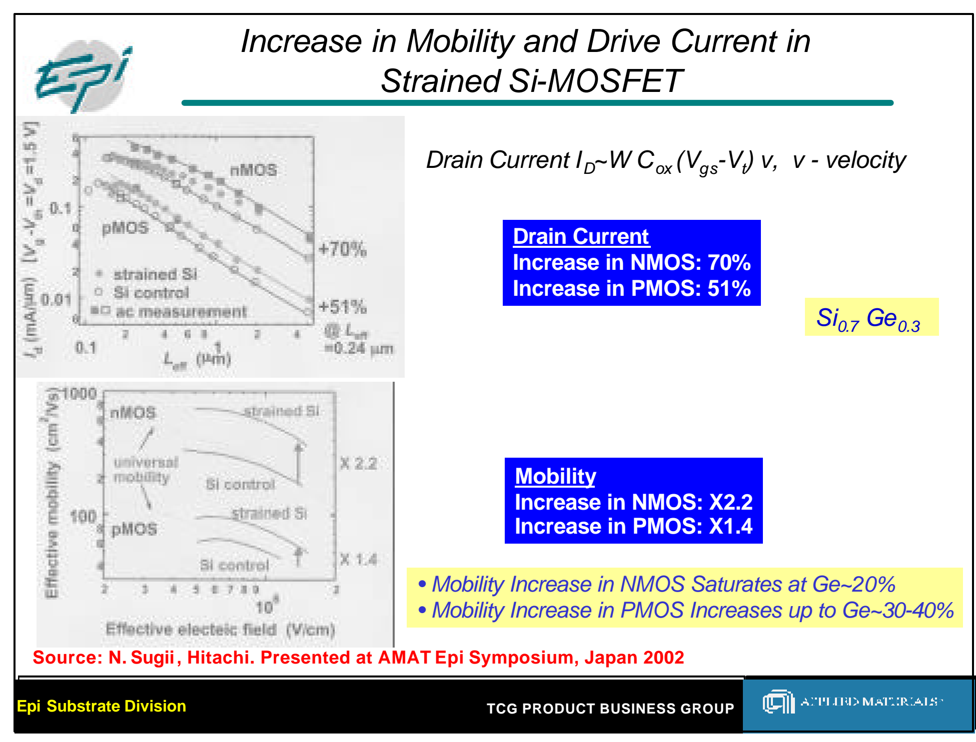

Increase in Mobility and Drive Current in Strained Si-MOSFET
Drain Current I_D~W C_{ox} (V_{gs}-V_t) v, v - velocity
Drain Current
Increase in NMOS: 70%
Increase in PMOS: 51%
$Si_{0.7}$ $Ge_{0.3}$
Mobility
Increase in NMOS: X2.2
Increase in PMOS: X1.4
• Mobility Increase in NMOS Saturates at Ge~20%
• Mobility Increase in PMOS Increases up to Ge~30-40%
nMOS
pMOS
strained Si
Si control
ac measurement
+70%
+51%
universal mobility
X 2.2
X 1.4
Effective electeic field (V/cm)
Effective mobility (cm²/Vs)
Source: N. Sugii, Hitachi. Presented at AMAT Epi Symposium, Japan 2002
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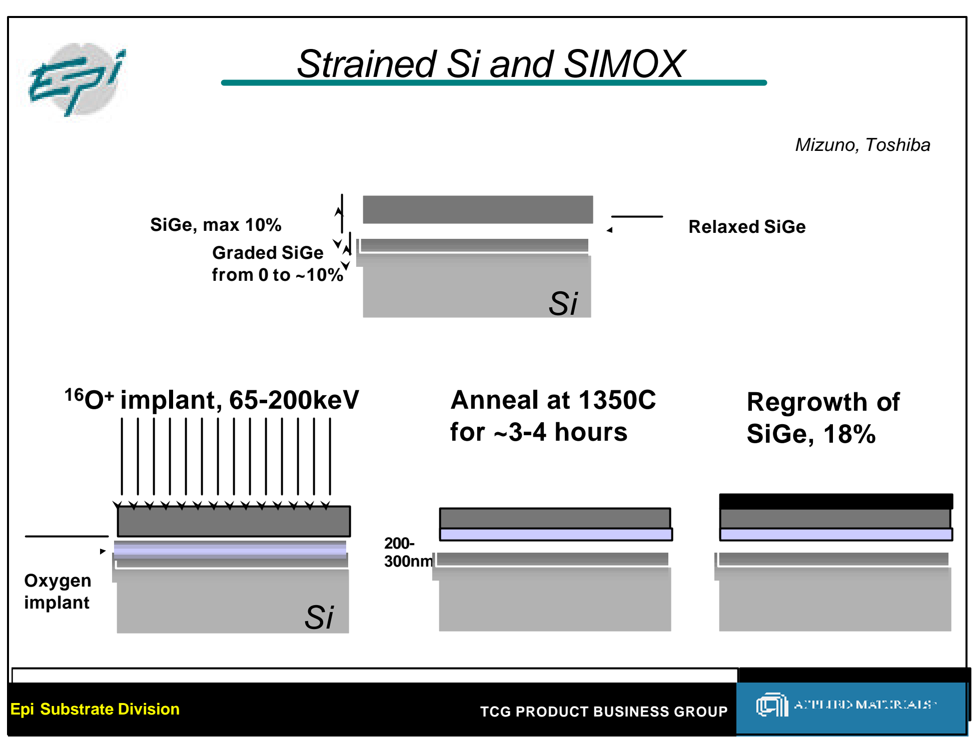

Strained Si and SIMOX
Mizuno, Toshiba
SiGe, max 10%
Graded SiGe from 0 to ~10%
Relaxed SiGe
Si
¹⁶O⁺ implant, 65-200keV
Anneal at 1350C for ~3-4 hours
Regrowth of SiGe, 18%
200-300nm
Oxygen implant
Si
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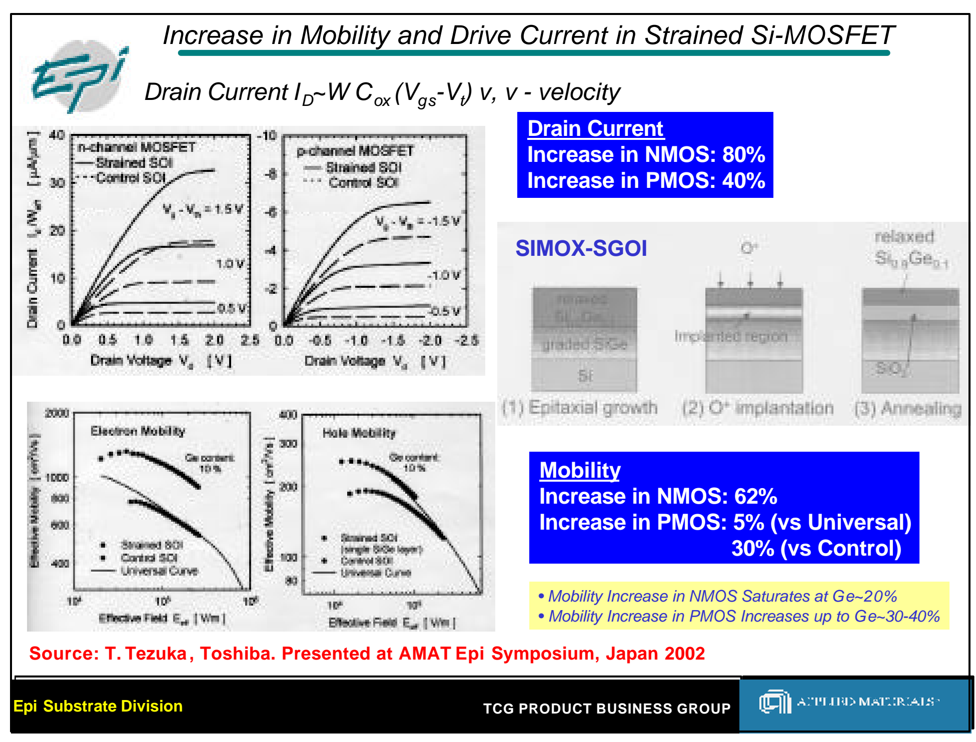

Increase in Mobility and Drive Current in Strained Si-MOSFET
Drain Current I_D~W C_{ox} (V_{gs}-V_t) v, v - velocity
Drain Current
Increase in NMOS: 80%
Increase in PMOS: 40%
SIMOX-SGOI
(1) Epitaxial growth
(2) O+ implantation
(3) Annealing
Mobility
Increase in NMOS: 62%
Increase in PMOS: 5% (vs Universal)
30% (vs Control)
• Mobility Increase in NMOS Saturates at Ge~20%
• Mobility Increase in PMOS Increases up to Ge~30-40%
Source: T. Tezuka, Toshiba. Presented at AMAT Epi Symposium, Japan 2002
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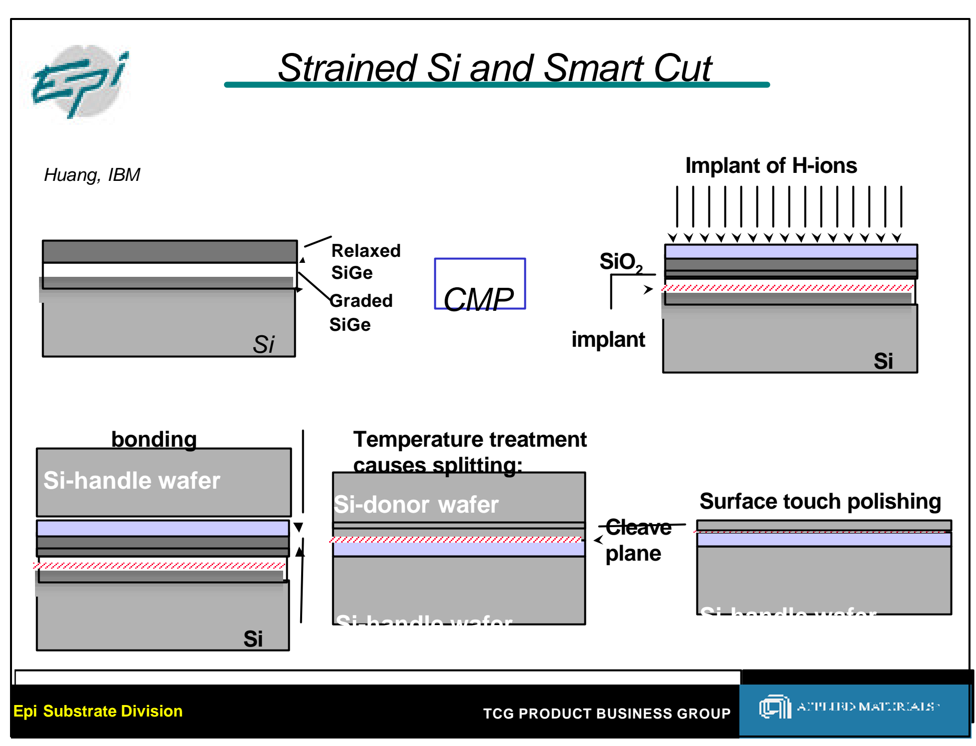

Strained Si and Smart Cut
Huang, IBM
Relaxed SiGe
Graded SiGe
Si
CMP
Implant of H-ions
SiO2
implant
Si
bonding
Si-handle wafer
Si
Temperature treatment causes splitting:
Si-donor wafer
Cleave plane
Surface touch polishing
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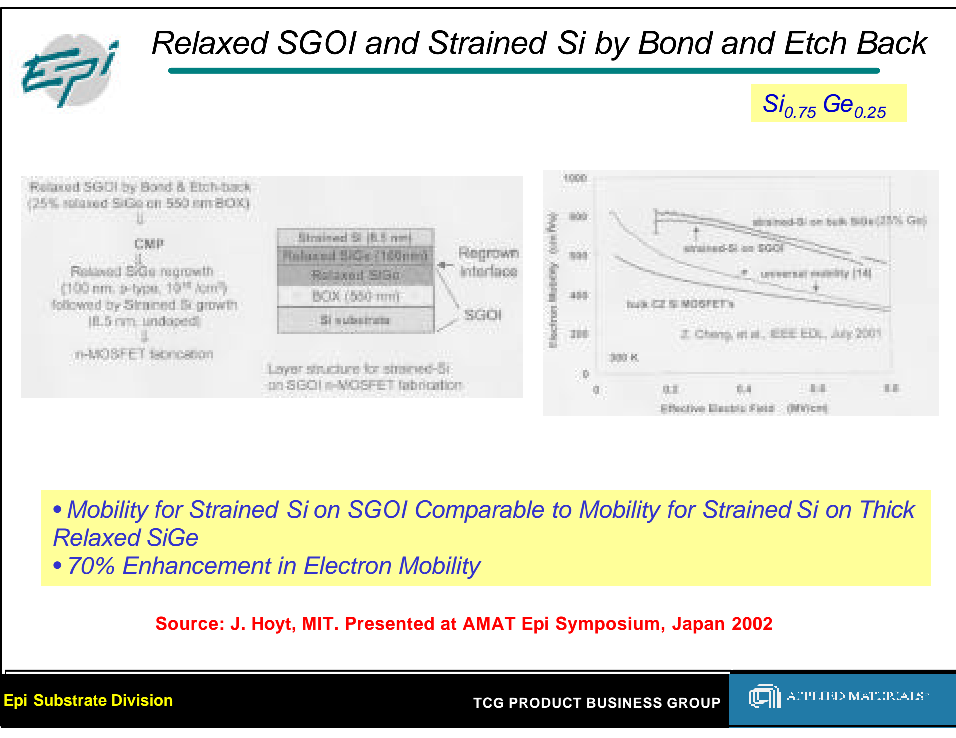
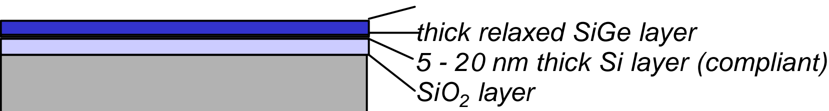


Compliant Substrate

- Very thin layer of Si (5-20 nm) on SiO_2. When growing SiGe layer on top of the thin Si, at a certain point the SiGe will relax, creating defects in the Si layer, which will comply to the relaxed SiGe.
- If this works, much thinner SiGe layers can be used, which results in higher throughput.



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Strained Si Technology

- Strained Si Process Has Been Demonstrated in Epi Centura
- Strain in Si and Relaxation of SiGe Has Been Verified by XRD, Raman, TEM
- Thermal Stability to Subsequent Processing:
  - Ge Diffusion: $2(Dt)^{1/2}$~6 nm for 1h at 900 C. Activation Energy 3.3 eV.
  - Strain Relaxation: Undetectable after 850 C 1h Anneal. RTA at Higher Temperatures Possible
- Key Issues:
  - Growth Rate is Key for Production-Worthiness
  - Defect Density is critical. The graded layer approach Leaves the Defects in the Bottom Layer. A Defect-Free Strained Layer Is Thus Achieved.

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Challenges of Strained Si on SiGe

1. Increased Junction Capacitance and Leakage (due to Higher Dielectric Constant and Lower Band Gap).
2. Reduced Thermal Conductivity (15x) of SiGe (Self-Heating).
3. Short Channel Effects.
4. Dislocations (>10^5/cm^2).
5. Integration of NMOS and PMOS.
6. Enhanced As, P Diffusion (Smaller L_{eff} for a Given L_{poly}).
7. Parasitic Hole Channel at Strained SiGe/Si Interface.

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Ways to Reduce Dislocation Density

1. Optimize Grade (~10%Ge/um), Temperature.
2. Restricted Geometry (Termination of Dislocations at Dielectric).
3. CMP (Reduced Pile-Up: Less Dislocations Relieve the Same Stress).

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