Properties and Applications of Strained Si/SiGe

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Outline of talk

• Bandgap Engineering
• Strained Si - Growth
• Film Characterization - Strain, Defect density
• Device Structure, challenges
• Strained Si on SOI
• Conclusions
Si, Ge, and C: Building Blocks of New Electronic Materials

Strained $\text{Si}_{1-y}C_y$ on Si

Strained $\text{Si}_{1-x}\text{Ge}_xC_y$ on Si

Strained $\text{Si}_{1-x}\text{Ge}_x$ on Si

Strained Si on Si$_{1-x}\text{Ge}_x$

Tension

No Strain when $x \sim 10y$

Compression

Band Gap Engineering

Strained $\text{Si}_{1-y}C_y$ on Si

$\Delta E_c \sim 5y$ [eV]

Strained $\text{Si}_{1-x}\text{Ge}_x$ on Si

$\Delta E_c \sim 0.6x$ [eV]

Strained Si on Si$_{1-x}\text{Ge}_x$

$\Delta E_c \sim 0.5x$ [eV]
Applications for Low Temperature SiGe and SiGeC Epitaxy

<table>
<thead>
<tr>
<th>Material</th>
<th>Application</th>
<th>Benefits</th>
<th>Status</th>
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</table>
| Si$_{1-x}$Ge$_x$, 0<x<0.3 | Base of npn HBT | • Enhanced gain due to barrier for holes drifting from SiGe base to Si emitter  
• Enhanced frequency due to drift electrical field | Volume production |
| Si$_{1-x}$Ge$_x$C$_y$, 0<x<0.3, y<0.002 | Base of npn HBT | • Reduction of boron diffusion by carbon                                | R&D / Pilot production |
| Si$_{1-x}$Ge$_x$, 0<x<0.3 | Elevated source/drain of MOSFET | • Reduced thinning of source/drain areas during silicidation  
(Ge can be used to increase growth rate) | R&D / Pilot production |
| Strained Si on Si$_{1-x}$Ge$_x$, 0.2<x<0.5 | Channel of MOSFET | • Enhanced speed due to increase in mobility                          | R&D            |
| SiC, 0<y<0.02 | Channel of MOSFET | • Enhanced speed due to increase in mobility                            | R&D            |
| Si$_{1-x}$Ge$_x$, 0<x<0.3 | Base of npn HBT | • Enhanced gain due to barrier for electrons drifting from SiC base to Si emitter  
• Enhanced frequency due to drift electrical field | R&D            |
| Si$_{1-x}$Ge$_x$, 0<x<0.3 | Waveguides | • Increased refractive index                                          | R&D            |
| Si$_{1-x}$Ge$_x$, 0<x<0.3 | Photodetectors | • Increased infrared light absorption                                 | R&D            |

Strained Si on Si-substrate

- Strained Si-Epi, ~10-20 nm
- SiGe, 30 %, ~0.5 microns
- Graded Buffer SiGe, ~5-30 %, ~2 microns
Why Strained Si?

Advantages:
Bulk electron and hole mobility is enhanced in Strained Si:
For p-MOSFET, hole mobility increases for Ge content up to 30-40%, while for n-MOSFET, the electron mobility saturates at about 20% of Ge.

Reported Improvements:
- Electron mobilities > 70 % on bulk Si NMOS is reported by IBM which translates into > 35% Id improvement (VLSI ’01)
- Electron mobilities of > 50 % and hole mobilities 15-20 % on SOI is reported by IBM (VLSI ’01)
- Electron mobilities of 1.7x on SOI is reported by Hoyt (IEEE El. Dev. Letr ‘01)
- Electron mobilities > 75 % on bulk Si is reported by Hoyt, Gibbons & Rim (IEEE Trans, ’00)

Key issues:
- Gate Oxidation
- Device Isolation
- Self Heating
- Growth rate - cost
- Defect density at surface
- Process integration difficulties

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Silicon Epitaxy Process Characterization

CEA/LETI - AMAT JDP
(Solid State Technology, July 2001)

- Ge Incorporation
- SiGe Growth Rate
- XRD of Si$_{1-x}$Ge$_x$

20 Torr
Silane: 650 C
DCS: 750 C
Monitoring the Process

Ge flow vs. time can be monitored with SECS
The Ge setpoint and actual flow can also be watched on screen

Non-linear GeH4 Flow Control

Non-linear Graded Ge Profile Control

Without Non-Linear Ramp Control

With Non-Linear Ramp Control
Control of Ge Grade for Strained Si Applications

Epi Centura Demonstrates Excellent Control of Constant Ge Concentration Deposition and Linear Ge Grade for Strained Si Applications.

Achieving High Growth Rates for Strained Silicon Structures

Growth Rates at 40%
Ge based on logarithmic fit to data

- 750 C 0.085 um/min
- 800 C 0.110 um/min
- 850 C 0.160 um/min
- 900 C 0.150 um/min

Using High Temperatures Ensures High Growth Rates.
**High Ge Incorporation**

Ge incorporation vs Ge flow and temperature

Ge Concentration as High as 50% is Easily Achievable

**Strained Si Structure**

Ge Concentration

Depth

2 μm

100 Å

Strain in Si and Relaxation of SiGe are Confirmed by Raman Spectroscopy
Raman Spectroscopy of SiGe

Raman Spectroscopy Can Provide Information on Molecular Vibrations of Lattice.

Raman Spectroscopy of Strained Si Structures

Tensile Stress in Strained Si is ~5 GPa (50,000 atm.).
Comparison of XRD of Strained SiGe and Strained Si

Stress in Strained SiGe is Compressive. Stress in Strained Si is Tensile. Increasing the Si Thickness Above 300 Å Decreases the Strain and Shifts the Strained Si Peak Closer to the Substrate Peak.

Achieving Low Defect Density

Higher Gliding Velocities of Misfit Dislocations At High Temperatures:
Lower Probability to Form Threading Dislocation
**Etch Pits: Measure of Threading Dislocation Density**

**Diluted Schimmel Etch: CrO₃, HF, DI Water**

<table>
<thead>
<tr>
<th></th>
<th>Field Count (cm⁻²)</th>
<th>EPD (pile-up) (cm⁻²)</th>
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</tr>
</thead>
<tbody>
<tr>
<td><strong>High Temperature</strong></td>
<td>2x10⁴</td>
<td>(0.8-1.1)x10⁴</td>
<td>(2.5-3.3)x10⁴</td>
</tr>
<tr>
<td><strong>Low Temperature</strong></td>
<td>9.7x10⁴</td>
<td>1.3x10⁵</td>
<td>(0.93-1.1)x10⁵</td>
</tr>
</tbody>
</table>

**Source:** AMAT Epi Technology, MIT

**High Temperature Deposition**
- One Threading Dislocation per Image Area

**Low Temperature Deposition**

Methods to Reduce Dislocation Density:
1. Optimize Grade (~10% Ge/um), Temperature.
2. Restricted Geometry (Termination of Dislocations at Dielectric).
3. CMP (Reduced Pile-Up: Less Dislocations Relieve the Same Stress).

**Low Etch Pit Density in Si₀.₈Ge₀.₂ Graded Structures**

**NMOS**

- *p-Strained Si*
- *p-Relaxed Siₓ₋₁₀ Geₓ*
- *p-Graded Layer Siₓ₋₀₅ Geₓ*
- *p⁺ Si-substrate*

**Source:** Epi Substrate Division, TCG PRODUCT BUSINESS GROUP
**Increase in Mobility and Drive Current in Strained Si-MOSFET**

Drain Current $I_D = W C_{ox} (V_{gs} - V_t) v$, $v$ - velocity

- **Drain Current**
  - Increase in NMOS: 70%
  - Increase in PMOS: 51%

- **Mobility**
  - Increase in NMOS: X2.2
  - Increase in PMOS: X1.4

- Mobility Increase in NMOS Saturates at Ge~20%
- Mobility Increase in PMOS Increases up to Ge~30-40%

**Source:** N. Sugii, Hitachi. Presented at AMAT Epi Symposium, Japan 2002

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**Strained Si and SIMOX**

Mizuno, Toshiba

- SiGe, max 10%
- Graded SiGe from 0 to ~10%
- Relaxed SiGe
- Si

- $^{16}$O$^+$ implant, 65-200keV
- Anneal at 1350C for ~3-4 hours
- Regrowth of SiGe, 18%

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Increase in Mobility and Drive Current in Strained Si-MOSFET

Drain Current $I_D = W C_{ox} (V_{gs} - V_T) v \cdot v$ - velocity

Drain Current

Increase in NMOS: 80%
Increase in PMOS: 40%

SIMOX-SGOI

Electron Mobility
Hole Mobility

Mobility
Increase in NMOS: 62%
Increase in PMOS: 5% (vs Universal)
30% (vs Control)

Source: T. Tezuka, Toshiba. Presented at AMAT Epi Symposium, Japan 2002

Strained Si and Smart Cut

Huang, IBM

Implant of H-ions

Relaxed SiGe
Graded SiGe

bonding

Temperature treatment
causes splitting:

Surface touch polishing

Subhandle wafer
Relaxed SGOI and Strained Si by Bond and Etch Back

- Mobility for Strained Si on SGOI Comparable to Mobility for Strained Si on Thick Relaxed SiGe
- 70% Enhancement in Electron Mobility

Source: J. Hoyt, MIT. Presented at AMAT Epi Symposium, Japan 2002

Compliant Substrate

- Very thin layer of Si (5-20 nm) on SiO₂. When growing SiGe layer on top of the thin Si, at a certain point the SiGe will relax, creating defects in the Si layer, which will comply to the relaxed SiGe.
- If this works, much thinner SiGe layers can be used, which results in higher throughput.
Strained Si Technology

- Strained Si Process Has Been Demonstrated in Epi Centura
- Strain in Si and Relaxation of SiGe Has BeenVerified by XRD, Raman, TEM
- Thermal Stability to Subsequent Processing:
  - Ge Diffusion: $2(Dt)^{1/2} \approx 6$ nm for 1h at 900°C. Activation Energy 3.3 eV.
  - Strain Relaxation: Undetectable after 850°C 1h Anneal.
  RTA at Higher Temperatures Possible
- Key Issues:
  - Growth Rate is Key for Production-Worthiness
  - Defect Density is critical. The graded layer approach Leaves the Defects
  in the Bottom Layer. A Defect-Free Strained Layer Is Thus Achieved.

Challenges of Strained Si on SiGe

1. Increased Junction Capacitance and Leakage (due to
   Higher Dielectric Constant and Lower Band Gap).
2. Reduced Thermal Conductivity (15x) of SiGe
   (Self-Heating).
3. Short Channel Effects.
4. Dislocations (>10¹⁵/cm²).
5. Integration of NMOS and PMOS.
6. Enhanced As, P Diffusion (Smaller $L_{\text{eff}}$ for a Given $L_{\text{pol}}$).
7. Parasitic Hole Channel at Strained SiGe/Si Interface.
Ways to Reduce Dislocation Density

1. Optimize Grade (~10%Ge/um), Temperature.
2. Restricted Geometry (Termination of Dislocations at Dielectric).
3. CMP (Reduced Pile-Up: Less Dislocations Relieve the Same Stress).

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