Silicon-Germanium:
from Microelectronics to Micromechanics

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Outline

• Introduction
  – IC technology advancement

• Microelectronics Applications for SiGe
  – Poly-SiGe gate
  – SiGe raised source/drain

• SiGe MEMS Technology
  – Properties of poly-SiGe
  – Modular integration with CMOS

• Summary
IC Technology Advancement

Rapid advances in IC technology have been achieved primarily by scaling down transistor lateral dimensions.

- Technology Scaling
- Investment
- Better Performance/Cost
- Market Growth

Bulk-Si MOSFET

- Leakage current is the primary barrier to scaling
- To suppress leakage, we need to employ:
  - Higher body doping → lower carrier mobility, higher junction capacitance, increased junction leakage
  - Thinner gate dielectric → higher gate leakage
  - Ultra-shallow S/D junctions → higher $R_{sd}$

Metal-Oxide-Semiconductor Field-Effect Transistor:

Desired characteristics:
- High ON current ($I_{dsat}$)
- Low OFF current
SIA Int’l Technology Roadmap for Semiconductors (2001)

<table>
<thead>
<tr>
<th>Year</th>
<th>2001</th>
<th>2002</th>
<th>2003</th>
<th>2004</th>
<th>2005</th>
<th>2006</th>
<th>2007</th>
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<tbody>
<tr>
<td>Technology Node</td>
<td>130 nm</td>
<td>115 nm</td>
<td>100 nm</td>
<td>90 nm</td>
<td>80 nm</td>
<td>70 nm</td>
<td>65 nm</td>
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<tr>
<td>$T_{ox}$</td>
<td>Solutions</td>
<td></td>
<td></td>
<td></td>
<td></td>
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<td></td>
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<tr>
<td>$I_{dsat}$</td>
<td>Being Pursued</td>
<td></td>
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</table>

- Advanced materials will be needed for bulk-Si MOSFETs to meet ITRS specifications

Why Silicon-Germanium?

- Compatible with Si
- Easily integrated into CMOS technology
- Properties can be tailored by adjusting Ge content
Properties of Si and Ge

<table>
<thead>
<tr>
<th></th>
<th>Si</th>
<th>Ge</th>
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<tbody>
<tr>
<td>Band gap</td>
<td>1.12 eV</td>
<td>0.67 eV</td>
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<tr>
<td>Lattice constant</td>
<td>5.431 Å</td>
<td>5.646 Å</td>
</tr>
<tr>
<td>Carrier mobilities</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1350 cm²/Vs</td>
<td>3900 cm²/Vs</td>
</tr>
<tr>
<td></td>
<td>480 cm²/Vs</td>
<td>1900 cm²/Vs</td>
</tr>
<tr>
<td>Melting point</td>
<td>1415°C</td>
<td>937°C</td>
</tr>
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</table>

- Si₁₋ₓGeₓ properties are advantageous for
  - Band-gap engineering (e.g. HBTs)
  - Strain-engineered MOSFETs
  - Low resistivity source/drain contacts
  - Low-T processing (e.g. integrated CMOS/MEMS)

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- **Summary**
Approaching 1.4 nm $T_{ox,eq}$

- **Use high-$\kappa$ gate dielectric** (by 2005?)
  - Thicker physical thickness for given $C_{gate}$ (F/cm$^2$)
  - $\Rightarrow$ lower gate leakage current
  - HfO$_2$ is a promising candidate
  - **Issues:**
    - Thermal stability
    - Interfacial SiO$_2$ layer $\Rightarrow$ increased $T_{ox,eq}$
      - may be needed for good mobilities

- **Reduce/eliminate gate depletion effect**
  - Poly-Si$_{1-x}$Ge$_x$ or metal (by 2007?)
  - **Issues:**
    - Process compatibility
    - Work function

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**Poly-SiGe Gate**

- **Advantages:**
  - Reduced gate depletion effect (GDE)
  - Less boron penetration through gate oxide
  - Process integration is straightforward
  - Work functions are appropriate
    - N+ poly-SiGe gate for NMOS
    - P+ poly-SiGe gate for PMOS

- **Optimal Ge content $\sim$20%**

- **Poly-SiGe on high-$\kappa$ gate dielectric?**
Poly-SiGe/HfO$_2$ MOSFET

- PVD HfO$_2$ at UT Austin
  - Prof. Jack Lee’s group
- Conventional CMOS process flow
  - 800°C, 30m furnace anneal
  - +1000°C, 10 sec RTA
- Poly-SiGe gate yields lower $T_{ox}$ (EOT)!
- Low gate leakage current maintained

![Graph showing gate capacitance vs. gate voltage](image)

Q. Lu et al., to be presented at 2002 VLSI Tech. Symp.

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Poly-SiGe/HfO$_2$ Gate Stack

- Interfacial layer eliminated!
- EOT reduction similar to that achieved with surface nitridation (SN)
  - SN -> degraded mobilities
- Promising for low EOT with low leakage, good mobilities (?)

![XTEM of gate stack](image)

Q. Lu et al., to be presented at 2002 VLSI Tech. Symp.
Achieving Low $R_{sd}$

- Increase source/drain dopant concentration
  **Issue:** Ultra-shallow junction formation

- Use elevated source/drain structure
  **Issue:** Process complexity

- Lower source/drain contact resistance
  **Issue:** New materials / process complexity

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SiGe Raised Source/Drain

- Raised S/D -> low sheet resistance
  - thicker S/D contact region

- SiGe -> low specific contact resistivity $\rho_c$
  - smaller bandgap -> smaller Schottky barrier
  - lower resistivity

  $\rho_c \sim 10^{-8} \ \Omega\cdot\text{cm}^2$ for germanosilicides on SiGe
  Prof. Ozturk’s group at NCSU
  => meets ITRS requirement!
Selective Deposition of Ge

- Conventional LPCVD tool
  - GeH$_4$ gas, 340°C, 300mT
- Ge deposits selectively onto Si

XTEM of selectively grown Ge

XTEM of UTB MOSFET w/ raised Ge S/D

SiGe Raised S/D Process

Gate patterning
6 nm CVD oxide
(etch stop for spacer formation)

Nitride spacer formation($L_{sw}$=25 nm)

Oxide removal in S/D regions by HF dip
Selective Ge LPCVD, 60 nm

20nm CVD oxide for capping layer
B⁺ implantation (6x10¹⁵/cm², 5keV)

Ge-B/Si intermixing(900°C, 7min)

“Single drain” structure w/ shallow S/D extensions

SiGe Raised S/D PMOSFET

- Good SCE
  - $N_{\text{sub}} = 10^{17} \text{ cm}^{-3}$
  - No halo doping

- Low $I_{\text{dsat}}$
  - S&D underlap gate; process not yet optimized

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Thin-Body SOI MOSFETs
(by 2007?)

**Ultra-Thin Body**

- Gate
- Source
- SOI
- Drain
- $T_{SOI}$
- $T_{Si}$
- $T_{BOX}$

**Double Gate**

- Gate
- Source
- SOI
- Drain
- $V_g$
- $T_{Si}$
- $T_{ox}$

Common feature: A thin body, such that no conduction path is far from the gate

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Double-Gate “FinFET”

- Self-aligned gates straddle thin silicon fin
- Current flows parallel to wafer surface

FinFET Structures

**Original:**

**Simplified:**
- “quasi-planar”
- simple CMOS layout
**FinFET with SiGe Raised S/D**

- Ge can be selectively deposited on top of Si fin(s)

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**Plan-view SEM of sub-50 nm \(L_{\text{gate}}\) multi-fin device after selective Ge**

**XTEM of Si fin with selectively deposited Ge**

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**\(I_{\text{dsat}}\) Improvement w/ Raised S/D**

\[L_{\text{gate}} = 90 \text{ nm}; W_{\text{fin}} = 70 \text{ nm}; W = 2 \times H_{\text{fin}} = 100 \text{ nm}\]

**Additional process steps:**
- Remove SiO\(_2\) over S/D
- Selectively grow 70 nm Ge
- Implant dopants
- 750°C activation anneal*
- 400°C FGA

\[\rightarrow 28\% \text{ improvement in } I_{\text{dsat}}\]

*Ge offers low thermal processing budget for S/D formation
- useful for advanced gate-stack materials

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Why MEMS?

• Enhance functionality/value of IC products using available microfabrication technology

Product examples:
  – low-power, wireless building blocks
    • MEMS antennas, microswitches, filters
  – cooler microprocessors
    • micropumps, valves, and channels for cooling
  – bio chips
    • microfluidics
MEMS Technology

Surface-micromachining steps

- Mechanical structures are fabricated using conventional IC fabrication techniques
- Microstructures are freed by selective removal of sacrificial layer(s)
- Si is structural material of choice
  - Excellent mechanical properties
  - Residual stress and strain gradient are issues
- High-temperature (>900°C) annealing necessary

MEMS Resonator

- Electrostatic force is applied by a comb drive to a suspended shuttle
- Motion is detected capacitively by a sense comb
Integrated Microsystems

- Modular, electronics-first approach is attractive
  - Separate development of micromechanics, microelectronics
  - Manufacture using IC and MEMS foundries
  - Minimization of chip area
- Presents technological challenges for poly-Si MEMS technology

→ Low-temperature micromachining process needed to simplify modular integration of CMOS and MEMS!

Deposition of SiGe Films

Arrhenius plot of deposition rate

- Conventional LPCVD tool
  - add GeH₄ as Ge source
- Dep. rate increases as Ge↑
- $T_{dep.}$ can be lowered as Ge↑
- $T_{transition}$ decreases as Ge↑

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Etching of SiGe Films

Films are compatible with:

- wet-cleaning processes (x<0.6, except “SC-1” bath)
- conventional dry-etch processes (F, Cl, HBr chemistries)

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Properties of Poly-SiGe
Residual Stress

- Undoped films deposited in polycrystalline form
- As-deposited Si\textsubscript{1-x}Ge\textsubscript{x} films have low stress!

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**Properties of Poly-SiGe**

**Stress Gradient**

Undoped as-deposited poly-Si_{0.8}Ge_{0.2} cantilevers
(up to 1 mm long, 1 µm thick)

- Tip deflection for 1 mm beam: 15 µm
  \[\Rightarrow \text{Linear strain gradient} = 3 \times 10^{-5} \, \mu\text{m}^{-1}\]
  (reference: N+ poly-Si (ADI) after anneal -> 2.67 \times 10^{-5} \, \mu\text{m}^{-1})

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**Properties of Poly-SiGe**

**Etch Selectivity**

<table>
<thead>
<tr>
<th>Etch Rates in µm/min</th>
<th>HF</th>
<th>RCA, SC1</th>
<th>H_2O_2</th>
<th>Cl_2/HBr Plasma</th>
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<tbody>
<tr>
<td>Poly-Ge</td>
<td>~0</td>
<td>3.0</td>
<td>0.4</td>
<td>0.41</td>
</tr>
<tr>
<td>Poly-Si_{0.2}Ge_{0.8}</td>
<td>~0</td>
<td>~0.75</td>
<td>~0.08</td>
<td>0.37</td>
</tr>
<tr>
<td>Poly-Si_{0.4}Ge_{0.6}</td>
<td>~0</td>
<td>0.06</td>
<td>~0</td>
<td>0.31</td>
</tr>
<tr>
<td>Poly-Si</td>
<td>~0</td>
<td>~0</td>
<td>~0</td>
<td>0.16</td>
</tr>
<tr>
<td>Annealed PSG</td>
<td>3.6</td>
<td>~0</td>
<td>~0</td>
<td>~0</td>
</tr>
</tbody>
</table>

- Ge-rich films etch rapidly in oxidizing solutions
  \[\Rightarrow \text{Poly-Ge can be a sacrificial material!}\]
Properties of Poly-SiGe
Germanium as a Sacrificial Material

Advantages:

– non-HF-based etchant
  • eliminates need for protective layer for electronics
  • does not damage Si
– high etch selectivity w.r.t. poly-Si, SiO₂, Si₃N₄

Si₀.₃₅Ge₀.₆₅-MEMS/CMOS Technology

Schematic cross-sectional view of modularly integrated devices

• Conventional CMOS process (Al metallization)
• Structural layer: ~65% Ge, 2.5 μm thick
  – deposited by LPCVD at 450°C (1μm/hr), in-situ B doped (6 Ω/□)
  – no post-dep. anneal (~10 MPa stress; ~10⁷μm strain gradient)
• Sacrificial layer: 100% Ge, 2 μm thick
  – deposited by LPCVD at 450°C (~1 μm/hr)
  – selectively removed using H₂O₂ (80°C) to release microstructures
Integrated SiGe-MEMS/CMOS

**Resonator next to Amplifier**
- conventional layout of integrated MEMS

**Resonator on top of Amplifier**
- smaller area → lower cost
- reduced interconnect parasitics → improved performance

A. E. Franke et al., Solid-State Sensor and Actuator Workshop Technical Digest, pp. 18-21, June 2000

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**Si$_{0.35}$Ge$_{0.65}$ Resonator Response**

Q = 70
Tested In Air

Q = 14,000 at 40 µTorr

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RF MEMS Technology

- Advantages of MEMS filters:
  - Small size
  - Low cost
  - High Q (?)
  - Low phase noise

RF Transceivers of the Future

- Single-Chip, Scaled CMOS or BiCMOS
- Minimum External Components

Wireless devices will be ubiquitous!
- E.g. sensor networks

Key goals:
- Minimum power dissipation
- Minimum cost
- Small form factor
Summary

• MOSFET performance can be improved to meet ITRS specifications by using SiGe for
  – gate electrode (thinner $T_{ox,eq}$)
  – SiGe raised S/D (lower $R_{sd}$)

• SiGe can make MEMS more accessible for the semiconductor industry
  – Modular integration of high-performance MEMS and electronics

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