Silicon-Germanium:
from Microelectronics to Micromechanics

Tsu-Jae King

Department of Electrical Engineering and Computer Sciences
University of California, Berkeley, CA 94720-1770 USA

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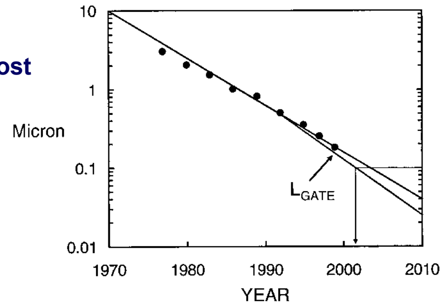
Outline

- **Introduction**
  - IC technology advancement
- **Microelectronics Applications for SiGe**
  - Poly-SiGe gate
  - SiGe raised source/drain
- **SiGe MEMS Technology**
  - Properties of poly-SiGe
  - Modular integration with CMOS
- **Summary**

IC Technology Advancement

Rapid advances in IC technology have been achieved primarily by scaling down transistor lateral dimensions



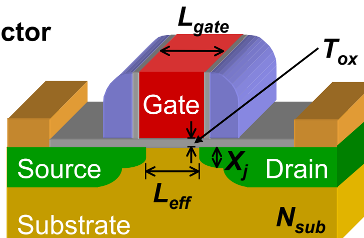
Source: Mark Bohr, Intel Corporation

Bulk-Si MOSFET

- Leakage current is the primary barrier to scaling
- To suppress leakage, we need to employ:
  - Higher body doping → lower carrier mobility, higher junction capacitance, increased junction leakage
  - Thinner gate dielectric → higher gate leakage
  - Ultra-shallow S/D junctions → higher R_{sd}

Metal-Oxide-Semiconductor Field-Effect Transistor:

Desired characteristics:
- High ON current (I_{dsat})
- Low OFF current



SIA Int'l Technology Roadmap for Semiconductors (2001)

Year	2001	2002	2003	2004	2005	2006	2007
Technology Node	130 nm	115 nm	100 nm	90 nm	80 nm	70 nm	65 nm
T_{ox}			Solutions		No Known		
I_{dsat}			Being Pursued		Solutions		

- Advanced materials will be needed for bulk-Si MOSFETs to meet ITRS specifications

Why Silicon-Germanium?

- Compatible with Si

III	IV	V
B	C	N
Al	Si	P
Ga	Ge	As

- Easily integrated into CMOS technology
- Properties can be tailored by adjusting Ge content

Properties of Si and Ge

	Si	Ge
Band gap	1.12 eV	0.67 eV
Lattice constant	5.431 Å	5.646 Å
Carrier mobilities	1350 cm^2/Vs 480 cm^2/Vs	3900 cm^2/Vs 1900 cm^2/Vs
Melting point	1415°C	937°C

- **$Si_{1-x}Ge_x$ properties are advantageous for**
  - Band-gap engineering (*e.g.* HBTs)
  - Strain-engineered MOSFETs
  - Low resistivity source/drain contacts
  - Low-T processing (*e.g.* integrated CMOS/MEMS)

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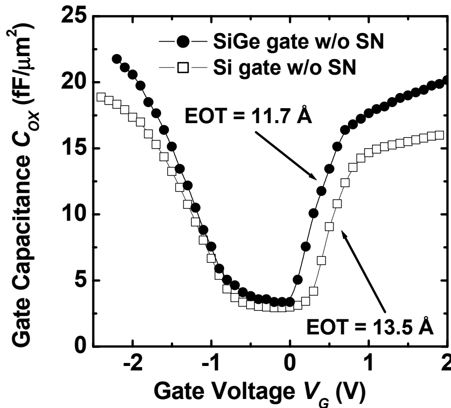
Approaching 1.4 nm $T_{ox,eq}$

- **Use high-κ gate dielectric** (by 2005?)
  Thicker physical thickness for given C_{gate} (F/cm^2)
  -> lower gate leakage current
  HfO_2 is a promising candidate
  Issues: • Thermal stability
  • Interfacial SiO_2 layer -> increased $T_{ox,eq}$
  - may be needed for good mobilities
- **Reduce/eliminate gate depletion effect**
  Poly-$Si_{1-x}Ge_x$ or metal (by 2007?)
  Issues: • Process compatibility
  • Work function

Poly-SiGe Gate

- **Advantages:**
  - Reduced gate depletion effect (GDE)
  - Less boron penetration through gate oxide
  - Process integration is straightforward
  - Work functions are appropriate
    - N+ poly-SiGe gate for NMOS
    - P+ poly-SiGe gate for PMOS
- **Optimal Ge content ~20%**
  (W.-C. Lee *et al.*, *IEEE Electron Device Letters*, Vol. 19, p. 247, 1998)
- **Poly-SiGe on high-κ gate dielectric?**

Poly-SiGe/HfO_2 MOSFET

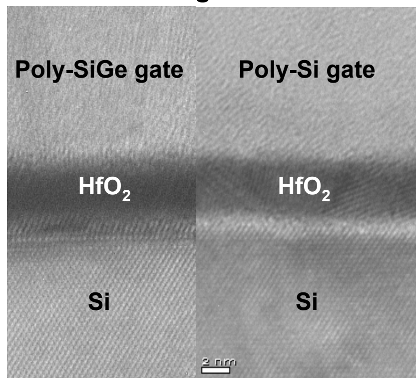


- PVD HfO_2 at UT Austin
  Prof. Jack Lee's group
- Conventional CMOS process flow
  - 800°C, 30m furnace anneal + 1000°C, 10 sec RTA
- **Poly-SiGe gate yields lower T_{ox} (EOT)!**
- **Low gate leakage current maintained**

Q. Lu *et al.*, to be presented at *2002 VLSI Tech. Symp.*

Poly-SiGe/HfO_2 Gate Stack

XTEM of gate stack



- Interfacial layer eliminated!
- EOT reduction similar to that achieved with surface nitridation (SN)
  - SN -> degraded mobilities
- Promising for low EOT with low leakage, good mobilities (?)

Q. Lu *et al.*, to be presented at *2002 VLSI Tech. Symp.*

Achieving Low R_{sd}

- **Increase source/drain dopant concentration**
  Issue: • Ultra-shallow junction formation
- **Use elevated source/drain structure**
  Issue: • Process complexity
- **Lower source/drain contact resistance**
  Issue: • New materials / process complexity

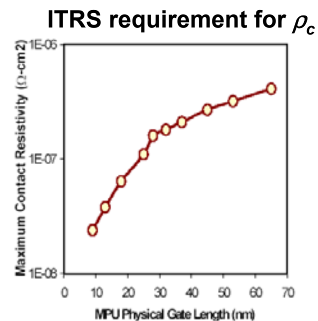
SiGe Raised Source/Drain

- **Raised S/D -> low sheet resistance**
  - thicker S/D contact region
- **SiGe -> low specific contact resistivity ρ_c**
  - smaller bandgap -> smaller Schottky barrier
  - lower resistivity

ρ_c ~10^{-8} Ω-cm^2 for germanosilicides on SiGe
Prof. Ozturk's group at NCSU

=> meets ITRS requirement!

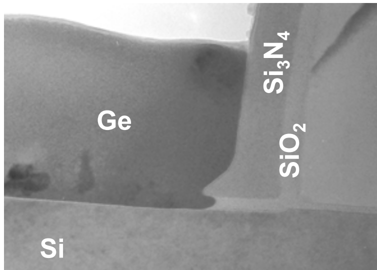
ITRS requirement for ρ_c



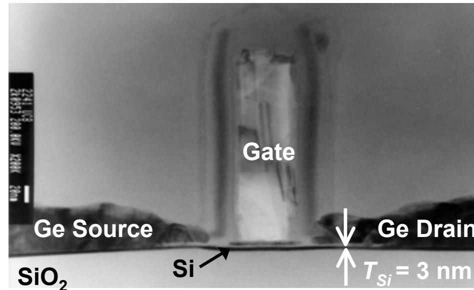
Selective Deposition of Ge

- **Conventional LPCVD tool**
  - GeH_4 gas, 340°C, 300mT
- **Ge deposits selectively onto Si**

XTEM of selectively grown Ge

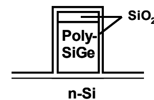


XTEM of UTB MOSFET w/ raised Ge S/D

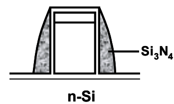


Y.-K. Choi *et al.*, *IEEE Electron Device Lett.*, Vol. 22, p. 447, 2001

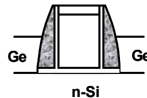
SiGe Raised S/D Process



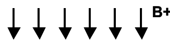
Gate patterning
6 nm CVD oxide
(etch stop for spacer formation)

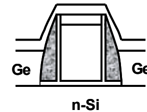


Nitride spacer formation(L_{sw}=25 nm)



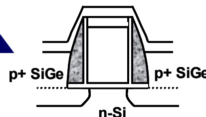
Oxide removal in S/D regions by HF dip
Selective Ge LPCVD, 60 nm





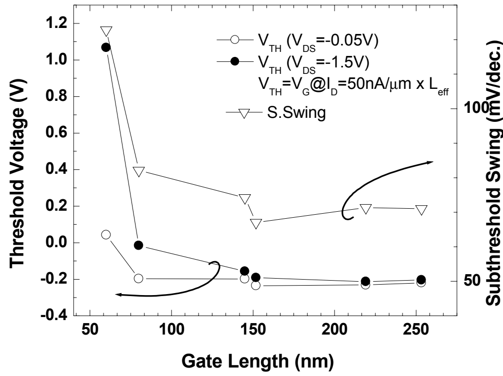
20nm CVD oxide for capping layer
B^+ implantation ($6x10^{15}cm^{-3}$, 5keV)

"Single drain" structure w/ shallow S/D extensions



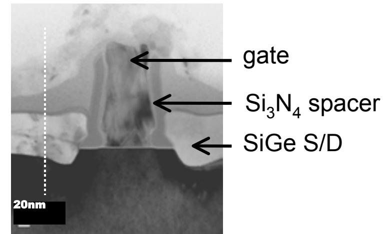
Ge-B/Si intermixing(900°C, 7min)

SiGe Raised S/D PMOSFET



P. Ranade *et al., IEEE Electron Device Lett.*, April 2002

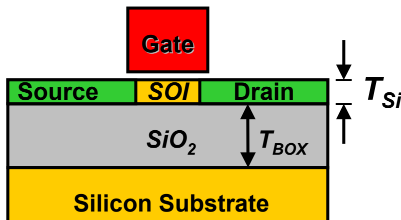
- ✓ **Good SCE**
  $N_{sub}=10^{17}$ cm³;
  no halo doping
- × **Low I_{dsat}**
  S&D underlap gate;
  process not yet optimized



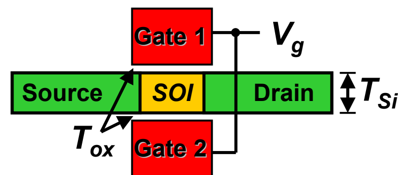
Thin-Body SOI MOSFETs

(by 2007?)

Ultra-Thin Body



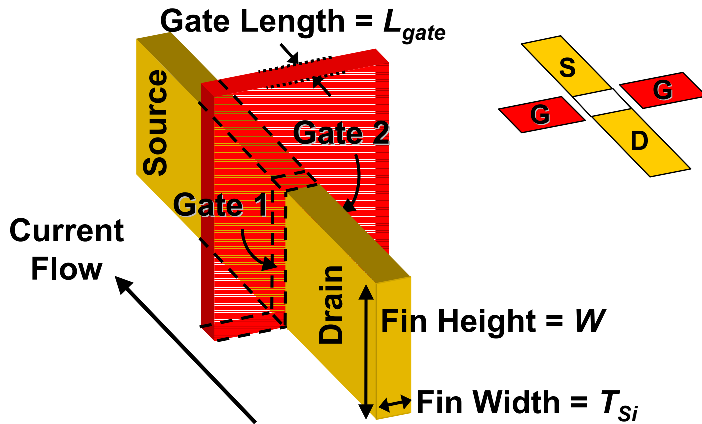
Double Gate



Common feature: A thin body, such that no conduction path is far from the gate

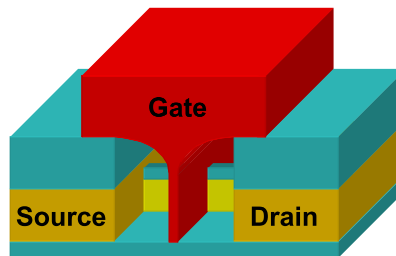
Double-Gate “FinFET”

- Self-aligned gates straddle thin silicon fin
- Current flows parallel to wafer surface

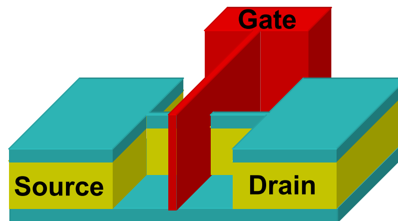


FinFET Structures

Original:



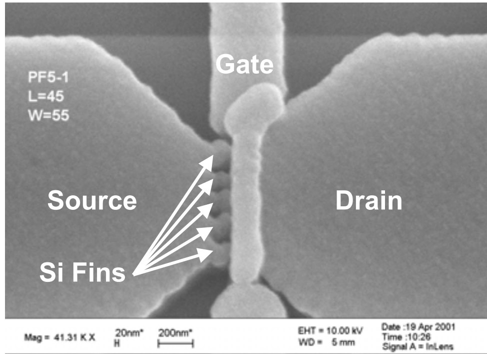
Simplified:
- “quasi-planar”
- simple CMOS layout



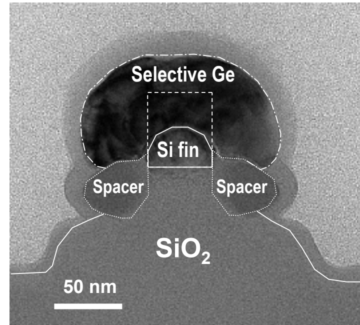
FinFET with SiGe Raised S/D

- Ge can be selectively deposited on top of Si fin(s)

Plan-view SEM of sub-50 nm L_{gate} multi-fin device after selective Ge



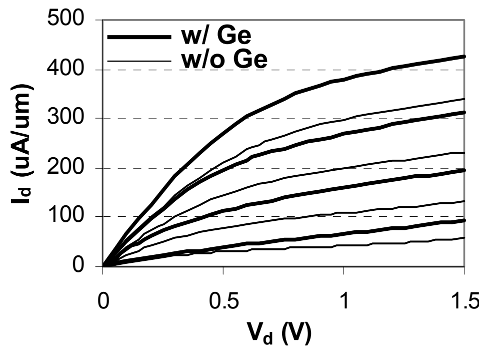
XTEM of Si fin with selectively deposited Ge



N. Lindert *et al., 2001 IEEE Int'l. SOI Conference*

I_{dsat} Improvement w/ Raised S/D

L_{gate} = 90 nm; W_{fin} = 70 nm; $W = 2 \times H_{fin}$ = 100 nm



Additional process steps:

- Remove SiO_2 over S/D
- Selectively grow 70 nm Ge
- Implant dopants
- **750°C activation anneal***
- 400°C FGA

→ **28% improvement in I_{dsat}**

N. Lindert *et al., 2001 IEEE Int'l. SOI Conference*

***Ge offers low thermal processing budget for S/D formation**

- useful for advanced gate-stack materials

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Why MEMS?

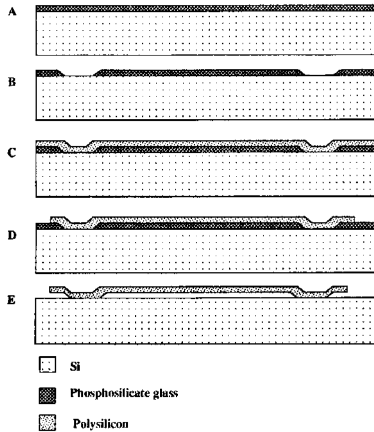
- **Enhance functionality/value of IC products using available microfabrication technology**

  Product examples:

  - **low-power, wireless building blocks**
    - MEMS antennas, microswitches, filters
  - **cooler microprocessors**
    - micropumps, valves, and channels for cooling
  - **bio chips**
    - microfluidics

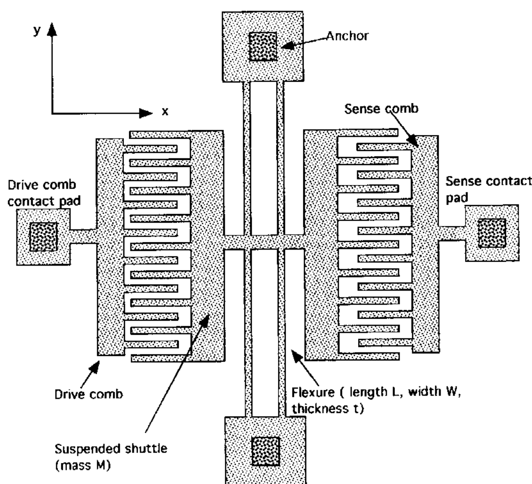
MEMS Technology

Surface-micromachining steps



- Mechanical structures are fabricated using conventional IC fabrication techniques
- Microstructures are freed by selective removal of sacrificial layer(s)
- Si is structural material of choice
  - ✓ **Excellent mechanical properties**
  - × **Residual stress and strain gradient are issues**
  - **High-temperature (>900°C) annealing necessary**

MEMS Resonator



- Electrostatic force is applied by a comb drive to a suspended shuttle
- Motion is detected capacitively by a sense comb

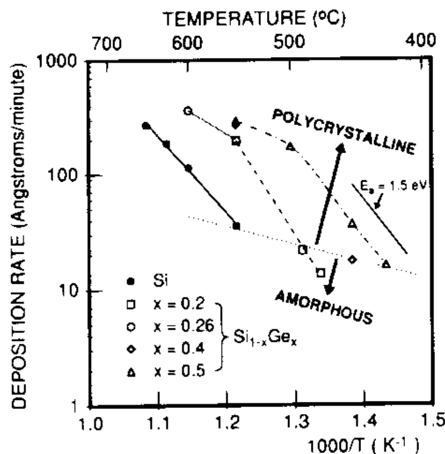
Integrated Microsystems

- **Modular, electronics-first approach is attractive**
  - ✓ Separate development of micromechanics, microelectronics
  - ✓ Manufacture using IC and MEMS foundries
  - ✓ Minimization of chip area
  - × Presents technological challenges for poly-Si MEMS technology

→ **Low-temperature micromachining process needed to simplify modular integration of CMOS and MEMS!**

Deposition of SiGe Films

Arrhenius plot of deposition rate

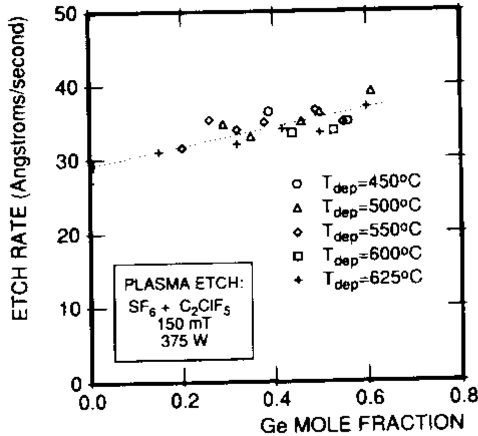


- **Conventional LPCVD tool**
  - **add GeH_4 as Ge source**
- **Dep. rate increases as Ge ↑**
- **$T_{dep.}$ can be lowered as Ge ↑**
- **$T_{transition}$ decreases as Ge ↑**

T.-J. King *et al., J. Electrochem. Soc.* 141, p. 2237, 1994

Etching of SiGe Films

Etch rate *vs.* Ge content



Films are compatible with:

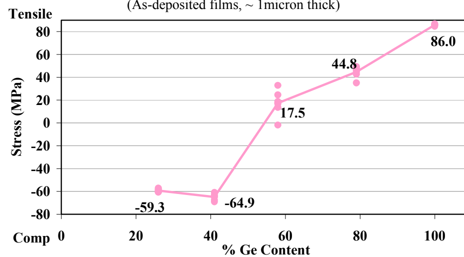
- **wet-cleaning processes** (x<0.6, except "SC-1" bath)
- **conventional dry-etch processes** (F, Cl, HBr chemistries)

T.-J. King *et al.*, *J. Electrochem. Soc.* 141, p. 2237, 1994

Properties of Poly-SiGe

Residual Stress

Ge Content (%)	100	79	58	41	26
Dep. Temp. (C)	375	425	475	500	550
Pressure (mtorr)	100	100	100	100	100
SiH4 (sccm)	0	17	46	100	200
GeH4 (sccm)	20	20	20	18	19
Dep. Time (min.)	155	120	80	80	50
Film Thickness (nm)	940	760	765	710	871



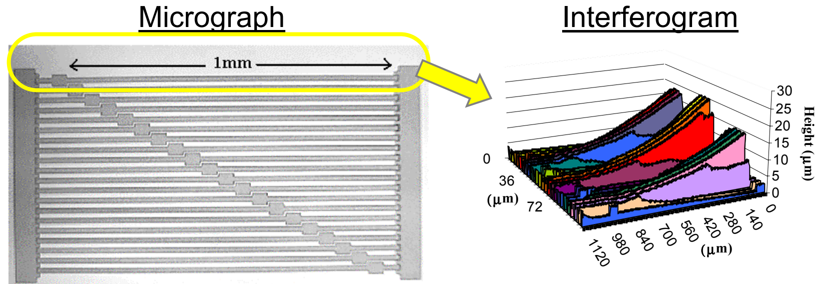
- Undoped films deposited in polycrystalline form
- **As-deposited $Si_{1-x}Ge_x$ films have low stress!**

Properties of Poly-SiGe

Stress Gradient

Undoped as-deposited poly-$Si_{0.8}Ge_{0.2}$ cantilevers
(up to 1 mm long, 1 μm thick)

Micrograph / Interferogram



- Tip deflection for 1 mm beam: 15 μm
  ⇒ Linear strain gradient = **3×10^{-5} μm^{-1}**
  (reference: N+ poly-Si (ADI) after anneal -> 2.67×10^{-5} μm^{-1})

Properties of Poly-SiGe

Etch Selectivity

Etch Rates in μm/min

	HF	RCA, SC1	H_2O_2*	Cl_2/HBr Plasma
Poly-Ge	~0	3.0	0.4	0.41
Poly-$Si_{0.2}Ge_{0.8}$	~0	0.75	0.08	0.37
Poly-$Si_{0.4}Ge_{0.6}$	~0	0.06	~0	0.31
Poly-Si	~0	~0	~0	0.16
Annealed PSG	3.6	~0	~0	~0

- Ge-rich films etch rapidly in oxidizing solutions
  ⇒ **Poly-Ge can be a sacrificial material!**

Properties of Poly-SiGe

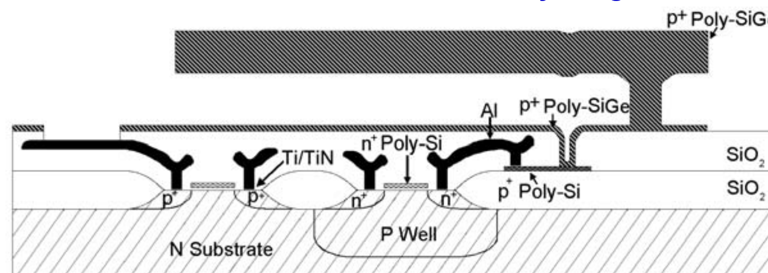
Germanium as a Sacrificial Material

Advantages:

- non-HF-based etchant
  - eliminates need for protective layer for electronics
  - does not damage Si
- high etch selectivity w.r.t. poly-Si, SiO_2, Si_3N_4

$Si_{0.35}Ge_{0.65}$-MEMS/CMOS Technology

Schematic cross-sectional view of modularly integrated devices

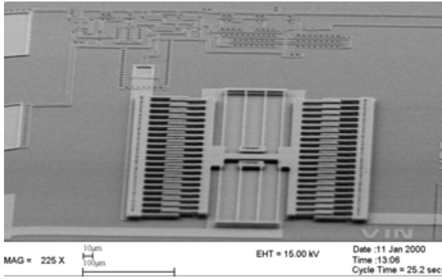


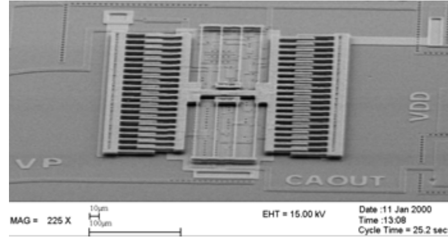
- **Conventional CMOS process (Al metallization)**
- **Structural layer: ~65% Ge**, 2.5 µm thick
  - deposited by LPCVD at 450ºC (1µm/hr), in-situ B doped (6 Ω/☐)
  - **no post-dep. anneal (-10 MPa stress; ~10^{-4}/µm strain gradient)**
- **Sacrificial layer: 100% Ge**, 2 µm thick
  - deposited by LPCVD at 450ºC (~1 µm/hr)
  - selectively removed using H_2O_2 (80ºC) to release microstructures

Integrated SiGe-MEMS/CMOS

Resonator next to Amplifier
- conventional layout of integrated MEMS

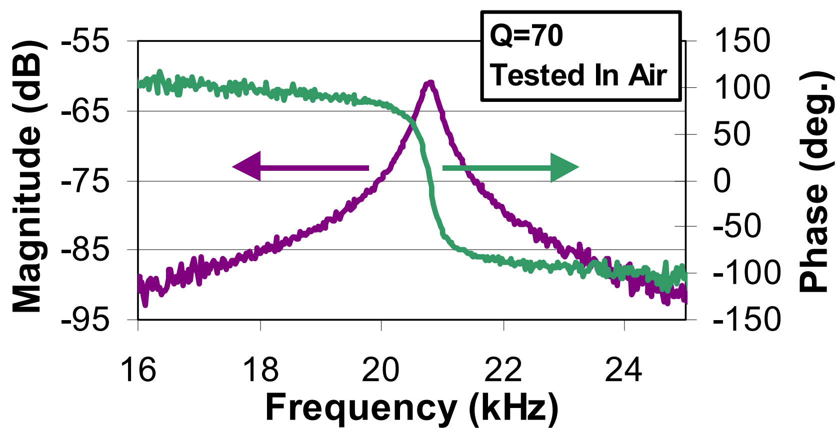
Resonator on top of Amplifier
- smaller area --> lower cost
- reduced interconnect parasitics --> improved performance





A. E. Franke *et al.*, *Solid-State Sensor and Actuator Workshop Technical Digest*, pp. 18-21, June 2000

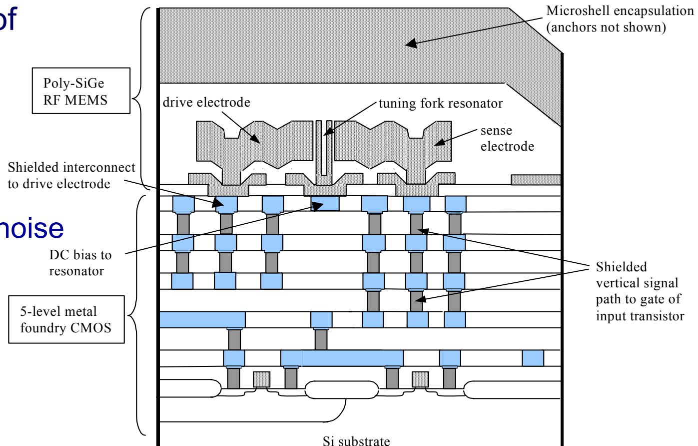
$Si_{0.35}Ge_{0.65}$ Resonator Response



Q = 14,000 at 40 μTorr

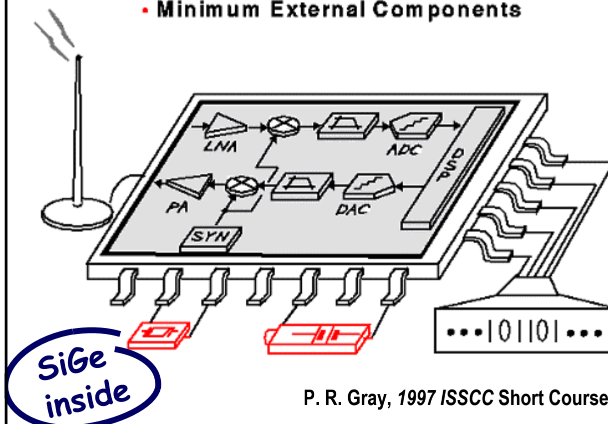
RF MEMS Technology

- Advantages of MEMS filters:
  - Small size
  - Low cost
  - high Q (?)
  - low phase noise



RF Transceivers of the Future

- Single-Chip, Scaled CMOS or BiCMOS
- Minimum External Components



P. R. Gray, *1997 ISSCC* Short Course

Wireless devices will be ubiquitous!

- *e.g.* sensor networks

Key goals:

- minimum power dissipation
- minimum cost
- small form factor

T.-J. King, UC Berkeley April 17, 2002

Summary

- **MOSFET performance can be improved to meet ITRS specifications by using SiGe for**
  - gate electrode (thinner $T_{ox,eq}$)
  - SiGe raised S/D (lower R_{sd})
- **SiGe can make MEMS more accessible for the semiconductor industry**
  - Modular integration of high-performance MEMS and electronics

Acknowledgements

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  - Professors: Jeffrey Bokor, Roger Howe, Chenming Hu*
  - Students: Leland Chang, Andrea Franke[2], Daewon Ha, John Heck[1], Nick Lindert[1], Qiang Lu, Pushkar Ranade, Yee-Chia Yeo
  - Dr. Yang-Kyu Choi, Hideki Takeuchi, Dr. Erik Anderson^

  ***on leave at TSMC [1]now with Intel [2]now with Motorola ^LBNL**
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  - SRC Advanced Devices and Technology Program
  - MARCO Focus Center for Advanced Materials, Structures and Devices
  - DARPA MEMS & IMT Programs