Massively Parallel Direct Write E-Beam System

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Integrated Electron-Beam Source Cartridge

- Maskless, Direct-Write E-Beam Tool
- Thousands of micro-beams
- Field Emission Array combined with Microchannel Amplifier Array for stable, low-current operation and long-term reliability
- Integrated Micro-Column electrostatic lens array
- Patterning to 70 nm and below
- Short excursion (< 500 µm) stage travel for large area patterning
- Compact 25 mm high assembly
- Scalable to any wafer diameter
- High throughput potential
Microchannel Amplifier Operation

Input Electron → Single Channel → Emissive Layer → Output Electrons

Secondary Electrons

Contact Electrode
MCA Schematic

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Issues

• Angular Distribution (ADOE)
• Energy Distribution (EDOE)
• Thermal Dissipation
• Modeling/Design

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MCA Transfer Characteristic

- Operating Point
- Saturated Regime ($g \sim 10^{-2}-10^{-4}$)
- Linear Regime ($g \sim 10^3$)

Input Current

Output (MCA) Current
Si MCA Gain Comparison with Glass MCP
Effective L/D = 10:1

Bias Voltage

Si MCA (measured)

Lead glass MCP (typical)

e- input: 300 eV

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3-Electrode EINZEL (unfocused input beam from MCA)

Large Spacer

Large Spacer

Beam limiting aperture electrode

3-Electrode EINZEL (focused output beam to substrate)
Einzel#4 Alignment: EBLA#2, 1, 3 & CLA#2

Last Update: 4/2/2000

Wafer Order
"EBLA#2": bottom (1)
"EBLA#1": middle (2)
"EBLA#3": middle (3)
"CLA#2": top (4)

Wafer Offsets (µm)
"EBLA#2":  x = 0.0  y = 0.0  θ = 0µradians
"EBLA#1":  Δx = 0.2  Δy = -0.4  Δθ = 16 µradians
"EBLA#3":  Δx = -0.4  Δy = 0.1  Δθ = 6 µradians
"CLA#2":  Δx = 0.1  Δy = 0.4  Δθ = 11 µradians
Fully connected Source Cartridge

Electrostatic Wafer Chuck
Proof of Principle Completed

• Designed and built new generation Si MCA
  – All CMOS-type processing.
  – Gain, noise, brightness.

• Designed and built EBLA
  – Manufacturability

• Integrated components into Source Cartridge

• Patterned features at < 100 nm
Proof of Lithography (PoL)

Issues

• Optimize MCA design
• Incorporate deflection in EBLA
• Demonstrate wafer throughput > 100 wph for 300 mm wafers
• Develop writing strategy (Key: redundancy)
Wafer Throughput

Incorporating Deflection (PoL)

Orthogonal displacement = ± 2.5 µm (± 50 pixels)

Table speed = 2 mm/s, a = 1g

Wafer throughput > 140 wph

Deflection frequency = 40 kHz

(Preliminary EBLA design complete)
Writing Strategy

• K6-2 poly Si gate-level file is 800 MB corresponding to total *information* rate of 800 MB/25 s = 32 MB/s. Redundancy is key.

• To write single line across 300 mm wafer (6 Mp) requires only 600 bits.

• Writing strategy should look to *global change of state* with each clock cycle rather than change in every pixel.
Conclusions

• Massively parallel system appears feasible
• Multi-generation technology
• Attractive cost of ownership
  – Low initial cost
  – Relatively small footprint
  – Simple maintenance
• Virtual Mask - new paradigm for Semicon industry