



Fabrication and Characterization of Sub-100 nm Carbon Nanotube Vias

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Outline



- Introduction
- CNT Via Test Structure
- Electrical Characterization
- Results and Discussion
- Summary

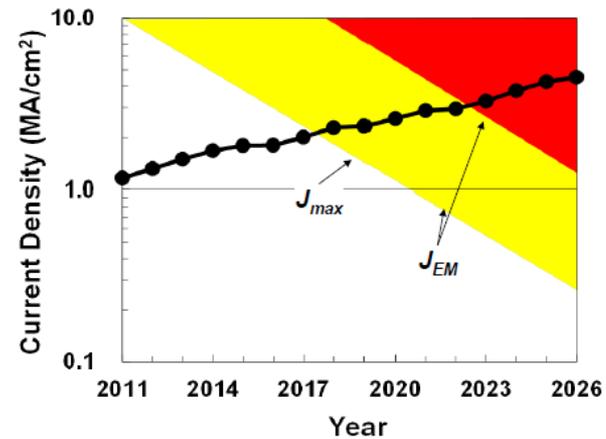
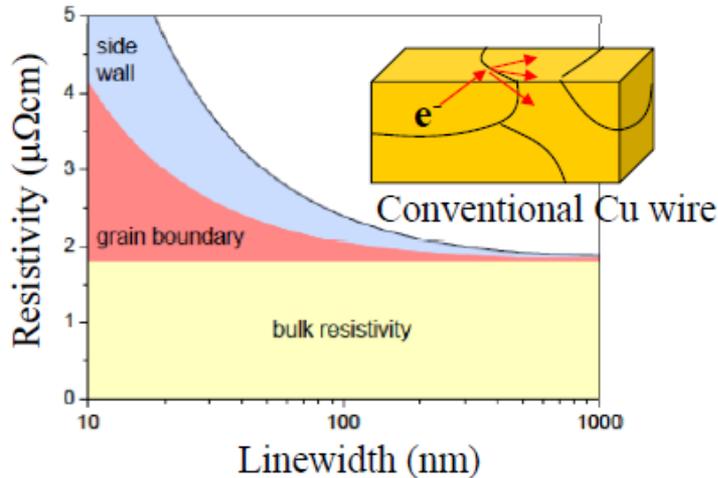
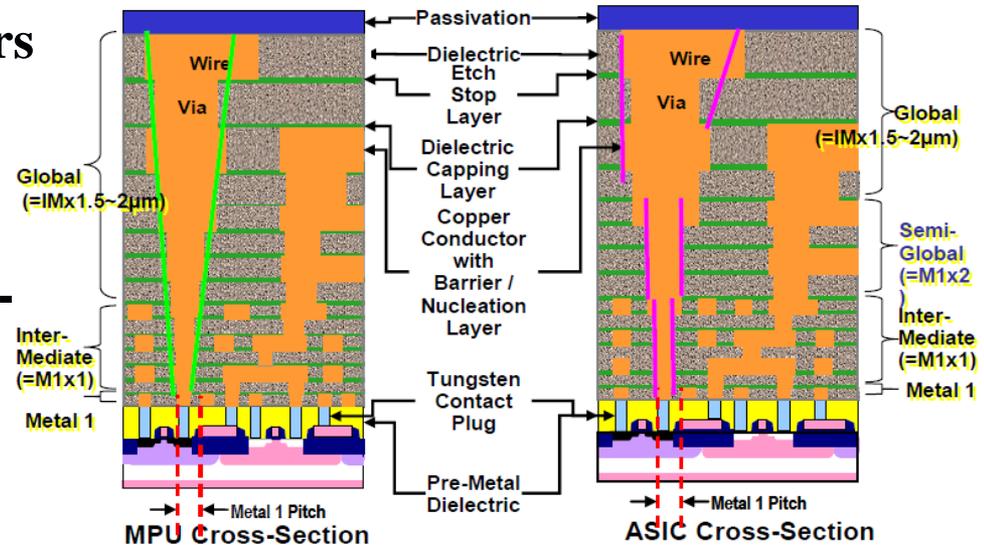
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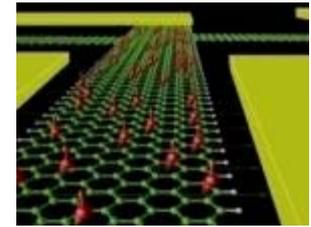
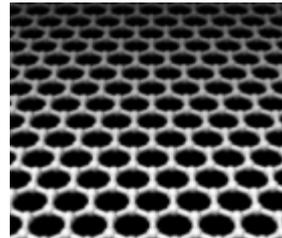
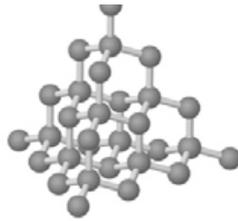
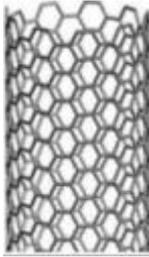
New interconnect materials needed

- Current copper interconnect suffers from electromigration at current density $\sim 1 \text{ MA/cm}^2$
- Increase of resistivity due to width-dependent scattering



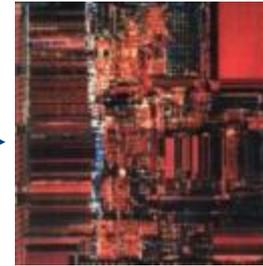
Source: ITRS 2011

Nanocarbons

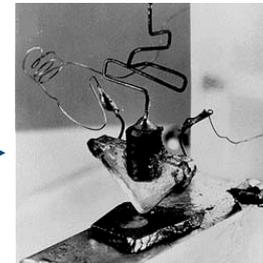


~2000
~1960
~1947

5 B Boron 10.811	6 C Carbon 12.0107	7 N Nitrogen 14.00674
13 Al Aluminum 26.981538	14 Si Silicon 28.0855	15 P Phosphorus 30.973761
31 Ga Gallium 69.723	32 Ge Germanium 72.64	33 As Arsenic 74.92160



Intel CPU



The first transistor

Nanocarbons as Interconnect Materials

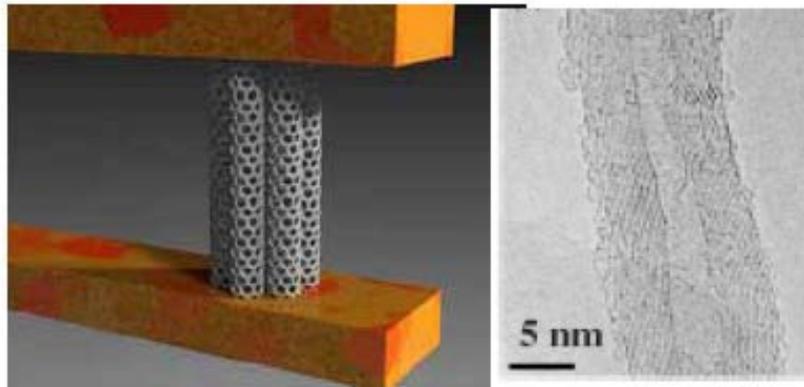
□ Physical properties of CNT:

➤ High current carrying capability

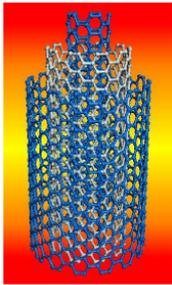
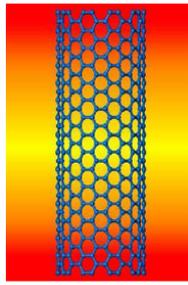
$> 10^7 \text{ A/cm}^2$ (Cu $\sim 10^6 \text{ A/cm}^2$) \implies Electromigration resistant

➤ High mobility and ballistic transport (6.45 K Ω /shell) \implies Low resistance

➤ High thermal conductivity $\sim 3000 \text{ W/K.m}$ (Cu $\sim 400 \text{ W/K.m}$)



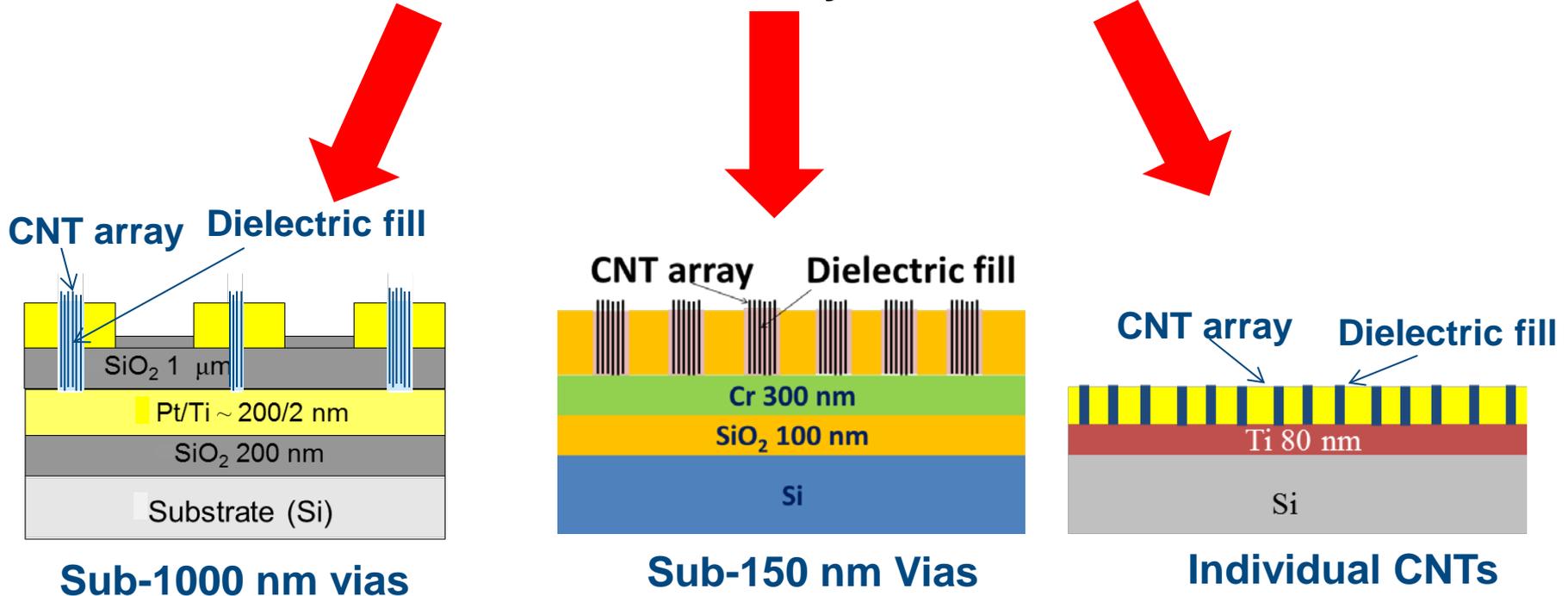
Nihei *et al.* Jpn. J. Apl. Phys. **44**, 1626 (2005)

Multi wall CNT (MWNT)	Single wall CNT (SWNT)
	
Metallic	Semiconductive /Metallic
Interconnect	Transistor

Objective and Approach

- Objective: To determine electrical characteristics of CNT on-chip via interconnects as a potential replacement for Cu.

CNT Via Interconnect Analysis for Advanced Nodes

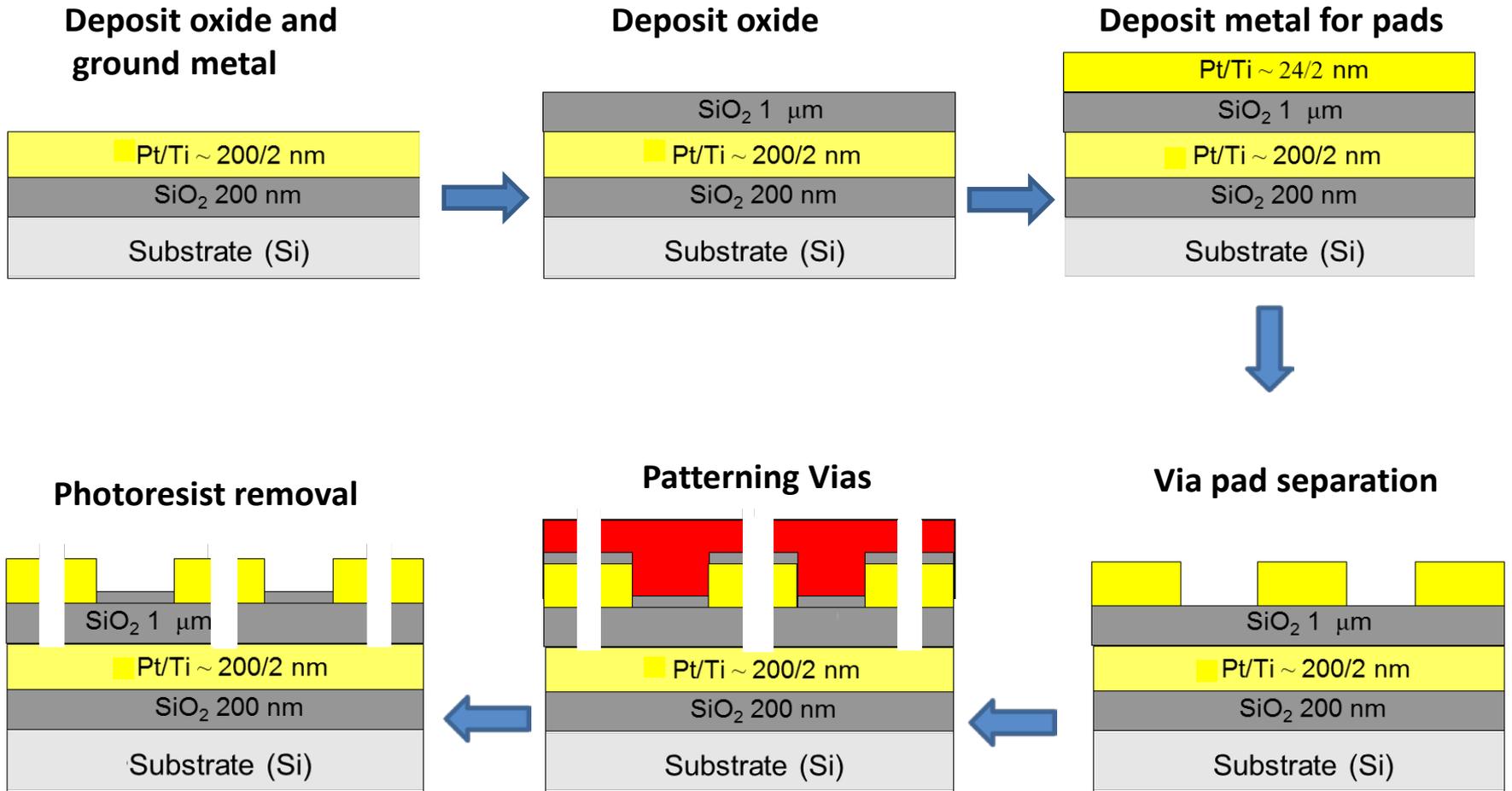


Outline

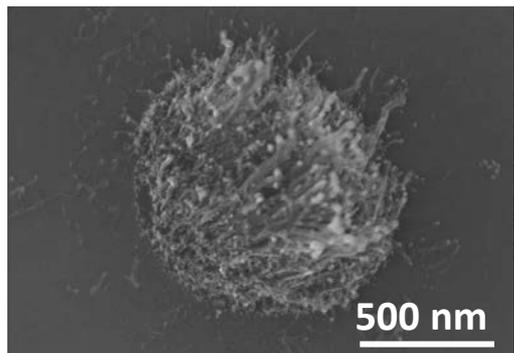
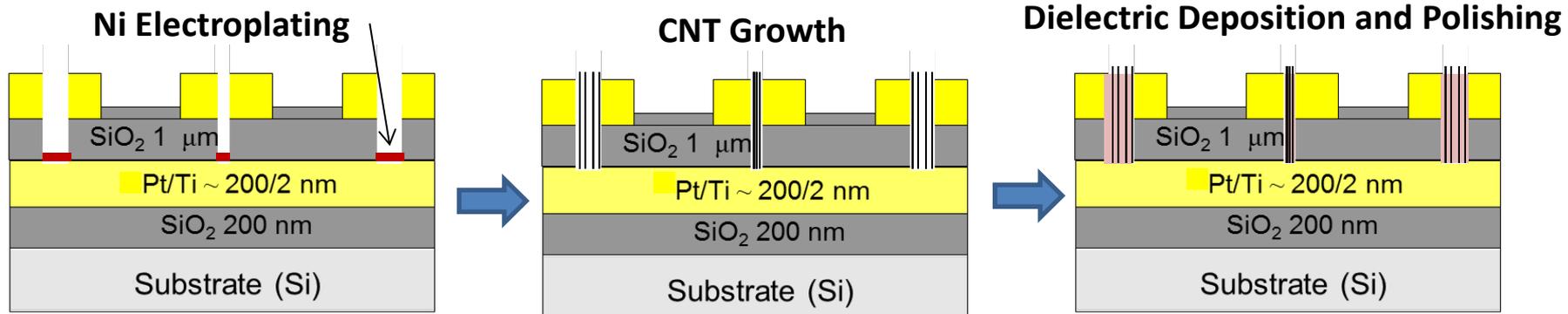


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- ❑ Electrical Characterization
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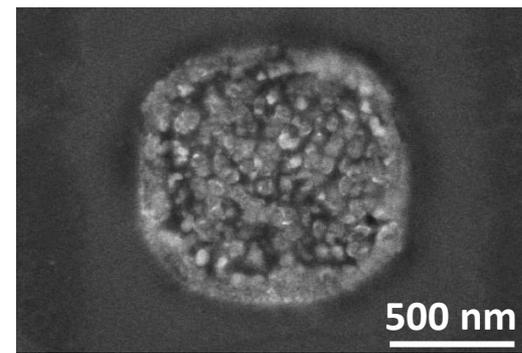
Fabrication of Sub-1000 nm Vias



Fabrication of Sub-1000 nm Vias

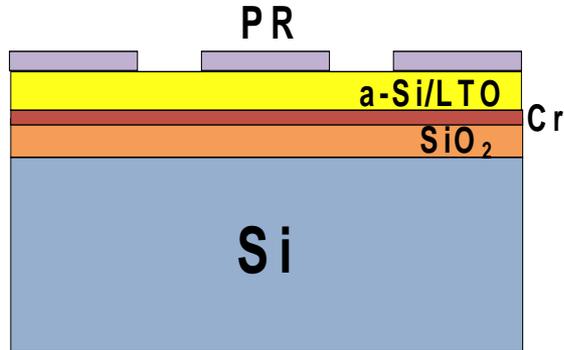


SEM image after CNT growth

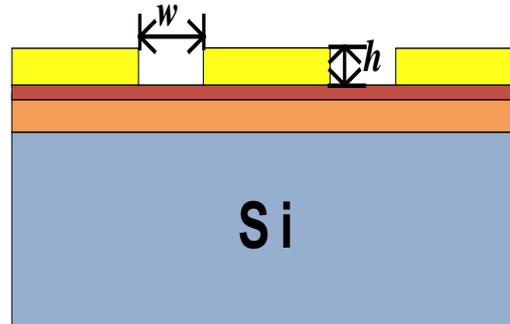


SEM image after polishing

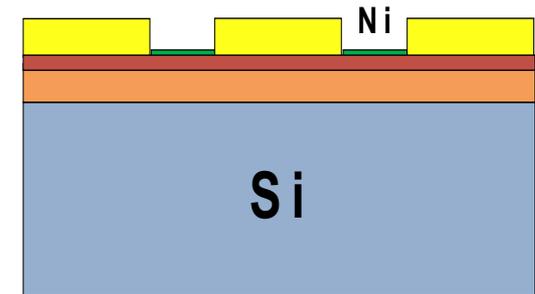
Fabrication of Sub-150 nm Vias



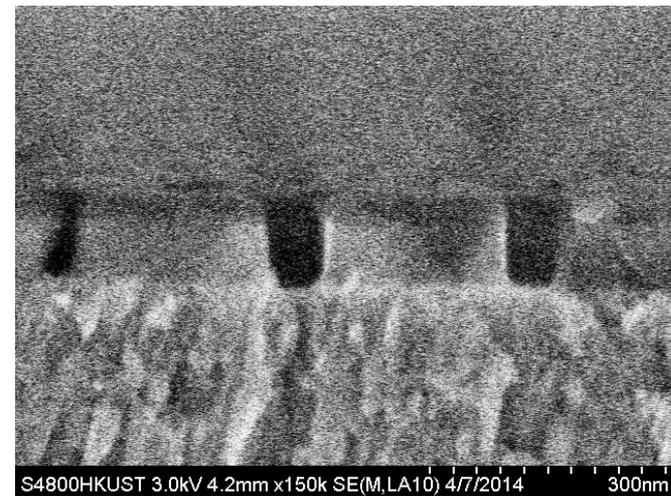
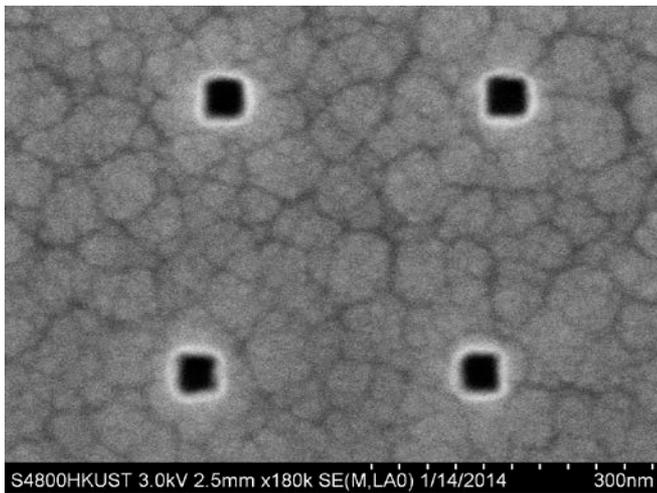
(a) Via patterning



(b) Dry etching and PR removal

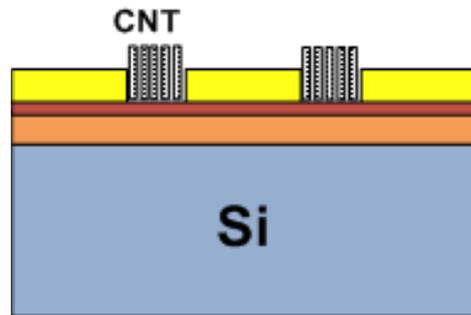


(c) Catalyst deposition and polishing

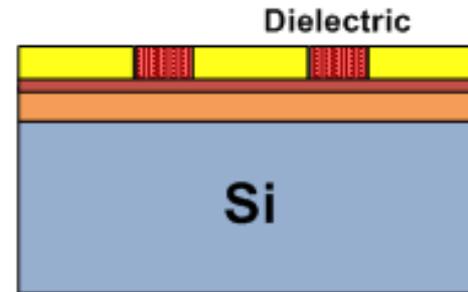


Top-view and cross-sectional SEM image of 60 nm vias for CNT growth

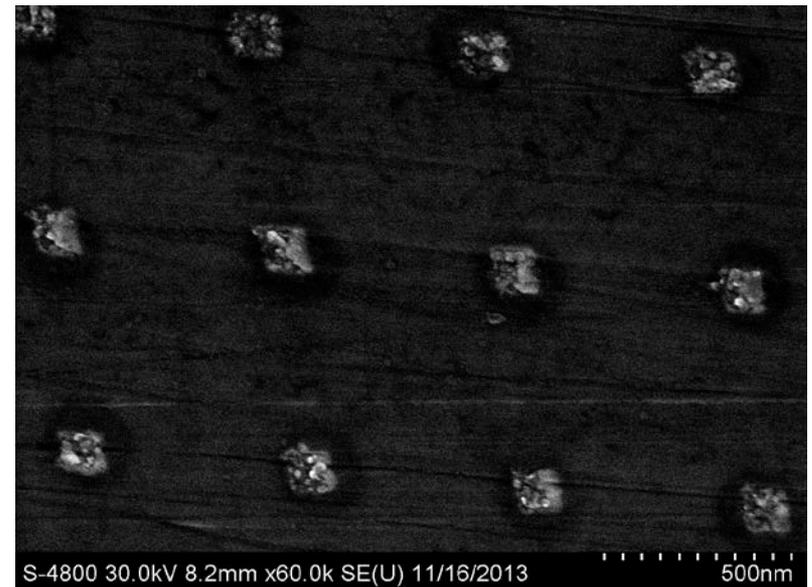
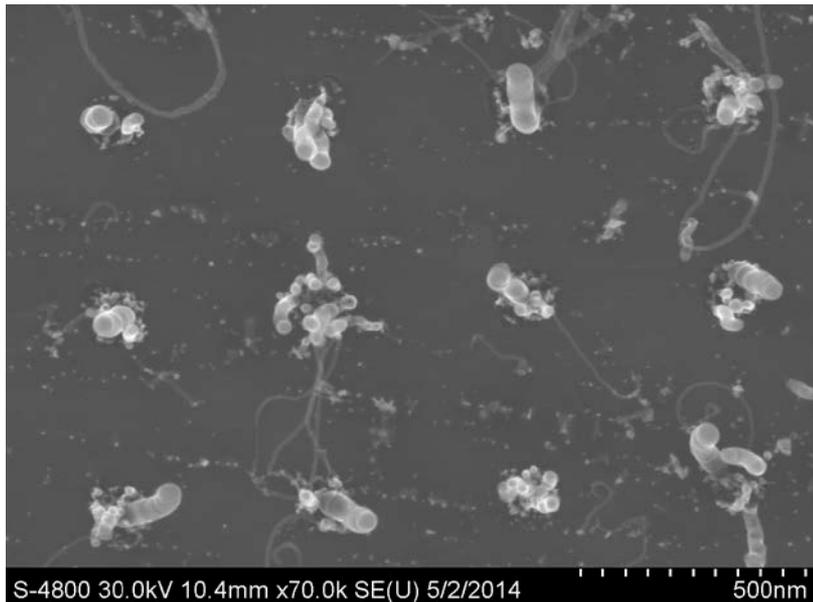
Fabrication of Sub-150 nm Vias



(4) CNT growth

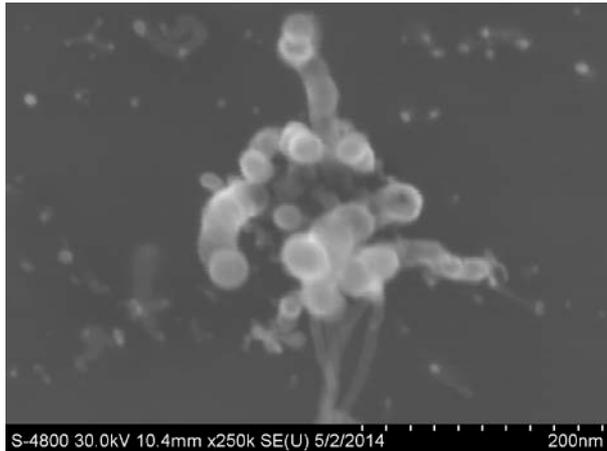


(5) Dielectric filling
and CMP



Fabrication of Sub-150 nm Vias

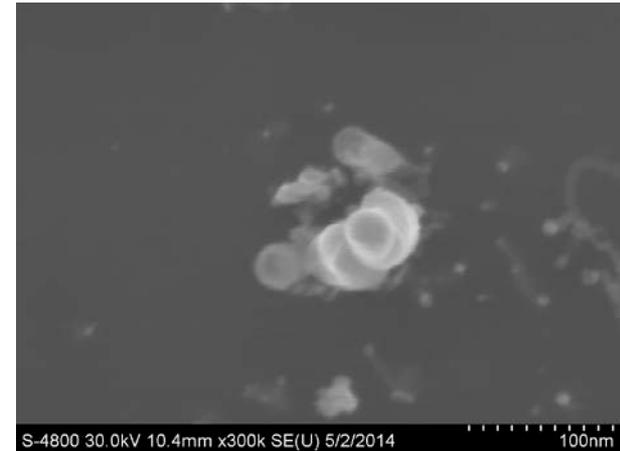
□ Estimation of CNT areal density in via, D_{CNT}



90 nm CNT via



$\sim 2.2 \times 10^{11} / \text{cm}^2$

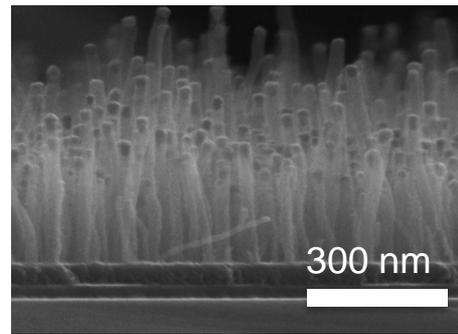
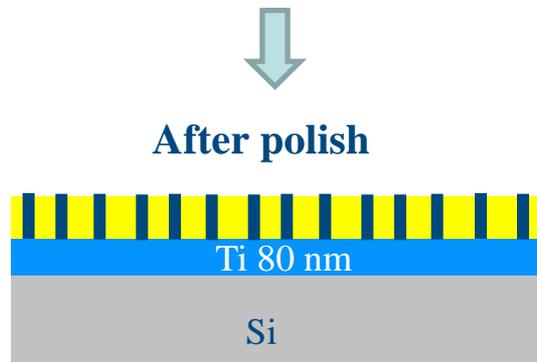
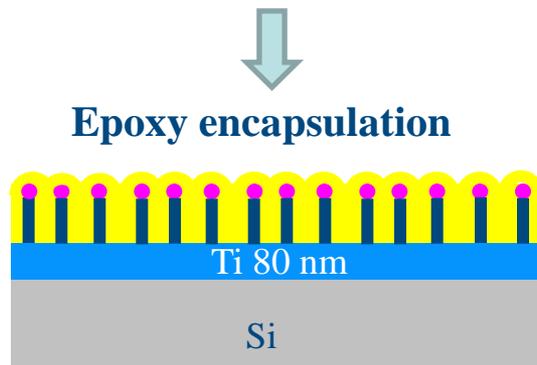
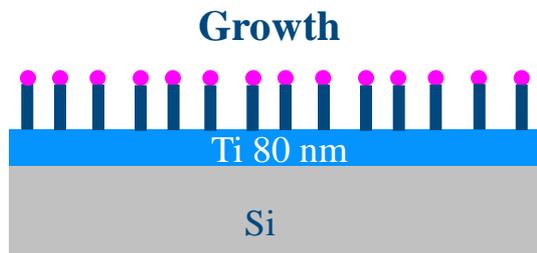


60 nm CNT via

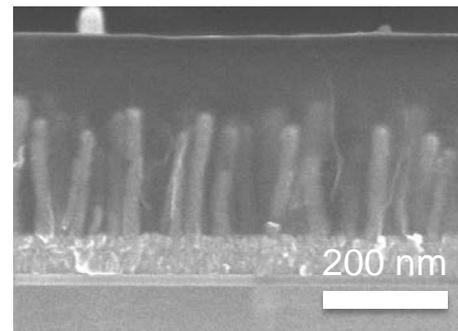


$\sim 1.7 \times 10^{11} / \text{cm}^2$

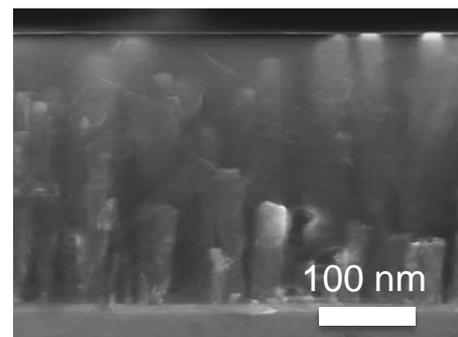
Fabrication for Individual CNT Probing



CNT grown on Ti/Si



After encapsulation & partial polish



After final polish

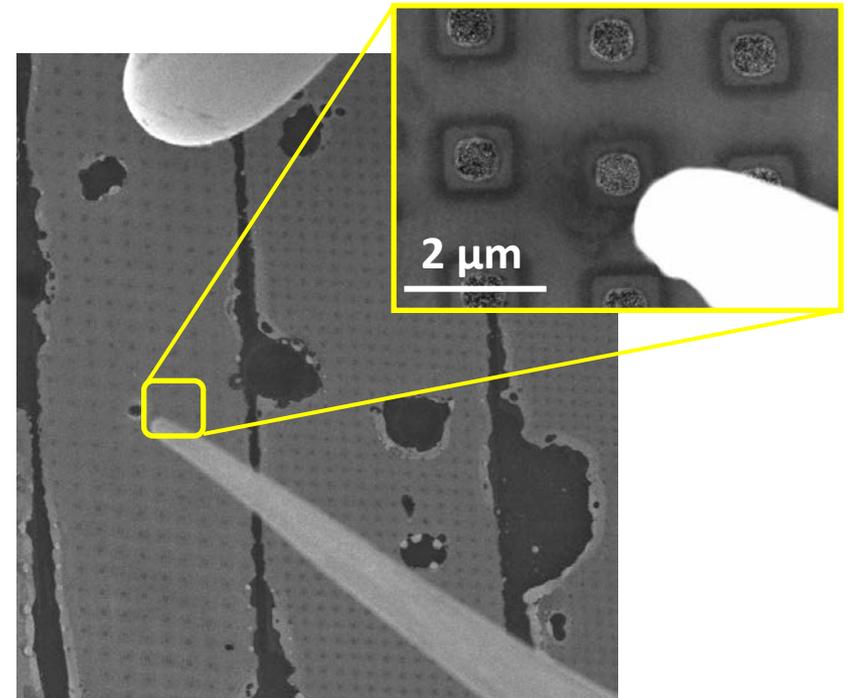
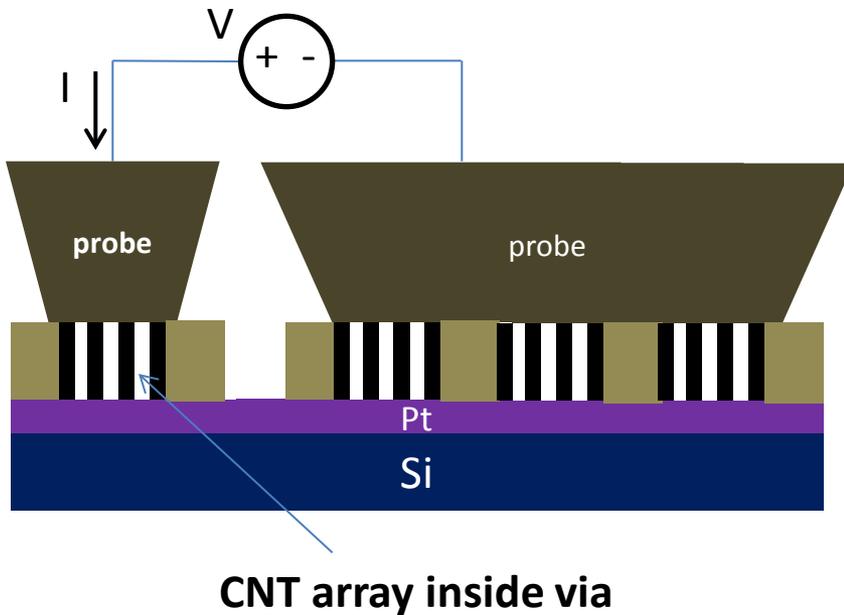
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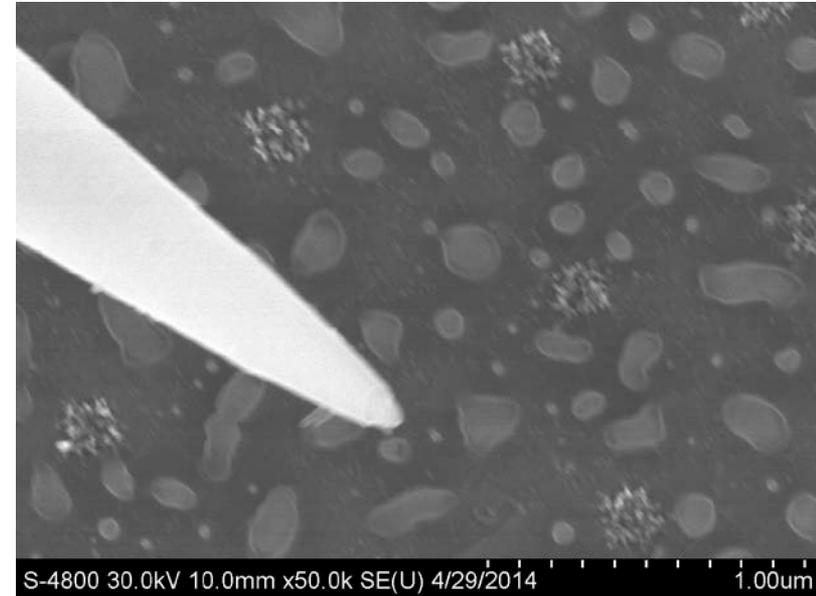
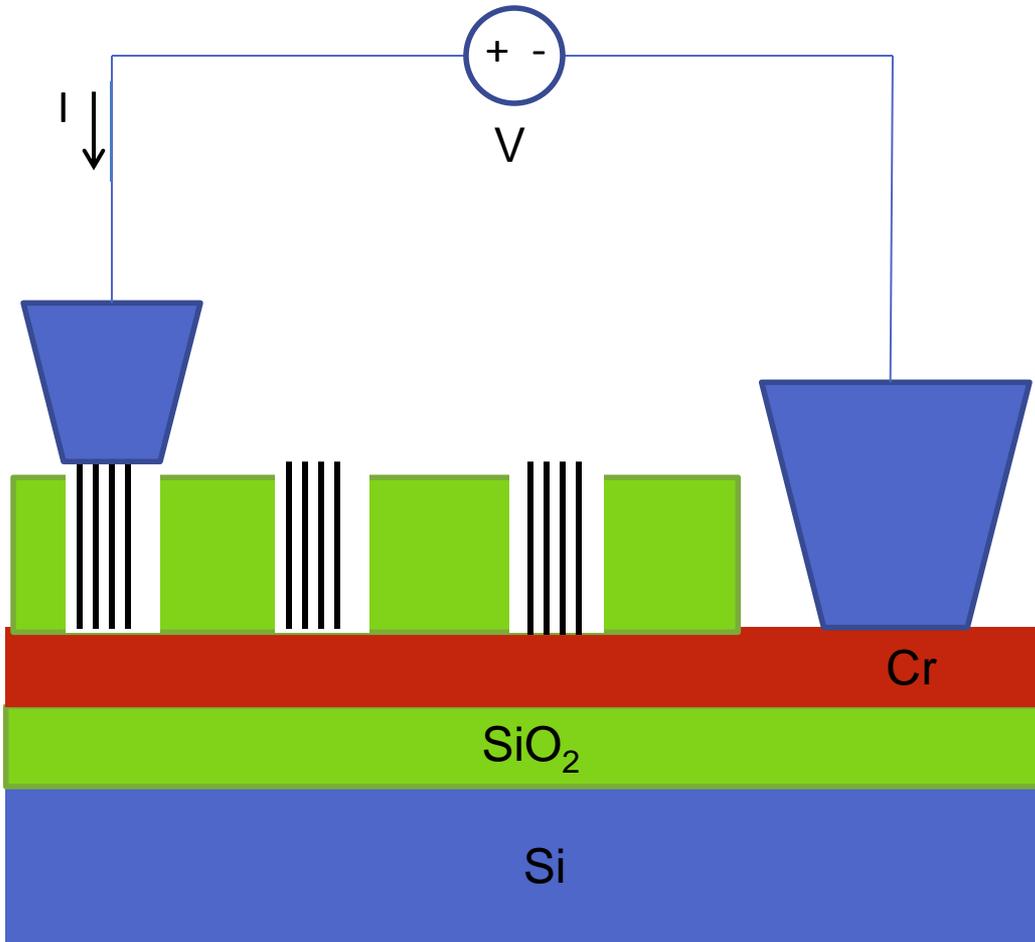
Measurement setup for Single CNT Via

- *In situ* nanoprobing inside SEM
- Sub-1000nm CNT via



Measurement setup for Single CNT Via

- ▣ *In situ* nanoprobing inside SEM
- Sub-150nm CNT via



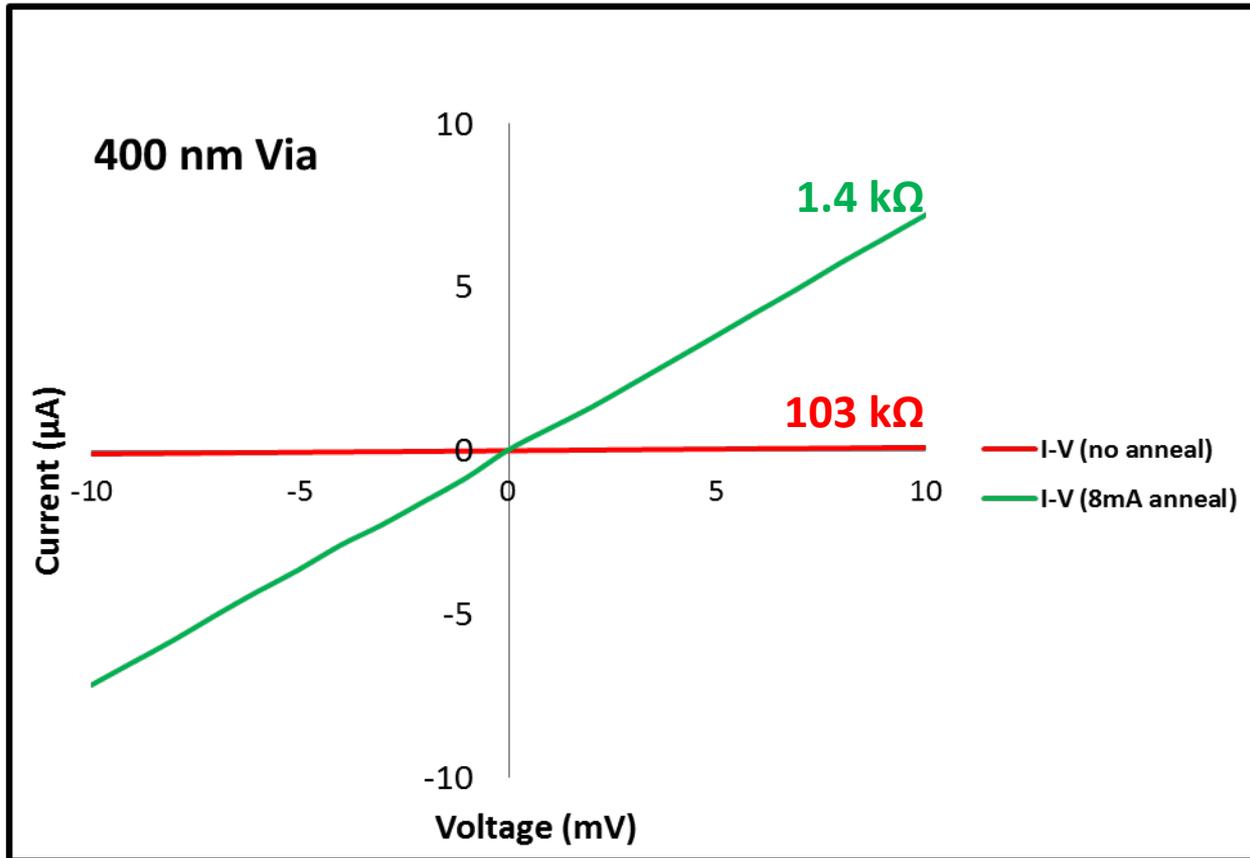
Probing a single CNT Via

Outline

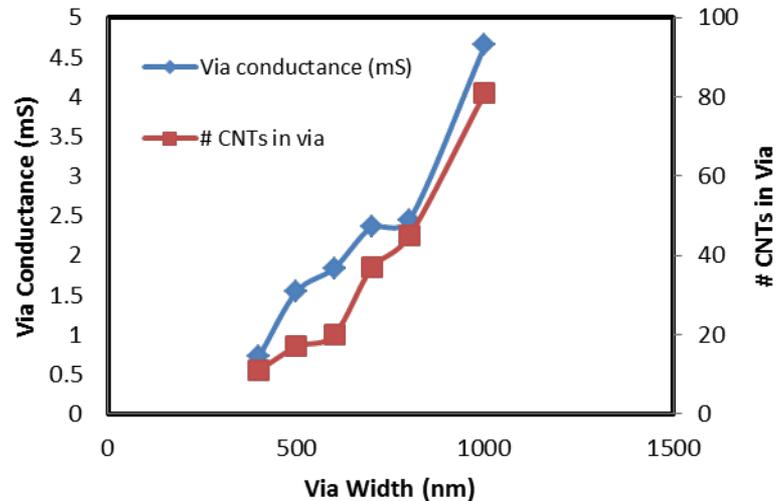


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Electrical Characteristics of Sub-1000 nm Vias



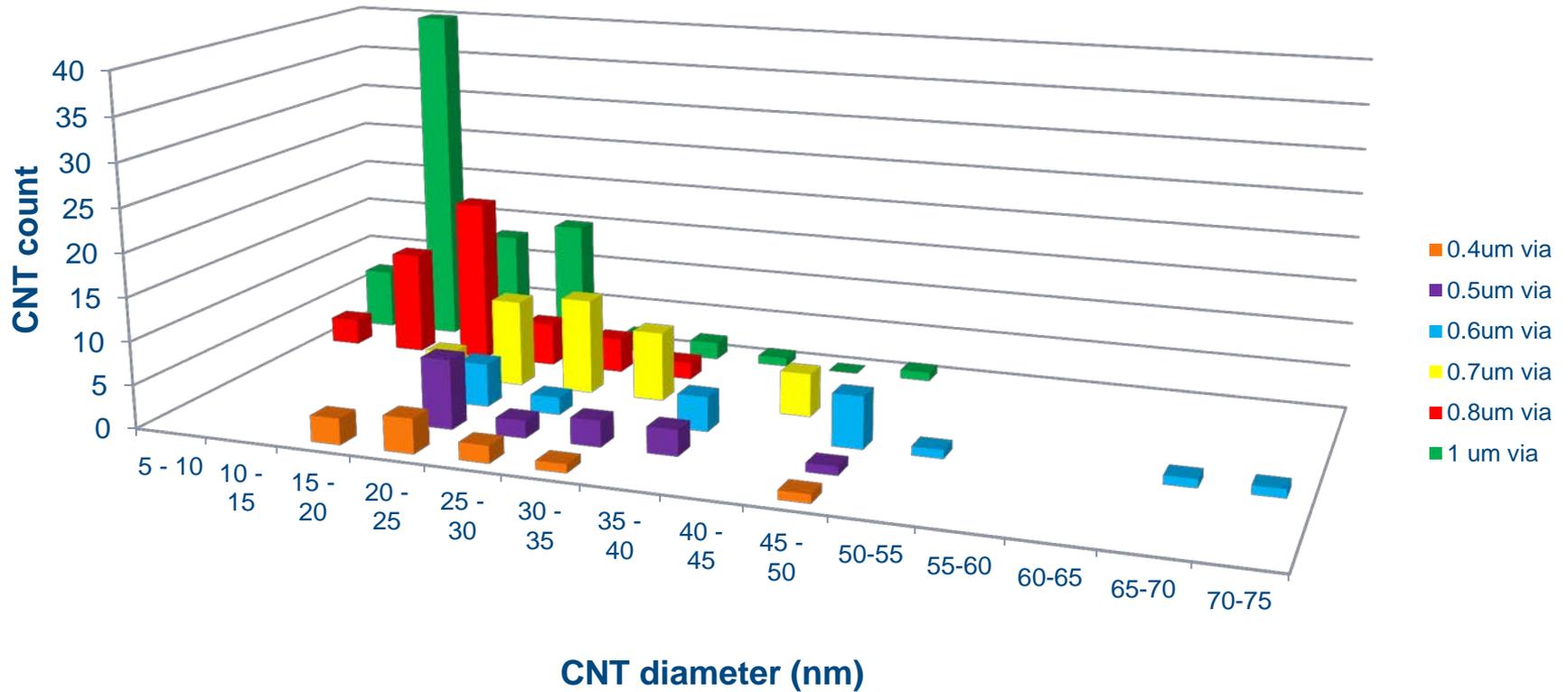
Electrical Characteristics of Sub-1000 nm Vias



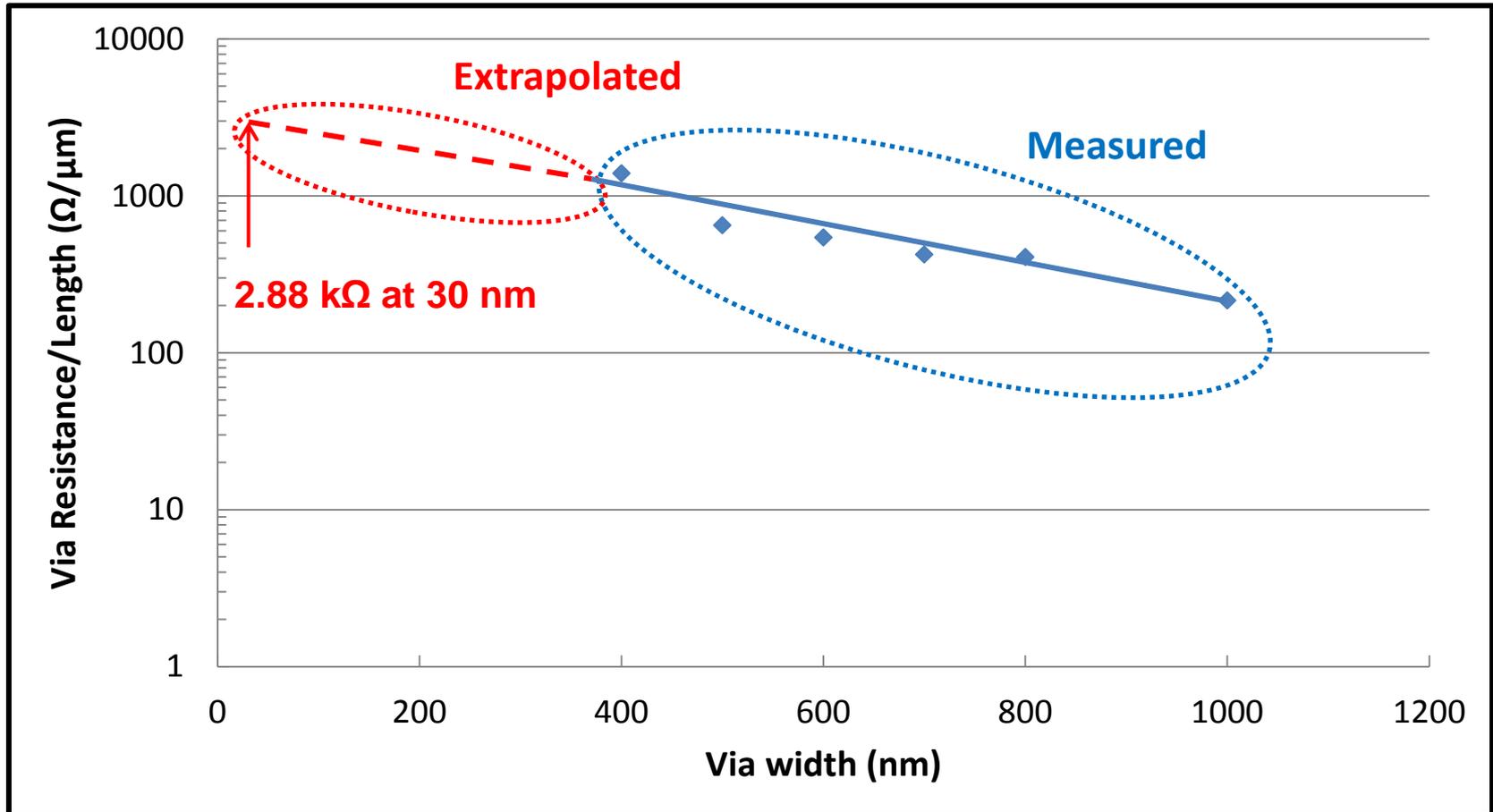
Via width (nm)	Via height (nm)	CNT diameter (nm)	# CNTs in via	CNT packing density (cm ⁻²)	Via resistance (Ω)	Via conductance (mS)
1000	1000	16.56	81	8.10E+09	215	4.65
800	1000	17.74	45	7.03E+09	408	2.45
700	1000	27.85	37	7.55E+09	423	2.36
600	1000	39.44	20	5.56E+09	543	1.84
500	1000	29.29	17	6.80E+09	649	1.54
400	1000	26.05	11	6.88E+09	1394	0.72

CNT diameter distribution in Sub-1000 nm Vias

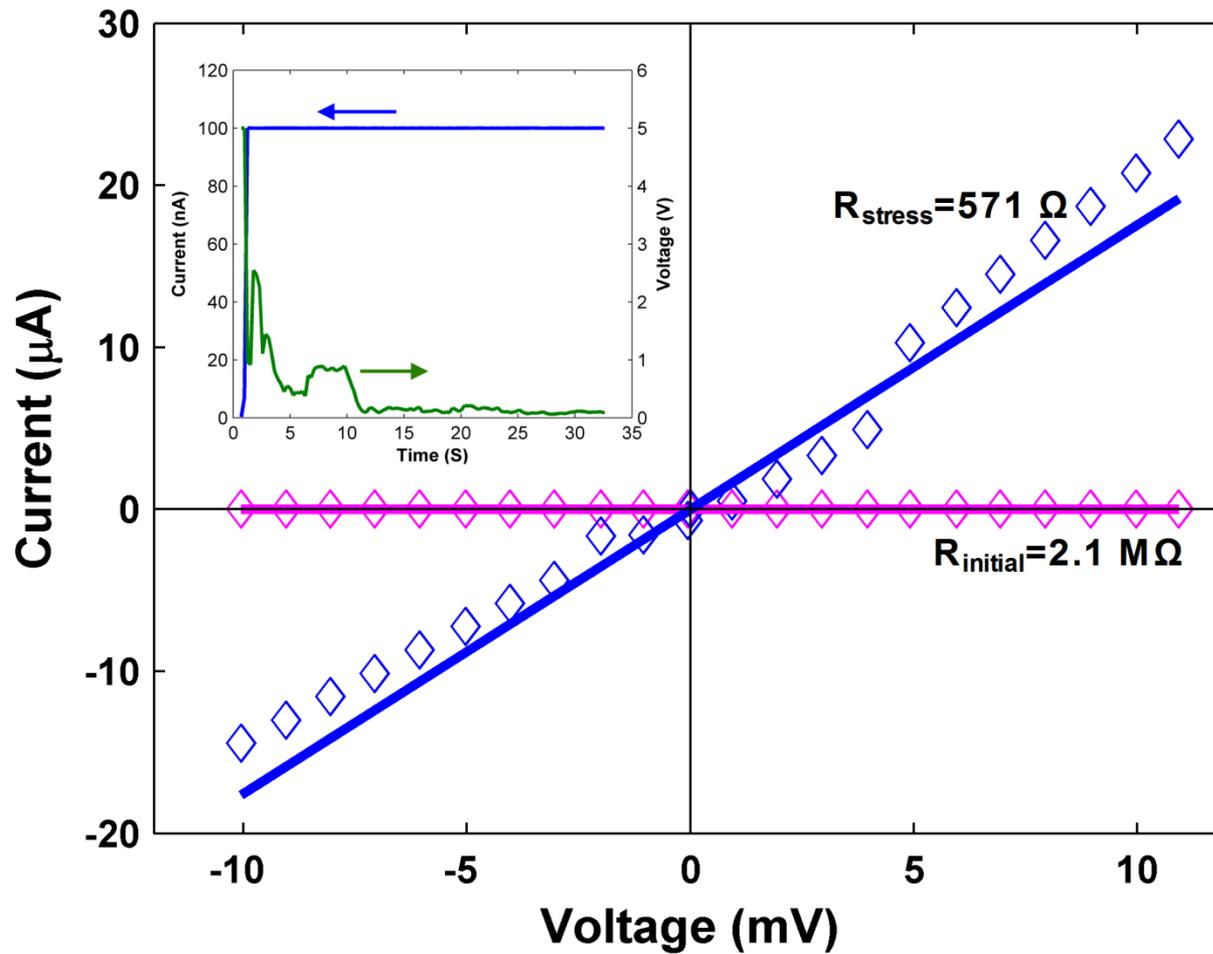
CNT diameter distribution



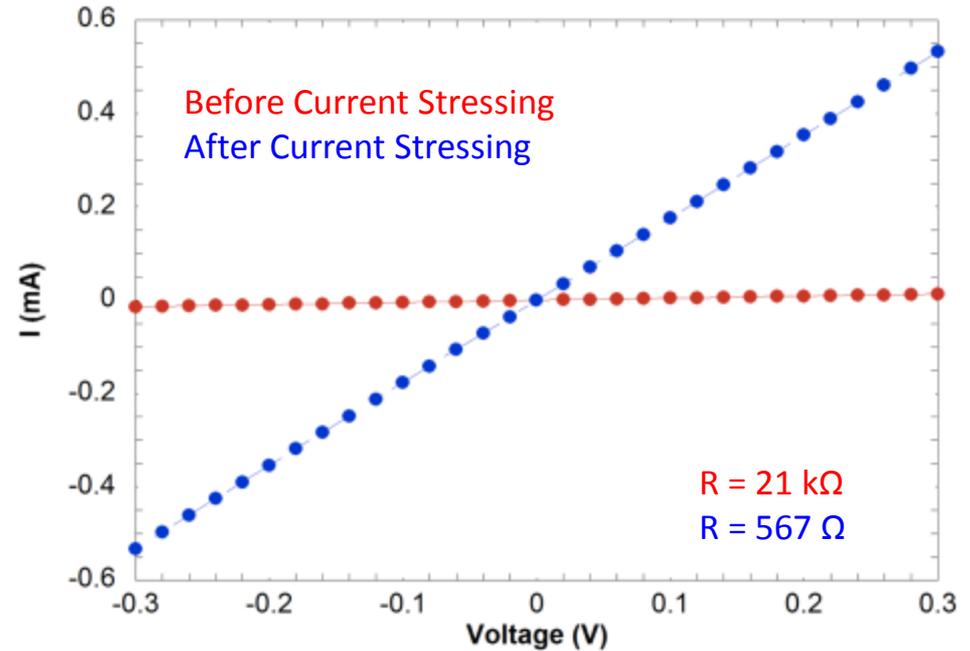
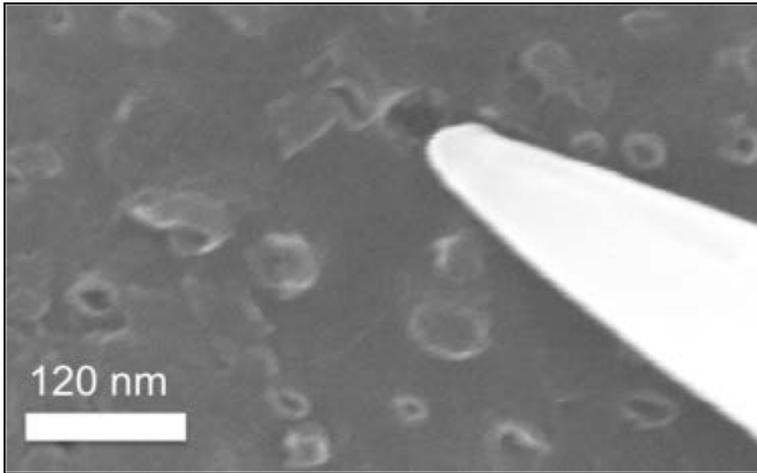
Projected resistance from Sub-1000 nm Vias



Electrical Characteristics of a 60 nm Via

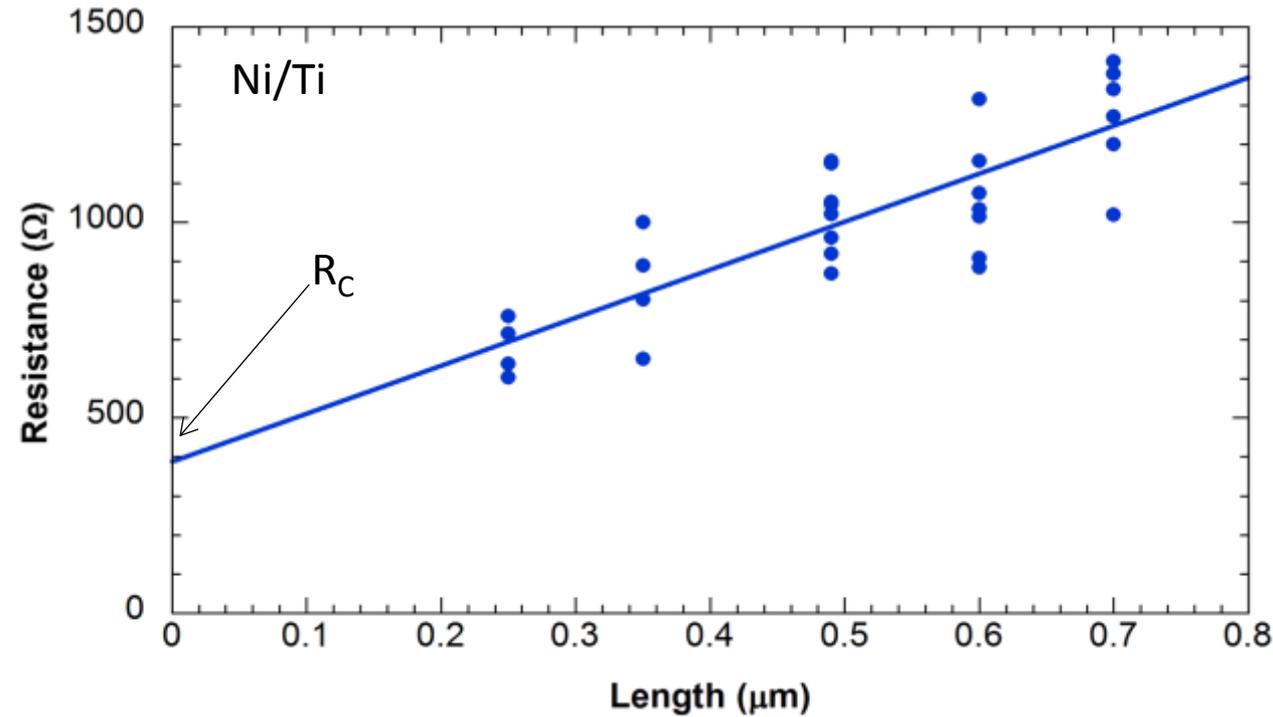


Electrical Characteristics of Single CNT



- W-probe enlarges during probing
- High-current annealing ($\sim 3.5 \text{ mA}$) improves probe contact

Electrical Characteristics of Single CNT

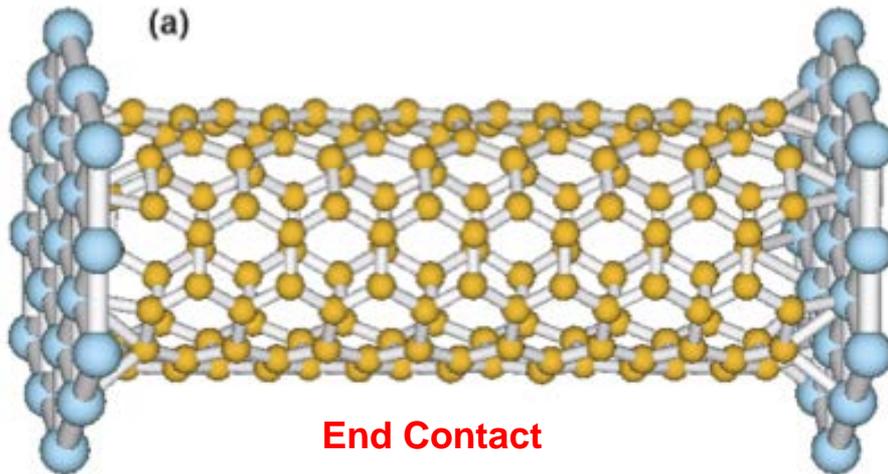


ρ (Ω -cm)	R_C (Ω)
2.4×10^{-4}	388

Diameter of probed samples:
~50 nm

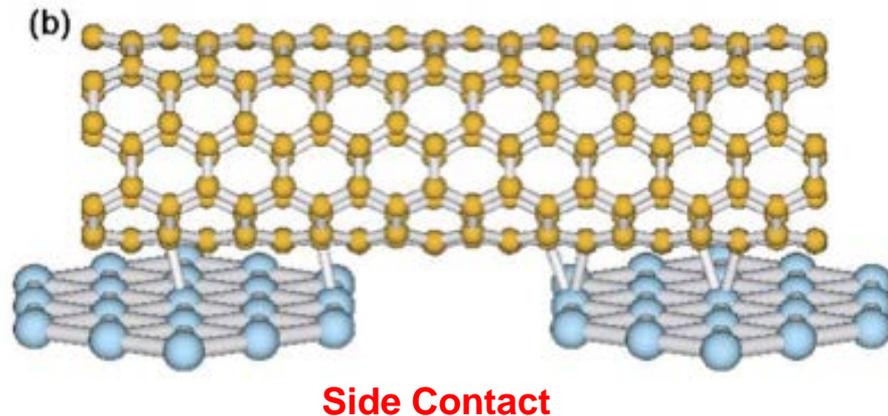
$$R_{Total} = R_C + R_{CNT} = R_C + \frac{4\rho}{\pi D_{CNT}^2} L_{CNT}$$

Further Consideration – Metal-CNT Contact



□ Chemical bonding at end contact

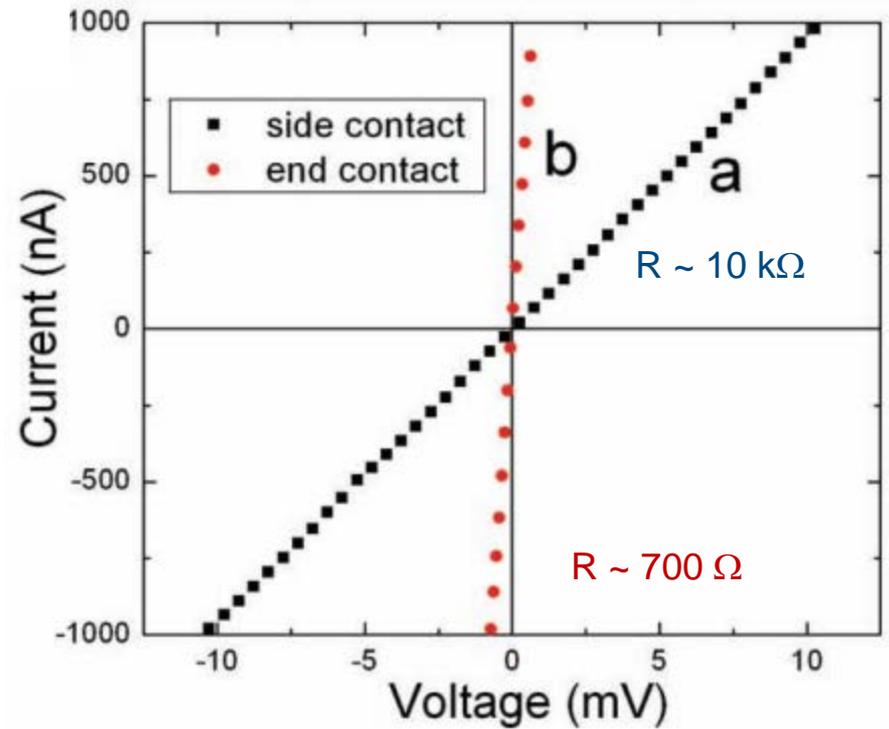
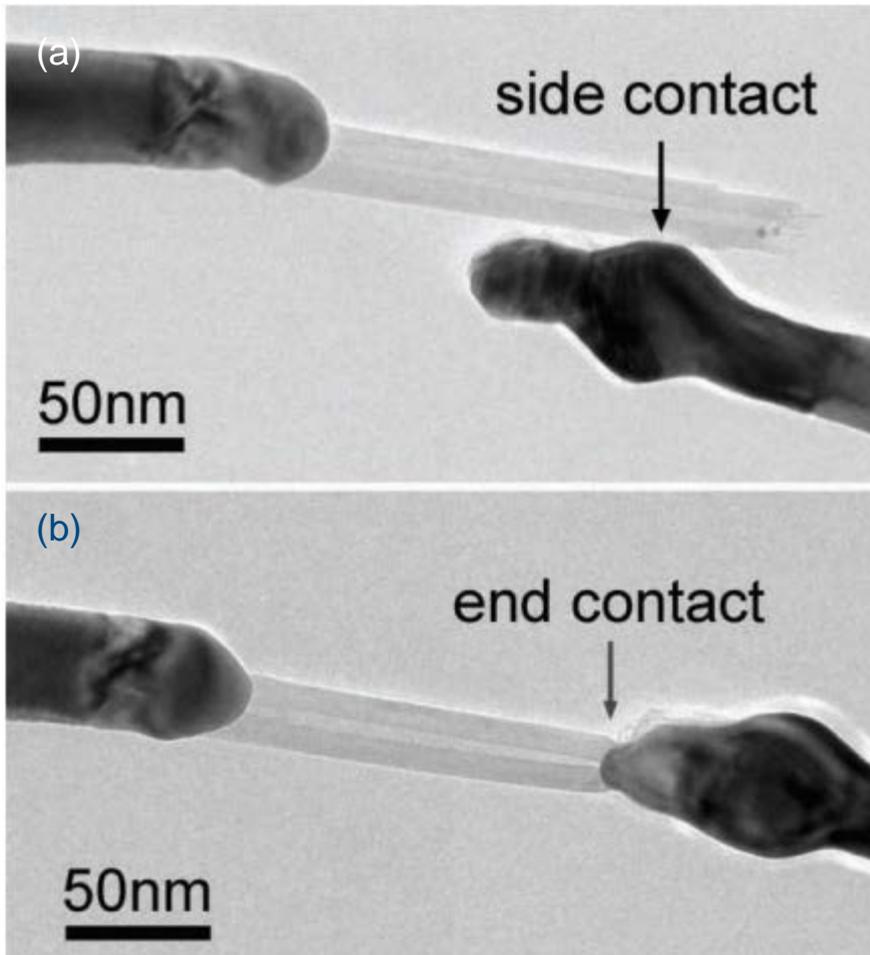
- Saturated C-bonds
- Conduction modes of graphitic structure is unaffected
- Interface with concentric walls



□ Van der Waals bonding at side contact

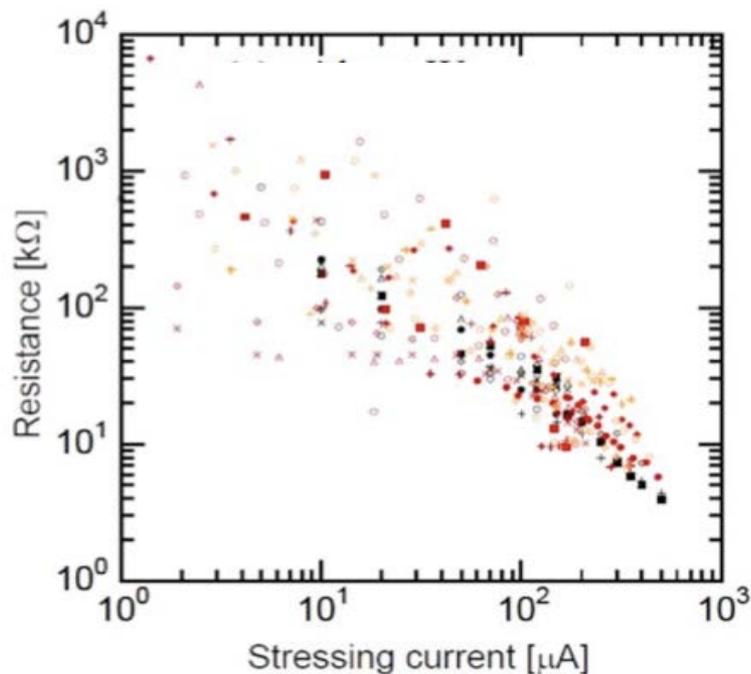
- Larger interfacial separation
- C-bonds remain unsaturated, inhibiting conduction
- Interface with outermost wall only

Side and End Contacts

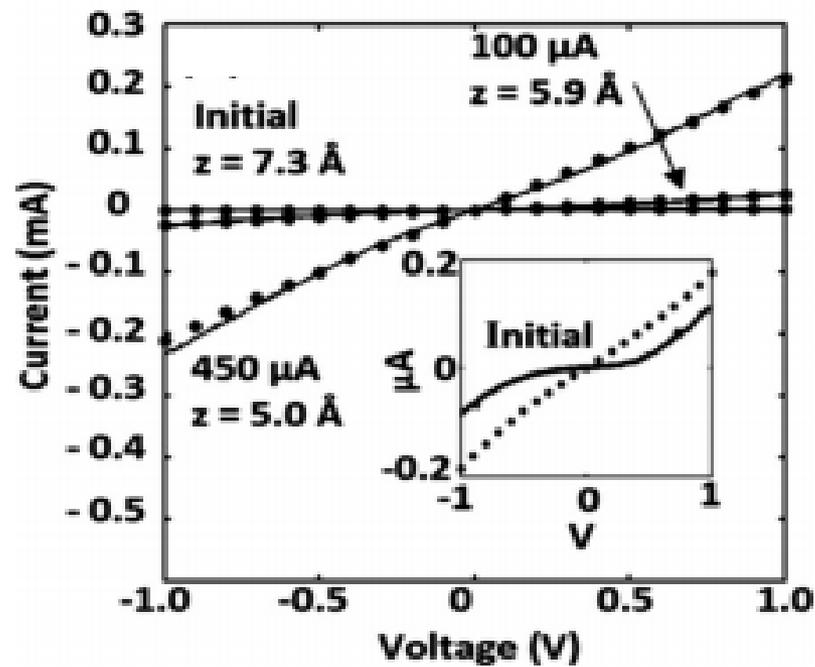


Wang *et al.*, *Adv. Mater.* **22**, 5350 (2010)

Contact improvement – Joule Heating



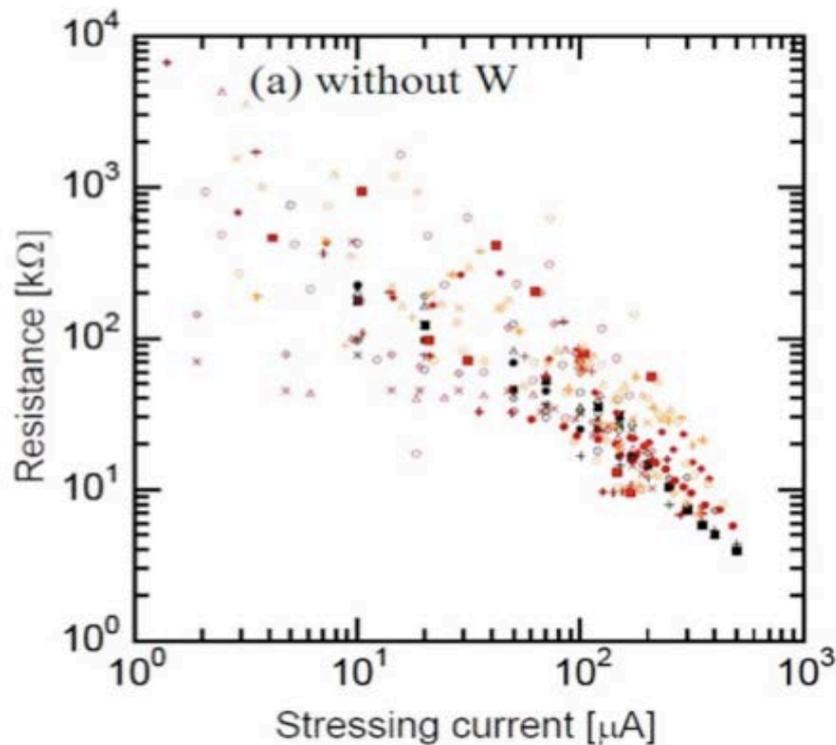
Kitsuki *et al*, *APL* **92**, 173110 (2008)



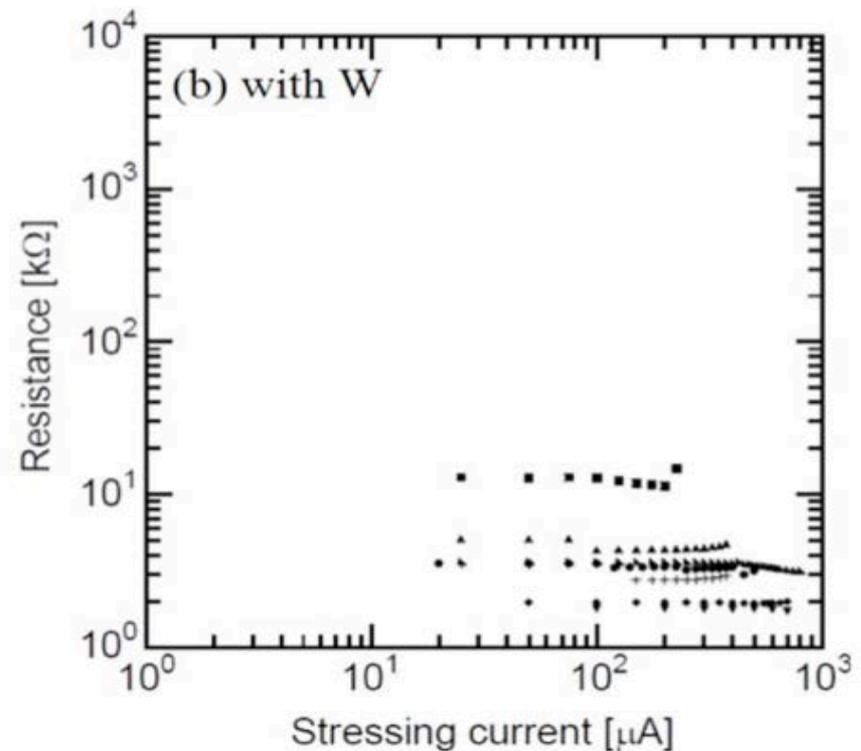
Yamada *et al*, *JAP* **107**, 044304 (2010)

- I-V nonlinearity reduced by stress current
- Interfacial gap remains large
- Contact resistance \sim few k Ω

Contact improvement – Deposited Tungsten



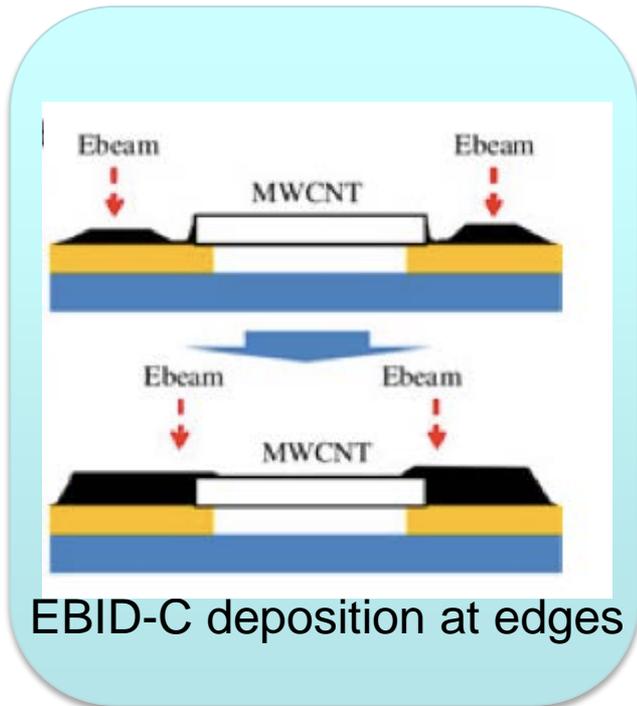
Kitsuki *et al*, *APL* **92**, 173110 (2008)



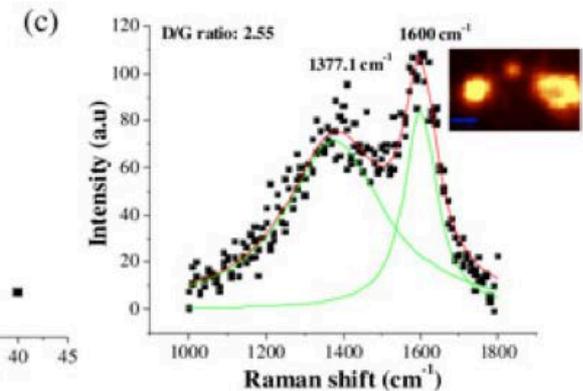
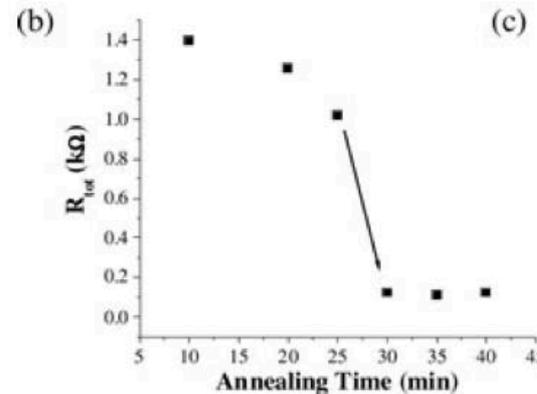
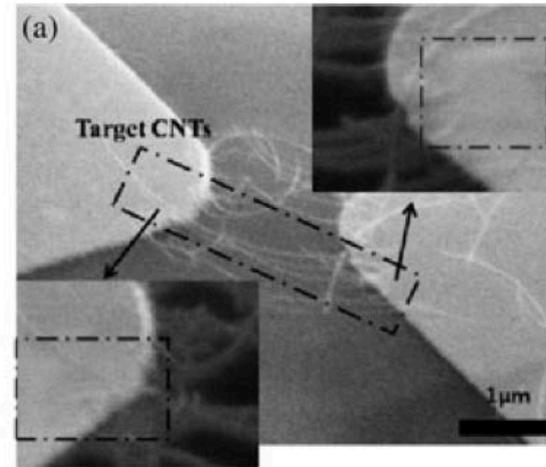
Saito *et al*, *APL* **93**, 102108 (2008)

- Resistance with W-deposited contacts reduced significantly and independent of stress current
- Contact resistance minimized

Contact improvement – EBID-C + Joule Heating



Total resistance reduced
from 300 k Ω to 116 Ω



Kim *et al*, *IEEE Trans Nanotech.* **11**, 1223 (2012)

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Summary

- ❑ CNT vias down to 60 nm width fabricated and characterized
 - Linear I-V characteristics for vias and individual CNTs
 - “Best” projected resistance for 30 nm CNT via $\sim 5 \times W$ via resistance
- ❑ Ongoing efforts to decrease CNT diameter and increase CNT packing density to reduce via resistance
- ❑ Additional contact engineering needed to reduce overall resistance
- ❑ Further considerations on contact resistance reduction with CNT growth process improvements



Thank You...

