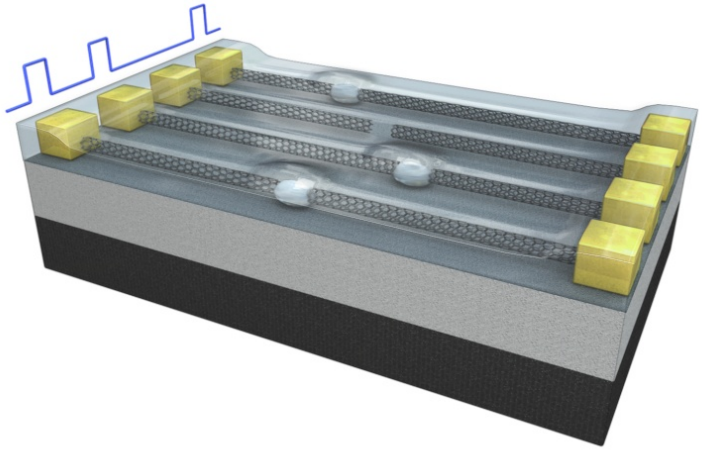
Low-Power Resistive Memory with 1D and 2D Electrodes

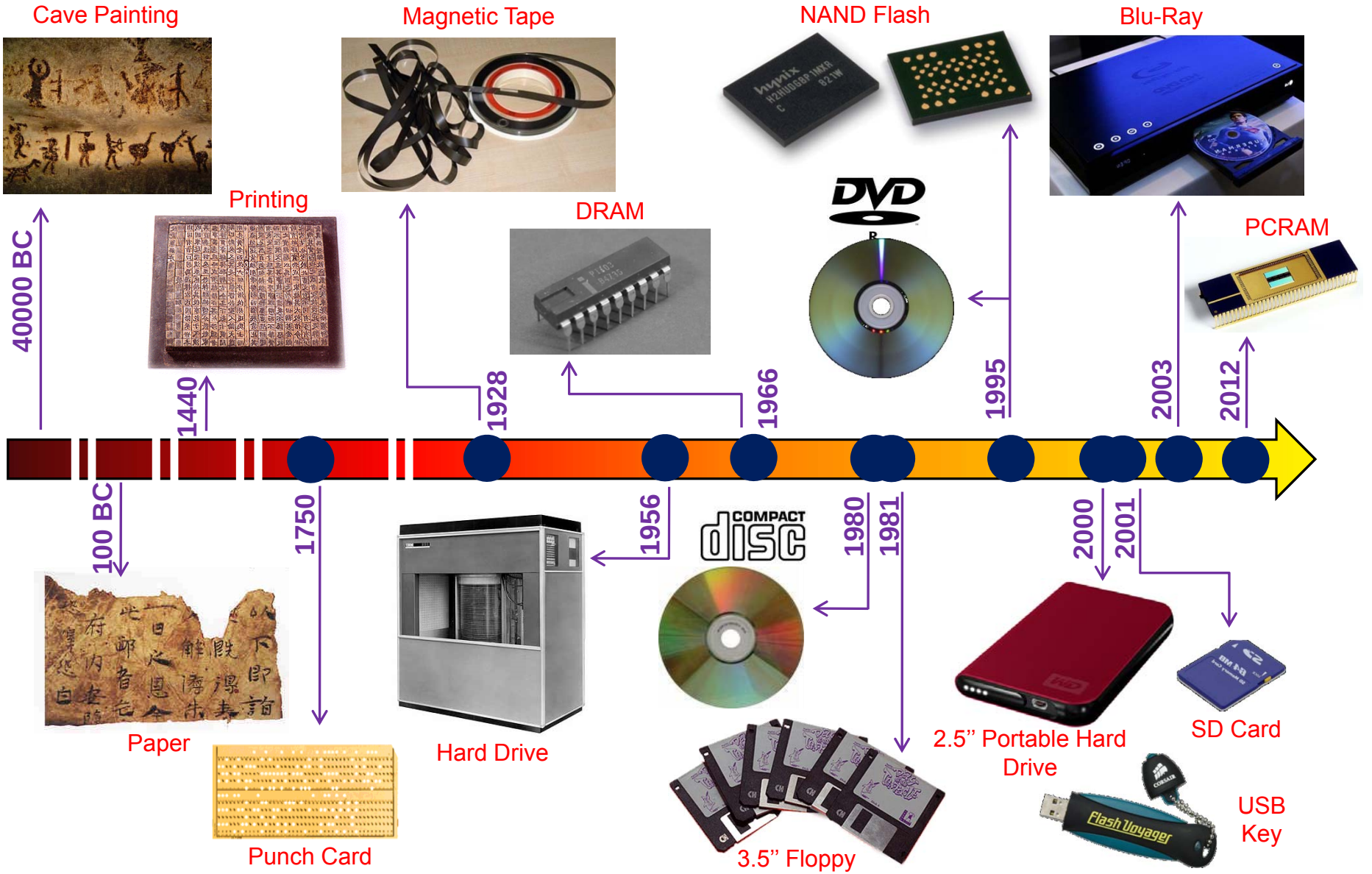
Feng Xiong

Co-advisor: Prof. Yi Cui
Co-advisor: Prof. Eric Pop

Electrical Engineering,
Stanford University



Timeline of Data Storage

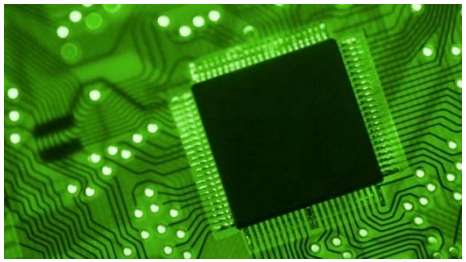


Memory in Our Lives

64 GB

Memory Industry
~ 500 GGB
~ $80 Billions

512 GB

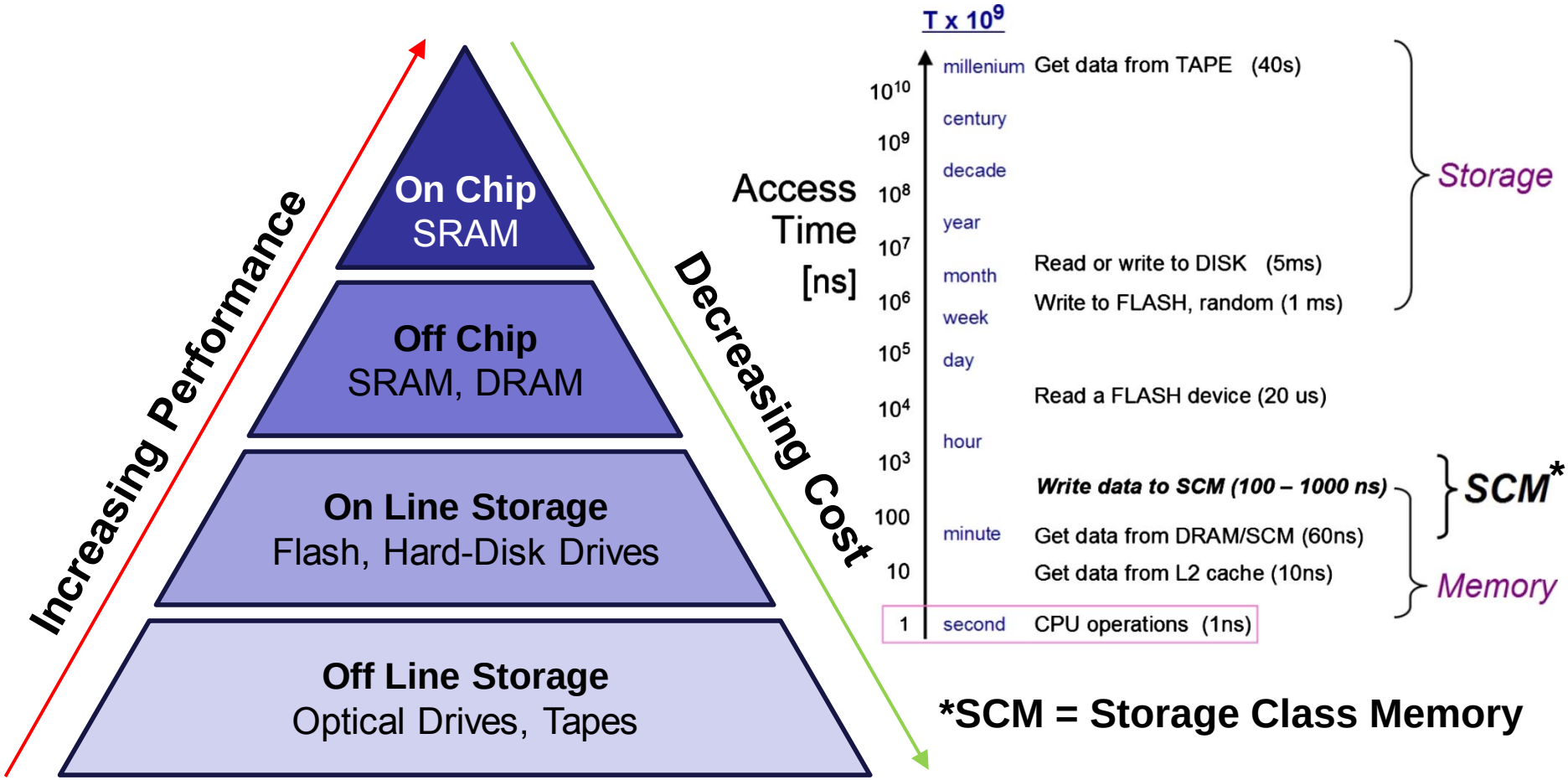


128 GB

32 GB

32 GB

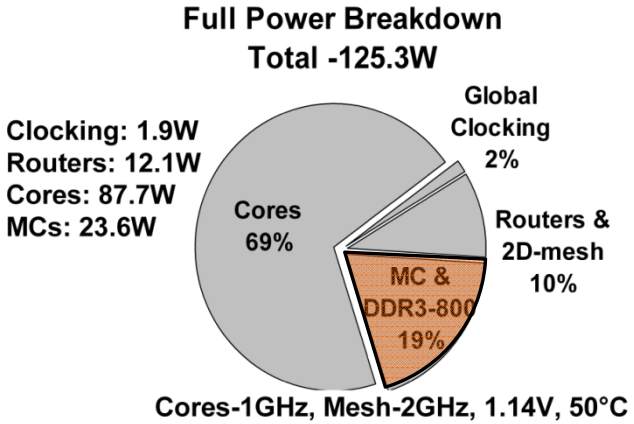
Memory Hierarchy

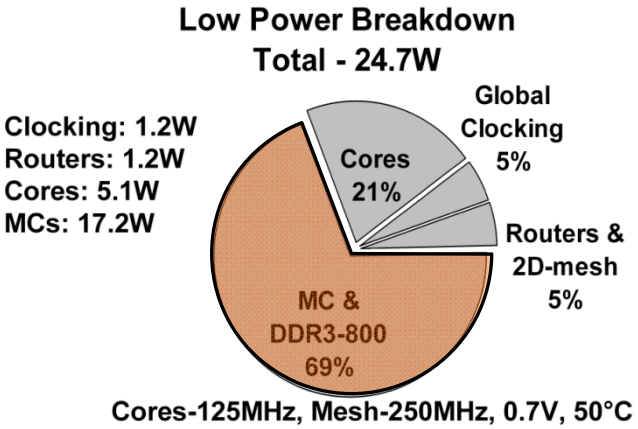


G.W. Burr et al, *J. of Vac. Sci & Tech.* **28**, 223 (2010)

Why Power Dissipation in Memory?

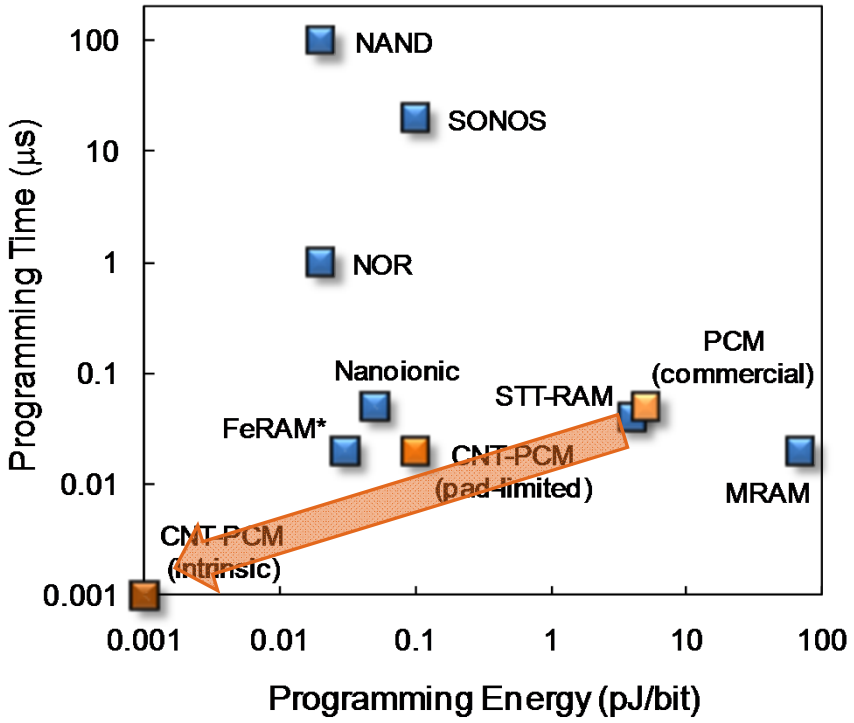
Intel CPU power in 45nm CMOS, memory is a big piece of the pie!





J. Howard, *ISSCC*, p. 108 (2010)

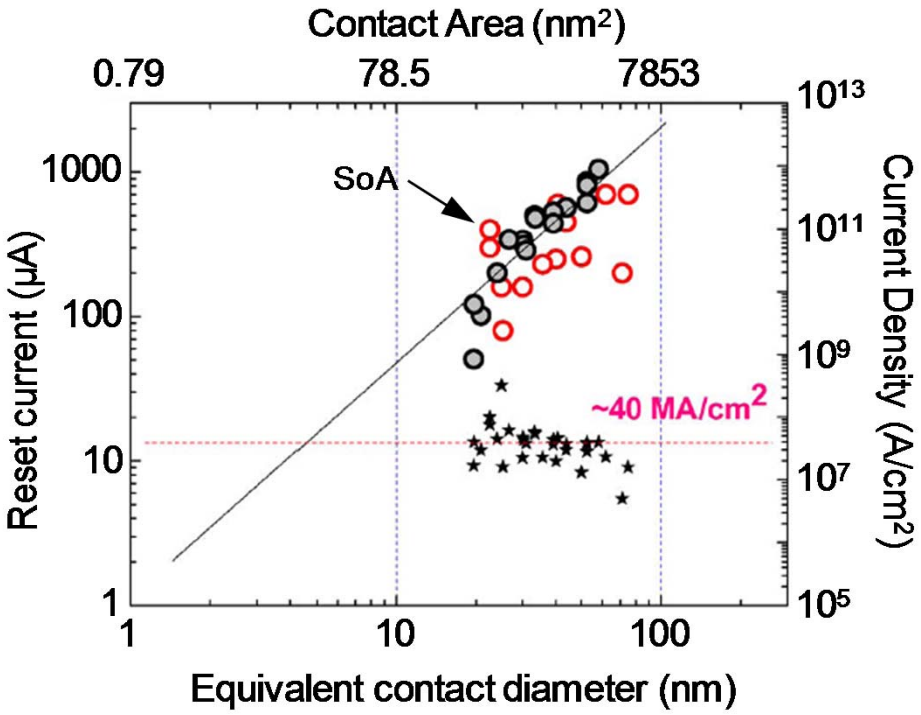
ITRS 2010



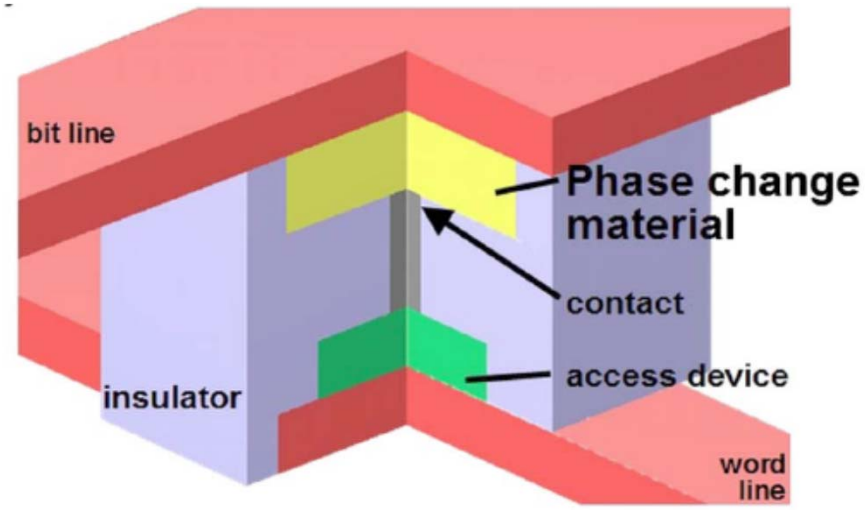
trade-off between **speed** vs. **energy**

Phase Change Memory Scaling

H.-S. P. Wong *et al*, *Proc. IEEE* 98, 2201 (2010)



PCM "Mushroom" Cell

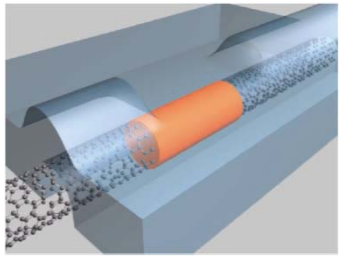


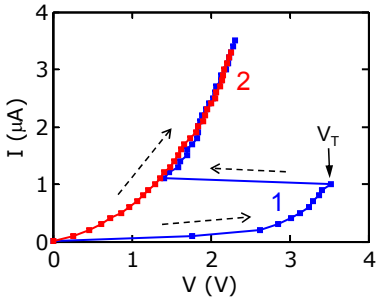
S. Raoux, *et al*, *IBM J.R.Dev.* 52, 468 (2008)

- Phase change memory is highly scalable with electrode size
- Use carbon nanotube (CNT) electrodes!

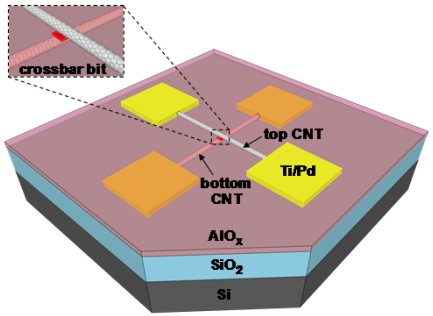
Outline

- Integrating CNT with PCMs
  - Phase change materials + CNT
  - Nanotube-PCM Device
  - Self-Aligned PCM Nanowire-Nanotube Device

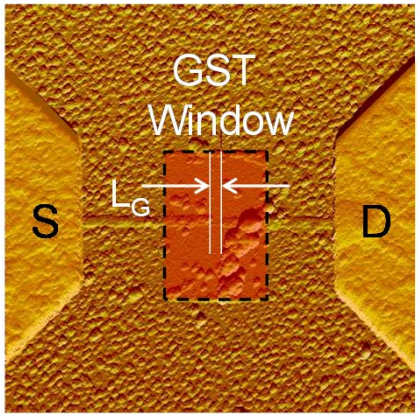




- CNT Crossbar RRAM
  - Resistive Random Access Memory
  - CNT Crossbar

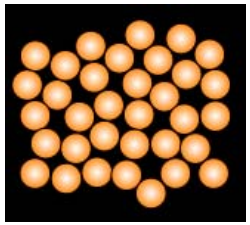
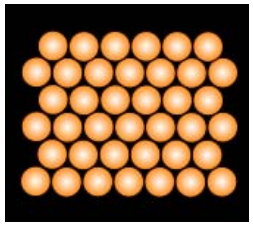


- Graphene Ribbons with PCM
  - 2D graphene ribbons
  - Scalable, flexible and inexpensive



- Summary

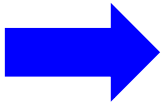
Phase Change Materials

Amorphous   **Crystalline** 

'**0**' and '**1**'

Optically

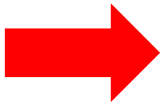
$R_{amorphous}$ **<<** $R_{crystalline}$

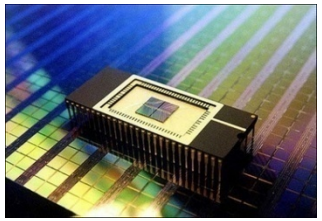


Optical Drive

Electrically

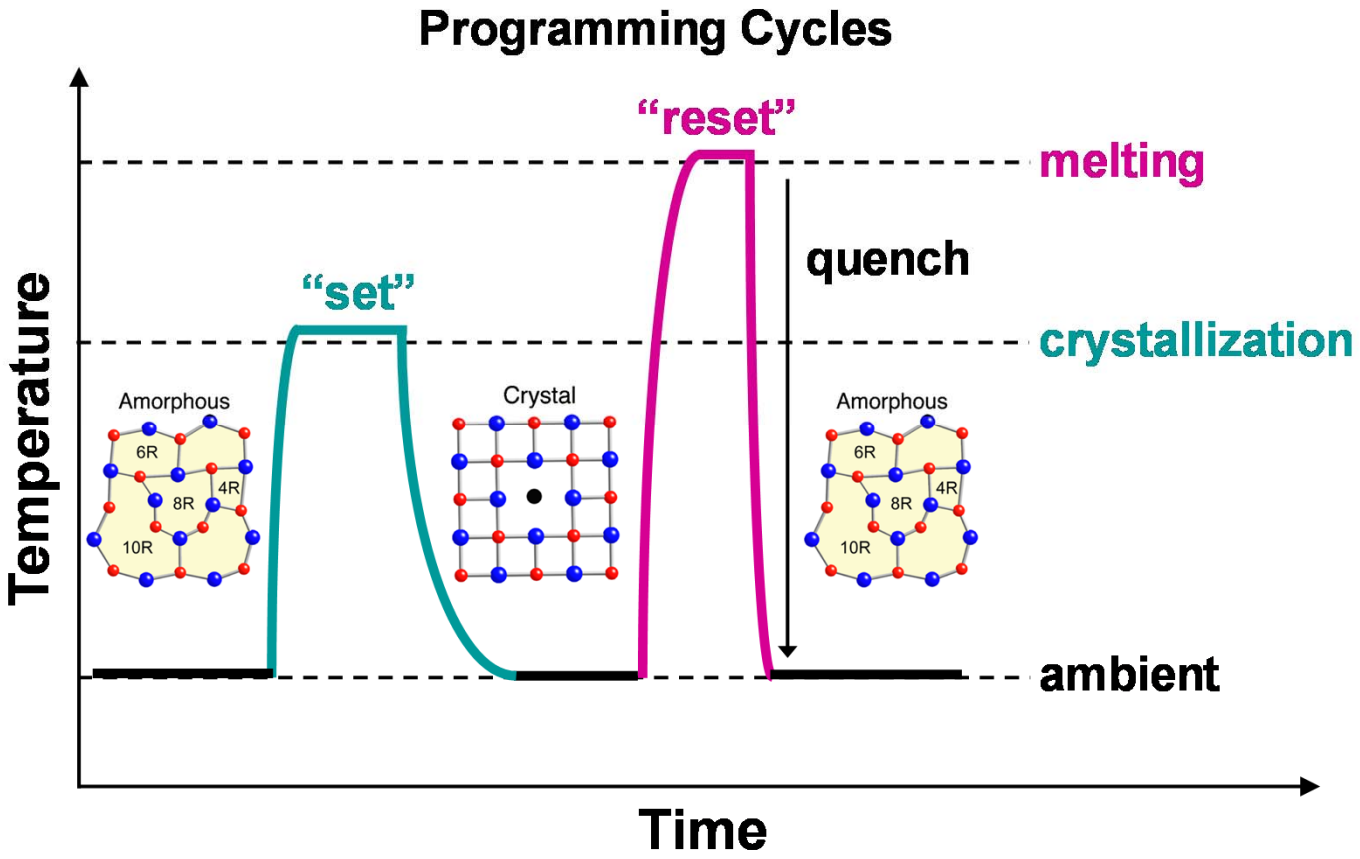
$\rho_{amorphous}$ **>>** $\rho_{crystalline}$





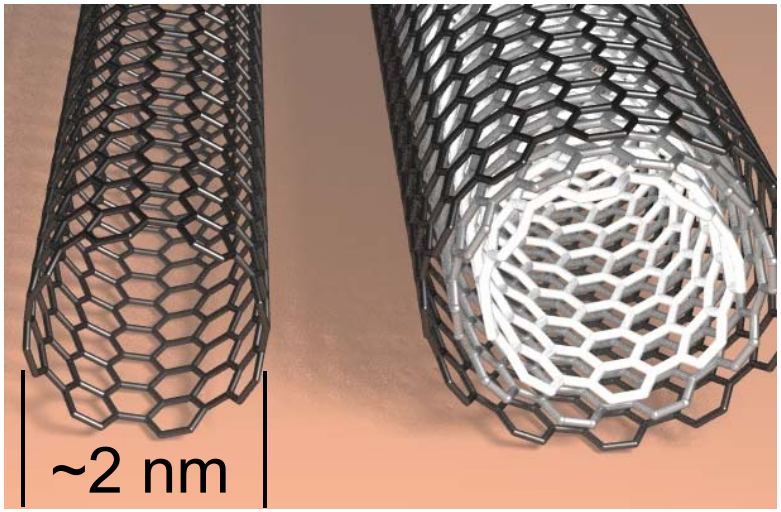
PCRAM

Phase Change Memory Working Principle

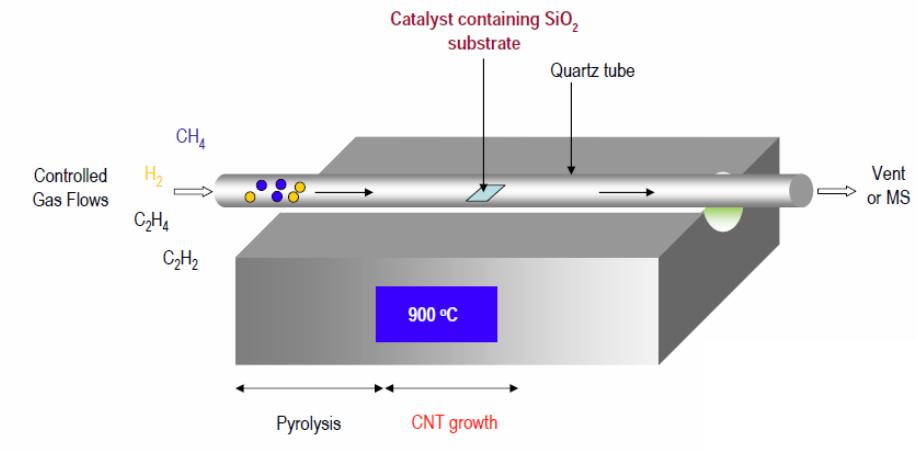


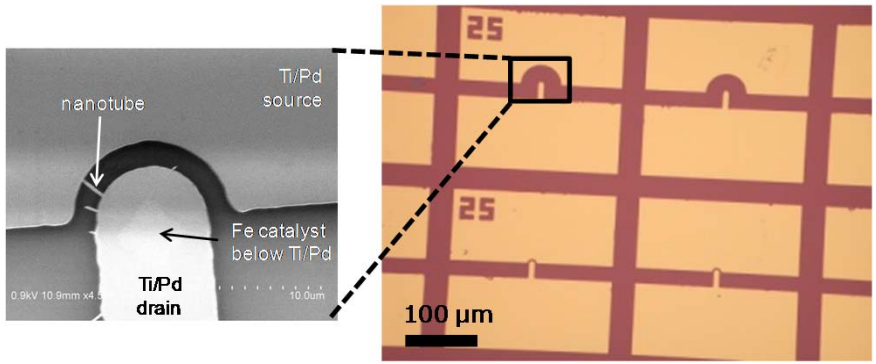
- "set": crystallization → data rate limiting (~10 ns)
- "reset": melt-quench → current and power limiting (>0.1 mA)

Carbon Nanotube Overview



- Carbon nanotubes → 1D cylinder of carbon atoms
- Excellent electrical properties
  - High mobility ~10^4 $cm^2V^{-1}s^{-1}$
  - Current density ~10^9 Acm^{-2} (~1000× of Cu)
  - No electromigration
- 1D heater – diameter 1~5 nm



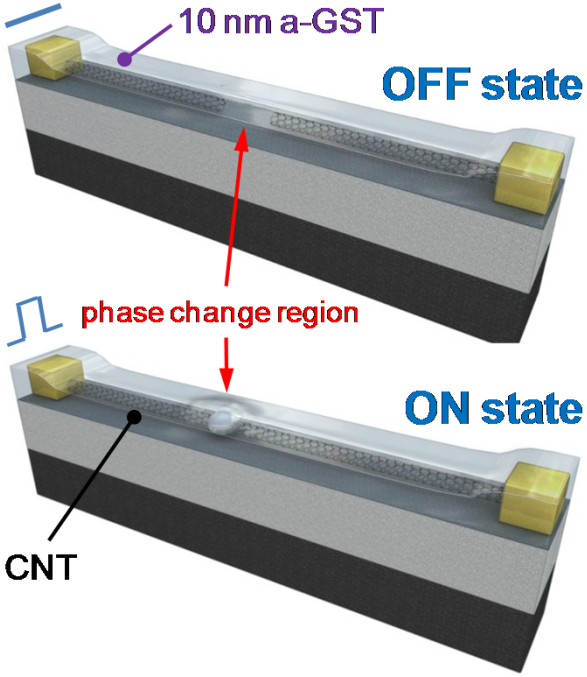


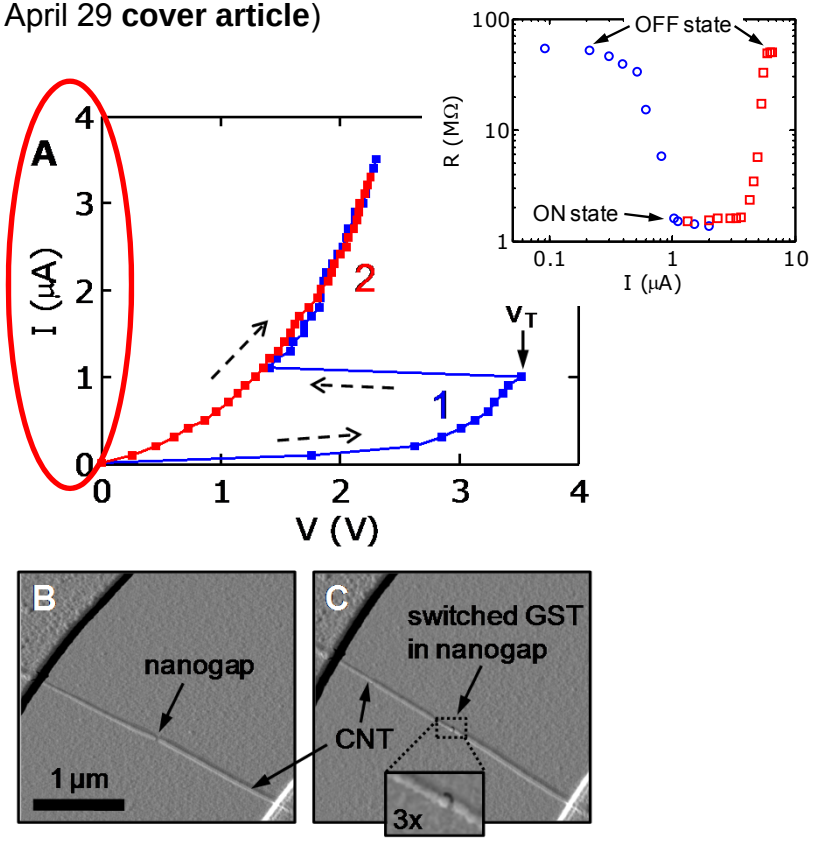
On-chip growth by Chemical Vapor Deposition (CVD)

A. Liao et al., *Phys. Rev. Lett.* (2008)

Nanotube – PCM Device

F. Xiong, A. Liao, D. Estrada, E. Pop, *Science* **332**, 568 (2011, April 29 **cover article**)



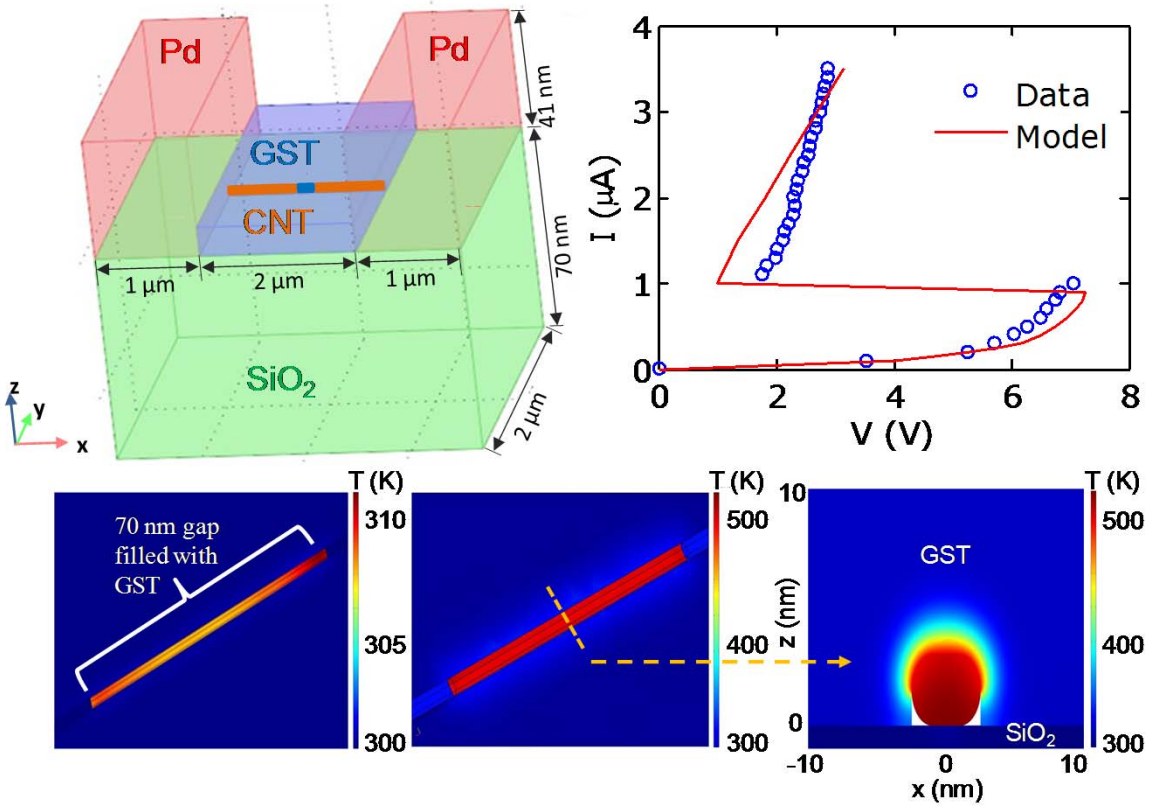


Patent TF11023 Filed

- Make CNT nanogaps by AFM or electrical "cutting"
- CNT nanogap filled with PCMs (here GST)
- I_{set} ~ 1 μA, I_{reset} ~ 5 μA **(~100× < conventional PCM)**

Modeling of Nanotube – PCM Device

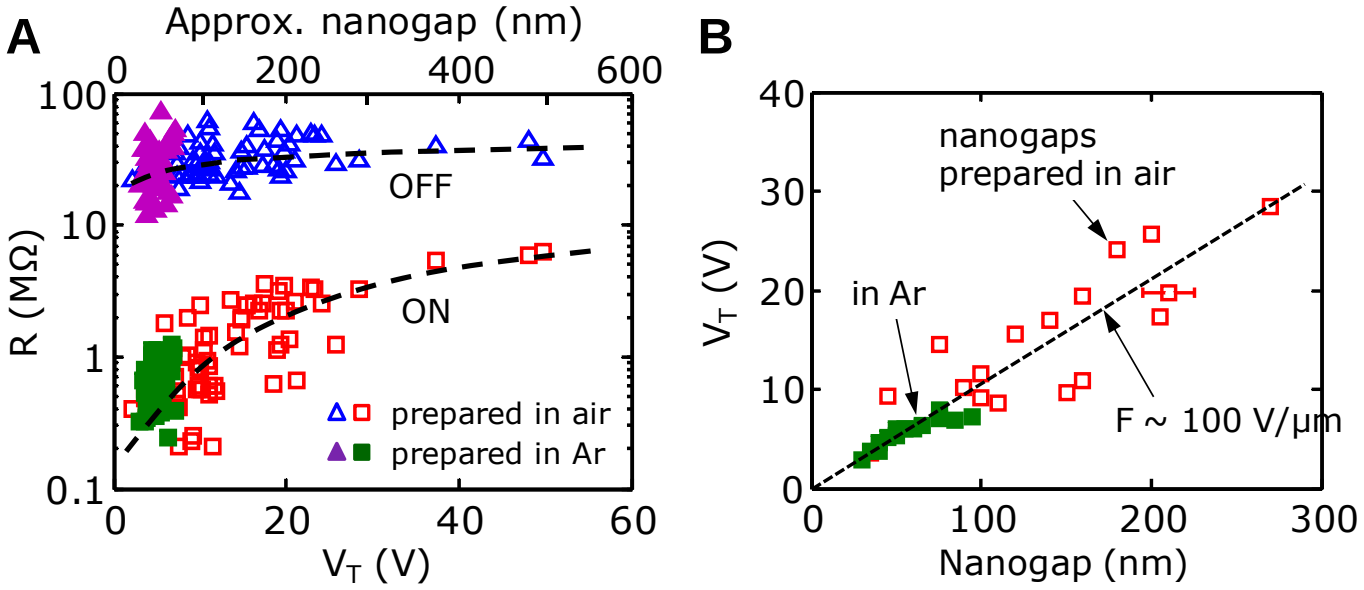
F. Xiong, A. Liao, D. Estrada, E. Pop, *Science* **332**, 568 (2011, April 29 **cover article**)



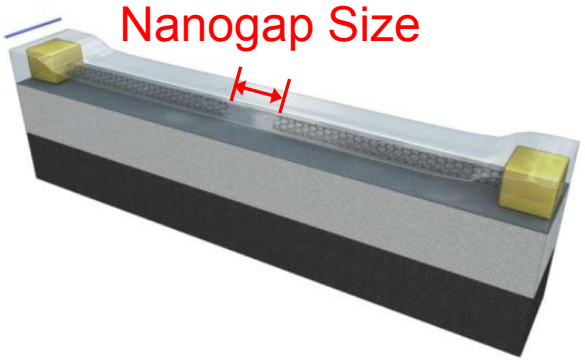
- Before switching, low current density → low ΔT
- After switching, high current density → high ΔT → crystallization
- Small volume of PCM bit ~70 × 2.5 × 2.5 nm^3 → 1 μA switching current

Scaling of Nanotube – PCM Devices

F. Xiong, A. Liao, D. Estrada, E. Pop, *Science* **332**, 568 (2011, April 29 **cover article**)

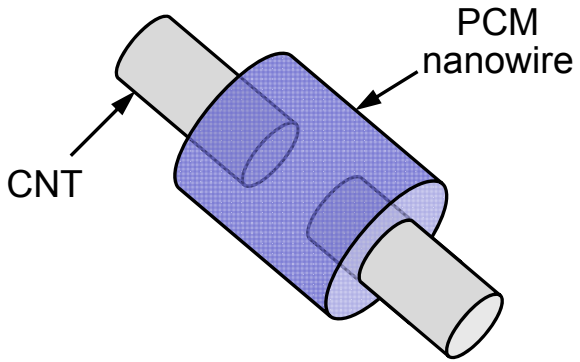


- Examined >100 devices
- Devices highly scalable with bit size
- Thresholds V_T ~ 3-10 V, currents I_{set} ~ 1 μA, I_{reset} ~ 5 μA **(~100× < conventional PCM)**



Where Do We Go From Here?

F. Xiong, M.-H. Bae, Y. Dai, A. Liao, A. Behnam, E. Carrion, S. Hong, D. Ielmini, E. Pop, *Nano Lett.* **13**, 464 (2013)



- How can we improve the PCM memory with nanotube electrodes?
- Create nanotube + nanowire device!

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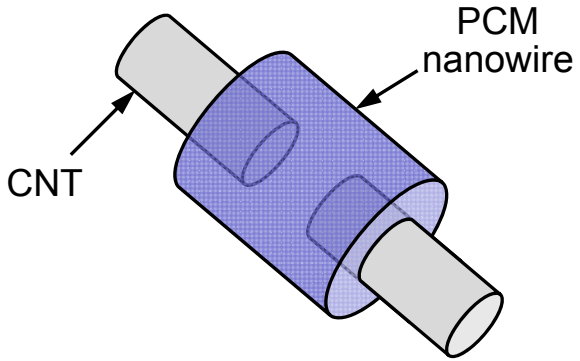

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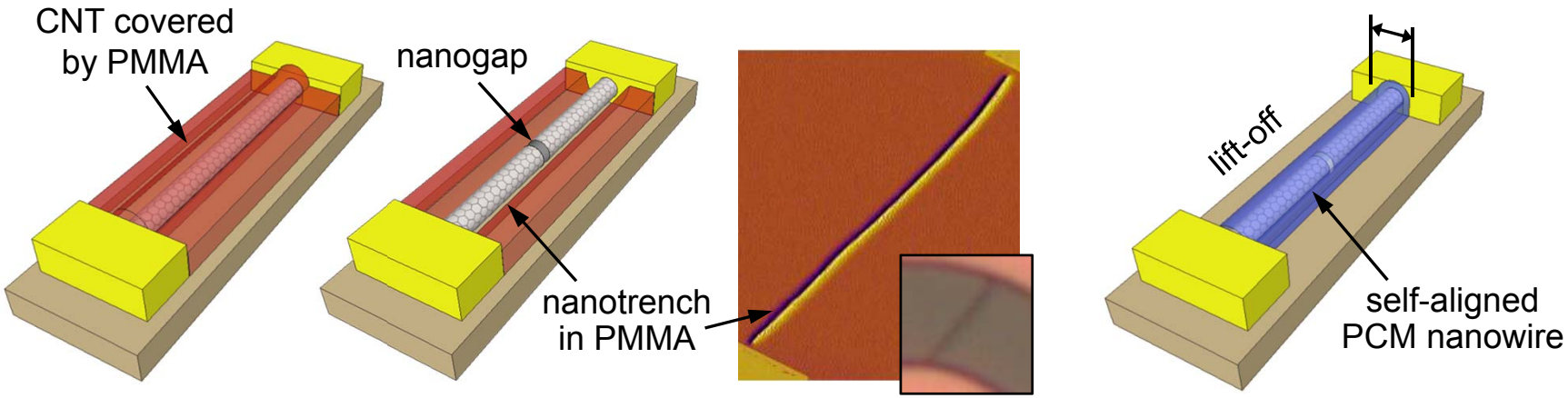
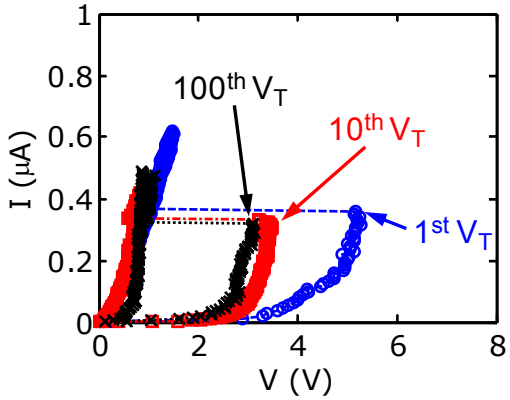


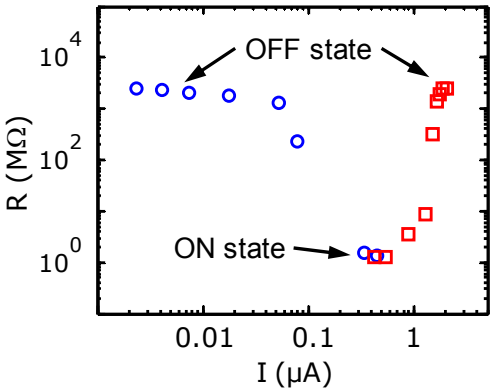
Patent TF11063 Filed

- CNT heats PMMA → creates nanotrench → deposit PCM → lift-off PMMA
- PCM **nanowire self-aligned with CNT** electrodes

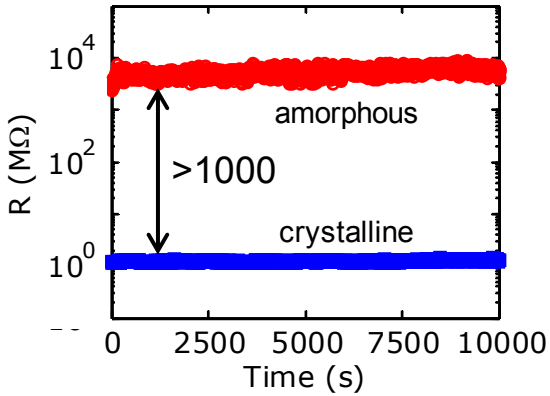
Self-Aligned Nanotube-Nanowire Devices

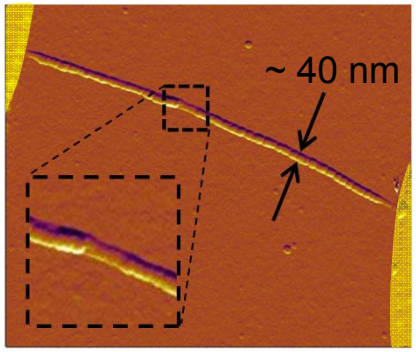
F. Xiong, M.-H. Bae, Y. Dai, A. Liao, A. Behnam, E. Carrion, S. Hong, D. Ielmini, E. Pop, *Nano Lett.* **13**, 464 (2013)





even lower power…
I_{set} ~ 0.4 μA
I_{reset} ~ 1.6 μA

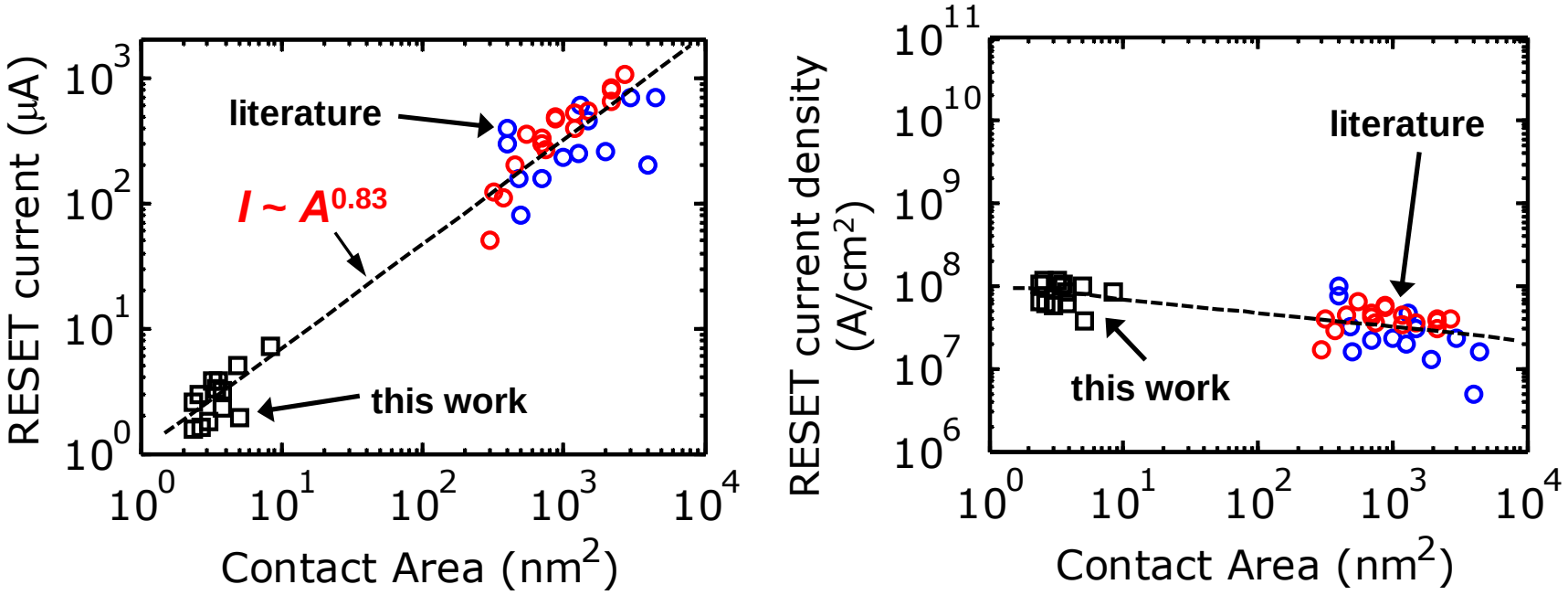




- Threshold voltage (V_T) shows some "burn-in"
- Excellent R_{OFF}/R_{ON} ratio (> 1000) approaches *intrinsic* GeSbTe limits
- Great platform to probe other materials, self-aligned DNA, molecules…

RESET Current Scaling

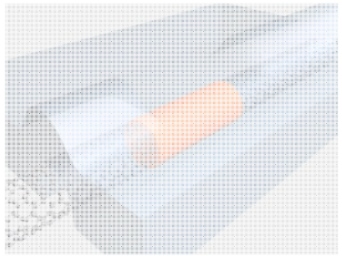
F. Xiong, M.-H. Bae, Y. Dai, A. Liao, A. Behnam, E. Carrion, S. Hong, D. Ielmini, E. Pop, *Nano Lett.* **13**, 464 (2013)

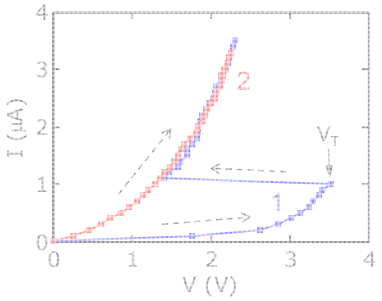


- $I_{reset} \sim A^{0.83}$
- CNT electrode → 100× reduction in I_{reset}
- Isotropic scaling (equal scaling of all three dimensions) → $I_{reset} \sim A^{1}$
- non-isotropic scaling → exponent of 0.83
- $I_{reset}/A \sim A^{-0.17}$ → higher current density as device scales

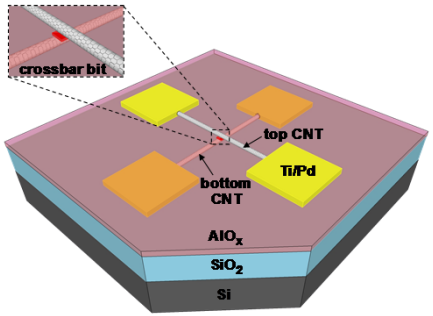
Outline

- Integrating CNT with PCMs
  - Phase change memory + CNT
  - Nanotube-PCM Device
  - Self-Aligned PCM Nanowire-Nanotube Device





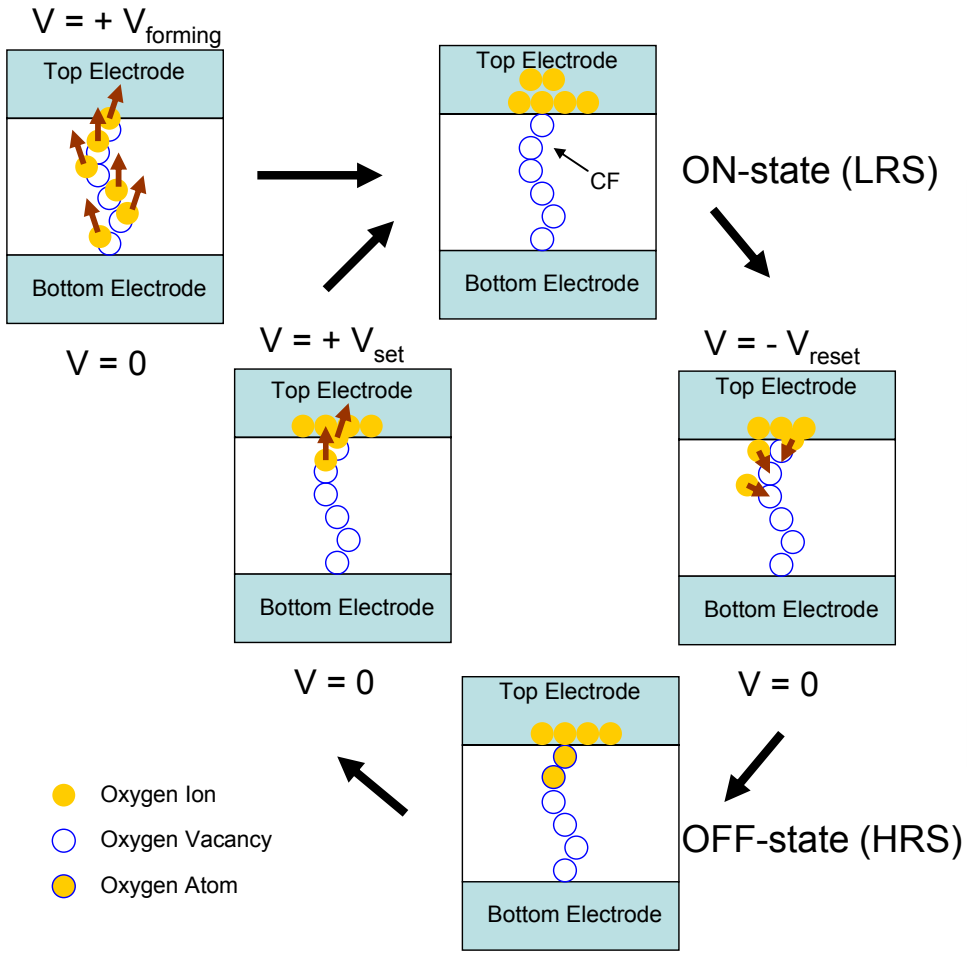
- CNT Crossbar RRAM
  - Resistive Random Access Memory
  - CNT Crossbar

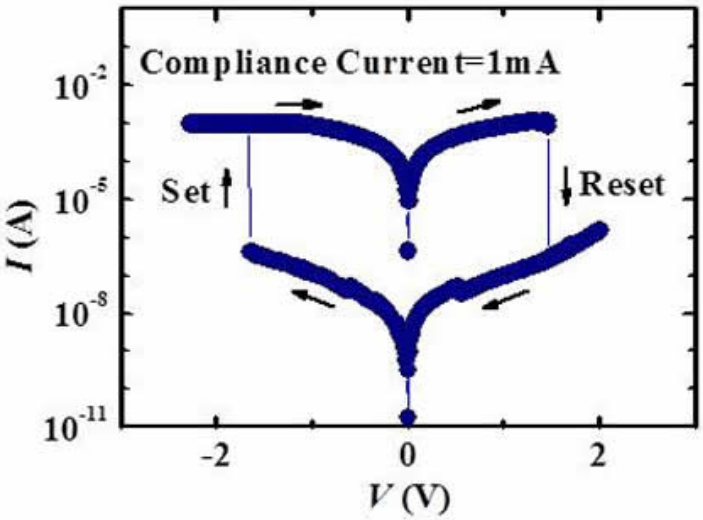


- Graphene Ribbons with PCM
  - 2D graphene ribbons
  - Scalable, flexible and inexpensive

- Summary

Resistive Random Access Memory



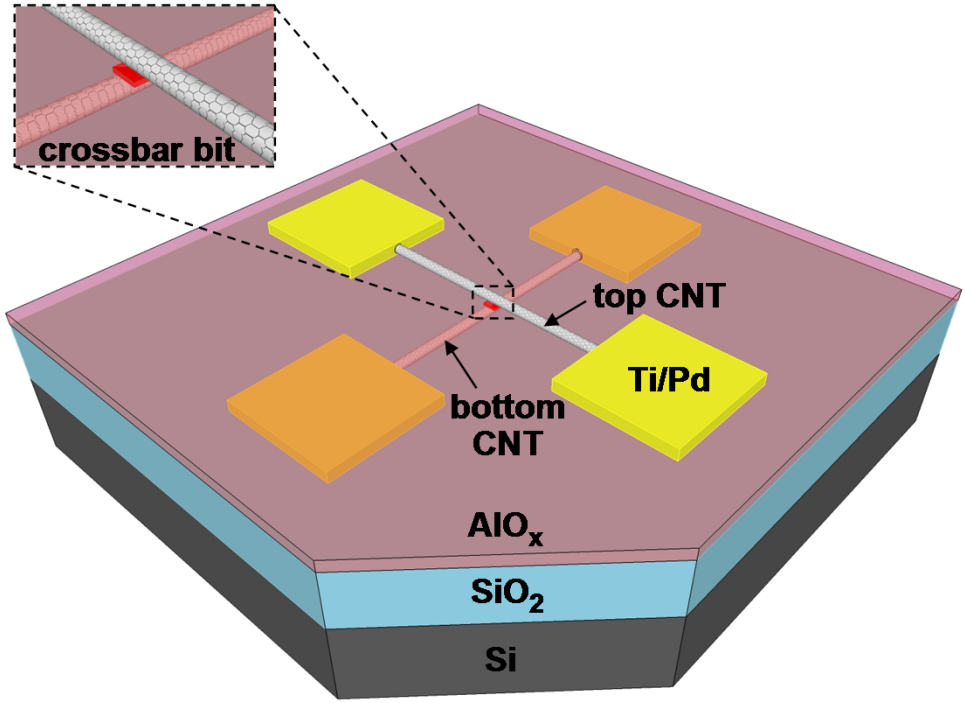


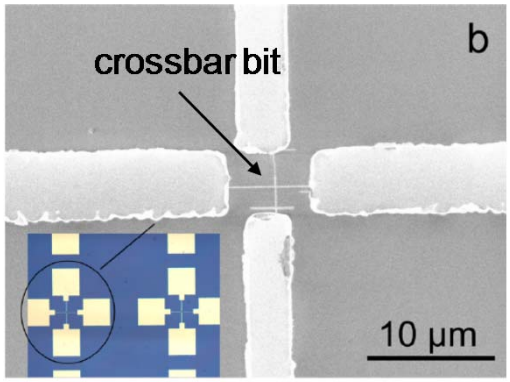
H.-S. P. Wong et al., *Proc. IEEE* (2012)

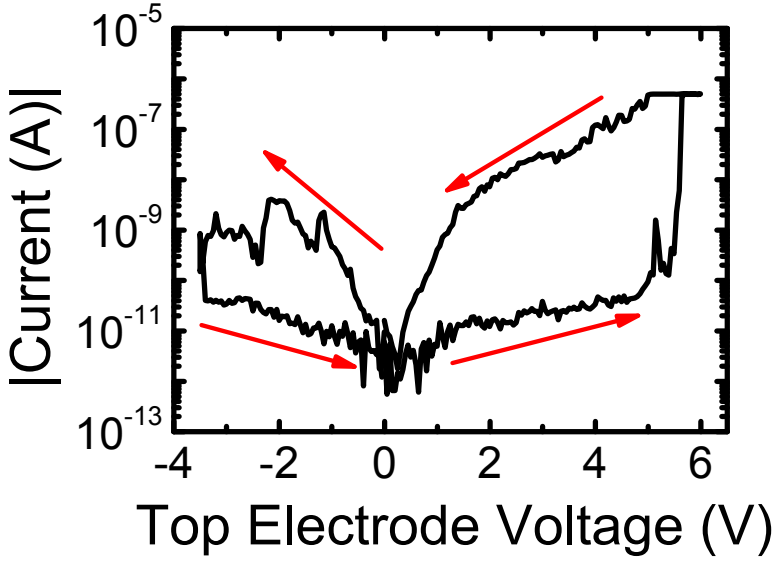
- Metal oxides (AlO_x, HfO_x, TiO_x)
- Movement of oxygen ions in E-field

CNT Crossbar RRAM

C.-L. Tsai, **F. Xiong**, E. Pop, M. Shim, *ACS Nano* **7**, 5360-5366 (2013)



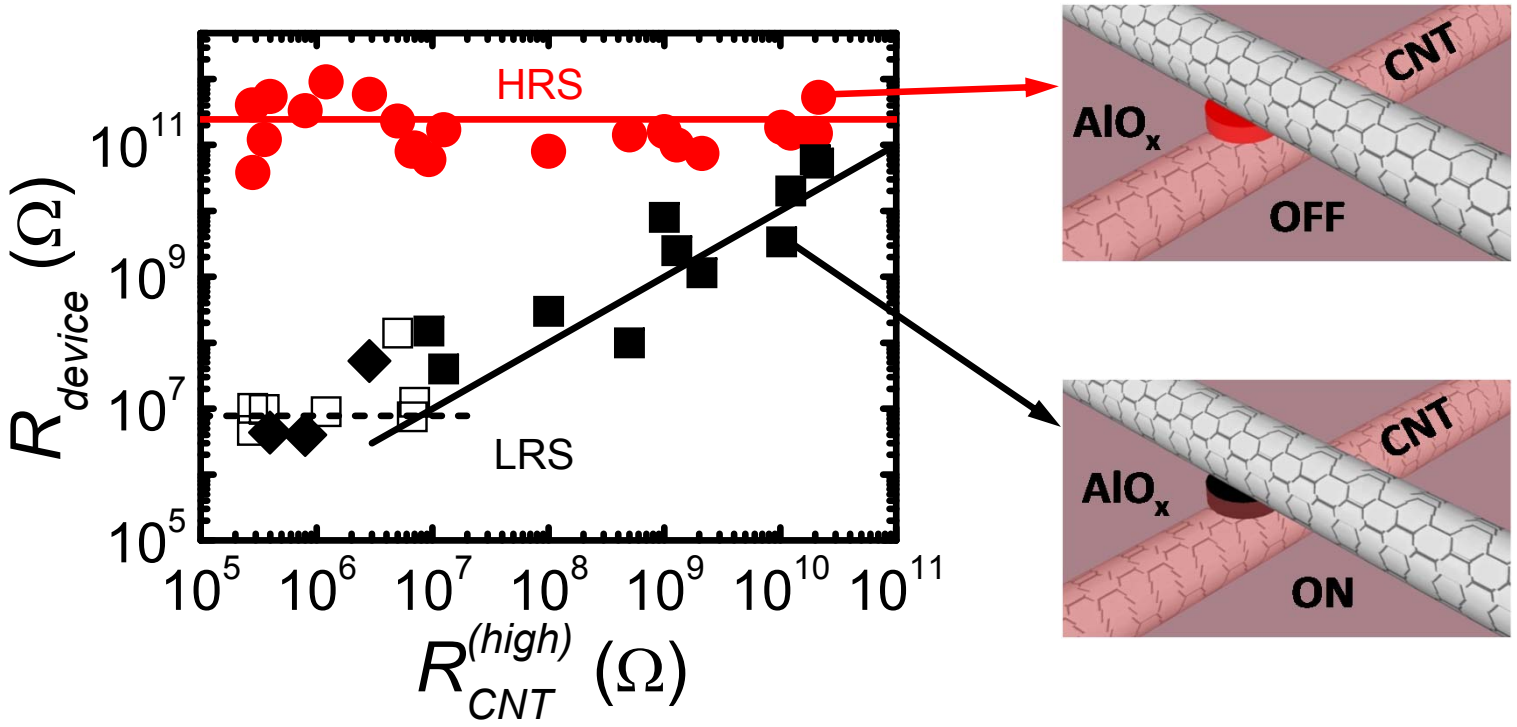




- CNT crossbar electrodes ~ 2 nm^2
- High performance and low power

CNT Crossbar RRAM

C.-L. Tsai, **F. Xiong**, E. Pop, M. Shim, *ACS Nano* **7**, 5360-5366 (2013)



$$R_{device} = R_{AlOx} + R_{CNT} + R_{contact}$$

- High-resistance-state (HRS) dominated by OFF state AlO_x bit
- Low-resistance-state (LRS) scales with CNT resistance to ~ 10 MΩ

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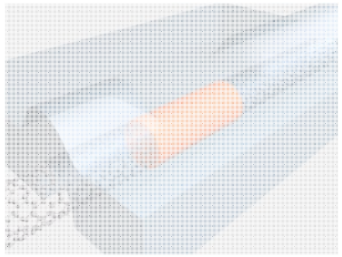

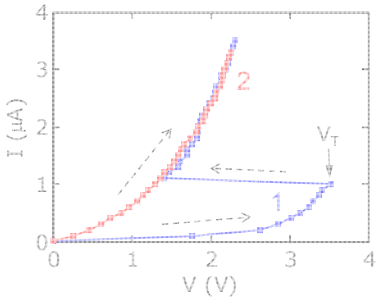

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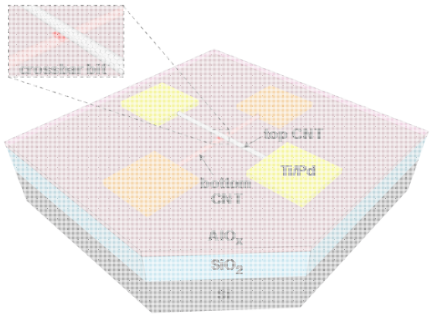

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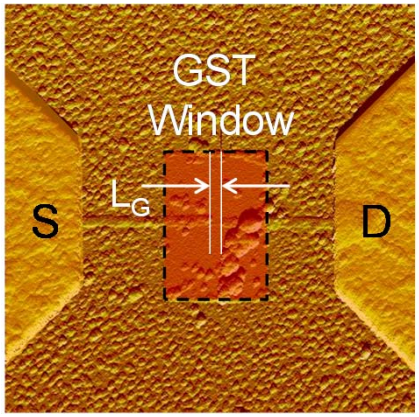
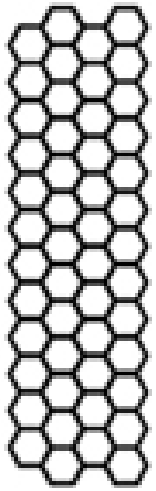
  - 2D graphene ribbons
  - Scalable, flexible and inexpensive



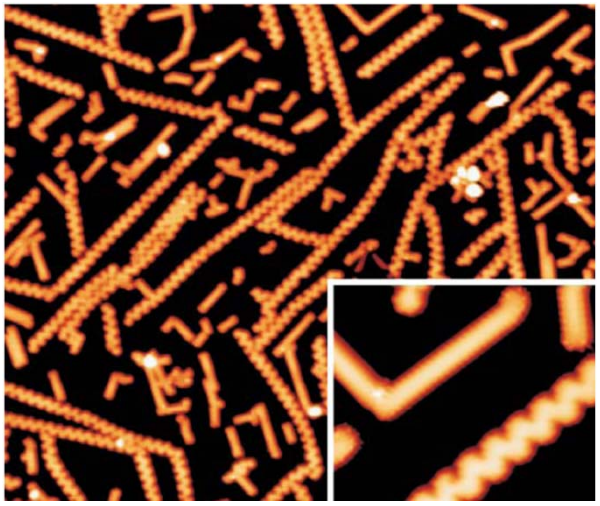
- Summary

2D Graphene Ribbons instead of 1D CNTs?

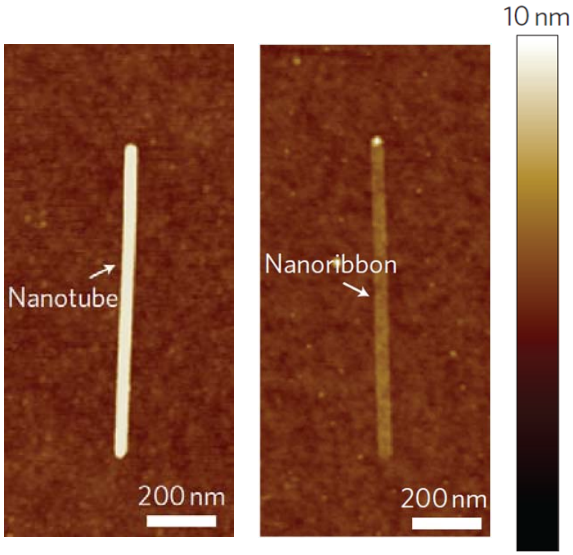
- Graphene Ribbons (GRs) as building blocks:
  - Interconnects: High current capacity, good scalability and flexibility
  - Transistors: Semiconducting (<10 nm width)
  - Sensors: High chemical sensitivity



X. Li, et al., *Science* (2008).

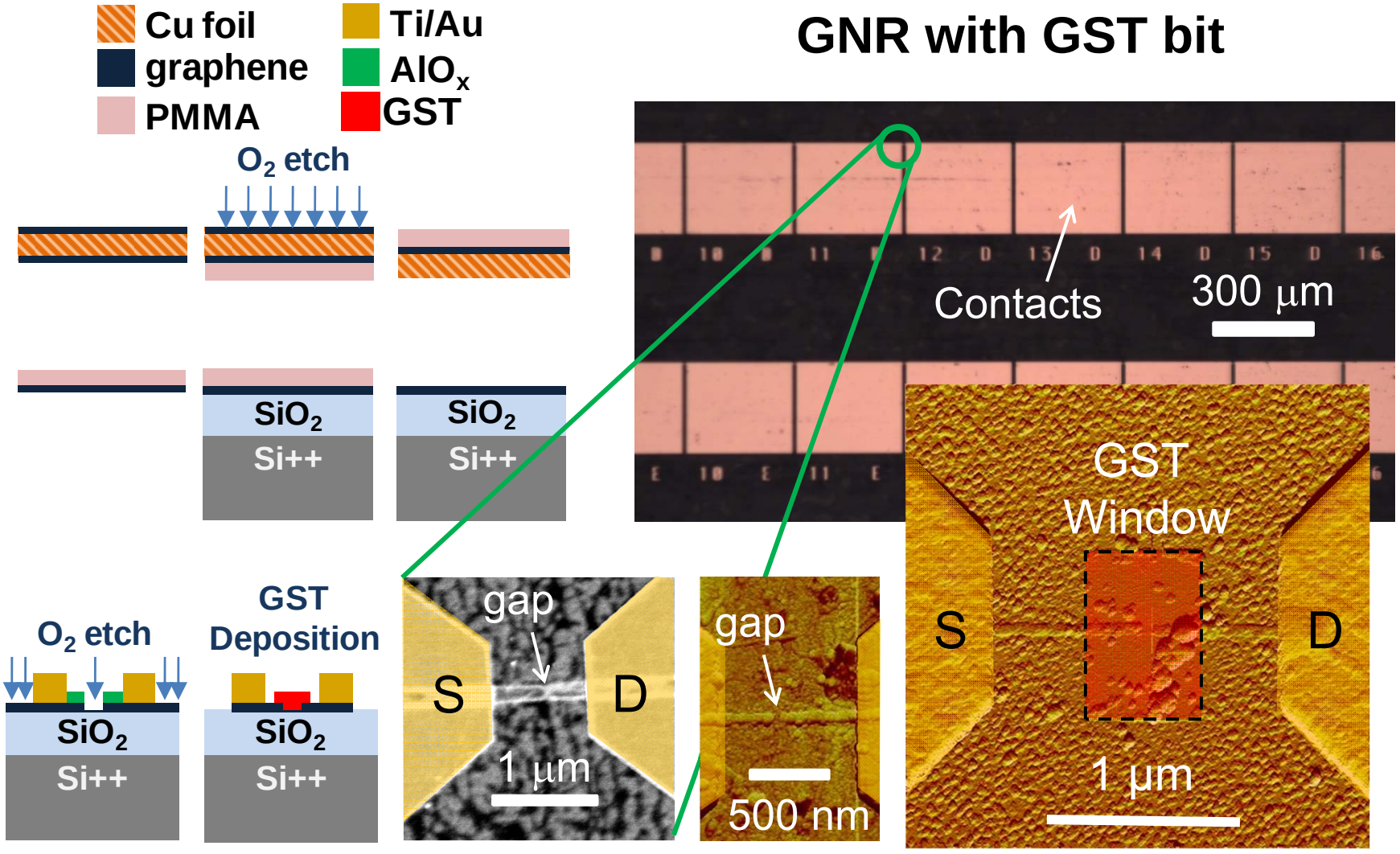


J. Cai, et al., *Nature* (2010).



L. Jiao, et al., *Nat. Nanotechnol.* (2010).

Graphene-PCM Schematics

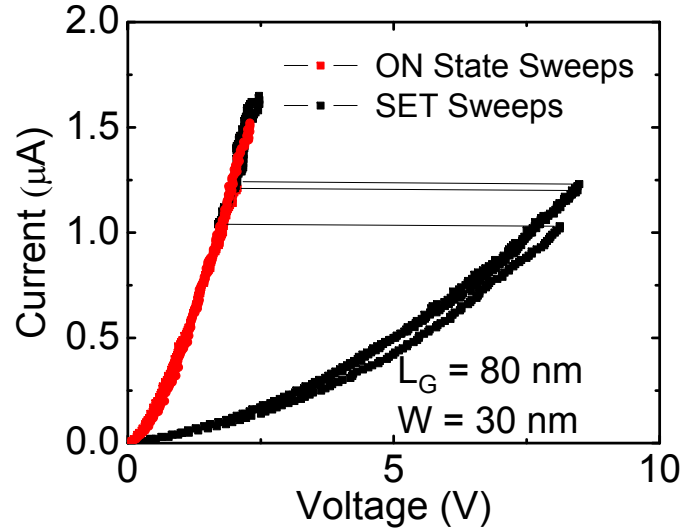


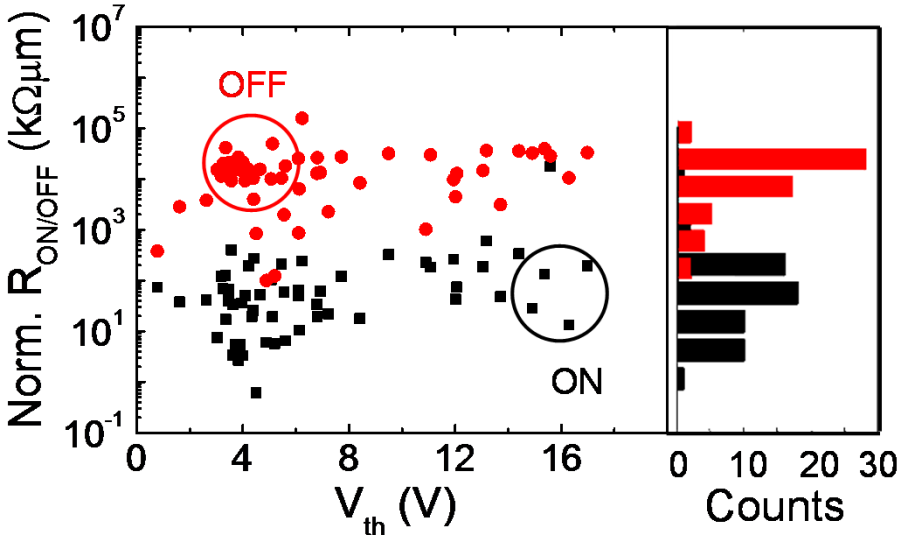
A. Behnam, et al., *Nano Lett.* **12**, 4424 (2012)
A. Behnam, **F. Xiong**, et al., in review (2014)

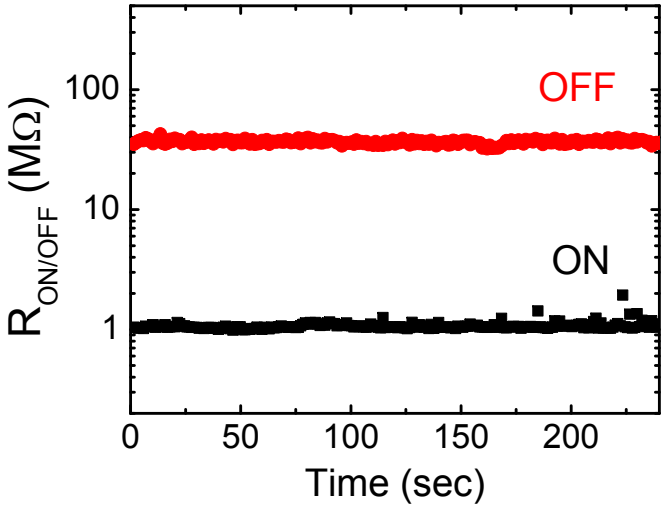
L = 2 μm, W = 40 nm, L_G = 70 nm

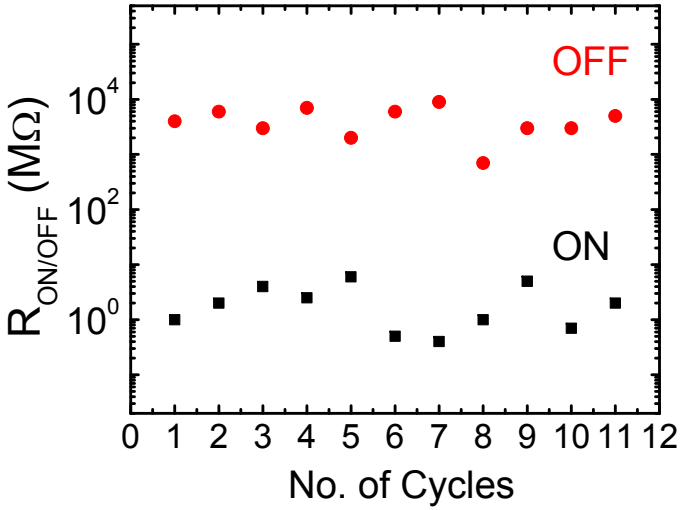
Graphene-PCM Device Characteristics

A. Behnam, **F. Xiong**, et al., in review (2014)



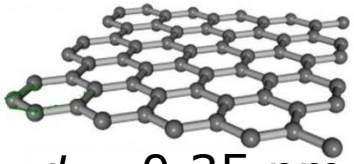






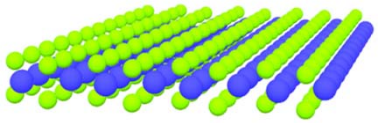
Two-Dimensional Materials

Graphene



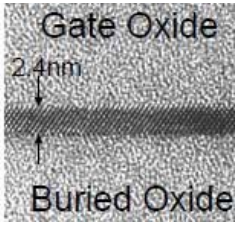
d ~ 0.35 nm

MoS_2

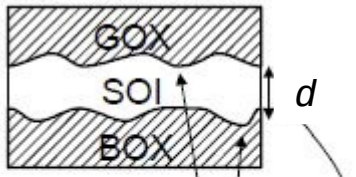


d ~ 0.65 nm

Silicon on Insulator (SOI)



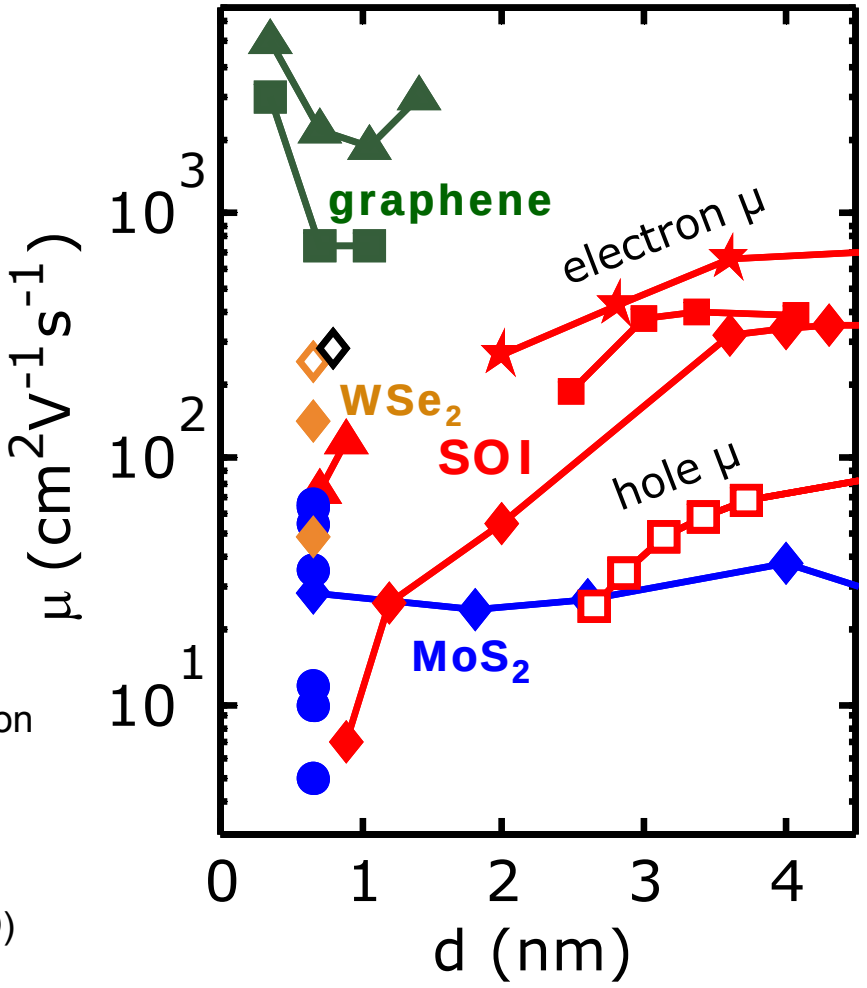
K. Uchida et. al. (2003)



Interface roughness

Thickness fluctuation

- **Layered materials** (on SiO_2 at T = 300 K)
  - Graphene
    - $\mu \approx 1000 - 5000$ $cm^2V^{-1}s^{-1}$
  - Transition Metal Dichalcogenides (TMD)
    - MoS_2, $MoTe_2$, WS_2, WSe_2
    - μ (TMD) $\approx 10 - 250$ $cm^2V^{-1}s^{-1}$
- **Silicon on Insulator (SOI)**
  - μ degradation below $d \approx 4$ nm
  - Poor hole mobility



[1] K. Nagashio et. al. (2009)
[2] W. Zhu et. al. (2010)
[4] K. Cheng, et. al. (2009)
[5] K. Uchida et. al. (2003)
[6] M. Schmidt et. al. (2009)
[6] Liu, et. al. (2013)
[7] Fang, et. al. (2013)
[8] Jariwala, et. al. (2013)
[9] Kis, et. al. (2012)
[10] Sangwan, et. al. (2013)

Contact Resistance to MoS_2

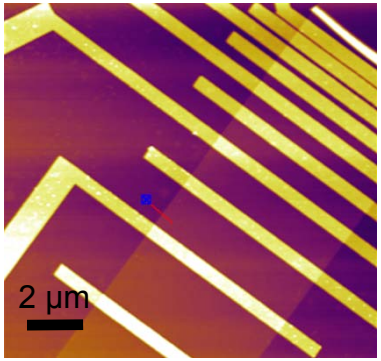
C. English, et al., *DRC* (2014) and submitted (2014)

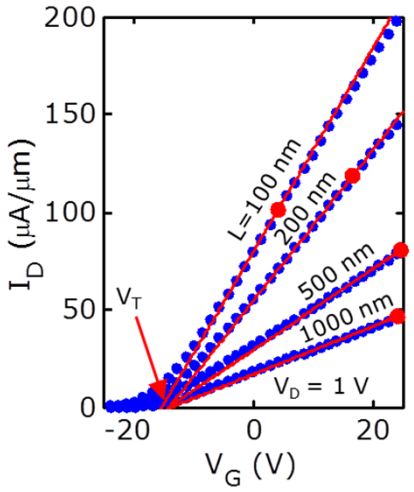
Systematic study of contact resistance (R_C)

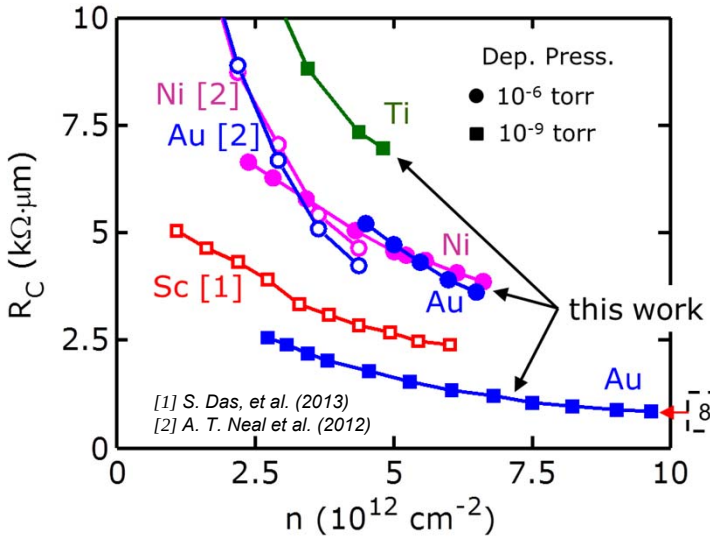
-Various contact metals: Ni, Ti, Au

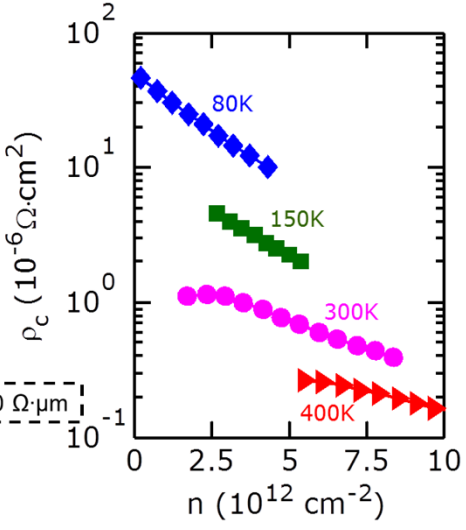
-Different metal deposition pressures P_D = 10^{-6} Torr, 10^{-9} Torr

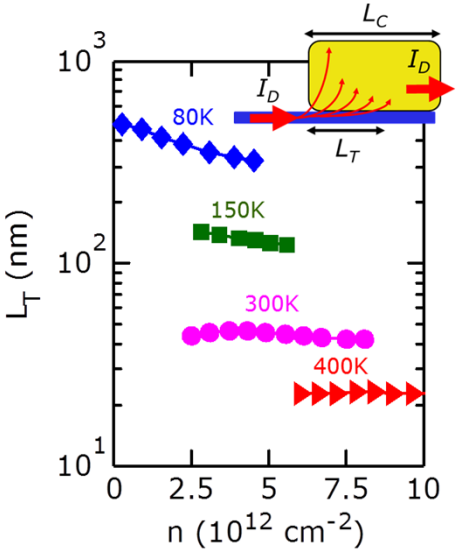
TLM







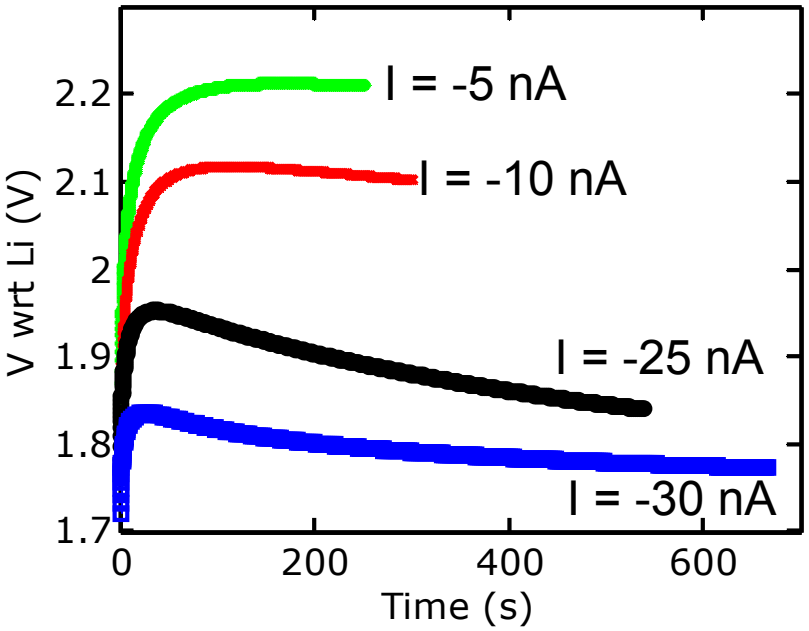




- Lower deposition pressure (P_D = 10^{-9} Torr) yields 3X improvement for Au contacts

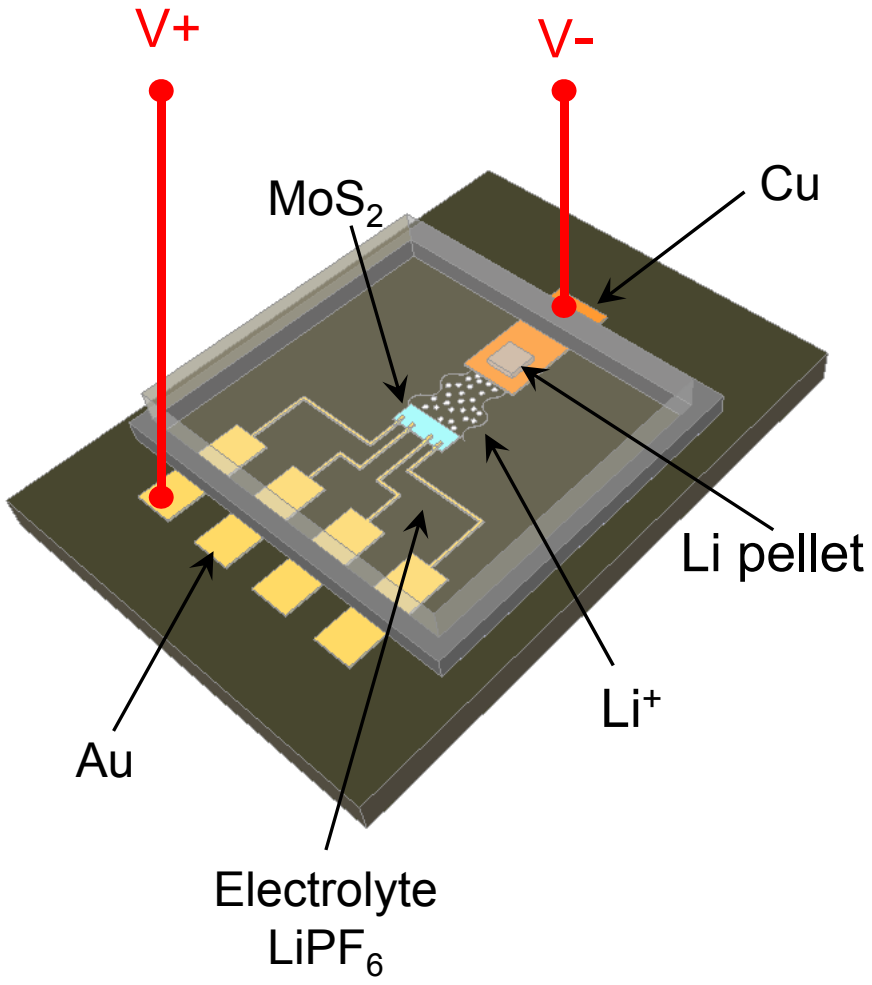
- $\rho_C \approx 5\text{x}10^{-7}$ Ω·cm^2 at T = 300 K
- $L_T \approx$ 50 nm at T = 300 K

In-situ Li Intercalation in MoS_2

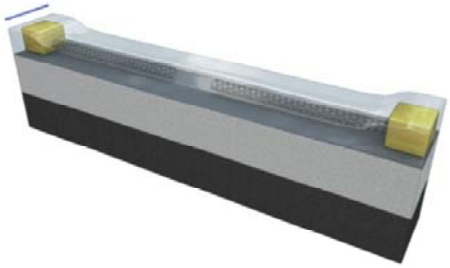


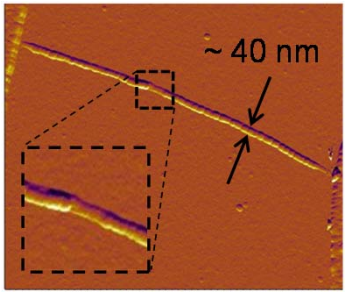
- In-situ lithiation via electrochemical process
- Explore reversible Li_xMoS_2 properties
  - optical, electrical, thermal, thermoelectric

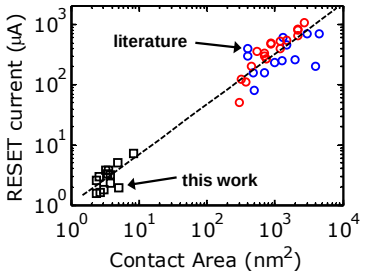
Lithiation / Delithiation

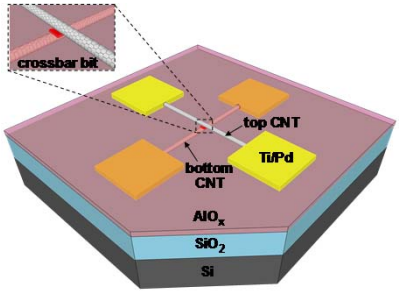


Summary









- Integration of CNT and PCMs
- Nanotube-PCM Device
  - 100× lower programming current/power
  - Device scaling
  - Supported by FEM
- Self-Aligned Lithography-Free Technique
  - Improve device performance
  - High on/off ratio and better endurance
- CNT Crossbar RRAM
  - High performance and low power
- Graphene-PCM Device
  - Scalable, flexible and CMOS compatible
  - Proof-of-concept

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- Cui Group
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