STANFORD UNIVERSITY

Tuning the threshold voltage of carbon nanotube transistors for flexible, CMOS circuit

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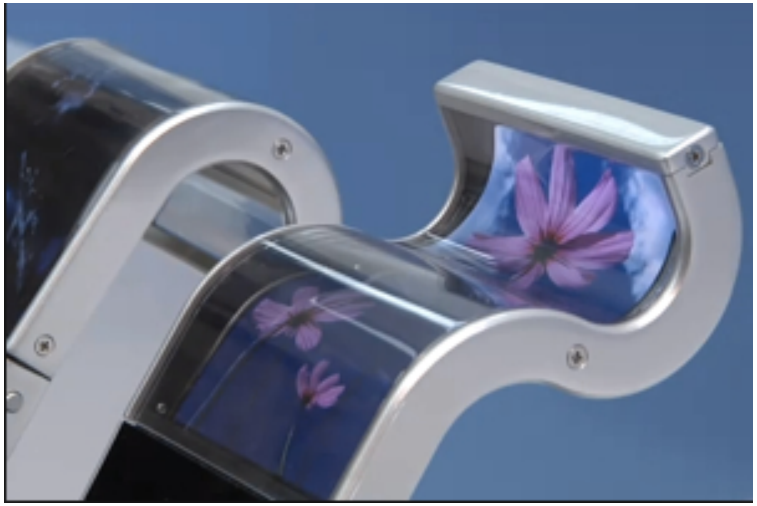
Department of Materials Science and Engineering
Stanford University

BAO RESEARCH

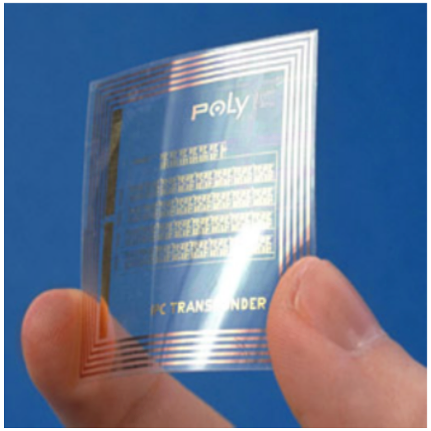
Motivation for flexible electronics

Foldable E-paper display



Bendable phone screens

Artificial skins

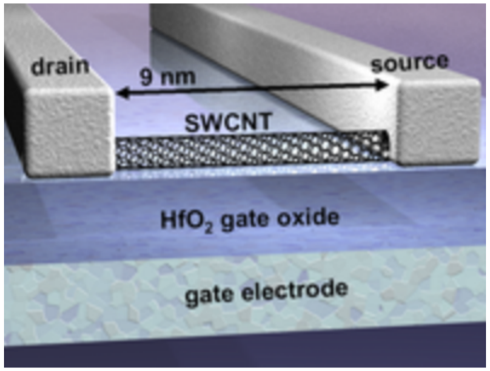


RFID

Wearable electronics

Motivation of carbon nanotubes

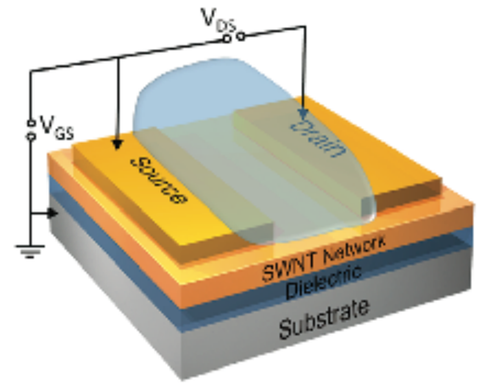
Transistors

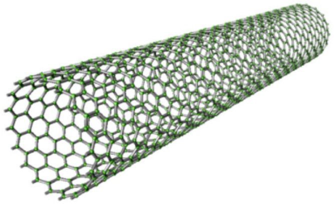


High Mobility

High Surface Area

Sensors

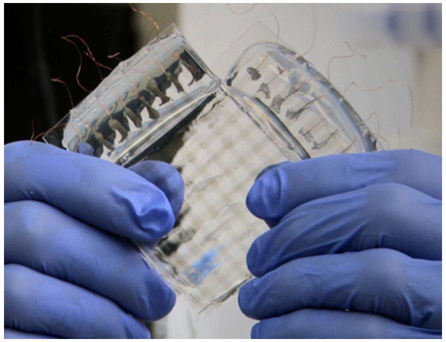




Single-walled Carbon nanotubes (SWNTs)

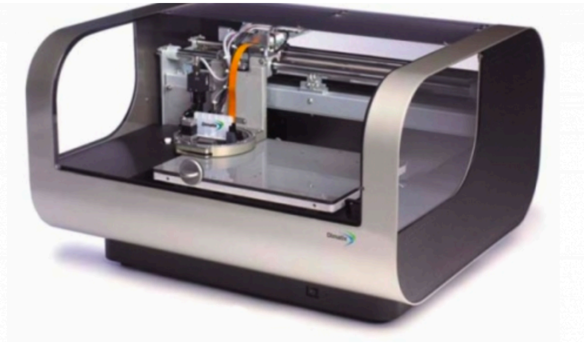
Stretchable electrode

Flexible / Stretchable



Solution Process

Printed electronics



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Technological Challenges

- Challenge #1: SWNTs synthesized as a mixture of metallic and semiconducting tubes,

Aim: only semiconducting SWNTs needed

- Challenge #2: Uncontrolled threshold voltage for lower-power, reliable circuit

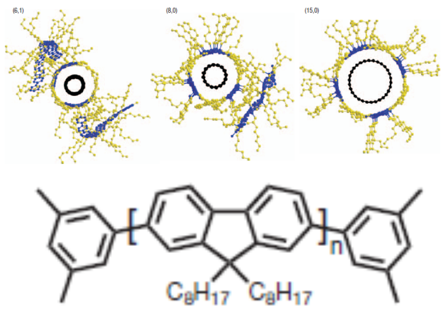
Aim: symmetrical p-type and n-type device

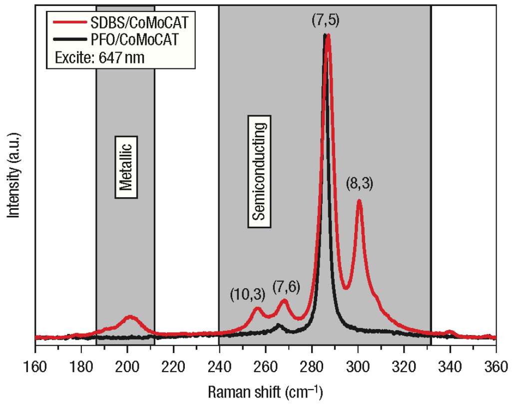
- Challenge #3: Shifts in the threshold voltage of device from previous voltage bias effect

Aim: Stable threshold voltage of device during operation

Sorting carbon nanotubes by polymers

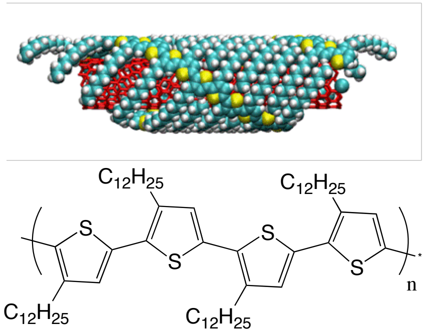
Sorting by Polyfluorene

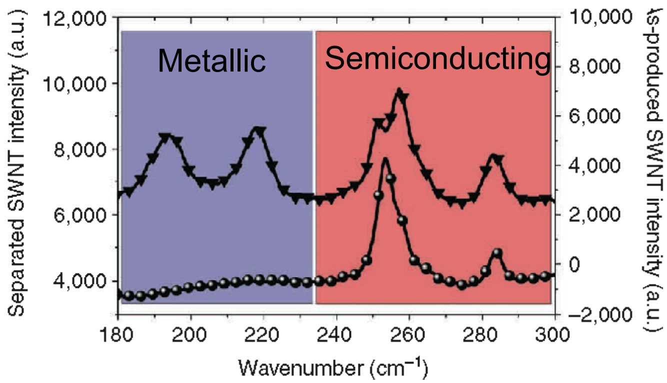


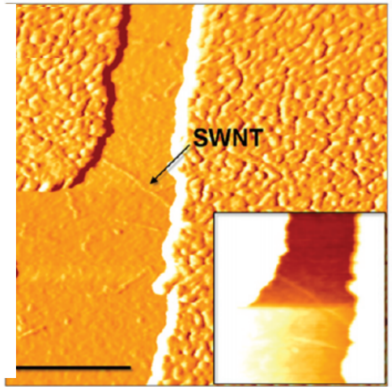


Nish *et. al.*, ***Nat. Nanotechnol.***, 2007, 2, p640-6

Sorting by Polythiophene







*H.W.Lee, **H.Wang**. Z.Bao et. al.*, ***Nat. Communication****, 2011*, 2, 541

*S. Park, **H. Wang**, Z. Bao et al.*, ***ACS Nano***, 2012, 6, 2487.

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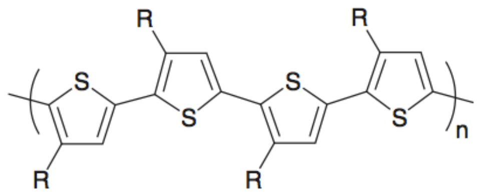
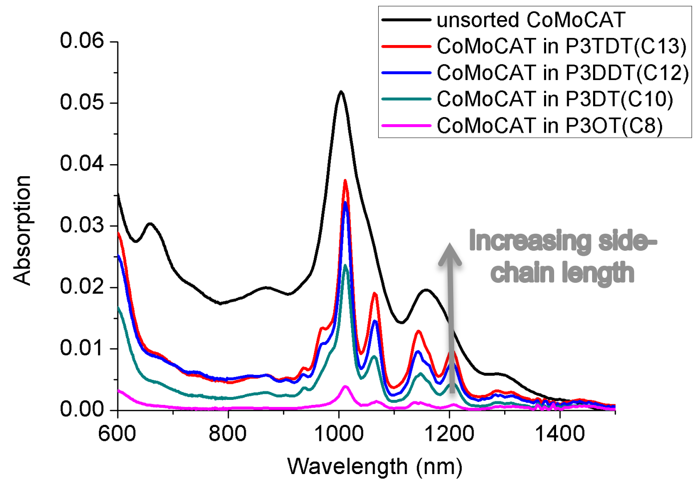
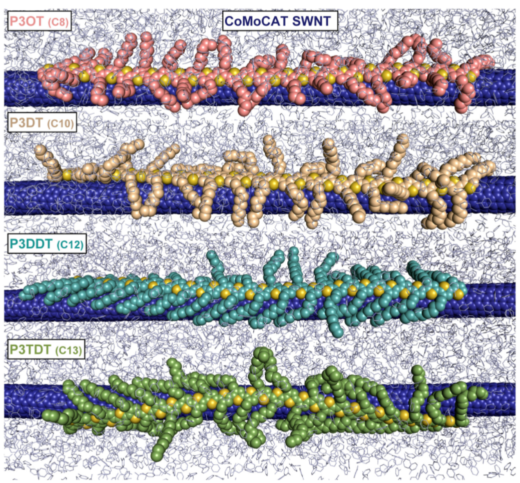
Polymer side-chain effects

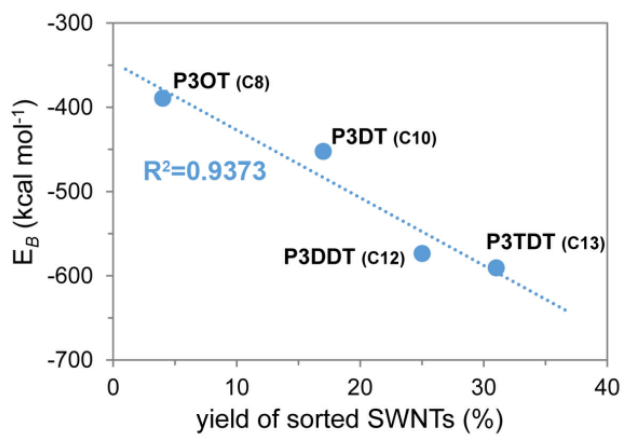


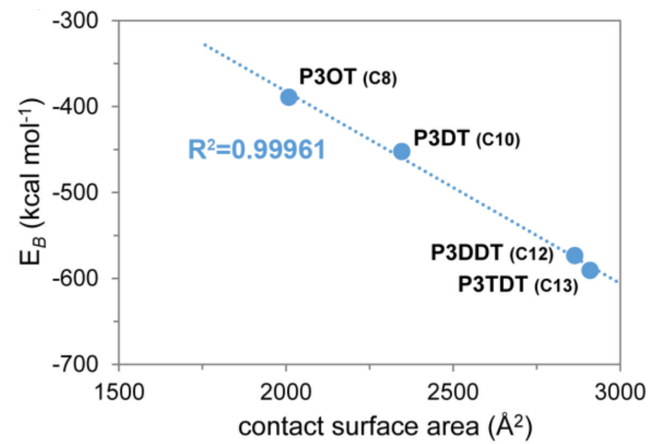
rr-P3At

R = 8, 10, 12, 13









***H.Wang**, K.N.Houk, Z.Bao et. al., **ACS Nano**, 2014,* 3, 2609-2617

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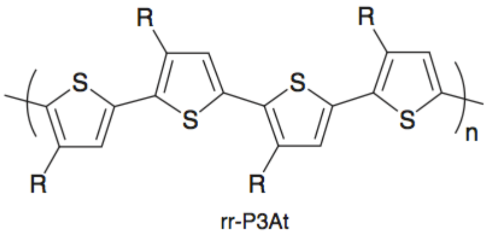
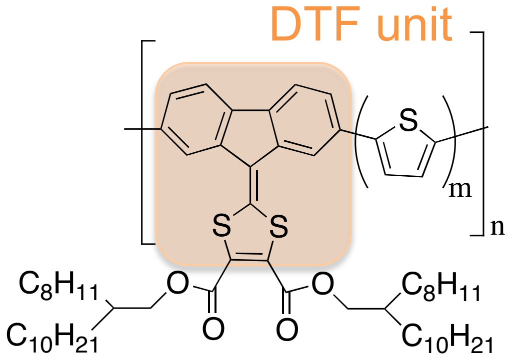
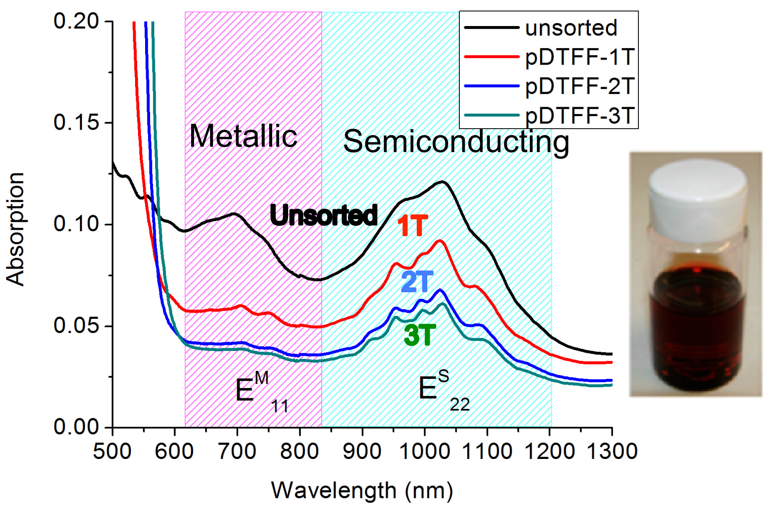
Polymer backbone effects for large-diameter SWNTs

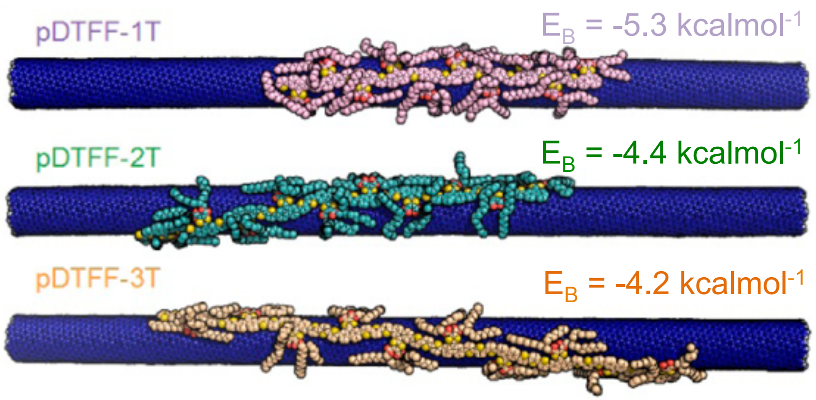


large-plane polymer



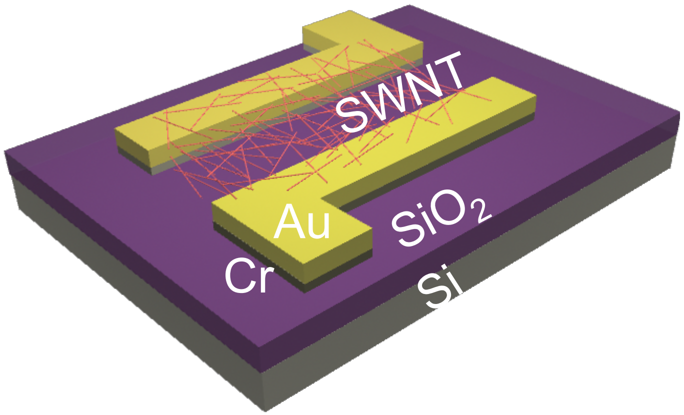
PDTFF-***m***T m = 1,2,3

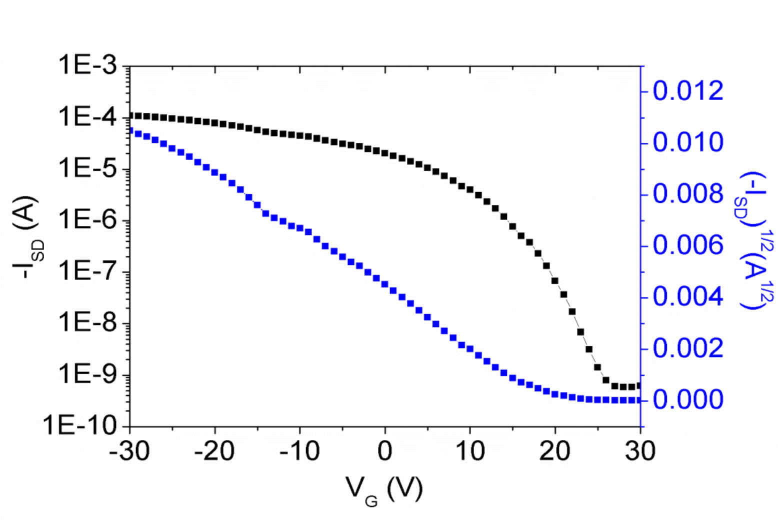


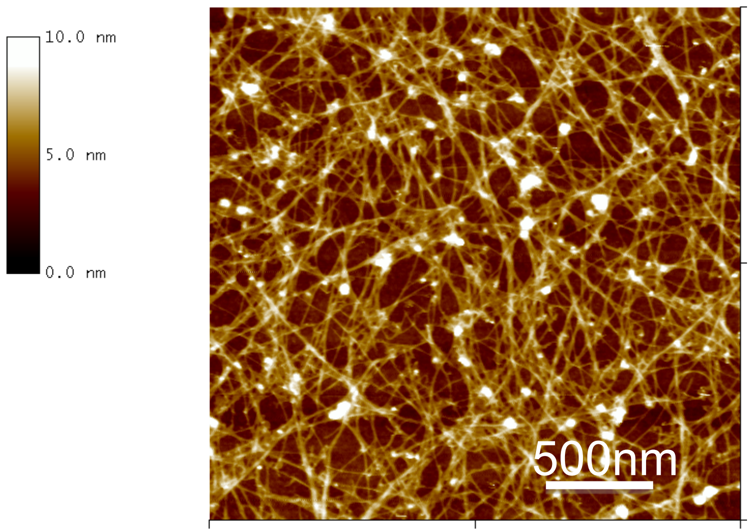


H.Wang, *K.N.Houk, Z.Bao et. al.*, ***ACS Nano***, *2013*, 3, 2659-2668

Transistor performance of our sorted tubes







mobility: up to 12 cm^2 / Vs
on/off ratio: 10^6

H.W.Lee, ***H.Wang****. Z.Bao et. al.*, ***Nat. Communication***, *2011*, 2, 541
H.Wang*, Z.Bao et. al.*, ***ACS Nano***, *2013*, 3, 2659-2668
H.Wang*, Z.Bao et. al.*, ***ACS Nano***, *2014*

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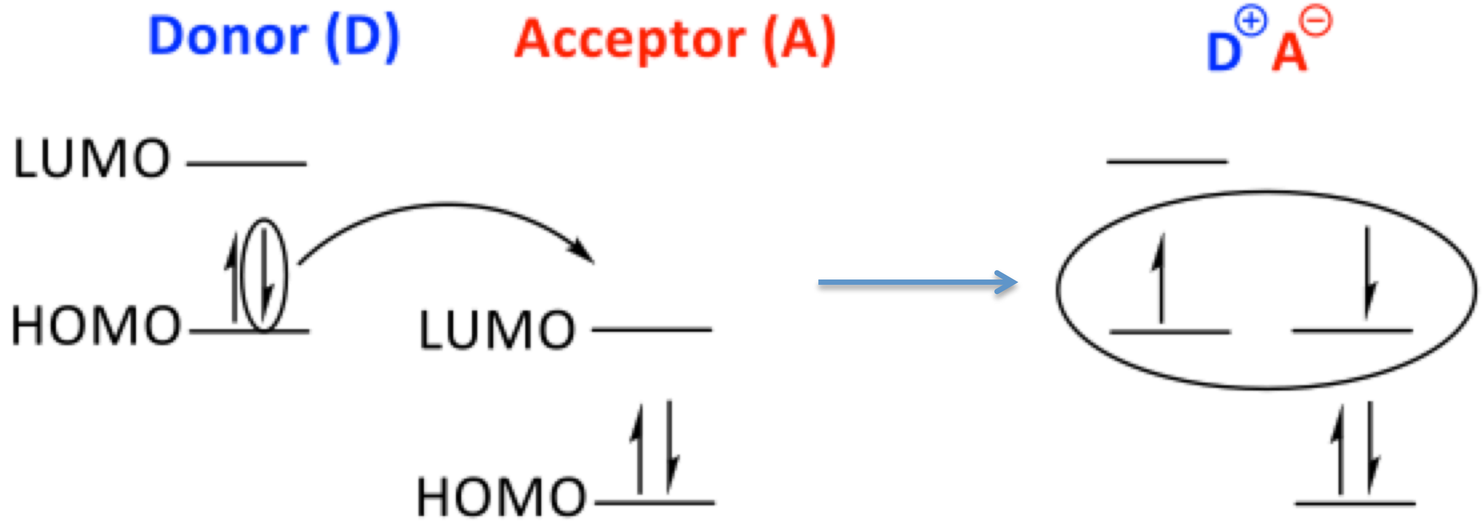
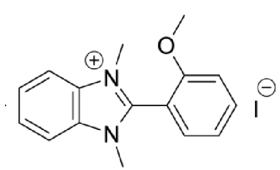
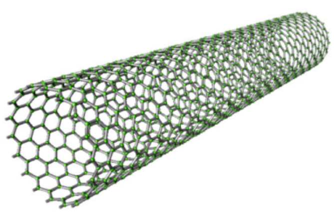
Aim: Stable threshold voltage of device during operation

Doping of organic semiconductors



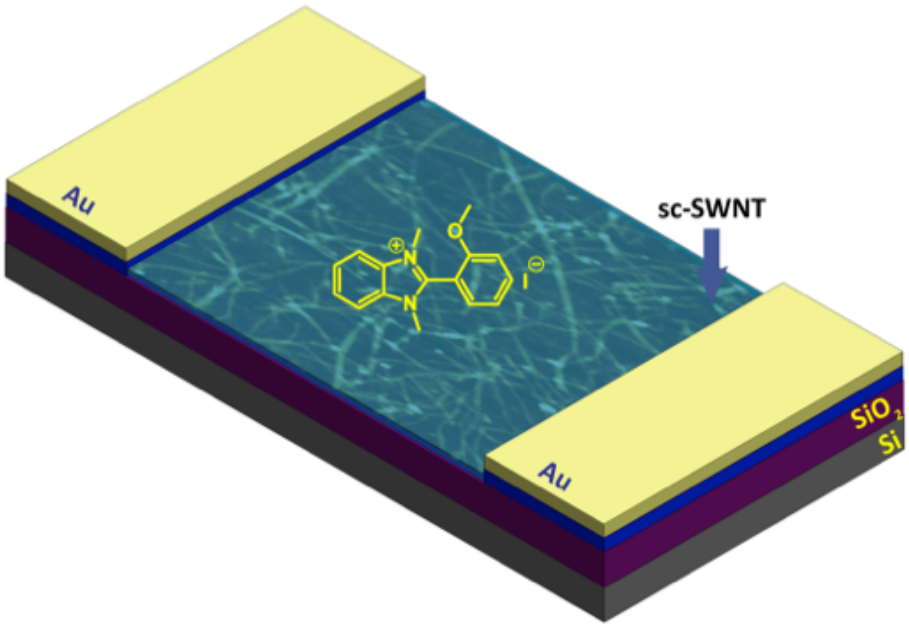


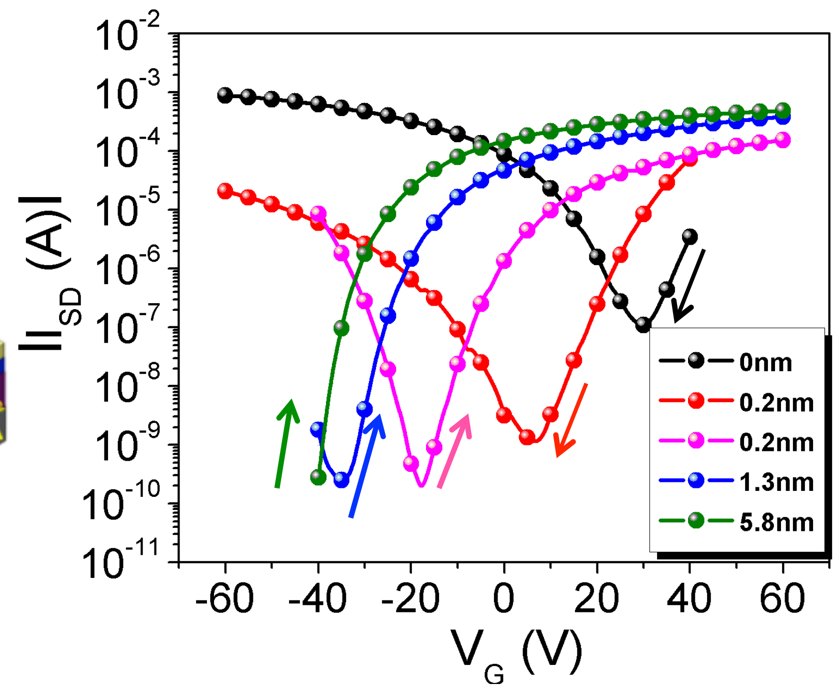
o-MeO-DMBI-I



P Wei, Z. Bao et. al. ***J. Am. Chem. Soc****., 2010, 132, 8852*
H. Wang*, Z. Bao et al.* ***PNAS****, 2014, 111(13), 4776-4781*

Doping by vacuum evaporation

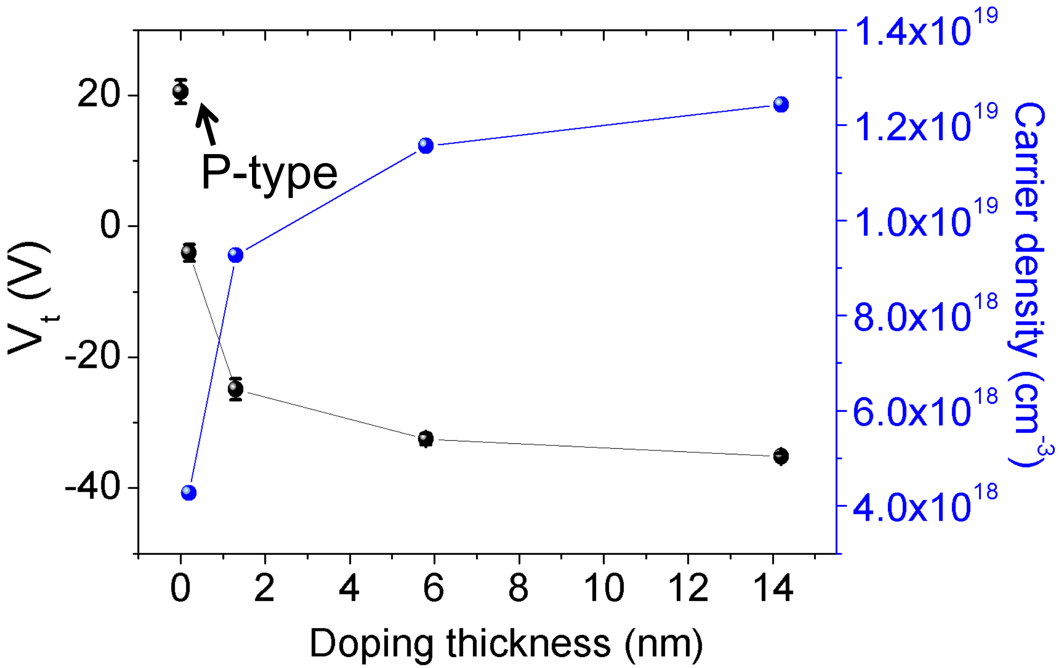




Tuning the threshold voltage by different thickness of dopants

***H. Wang**, Z. Bao et al. **PNAS**, 2014, 111(13), 4776-4781*

Tuning of threshold voltage and carrier density



$$I_D = \left(\frac{C_i \mu W}{2L}\right)(V_G - V_{th})^2$$

$$\sigma = q\mu n = \frac{I_D L}{V_D W d}$$

S.M.Sze (1981) *Physics of Semiconductor Devices* (Wiley, New York).

5 devices were measured at each doping thickness, small error bars

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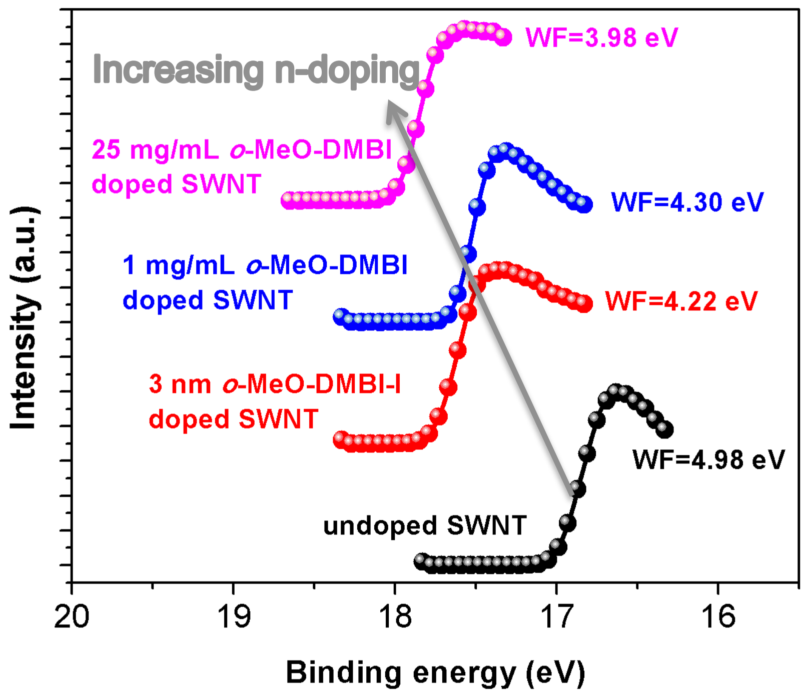
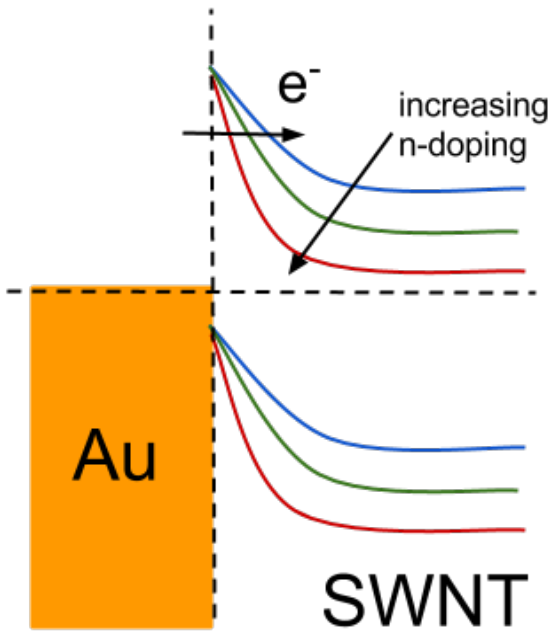
Why we have threshold voltage shifts





The Fermi energy of SWNT reduces with the higher doping concentrations
From photoelectron spectroscopy measurement

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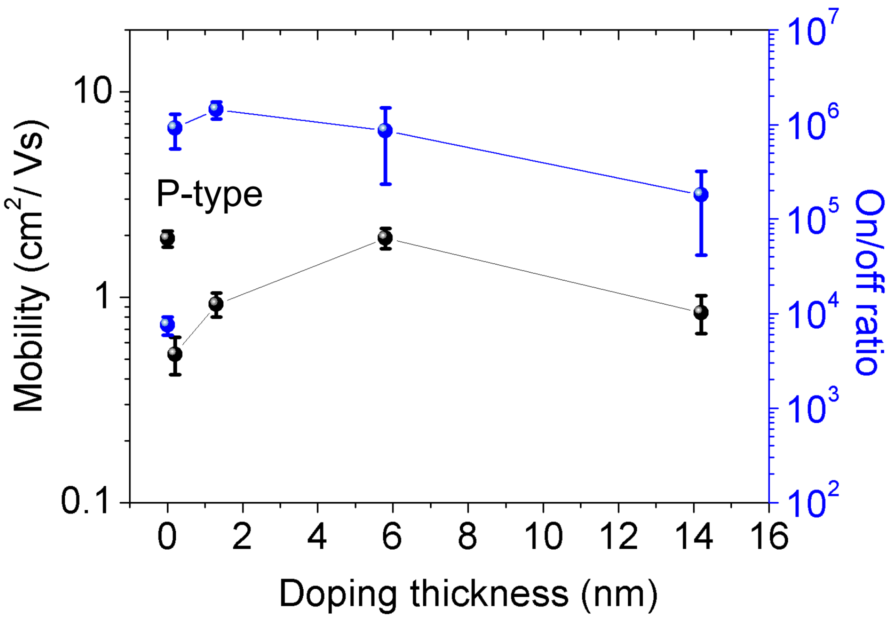
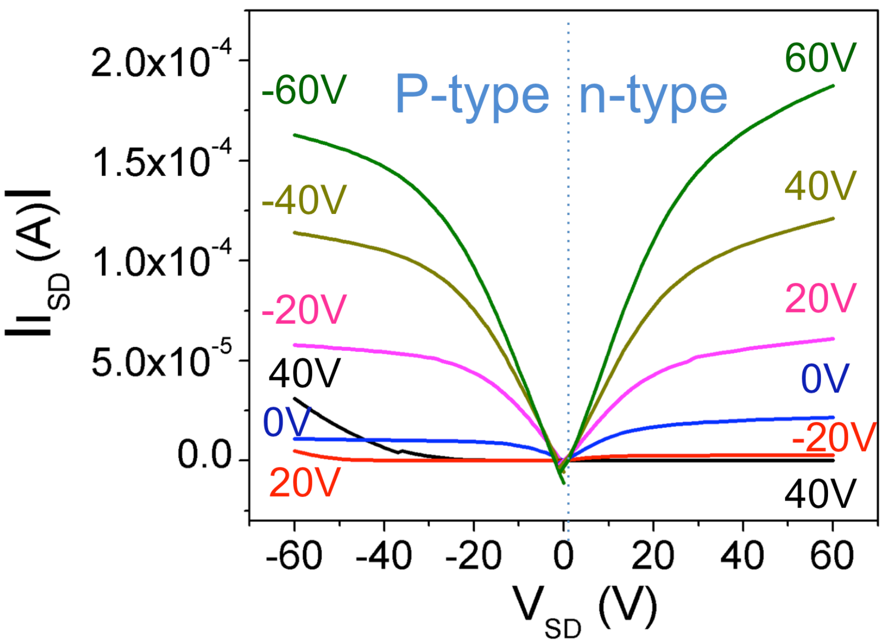
Device performance and output curves





Symmetrical p-type and n-type output curve for n-doped devices at certain thickness

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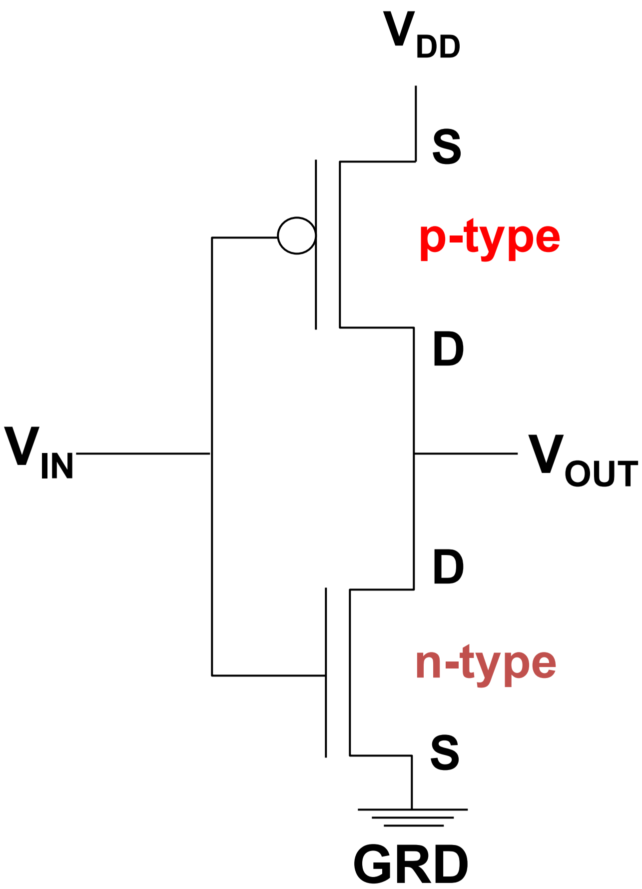
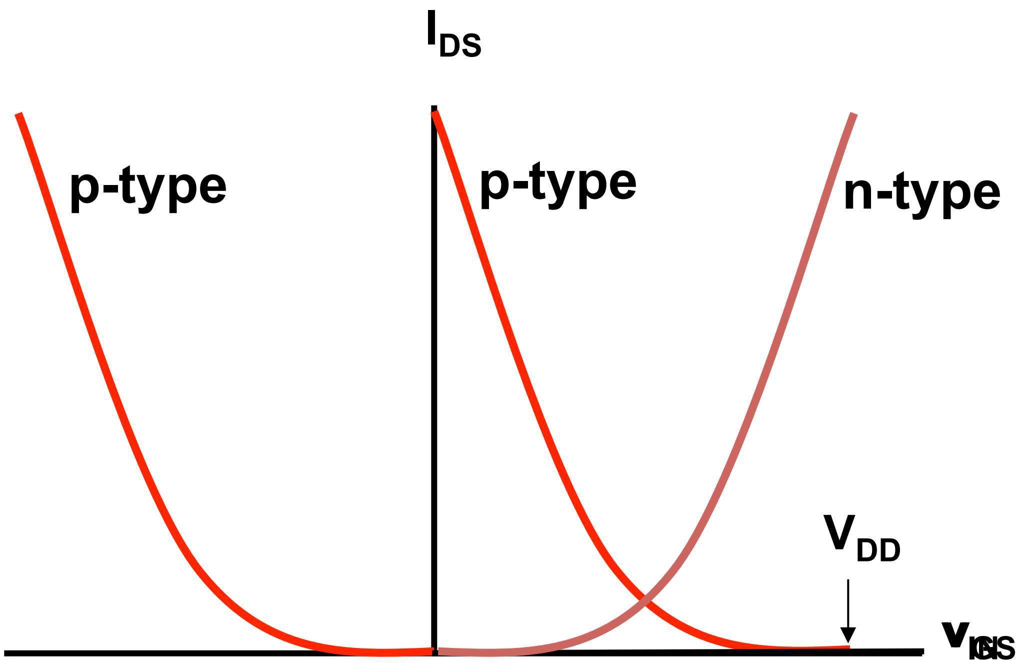
CMOS inverter and their advantage

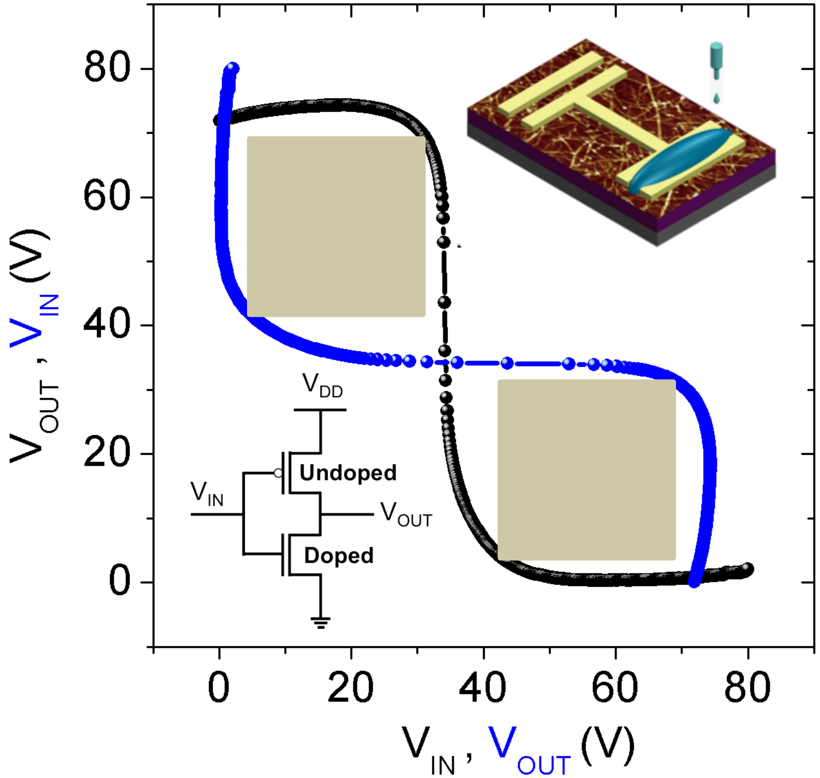


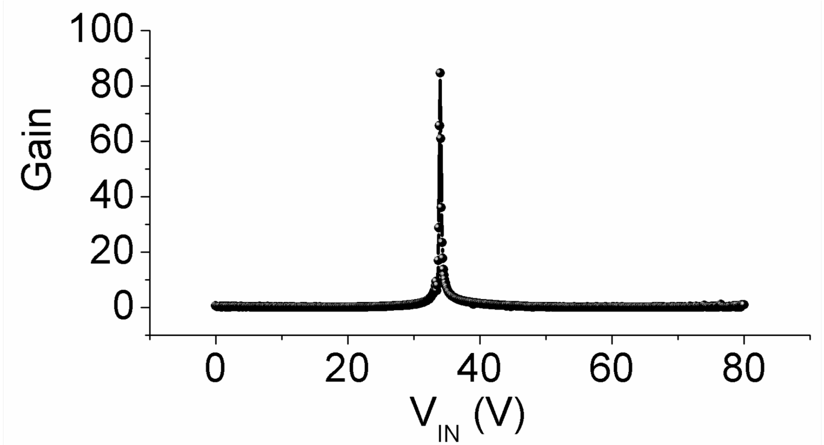


Advantage of CMOS:

1. Low power consumption
2. High reliability

Inverter with inkjet printed dopants





Gain of **85**

Noise Margin:
28V at a V_{DD} of 80V
70% of $1/2V_{DD}$

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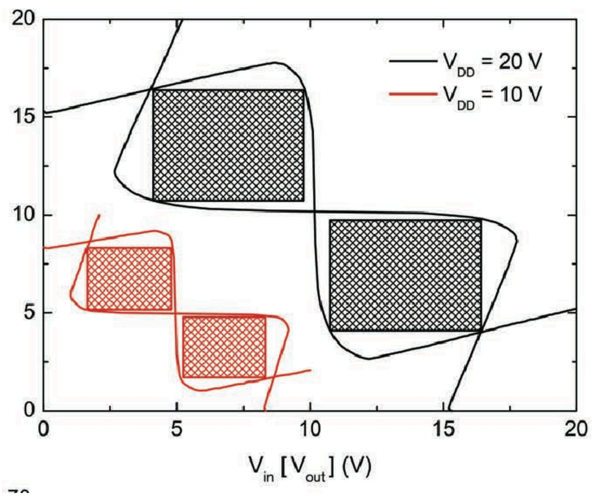
Comparison with other inverters

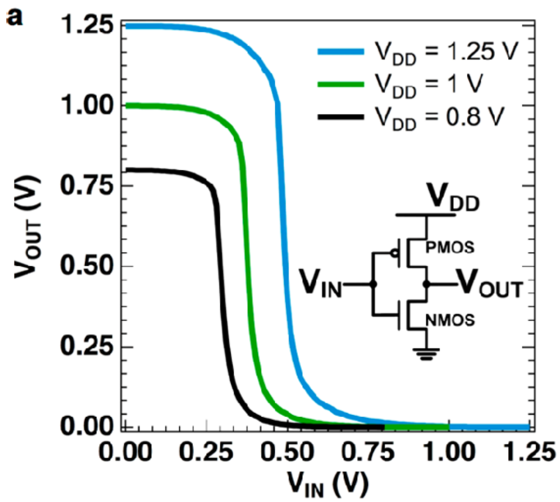
Organic inverter



Noise Margin = 65% $1/2V_{DD}$

H. Sirringhaus et al. **Adv. Mater.** 2012, 24, 1558–1565

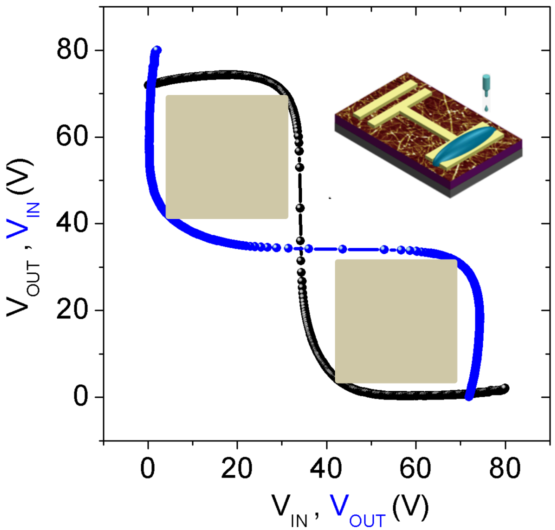
SWNTs inverter



Noise Margin = 64% $1/2V_{DD}$

M. Hersam et al. ***Nano lett.*** *2013,* 13, 4810

Our SWNTs inverter



Noise Margin = 70% $1/2V_{DD}$

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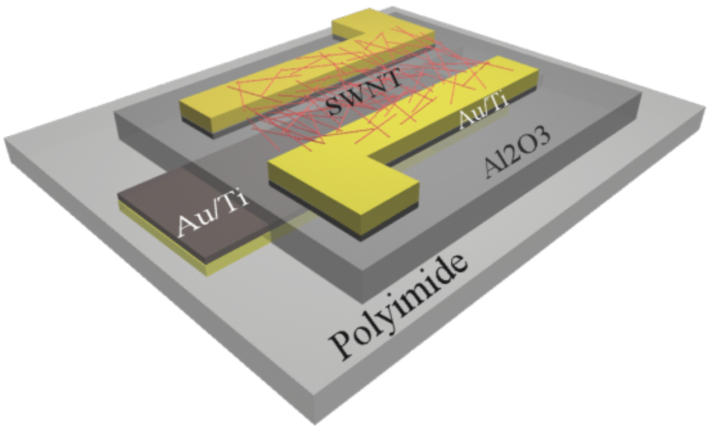
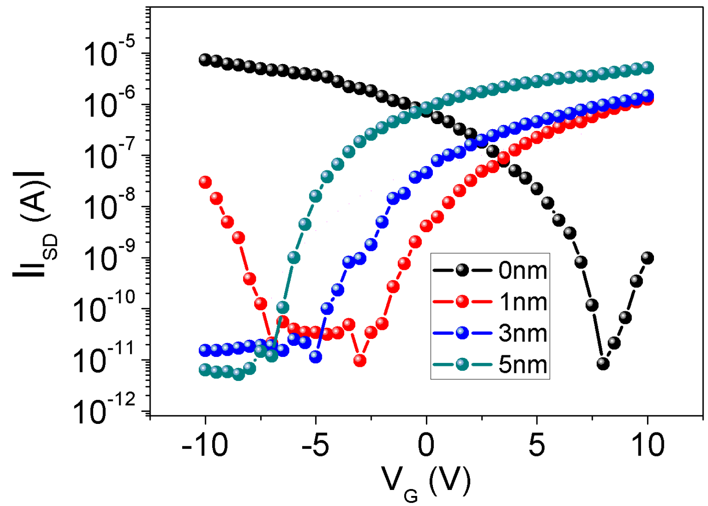
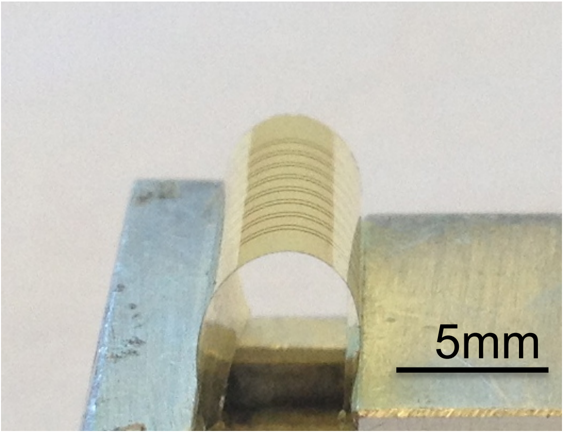
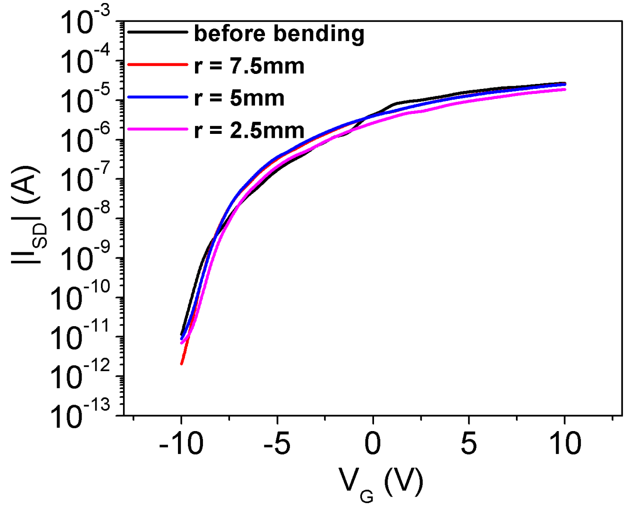
Tuning threshold voltage in flexible transistors

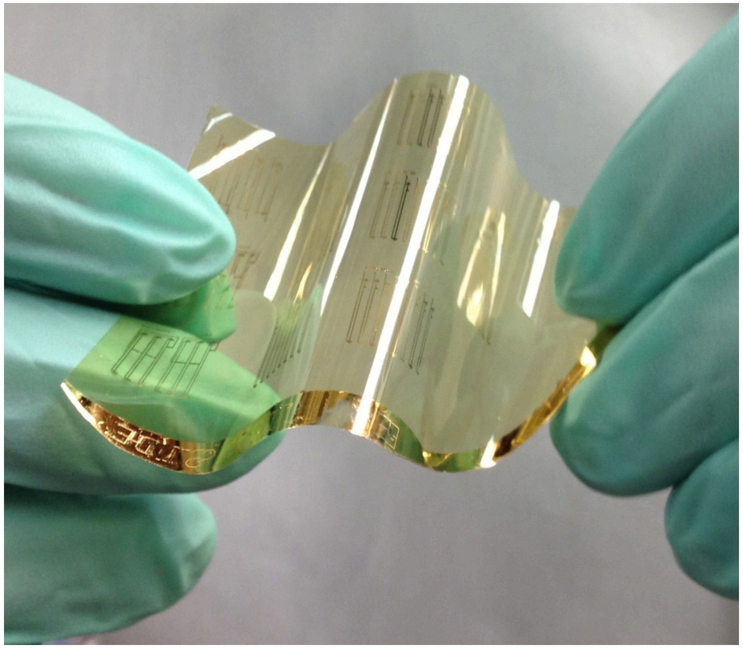


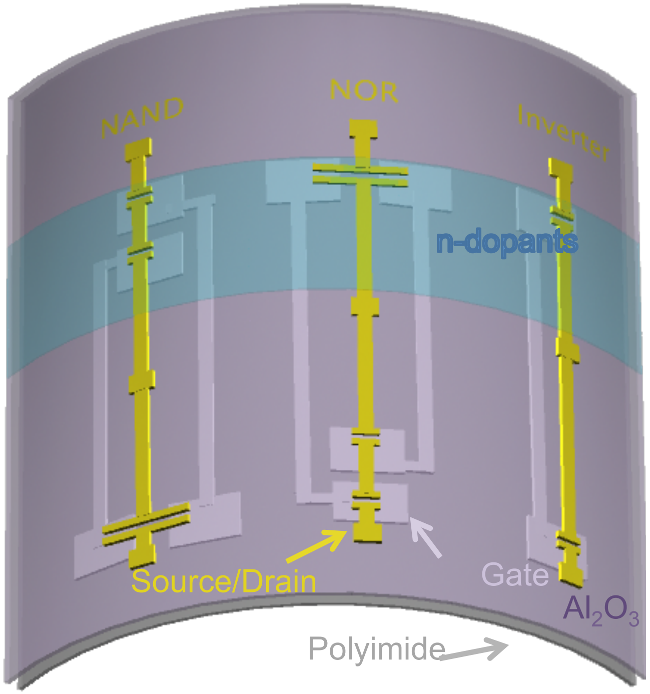






Flexible CMOS logic circuits





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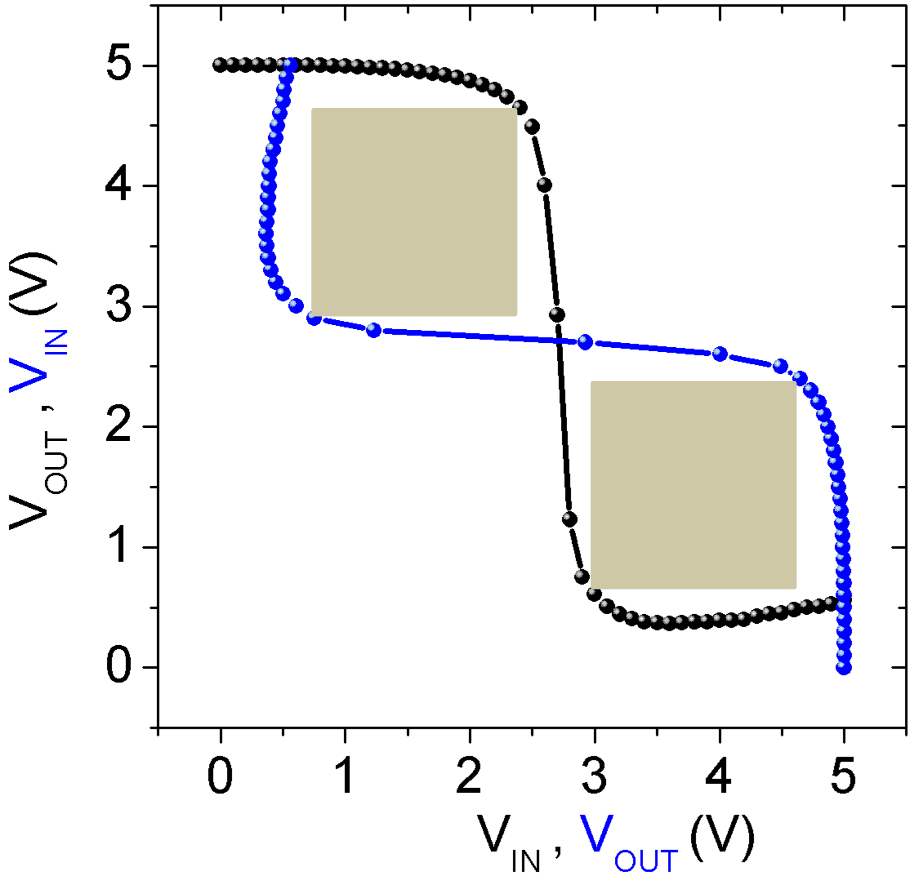
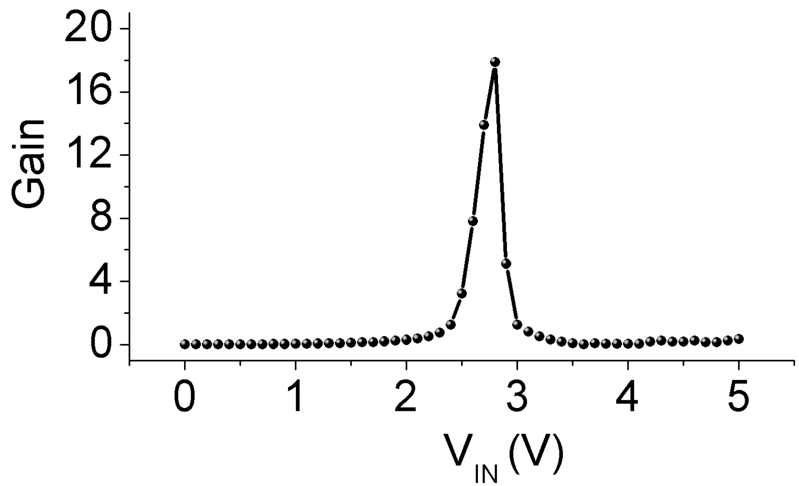
Flexible inverters with high noise margin





Gain of **18**

Noise Margin:

1.8 V at V_{DD} = 5 V
72% of $1/2V_{DD}$

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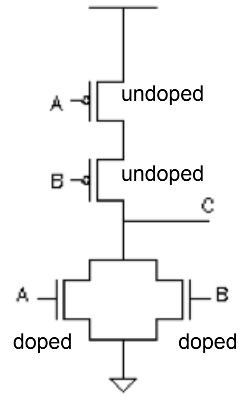
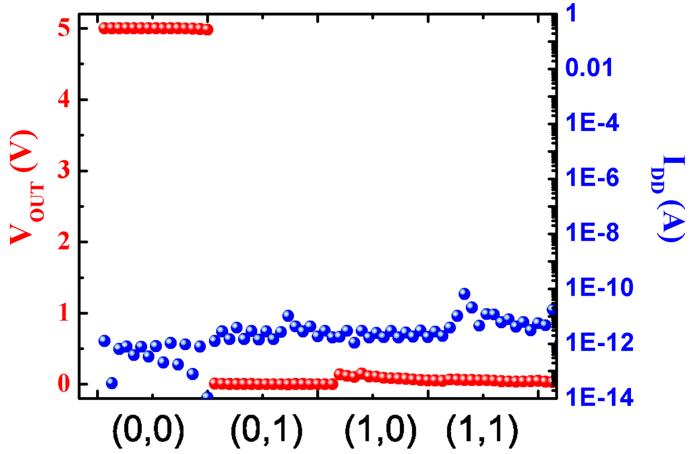
Nanowatt power-consumption CMOS NAND and NOR

NOR Gate

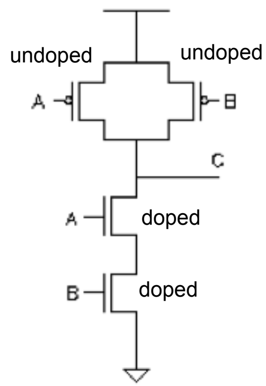
INPUT		OUTPUT
A	B	C
0	0	1
0	1	0
1	0	0
1	1	0

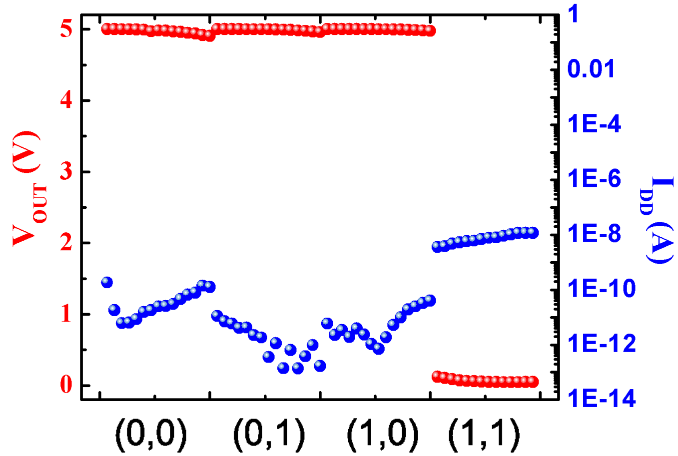




NAND Gate

INPUT		OUTPUT
A	B	C
0	0	1
0	1	1
1	0	1
1	1	0





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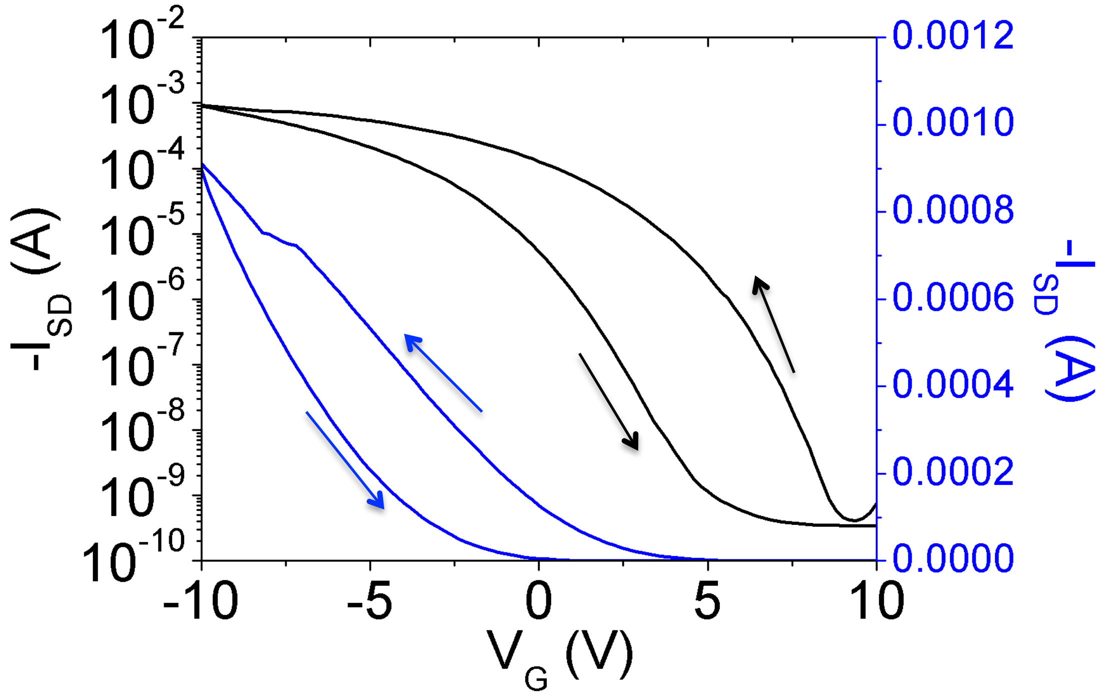
Aim: Stable threshold voltage of device during operation

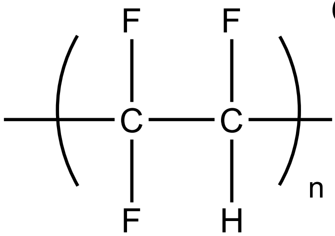
BAO RESEARCH

3rd Challenge: Stability of Devices



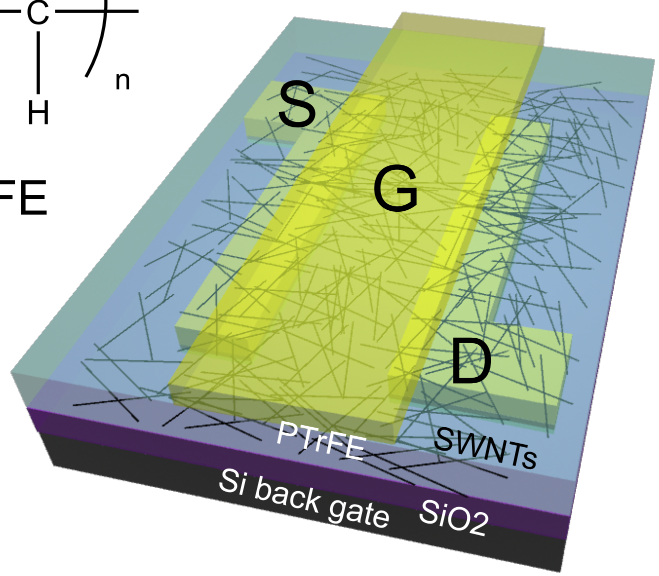
Large hysteresis, unstable threshold voltage (especially under bias stress)

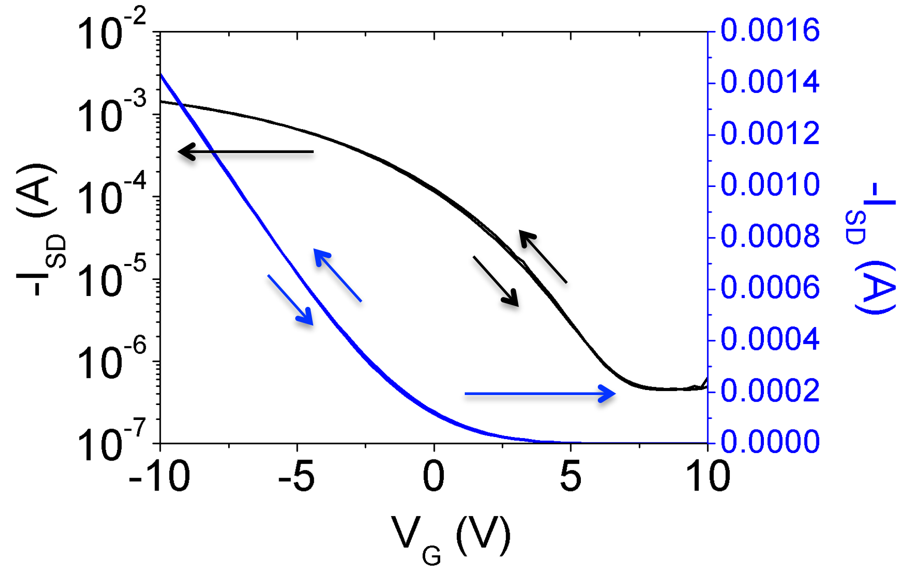
Using Fluorinated Polymers as Top-Gate Dielectrics



PTrFE

dielectic constant~10

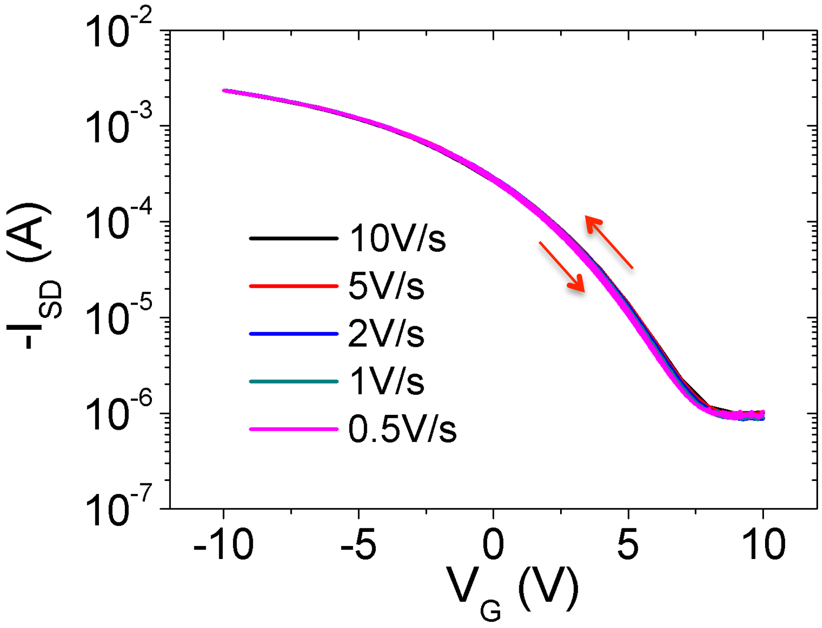




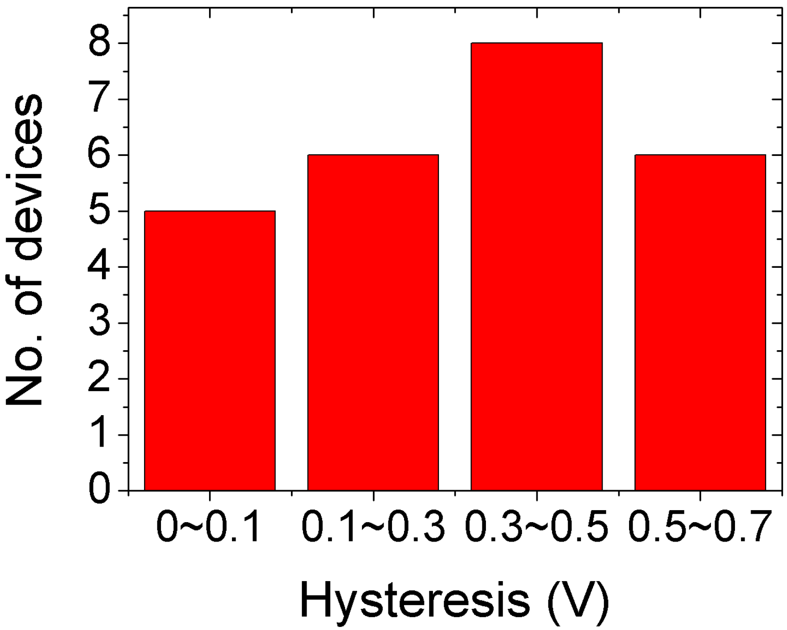
No hysteresis observed, near zero threshold voltage

H.Wang, *Z.Bao et. al.*, ***Advanced Materials***, *2014, 26,4588-4593*

Low-Hysteresis at Different Rates and Samples



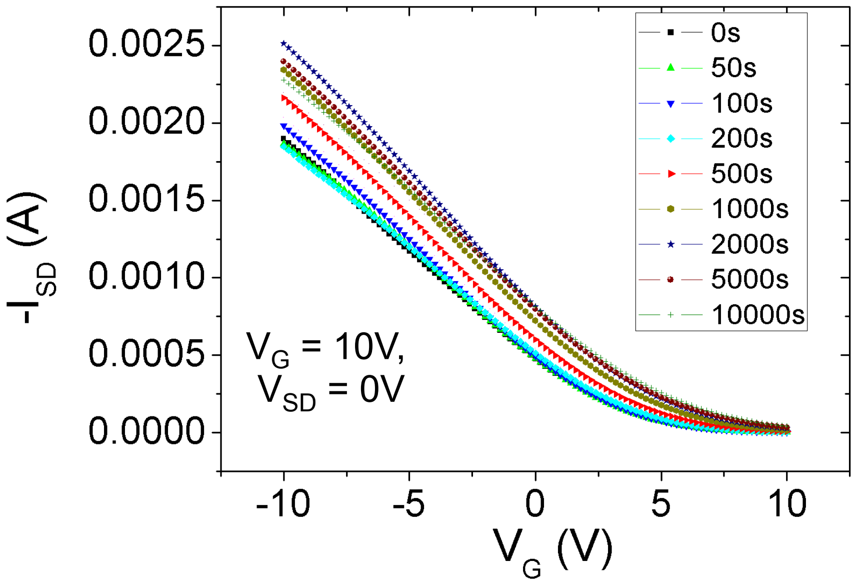
No hysteresis at different sweeping rate

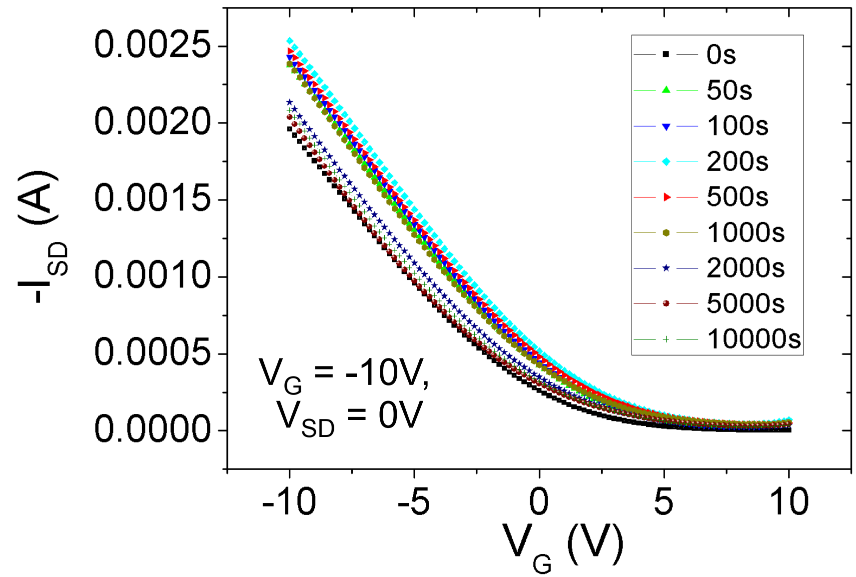


Hysteresis distribution between 24 different devices

H.Wang, *Z.Bao et. al.*, ***Advanced Materials***, *2014, 26,4588-4593*

Electrical Bias Stability of the Devices





Small threshold voltage shifts under bias stress in comparison with organic and oxide TFTs

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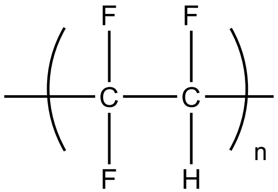
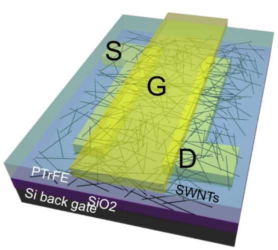
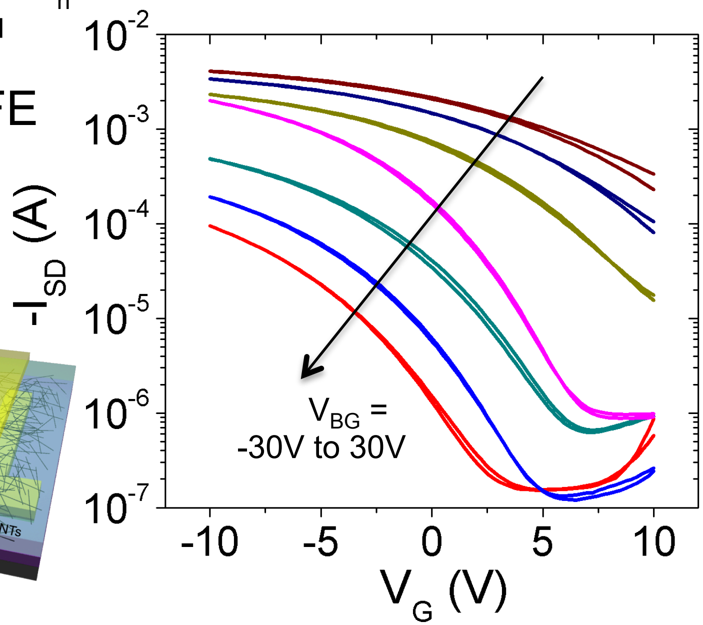
Tuning Threshold Voltage by Applying a Bottom Gate Voltage

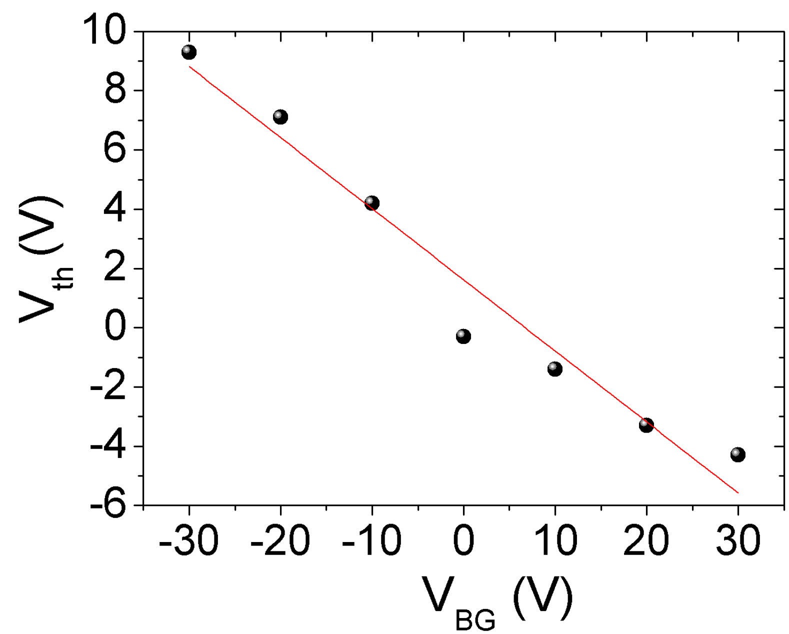


PTrFE

dielectic constant~10







Tuning depends on the ratio of the top-gate and bottom-gate capacitance

$$\Delta V_{th,top} = -\frac{C_{bottom}}{C_{top}} \Delta V_{bottom}$$

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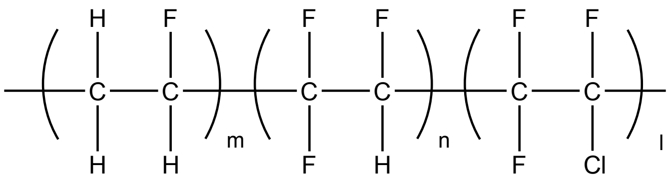
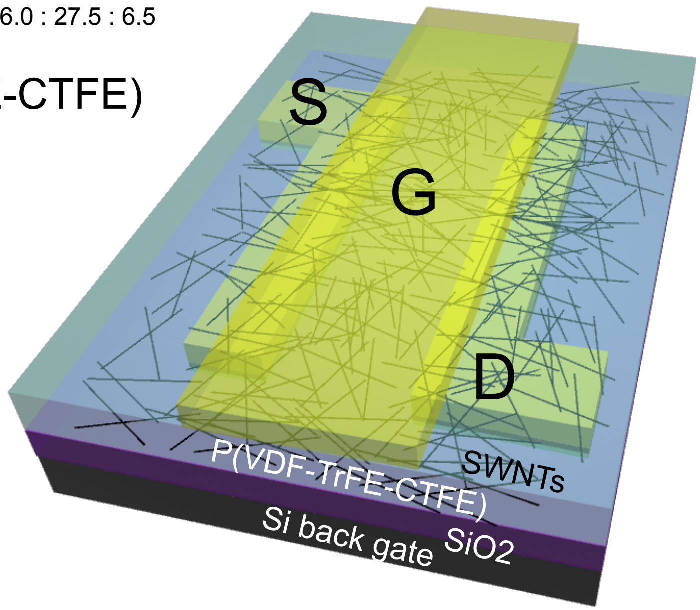
Ambipolar Device Behavior

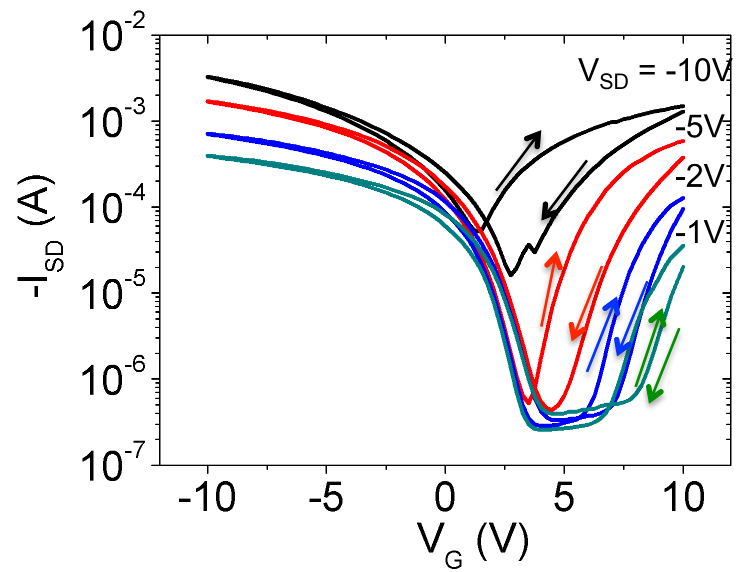


m : n : l = 66.0 : 27.5 : 6.5

P(VDF-TrFE-CTFE)

dielectic constant~25





Ambipolar device with P(VDF-TrFE-CTFE) as the gate dielectric

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Conclusion 1 – Polymer sorting of nanotubes

Polymer side-chain

Polymer backbone

Temperature
Solvents
Polymer/SWNT ratio

Polymer sorting of carbon nanotubes

High-yield and high purity sorting of semiconducting SWNTs

High mobility and high on/off ratio nanotube thin film transistors

Conclusion 2 – Improving Device Characteristics

Stability: using fluorinated polymers (PTrFE) as gate dielectrics

Threshold voltage tuning: chemical doping or second gate control

Ambipolar: using P(VDF-TrFE-CTFE) as gate dielectrics

Improving SWNT device characteristics

High noise margin inverter with inkjet printed dopants

Robust and flexible CMOS circuit with low power consumption

Acknowledgment

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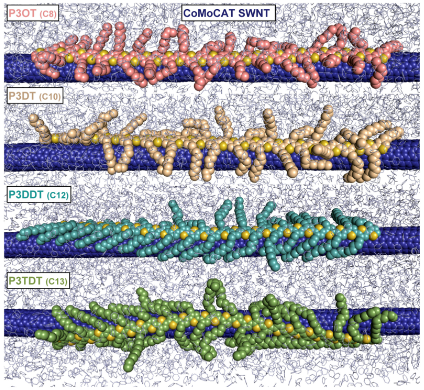
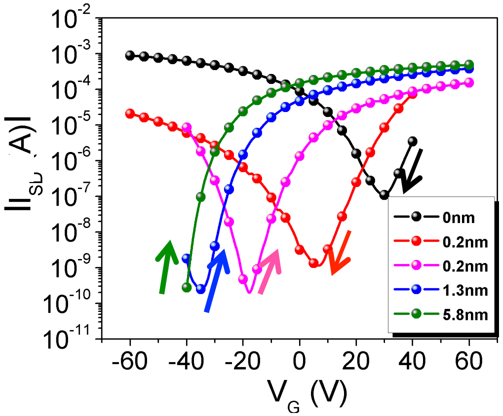
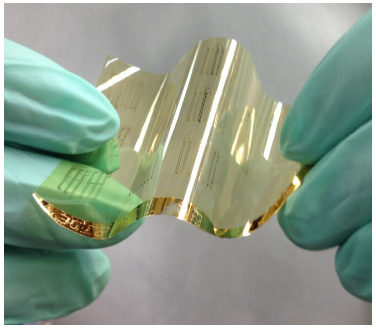
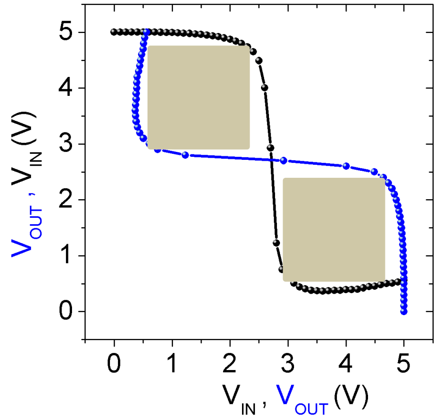
Any questions?

Thank you all for coming and listening!









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