FinFET Devices and Technologies

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Material Opportunities for Semiconductors

Why FinFETs?

• Planar MOSFETs cannot scale beyond 22nm
• Gate oxide thickness stops scaling
• Even with thin EOT, one still encounters electrostatic control problem
• Even with zero oxide thickness and with halo implant, “bad” current is still quite large
• Also heavy halo implant leads to band-to-band tunneling current
Why FinFETs?

- Ultra-thin body SOI devices provide improved electrostatic control
- A better solution is double-gate type devices → FinFETs

1998: First N-channel FinFETs

"6 folded-channel MOSFET for deep-sub-tenth micron era."

- Devices with $L_x$ down to 17 nm were successfully fabricated
Intel, Seeking Edge on Rivals, Rethinks Its Building Blocks

**Intel's Move Into 3-D**

The chip maker breaks from conventional approaches to make transistors.

**Conventional transistor:**
Electrons flow between components called a **source** and a **drain**, forming a two-dimensional **conducting channel**. A component called a **gate** starts and stops the flow, switching a transistor on or off.

**Intel's new transistor:** A fin-like **structure** rises above the surface of the transistor with the **gate** wrapped around it, forming **conducting channels** on three sides. The design takes less space on a chip, and improves speed and reduces power consumption.

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**Tri-Gate Transistor**

**22 nm Tri-Gate Transistor**

Tri-Gate transistors can have multiple fins connected together to increase total drive strength for higher performance.

**Source:** Intel
Tri-Gate Transistor

32 nm Planar Transistors
22 nm Tri-Gate Transistors

Tri-Gate Transistor – Scaling $H_{\text{fin}}$ and $W_{\text{fin}}$

$L_{\text{eff}} = L_{G} - 2 \times X_{UD}$
$W_{\text{eff}} = W_{SI} + 2(\varepsilon_{SI}/\varepsilon_{OX})T_{OX}$

where $X_{UD}$ is lateral diffusion from S/D; $W_{SI} = W_{\text{fin}}$

$W_{\text{fin}}$ is a key parameter for scaling

If is too wide, there is no advantage over planar devices

$W_{\text{eff}}$ must be decreased (along with $L_{\text{eff}}$) in order to have good electrostatic control

J. Kavalieros (Intel) Novel Device Architectures and Material Innovations, VLSI Symposium 2008 Technology Short Course
**Bulk Isolated FinFet Process (1)**

- Starting material: Silicon wafer
- Add channel stop doping
  - Blind/timed etch (i.e. no etch stop)
  - Depth control has many variables (local pattern density, etch chemistry, local surface condition, etc.)
  - Trench must be tapered for good fill

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**Bulk Isolated FinFet Process (2)**

- Deplech Oxide → Planarize Oxide → Recess Oxide

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T. Hook, IBM, FDSOI Workshop 4/2013
Bulk-FinFET vs. SOI FinFET

- Variation of fin heights ($\Delta H_{\text{fin}}$) – $\Delta H_{\text{fin}}$ might be less for SOI-FinFETs
- Cost – Substrate cost is less for bulk-FinFETs; but processing cost might be less for SOI-FinFETs
- Heat buildup in channel – Bulk FinFETs might be cooler because thermal conductivity is better for Si than SiO$_2$
- Parasitic BJT – SOI-FinFETs do not have parasitic BJT problem → lower leakage
- Epitaxial S/D – Might be less difficult for bulk-FinFETs
**Self-aligned double patterning (SADP)**

**Sub-Lithographic Fin Patterning**

1. Deposit & pattern sacrificial layer
2. Deposit mask layer (SiO$_2$ or Si$_3$N$_4$)
3. Etch back mask layer to form “spacers”
4. Remove sacrificial layer; etch SOI layer to form fins

Note that fin pitch is 1/2× that of patterned layer

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**Self-aligned double patterning (SADP)**

**Benefits of Spacer Lithography**

- Spacer litho. provides for better CD control and uniform fin width

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Fin fabrication by wet etch

- Etch: 2.38% TMAH solution at 50°C
- For (111)-oriented sidewall planes, the etch rate is extremely low → Very narrow and straight Si-fin channels can be fabricated

Tetramethylammonium hydroxide (TMAH) is a quaternary ammonium salt with the molecular formula \( \text{N(CH}_3\text{)}_4^+ \text{OH}^- \). TMAH is an anisotropic etching of silicon.

Fin fabrication by wet etch

- Experimental \( \mu_{\text{eff}} \)'s show good agreement with the universal curves for (111) bulk MOSFETs.
- 8.5% improvement in \( \mu_{\text{eff}} \) is obtained.

Damage-free and smooth Si-fin channel surface.
Bulk-FinFET vs. SOI FinFET Cost Comparison

The SOI finFET wafer cost increment over bulk depends on the final wafer cost.

SOURCE: SOI Industry Consortium

Process-Induced Variations

- Sub-wavelength lithography:
  - Resolution enhancement techniques are costly and increase process sensitivity

- Gate line-edge roughness:

- Random dopant fluctuations (RDF):
  - Atomistic effects become significant in nanoscale FETs


T. J. King-Liu (UC Berkeley) VLSI Technology 2012
Variability -- Bulk-FinFET vs. SOI FinFET

### SOI FinFET Variability

<table>
<thead>
<tr>
<th>Sources of Variability</th>
<th>Unit</th>
<th>Nominal</th>
<th>3-sigma Tolerance (current)</th>
<th>3-sigma Tolerance (future)</th>
</tr>
</thead>
<tbody>
<tr>
<td>SOI Layer</td>
<td>nm</td>
<td>70</td>
<td>2</td>
<td>1</td>
</tr>
<tr>
<td>Hardmask step</td>
<td>nm</td>
<td>10</td>
<td>1</td>
<td>0.5</td>
</tr>
<tr>
<td>Fin Etch</td>
<td>nm</td>
<td>70</td>
<td>4.2</td>
<td>2.1</td>
</tr>
<tr>
<td>Corner rounding</td>
<td>nm</td>
<td>2</td>
<td>0.1</td>
<td>0.05</td>
</tr>
<tr>
<td>Total fin height variability (nm)</td>
<td></td>
<td>4.8</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Total fin width variability (nm)</td>
<td></td>
<td>1.0</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

In 32nm technology, active area CD variability is 15nm across iso-dense patterns, multiple pitches and Fin - overetch from variability in vertical layers. For FinFETs, most of the CD variability is expected to come from the overetch, corrected for thickness variability in Fin. Consideration since the pitch will be fixed. Assumption is that 20% of the vertical variability will translate to CD (Fin width) variability.

**SOURCE:** SOI Industry Consortium

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Variability -- Bulk-FinFET vs. SOI FinFET

### Bulk FinFET (Junction isolated) Variability

<table>
<thead>
<tr>
<th>Sources of Variability</th>
<th>Unit</th>
<th>Nominal</th>
<th>3-sigma Tolerance (current)</th>
<th>3-sigma Tolerance (future)</th>
</tr>
</thead>
<tbody>
<tr>
<td>HM oxide</td>
<td>nm</td>
<td>8</td>
<td>0.4</td>
<td>0.2</td>
</tr>
<tr>
<td>HM nitride</td>
<td>nm</td>
<td>70</td>
<td>7</td>
<td>3.5</td>
</tr>
<tr>
<td>Trench etch</td>
<td>nm</td>
<td>170</td>
<td>8.5</td>
<td>4.25</td>
</tr>
<tr>
<td>Oxide etch</td>
<td>nm</td>
<td>100</td>
<td>5</td>
<td>2.5</td>
</tr>
<tr>
<td>Pad oxide</td>
<td>nm</td>
<td>2</td>
<td>0.1</td>
<td>0.05</td>
</tr>
<tr>
<td>Well anneal</td>
<td>nm</td>
<td>0</td>
<td>3</td>
<td>1.5</td>
</tr>
<tr>
<td>Total fin height variability (nm)</td>
<td></td>
<td>13.5</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Total fin width variability (nm)</td>
<td></td>
<td>2.5</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Assumption is that 20% of the vertical variability will translate to CD (Fin width) variability. See previous slide for more details on Fin width variability.

**SOURCE:** SOI Industry Consortium
Width quantization

\[ W = n \times (2 \, H_{\text{fin}} + W_{\text{fin}}) \]

where \( n \) = # of fins

= quantized

= especially bad for analog circuits application which

requires various widths

Width quantization (cont.)

• Analog design -- \( W \) as a circuit parameter goes from a
continuous variable to a set of small positive integers

• Width quantization changes layout practices (e.g. layout tool
to convert gate-width ratios into the necessary number of
fins)

• Layout design rules become more complicated – e.g.
  • Spacing rules to reduce coupling
  • SADP adds more complication to layout rules
  • Dummy gate – another layout-dependent effect

• There are already about 5,000 layout rules to check at 20 nm

• Result is increasing overall design time
**$V_T$ control and multiple threshold voltages**
Particularly important for analog applications

- How to achieve good threshold control and multiple $V_T$?

- Traditionally by changing substrate doping concentration $N_{\text{sub}}$ and/or by multiple dielectric thicknesses and/or back bias

- However, for FinFETs or Tri-gate transistors, body is generally undoped. It is also difficult to implement multiple dielectric thicknesses in 3D structures

- Another way to achieve multiple $V_T$ is by using multiple fin widths (i.e. wider fins $\rightarrow$ higher $V_T$)

- But fin width is defined by spacer technology. Need various spacer techniques for different widths.

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**Threshold voltage control and multiple $V_T$ schemes**

**$V_T$ tuning with aluminum implantation**

- SOI-FinFETs --- Hf-based high-K dielectrics / PVD TiN metal gate

- Aluminum implant ($1E15 - 1E16/cm^2$) into TiN metal but not the high-K; using ultra-low Trident implanter (3mA at 600eV).

- Effective work function (EWF) is modulated by Al implantation via Al-induced dipole at the HfO$_2$/SiO$_2$ interface.

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F. Rao (AMAT & Sematech) Ion Implantation Technology 2012
Threshold voltage control and multiple $V_T$ schemes

$V_T$ tuning using aluminum diffusion

- Interfacial layer SiO$_2$ by O$_3$-oxidation
- ALD TiN by TDMAT (tetrakis dimethyl amino titanium) or TiCl$_4$ based
- ALD-TaN and in-situ CVD-Co/HP-CVD Al as fill-metal (or W as fill metal)

Fig. 3 – Al diffusion into/through TiN depends strongly on the TiN deposition process used. A higher amount of Al diffusing into TiN results in a more Al-rich TiN on HfO$_2$ ↔ more n-type EWF.

- Al diffuses differently in/through TiN depending on its growth method
- Since Al-rich TiN has a more n-type EWF, stacks with higher amount of Al diffused into TiN translate into lower EWF values (i.e. more n-type EWF)
- Note: TDMAT-TiN is the least Al-rich TiN → Selected for P-MOSFET
- TiCl$_4$-TiN is the most Al-rich TiN → Selected for N-MOSFET

Orientation

- Multiple crystalline planes, depending on the orientation of the fins (i.e. layout)
- What should the fin direction be patterned?
- Kuhn SSDM 2009:
  (110) sidewall planes → better hole mobility
  (100) sidewall planes → better electron mobility
- Aggressively scaled $W_{\text{fin}}$ leads to more quantization (i.e. QM effects) → mobility decreases
- Tapered fin results in off-axis planes, causing mobility degradation
Temperature Effects of FinFETs

FinFETs might suffer worse self-heating effects, especially the so-called SOI-FinFETs.
Source/drain resistance – Merged epitaxy

- Merged vs. unmerged source/drain regions
- Merged S/D potentially provide lower source/drain resistance. However, epitaxial growth control can be challenging and may result in increased defect density. Furthermore, stress provided by merged fins for strained-Si channel is more difficult to control than unmerged fins.

3D InGaAs Gate-Wrap-Around FETs

Key features:
- 50nm undoped In_{0.53}Ga_{0.47}As channel
- 1 nm InP barrier layer
- 7 nm Al_{2}O_{3} / 60 nm TiN
- 20 nm N+ layer for Source/Drain

3D InGaAs Gate-Wrap-Around FETs

- SEM images of InGaAs GWAFETs

- Devices with \( W_{\text{fin}} \) from 40 nm to 200 nm, the gate length of 140 nm and 280 nm, and various numbers of parallel channels were fabricated.


Comparison of Scalability

- Better scalability was achieved by GWAFETs compare to planar structure with lower DIBL and SS.
- SS is limited by the interface at high-k and InGaAs.

Summary

• FinFETs are needed for 22nm and beyond

• Fabrication processes of bulk-FinFETs and SOI-FinFETs using self-aligned double patterning (SADP) have been developed successfully

• Both bulk-FinFETs and SOI-FinFETs are in development and production. Both have been compared in terms of process complexity, cost, temperature effects, variability; as well as vertical fins vs. tapered fins (e.g. Structural Stability, Corner Effects, S/D Doping, Mobility)
Summary

- Width quantization imposes some challenges on circuit design, especially for analog applications.

- Threshold voltage tuning / multiple $V_T$ is an important issue, which involves consideration of doped vs. undoped channel, QM effects, asymmetrical $t_{ox}$, implant/diffused aluminum and cap oxide schemes, gate workfunction control, etc…

- Channel orientation issues:
  - (110) sidewall planes $\rightarrow$ better hole mobility
  - (100) sidewall planes $\rightarrow$ better electron mobility
  Hybrid orientation scheme might be difficult to implement in practice.

- FinFET is applicable to analog circuit and mixed-signal applications.