# FinFET Devices and Technologies

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NCCAVS PAG Seminar 9/25/14
Material Opportunities for Semiconductors

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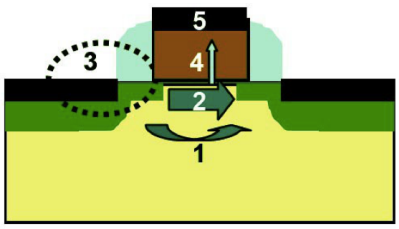
## Why FinFETs?




- Planar MOSFETs cannot scale beyond 22nm
- Gate oxide thickness stops scaling
- Even with thin EOT, one still encounters **electrostatic control problem**
- Even with zero oxide thickness and with halo implant, "bad" current is still quite large
- Also heavy halo implant leads to band-to-band tunneling current

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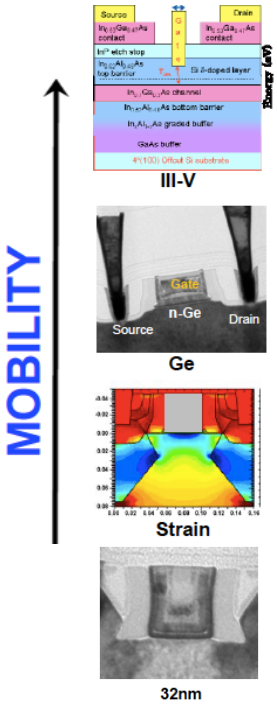
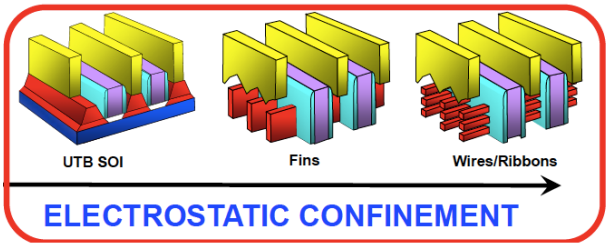
# Why FinFETs?




- Ultra-thin body SOI devices provide improved electrostatic control
- A better solution is double-gate type devices

→ FinFETs

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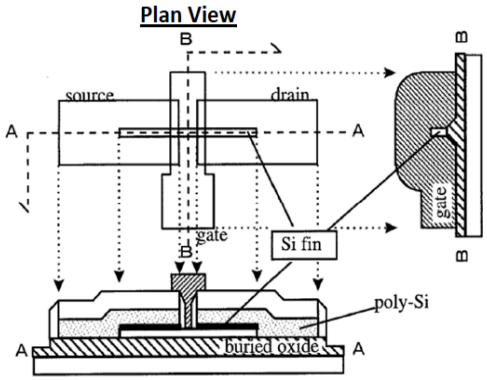
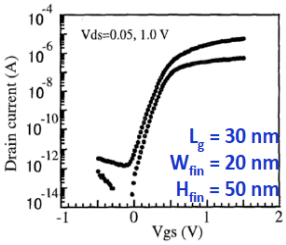
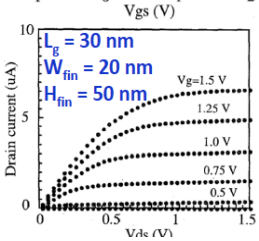
# 1998: First N-channel FinFETs

D. Hisamoto, W.-C. Lee, J. Kedzierski, E. Anderson, H. Takeuchi, K. Asano, T.-J. King, J. Bokor, and C. Hu,
"A folded-channel MOSFET for deep-sub-tenth micron era,"
*IEEE International Electron Devices Meeting Technical Digest*, pp. 1032-1034, 1998




- Devices with $L_g$ down to 17 nm were successfully fabricated

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T. J. King-Liu VLSI 2012

TECHNOLOGY | May 4, 2011

# Intel, Seeking Edge on Rivals, Rethinks Its Building Blocks

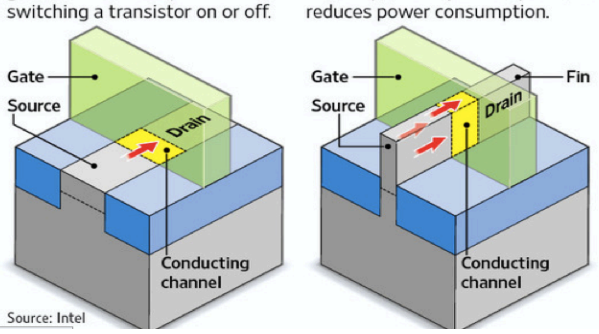
THE WALL STREET JOURNAL. U.S. EDITION Wednesday, May 4, 2011

## Intel's Move Into 3-D

The chip maker breaks from conventional approaches to make transistors.

**Conventional transistor:** Electrons flow between components called a **source** and a **drain**, forming a two-dimensional **conducting channel**. A component called a **gate** starts and stops the flow, switching a transistor on or off.

**Intel's new transistor:** A fin-like **structure** rises above the surface of the transistor with the **gate** wrapped around it, forming **conducting channels** on three sides. The design takes less space on a chip, and improves speed and reduces power consumption.




Source: Intel

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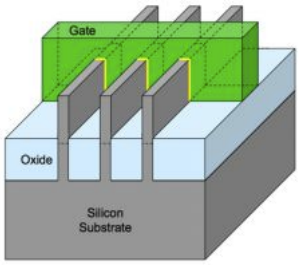
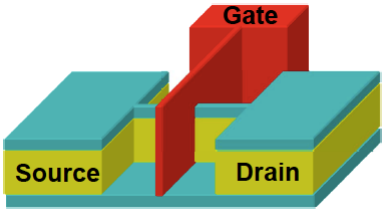
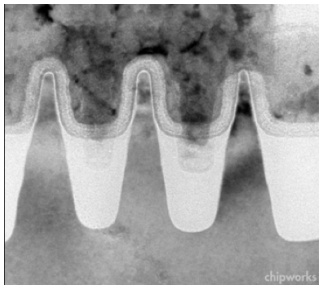
# Tri-Gate Transistor

22 nm Tri-Gate Transistor




Tri-Gate transistors can have multiple fins connected together to increase total drive strength for higher performance

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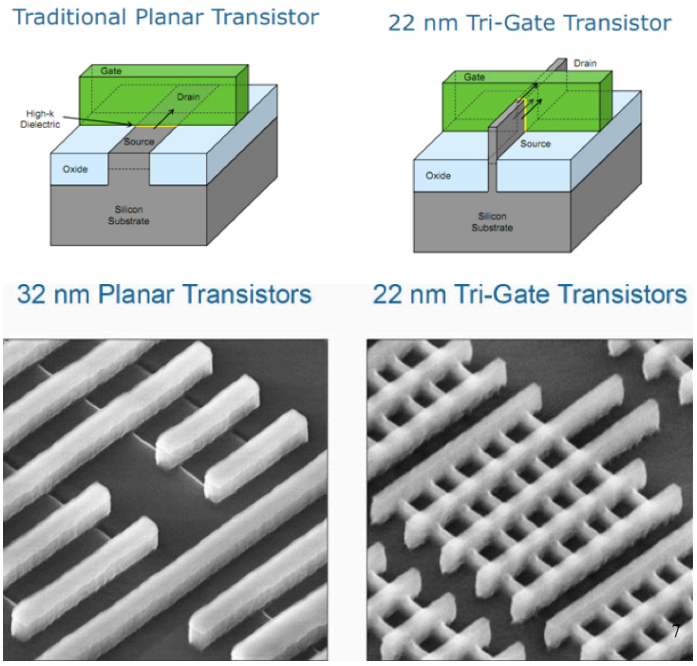
**SOURCE: Intel**

# Tri-Gate Transistor

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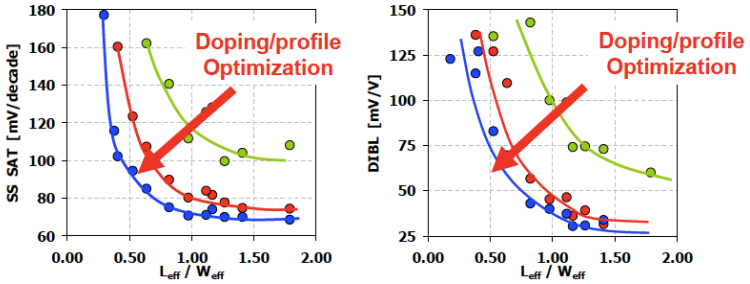
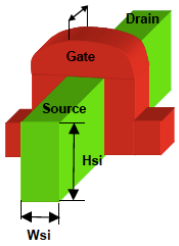
## Tri-Gate Transistor – Scaling $H_{fin}$ and $W_{fin}$




$L_{eff} = L_G - 2 * X_{UD}$

$W_{eff} = W_{Si} + 2(\varepsilon_{Si}/\varepsilon_{OX})*T_{OX}$

where $X_{UD}$ is lateral diffusion from S/D; $W_{si} = W_{fin}$

$W_{fin}$ is a key parameter for scaling

If is too wide, there is no advantage over planar devices

$W_{eff}$ must be decreased (along with $L_{eff}$) in order to have good electrostatic control

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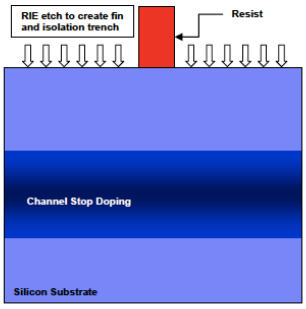
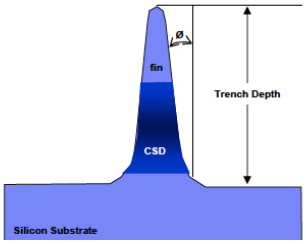
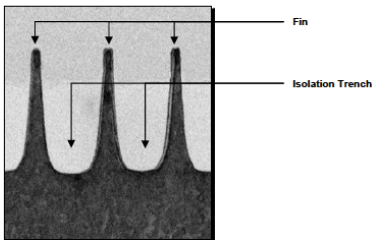
J. Kavalieros (Intel) Novel Device Architectures and Material Innovations, VLSI Symposium 2008 Technology Short Course

## Bulk Isolated FinFet Process (1)




- Starting material: **Silicon wafer**
- Add channel stop doping
- Etch silicon to create fin and isolation trench
  - Blind/timed etch (i.e. no etch stop)
  - Depth control has many variables (local pattern density, etch chemistry, local surface condition, etc.)
  - Trench must be tapered for good fill

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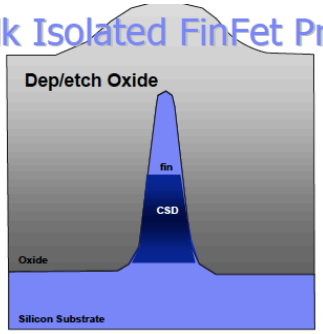
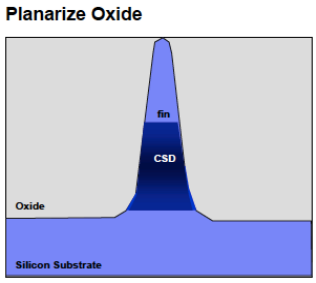
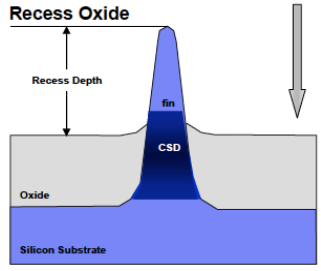
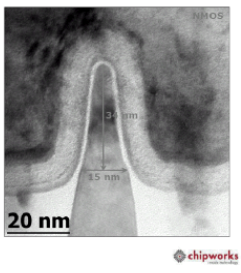
## Bulk Isolated FinFet Process (2)

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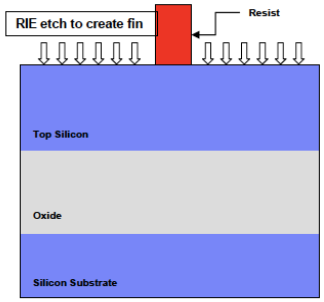
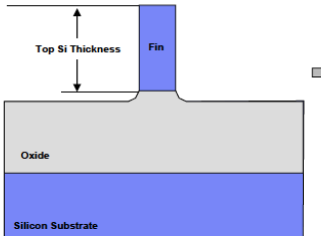
## SOI FinFet Process




- Starting material: **Silicon wafer with buried oxide**
- Etch silicon to create fin stopping on oxide
  - Fin height controlled by starting silicon thickness
  - Fin etched profile vertical (no fill constraint)
  - No channel stop doping impinging on the device





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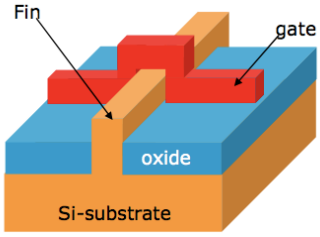
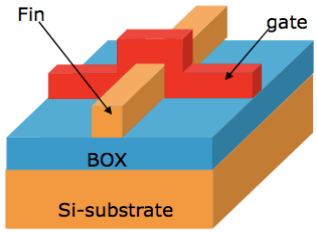
T. Hook, IBM, FDSOI Workshop 4/2013

## Bulk-FinFET vs. SOI FinFET




- Variation of fin heights ($\Delta H_{fin}$) – $\Delta H_{fin}$ might be less for SOI-FinFETs
- Cost – Substrate cost is less for bulk-FinFETs; but processing cost might be less for SOI-FinFETs
- Heat buildup in channel – Bulk FinFETs might be cooler because thermal conductivity is better for Si than $SiO_2$
- Parasitic BJT – SOI-FinFETs do not have parasitic BJT problem → lower leakage
- Epitaxial S/D – Might be less difficult for bulk-FinFETs

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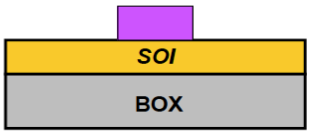
# Self-aligned double patterning (SADP)

## Sub-Lithographic Fin Patterning

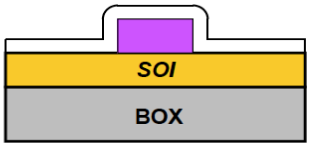
**Spacer Lithography**

**a.k.a. Sidewall Image Transfer (SIT) and Self-Aligned Double Patterning (SADP)**

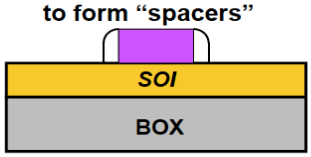
**1. Deposit & pattern sacrificial layer**



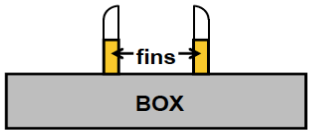

**2. Deposit mask layer ($SiO_2$ or $Si_3N_4$)**




**3. Etch back mask layer to form "spacers"**




**4. Remove sacrificial layer; etch SOI layer to form fins**




Note that fin pitch is 1/2× that of patterned layer

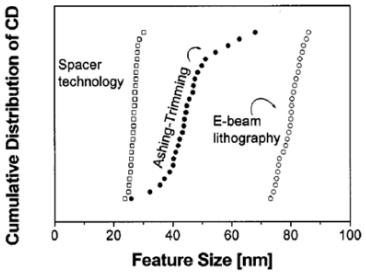




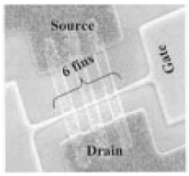
# Self-aligned double patterning (SADP)

## Benefits of Spacer Lithography

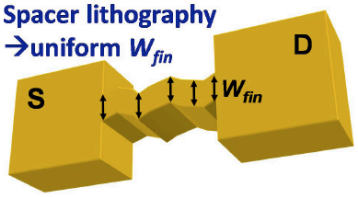
- Spacer litho. provides for better CD control and uniform fin width



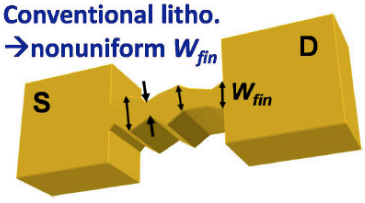

SEM image of FinFET with spacer-defined fins:



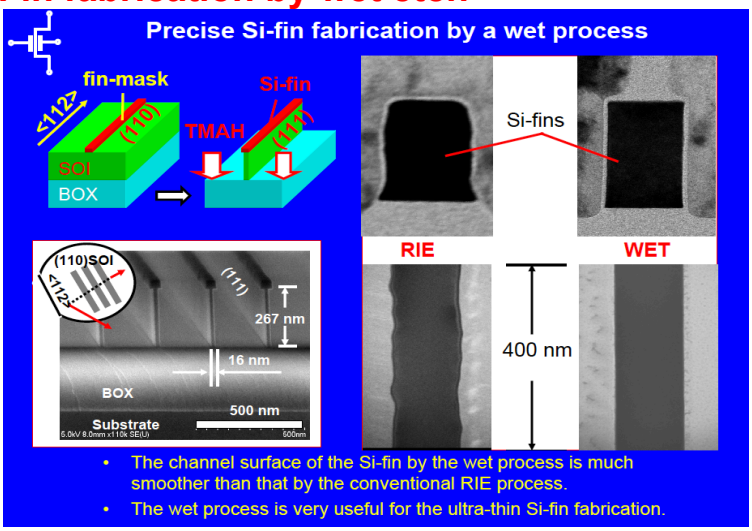

**Spacer lithography →uniform $W_{fin}$**




**Conventional litho. →nonuniform $W_{fin}$**



# Fin fabrication by wet etch




Tetramethyl-ammonium hydroxide (TMAH) is a quaternary ammonium salt with the molecular formula $N(CH_3)_4^+ OH^-$.

TMAH is an anisotropic etching of silicon.

- Etch: 2.38% TMAH solution at 50°C
- For (111)-oriented sidewall planes, the etch rate is extremely low → Very narrow and straight Si-fin channels can be fabricated

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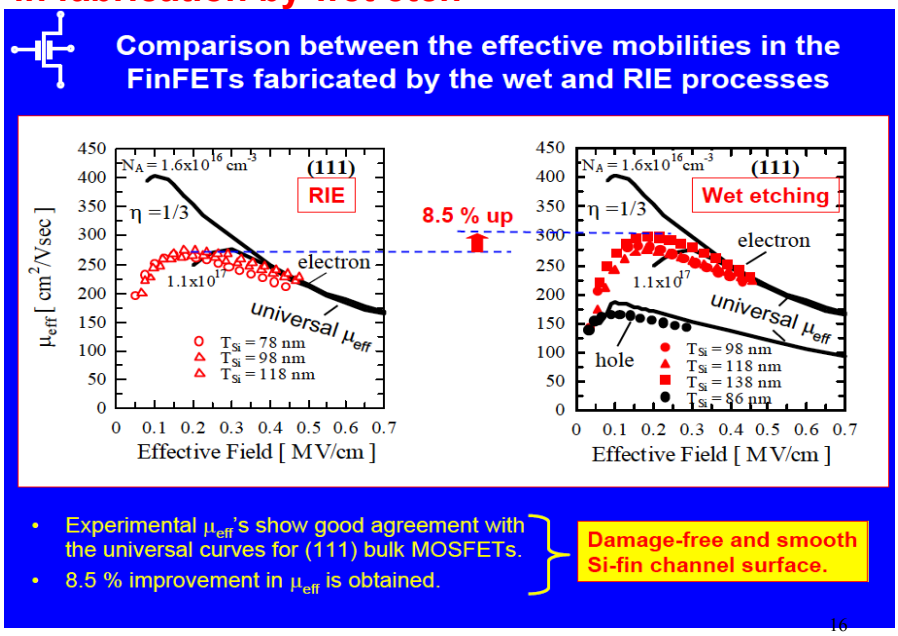
Y. X. Liu (Advanced Industrial Science and Technology AIST), IEEE IEDM 2006

# Fin fabrication by wet etch

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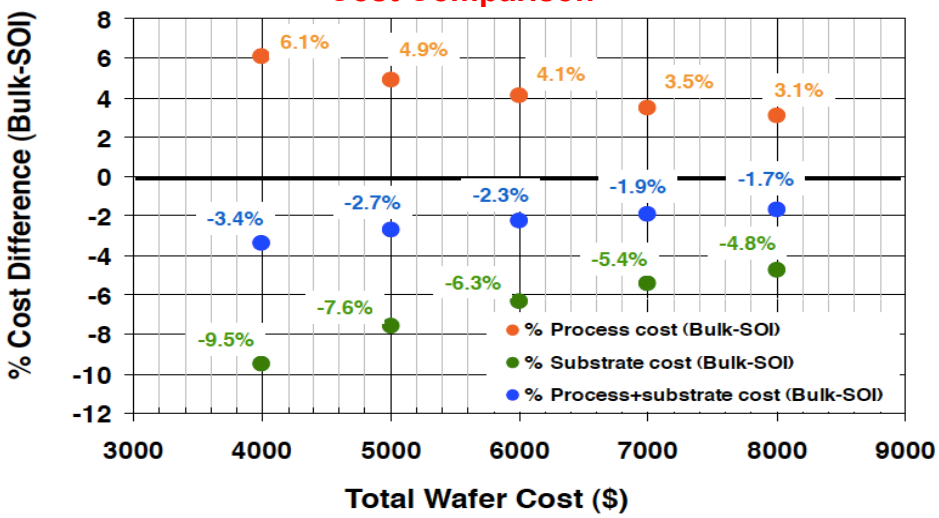
Y. X. Liu (Advanced Industrial Science and Technology AIST), IEEE IEDM 2006

## Bulk-FinFET vs. SOI FinFET Cost Comparison




The SOI finFET wafer cost increment over bulk depends on the final wafer cost.

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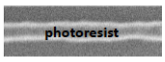
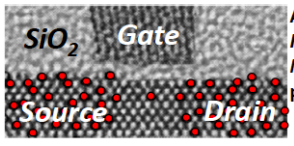
**SOURCE: SOI Industry Consortium**

## Process-Induced Variations

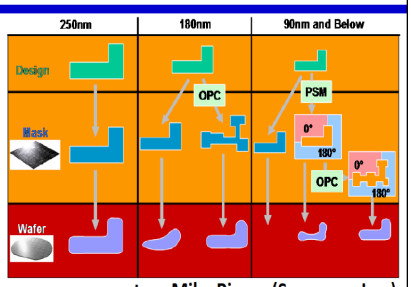
- **Sub-wavelength lithography:**
  - Resolution enhancement techniques are costly and increase process sensitivity
- **Gate line-edge roughness:**



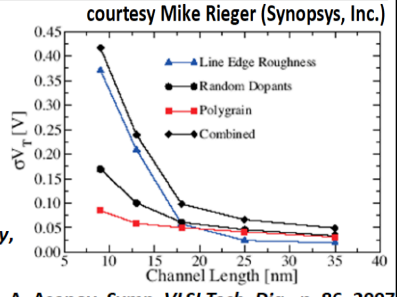

- **Random dopant fluctuations (RDF):**
  - Atomistic effects become significant in nanoscale FETs




A. Brown *et al.*, *IEEE Trans. Nanotechnology*, p. 195, 2002




courtesy Mike Rieger (Synopsys, Inc.)




A. Asenov, *Symp. VLSI Tech. Dig.*, p. 86, 2007

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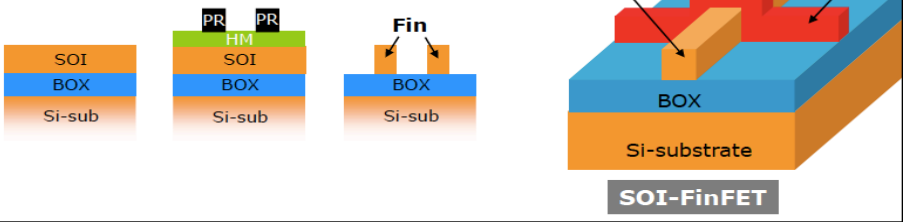
T. J. King-Liu (UC Berkeley) VLSI Technology 2012

## Variability -- Bulk-FinFET vs. SOI FinFET

### SOI FinFET Variability




| Sources of Variability | Unit | Nominal | 3-sigma Tolerance (current) | 3-sigma Tolerance (future) | |
|---|---|---|---|---|---|
| SOI Layer | nm | 70 | 2 | 1 | 5% 3sigma SOI thickness variability with future improvements in high volume manufacturing |
| Hardmask dep | nm | 10 | 1 | 0.5 | 10% cross-wafer 3sigma |
| Fin Etch | nm | 70 | 4.2 | 2.1 | 5% cross wafer + 1% overetch |
| Corner rounding | nm | 2 | 0.1 | 0.05 | |
| **Total fin height variability (nm)** | | | **4.8** | **2.4** | Root sum-square of all sources of variability |
| **Total fin width variability (nm)** | | | **1.0** | **0.5** | In 32nm technology, active area CD variability is 15nm across iso-dense patterns, multiple pitchs and RIE overetch from variability in vertical layers. For FinFETs, most of the CD variability is expected to come from the overetch to account for thickness variability in Fin definition since the pitch will be fixed. Assumption is that 20% of the vertical variability will translate to CD (Fin width) variabiliy. |

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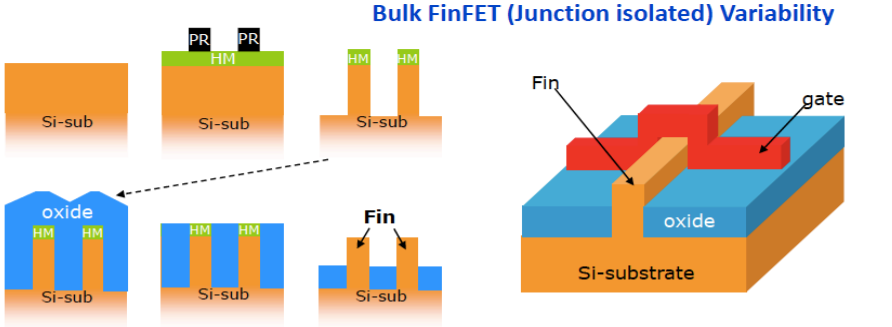
**SOURCE: SOI Industry Consortium**

## Variability -- Bulk-FinFET vs. SOI FinFET

### Bulk FinFET (Junction isolated) Variability




| Sources of Variability | Unit | Nominal | 3-sigma Tolerance (current) | 3-sigma Tolerance (future) | |
|---|---|---|---|---|---|
| HM oxide | nm | 8 | 0.4 | 0.2 | 5% 3sigma variation for oxide |
| HM nitride | nm | 70 | 7 | 3.5 | 10% 3sigma variation for deposited nitride |
| Trench etch | nm | 170 | 8.5 | 4.25 | 5% 3sigma from trench etch based on 32nm data |
| Oxide recess | nm | 100 | 5 | 2.5 | Oxide dry/wet etch with no etch stop. 100nm oxide etchback for 70nm fin height assumed. |
| Pad oxide | nm | 2 | 0.1 | 0.05 | |
| Well anneal | nm | 0 | 3 | 1.5 | 3sigma variability in junction depth from angled implants |
| **Total fin height variability (nm)** | | | **12.5** | **6.2** | Root sum-square of all sources of variability |
| **Total fin width variability (nm)** | | | **2.5** | **1.2** | Assumption is that 20% of the vertical variability will translate to CD (Fin width) variability. See previous slide for more details on fin width variability. |

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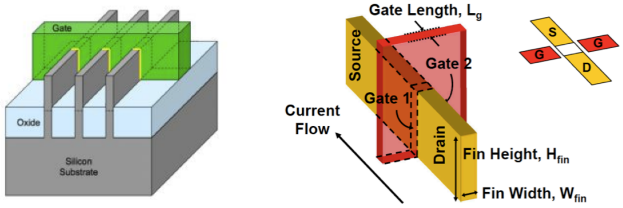
**SOURCE: SOI Industry Consortium**

## Width quantization




$W = n \times (2 H_{fin} + W_{fin})$ where n = # of fins
= quantized
= especially bad for analog circuits application which requires various widths

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## Width quantization (cont.)

- Analog design -- W as a circuit parameter goes from a continuous variable to a set of small positive integers
- Width quantization changes layout practices (e.g. layout tool to convert gate-width ratios into the necessary number of fins)
- Layout design rules become more complicated – e.g.
  - Spacing rules to reduce coupling
  - SADP adds more complication to layout rules
  - Dummy gate – another layout-dependent effect
- There are already about 5,000 layout rules to check at 20 nm
- Result is increasing overall design time

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## $V_T$ control and multiple threshold voltages
### Particularly important for analog applications

- How to achieve good threshold control and multiple $V_T$?
- Traditionally by changing substrate doping concentration $N_{sub}$ and/or by multiple dielectric thicknesses and/or back bias
- However, for FinFETs or Tri-gate transistors, body is generally undoped. It is also difficult to implement multiple dielectric thicknesses in 3D structures
- Another way to achieve multiple $V_T$ is by using multiple fin widths (i.e. wider fins → higher $V_T$)
- But fin width is defined by spacer technology. Need various spacer techniques for different widths.

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## Threshold voltage control and multiple $V_T$ schemes

### $V_T$ tuning with aluminum implantation

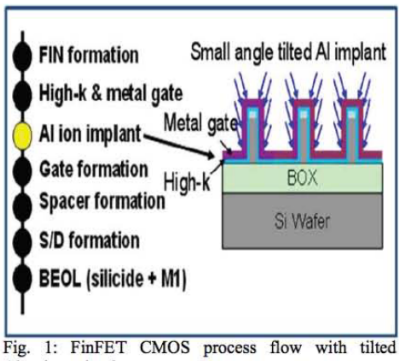


Fig. 1: FinFET CMOS process flow with tilted Aluminum implant

- SOI-FinFETs --- Hf-based high-K dielectrics / PVD TiN metal gate
- Aluminum implant (1E15 -1E16/cm$^2$) into TiN metal but not the high-K; using ultra-low Trident implanter (3mA at 600eV).
- Effective work function (EWF) is modulated by Al implantation via Al-induced dipole at the $HfO_2/SiO_2$ interface.

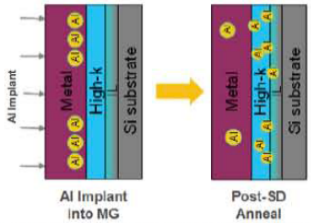


Fig. 3: Implanted Al is thermally driven (during SD activation spike anneal) to high-k/$SiO_x$ interface to form dipole

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F. Rao (AMAT & Sematech) Ion Implantation Technology 2012

# Threshold voltage control and multiple $V_T$ schemes

**$V_T$ tuning using aluminum diffusion**

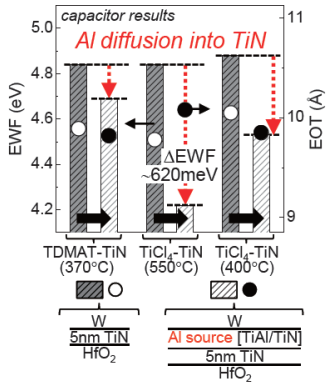


**Fig.3** – Al diffusion into/through TiN depends strongly on the TiN deposition process used. A higher amount of Al diffusing into TiN results in a more Al-rich TiN on $HfO_2$ ⇔ more n-type EWF.

- Interfacial layer $SiO_2$ by $O_3$-oxidation
- ALD TiN by TDMAT (tetrakis dimethyl amino titanium) or $TiCl_4$ based
- ALD-TaN and in-situ CVD-Co/HP-CVD Al as fill-metal (or W as fill metal)

- Al diffuses differently in/through TiN depending on its growth method
- Since Al-rich TiN has a more n-type EWF, stacks with higher amount of Al diffused into TiN translate into lower EWF values (i.e. more n-type EWF)
- Note: TDMAT-TiN is the least Al-rich TiN → Selected for P-MOSFET
- $TiCl_4$-TiN is the most Al-rich TiN → Selected for N-MOSFET

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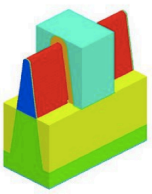
A. Veloso (IMEC) VLSI Technology Symposium 2013

# Orientation

- Multiple crystalline planes, depending on the orientation of the fins (i.e. layout)
- What should the fin direction be patterned?
- Kuhn SSDM 2009:
  (110) sidewall planes → better hole mobility
  (100) sidewall planes → better electron mobility
- Aggressively scaled $W_{fin}$ leads to more quantization (i.e. QM effects) → mobility decreases
- Tapered fin results in off-axis planes, causing mobility degradation



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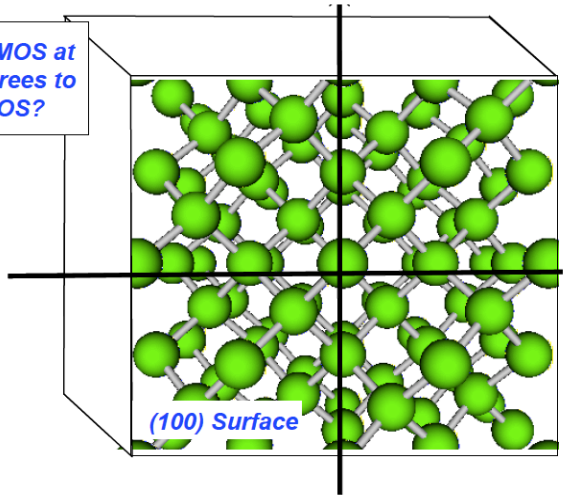
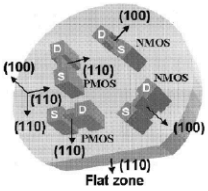
# NMOS Vertical Devices on (100)

*Put NMOS at 45degrees to PMOS?*




*<100> channel*




Chang - Berkeley
Proc. IEEE 2003

(100) surface <100> channel for a VFET fabricated at 45 degrees typical (100) Si – very challenging for lithography

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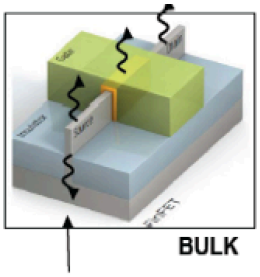
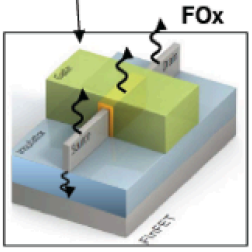
SOURCE: Intel

Kelin Kuhn / SSDM / Japan / 2009

## Temperature Effects of FinFETs




Thermal Conduction Paths




FinFETs might suffer worse self-heating effects, especially the so-called SOI-FinFETs.

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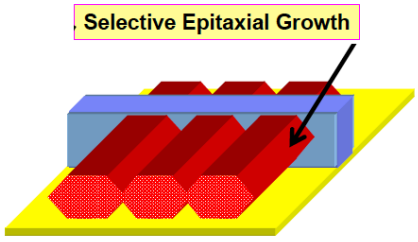
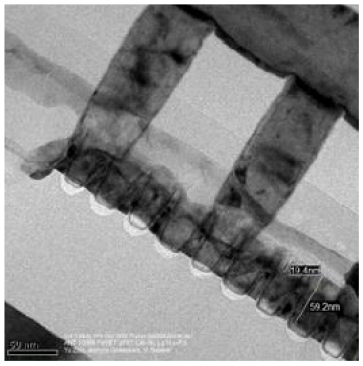
## Source/drain resistance – Merged epitaxy




-Merge Fins (Grows epi Si/SiGe/SiC)
-Insitu-doped or I/I

Merged epitaxy



- Merged vs. unmerged source/drain regions
- Merged S/D potentially provide lower source/drain resistance. However, epitaxial growth control can be challenging and may result in increased defect density. Furthermore, stress provided by merged fins for strained-Si channel is more difficult to control than unmerged fins

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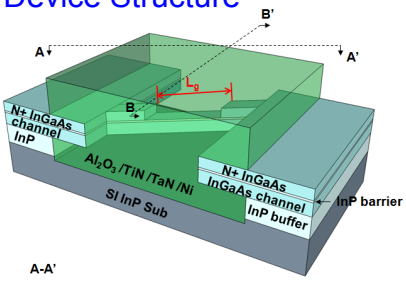
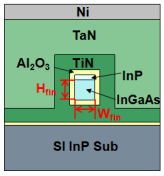
T. Hook (IBM) FDSOI Workshop 2012

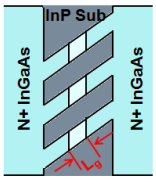
## 3D InGaAs Gate-Wrap-Around FETs

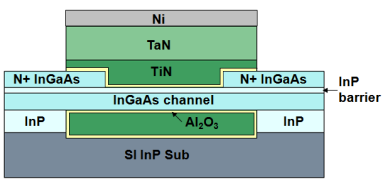
### Device Structure




Top view



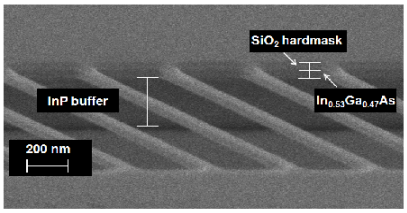

❑ Key features:

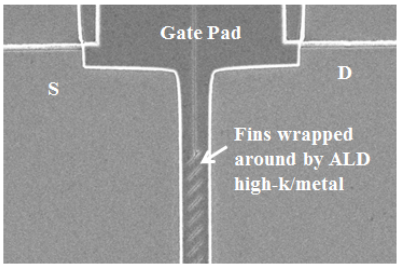
- 50nm undoped $In_{0.53}Ga_{0.47}As$ channel
- 1 nm InP barrier layer
- 7 nm $Al_2O_3$ / 60 nm TiN
- 20 nm N+ layer for Source/Drain

F. Xue and J. Lee, IEEE Trans. On Elec. Devices 7/2014 & IEEE IEDM 12/2012

# 3D InGaAs Gate-Wrap-Around FETs

- SEM images of InGaAs GWAFETs

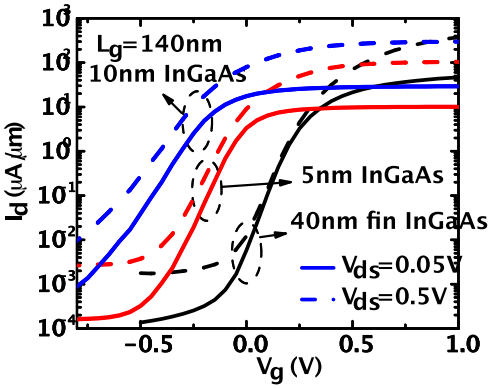



- Devices with $W_{fin}$ from 40 nm to 200 nm, the gate length of 140 nm and 280 nm, and various numbers of parallel channels were fabricated.

F. Xue and J. Lee, IEEE Trans. On Elec. Devices 7/2014 & IEEE IEDM 12/2012

# Comparison of Scalability




| InGaAs FETs | DIBL (mV/V) | SS (mA/dec) |
|---|---|---|
| GWA $W_{fin}$=40nm | 20 | 90 |
| Planar 5nm Channel | 121 | 100 |
| Planar 10nm Channel | 206 | 135 |

- Better scalability was achieved by GWAFETs compare to planar structure with lower DIBL and SS.
- SS is limited by the interface at high-k and InGaAs.

F. Xue and J. Lee, IEEE Trans. On Elec. Devices 7/2014 & IEEE IEDM 12/2012

# 3D InGaAs Gate-Wrap-Around FETs

| Device | Dielectric | $L_g$ (nm) | $W_{fin}$ (nm) | $I_{on}$ (μA/μm) | $I_{off}$ (nA/μm) | DIBL (mV/V) | SS (mV/dec) |
|---|---|---|---|---|---|---|---|
| $In_{0.53}Ga_{0.47}As$ GWAFET (This work) | 7nm ALD $Al_2O_3$/ 1nm InP | 140 | 40 | 600 ($V_d$=1V, $V_g$-$V_{th}$=1V) | 6 ($V_d$=1V) | 20 | 90 ($V_d$=0.5V) |
| $In_{0.53}Ga_{0.47}As$ GAAFET (Purdue, IEDM 2011) | 10nm ALD $Al_2O_3$ | 50 | 30 | 450 ($V_d$=1V, $V_g$-$V_{th}$=1V) | 4000 ($V_d$=1V) | 210 | 150 |
| | | 110 | 30 | 355 ($V_d$=1V, $V_g$-$V_{th}$=1V) | 4000 ($V_d$=1V) | 180 | 140 |
| $In_{0.53}Ga_{0.47}As$ Tri-gate FET (Intel, IEDM 2011) | High-k Stack EOT=12Å | 60 | 40 | 360 ($V_d$=0.5V, $V_g$=0.5V) | 100 ($V_d$=0.5V) | 65 | 100 ($V_d$=0.5V) |
| | | 120 | 30 | -- | -- | 35 | 85 ($V_d$=0.5V) |
| $In_{0.7}Ga_{0.3}As$ FinFET (NUS, EDL 2011 ) | 19nm MOCVD HfAlO | 130 | 220 | 220 ($V_d$=1V, $V_g$-$V_{th}$=1V) | 10 ($V_d$=1.2V) | 135 | 230 |
| $In_{0.7}Ga_{0.3}As$ Planer QWFET (UT, EDL 2012) | 6nm ALD $Al_2O_3$/ 1nm InP | 40 | -- | 476 ($V_d$=1V, $V_g$-$V_{th}$=1V) | 100 ($V_d$=1V) | 270 | 140 |
| | | 130 | -- | 430 ($V_d$=1V, $V_g$-$V_{th}$=1V) | 100 ($V_d$=1V) | 206 | 135 |

F. Xue and J. Lee, IEEE Trans. On Elec. Devices 7/2014 & IEEE IEDM 12/2012

## Summary

- FinFETs are needed for 22nm and beyond
- Fabrication processes of bulk-FinFETs and SOI-FinFETs using self-aligned double patterning (SADP) have been developed successfully
- Both bulk-FinFETs and SOI-FinFETs are in development and production. Both have been compared in terms of process complexity, cost, temperature effects, variability; as well as vertical fins vs. tapered fins (e.g. Structural Stability, Corner Effects, S/D Doping, Mobility)

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## Summary

- Width quantization imposes some challenges on circuit design, especially for analog applications
- Threshold voltage tuning / multiple $V_T$ is an important issue, which involves consideration of doped vs. undoped channel, QM effects, asymmetrical $t_{ox}$, implant/diffused aluminum and cap oxide schemes, gate workfunction control, etc…
- Channel orientation issues:
  (110) sidewall planes → better hole mobility
  (100) sidewall planes → better electron mobility
  Hybrid orientation scheme might be difficult to implement in practice
- FinFET is applicable to analog circuit and mixed-signal applications

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