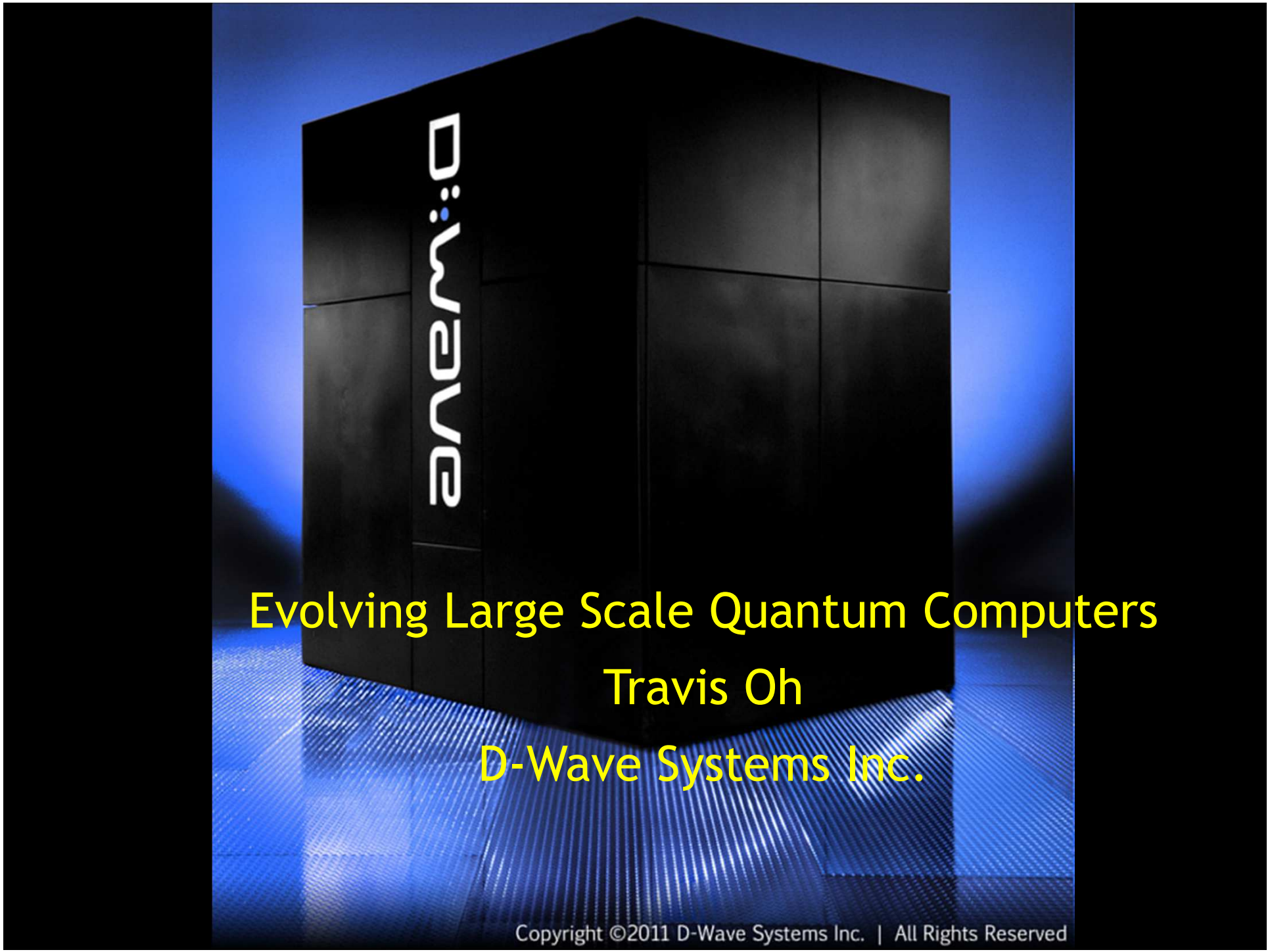
Evolving Large Scale Quantum Computers
Travis Oh
D-Wave Systems Inc.
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Agenda

- What is Quantum Computer?
- What do we do with it?
- Applications
- How do we Fabricate?

What is Quantum Computing

Computational paradigm shift from binary “bits” of information to “quantum bits”

How well can you draw the sun with black and white color?

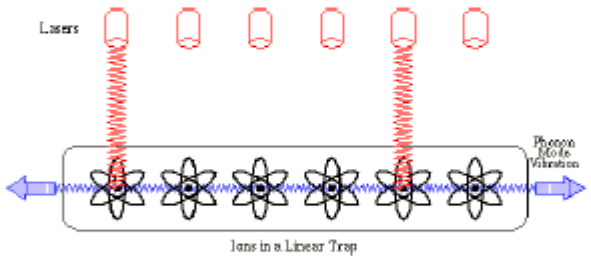
This is a red and yellow model of the sun

“Picture of the Sun” Markers, 2005, 8.5x11,
Tyson Rose, age 13 months

Quantum Parallelism ⇒ Massive Computational Parallelism

Quantum Register

2^n numbers



A 300 qubit register could hold more numbers simultaneously than there are atoms in the known Universe!

=

Equivalent Classical Registers

00000000

00000001

•
•
•

11111111

Factoring a 200 digit number
- classical - 3 billion MIPS-years
- quantum - one second

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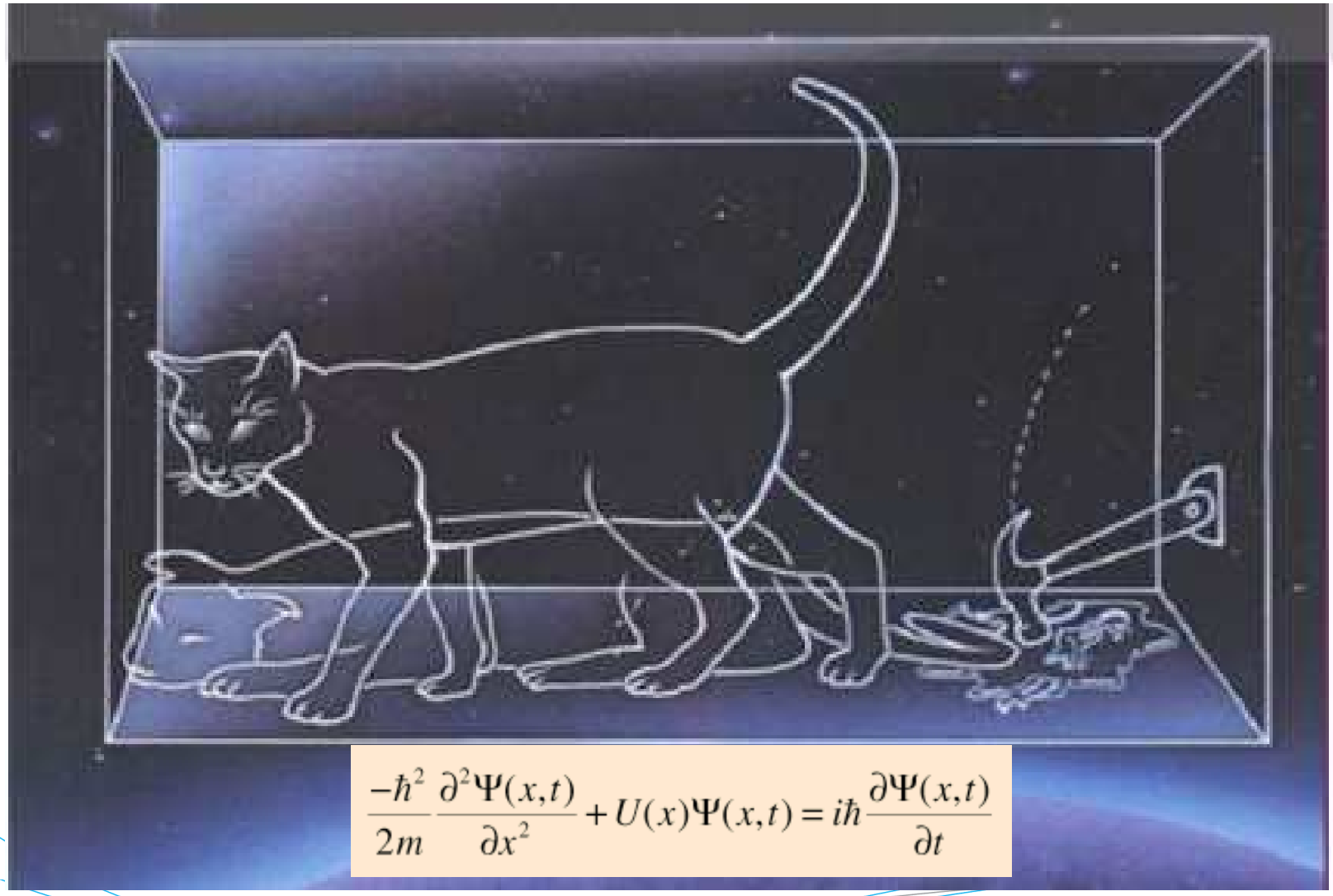
Quantum Computing … A New Way of Harnessing Nature



$$\frac{-\hbar^2}{2m}\frac{\partial^2\Psi(x,t)}{\partial x^2} + U(x)\Psi(x,t) = i\hbar\frac{\partial\Psi(x,t)}{\partial t}$$

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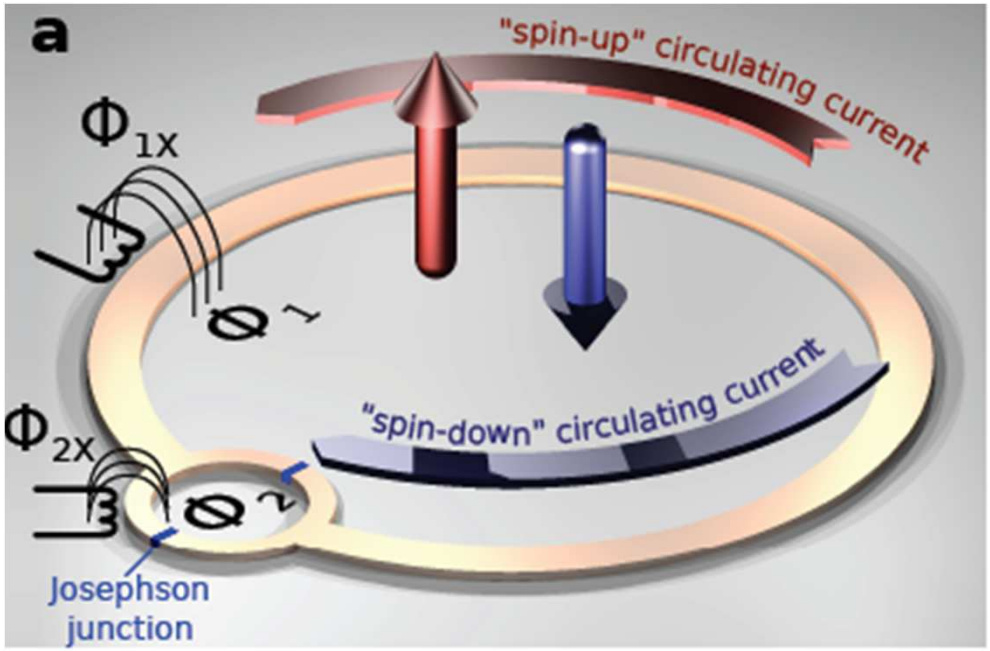
Schrodinger's Cat Lives!



A macroscopic object in two states at once

The basis of a scalable, macroscopic, quantum processor

Detection of a Schrödinger's Cat State in an rf-SQUID

Jonathan R. Friedman, Vijay Patel, W. Chen, S. K. Tolpygo & J. E. Lukens
Department of Physics and Astronomy, The State University of New York at Stony Brook, Stony Brook, NY 11794-3800
(April 19, 2000)

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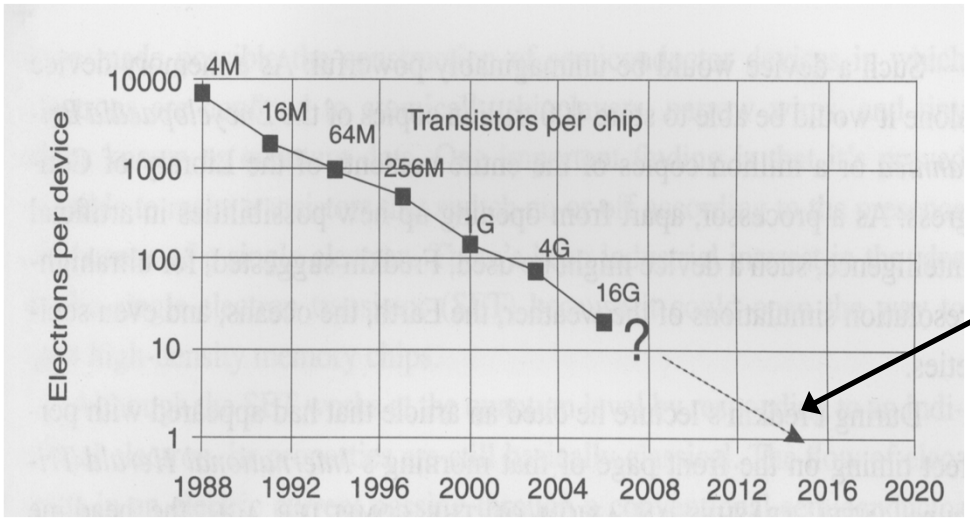
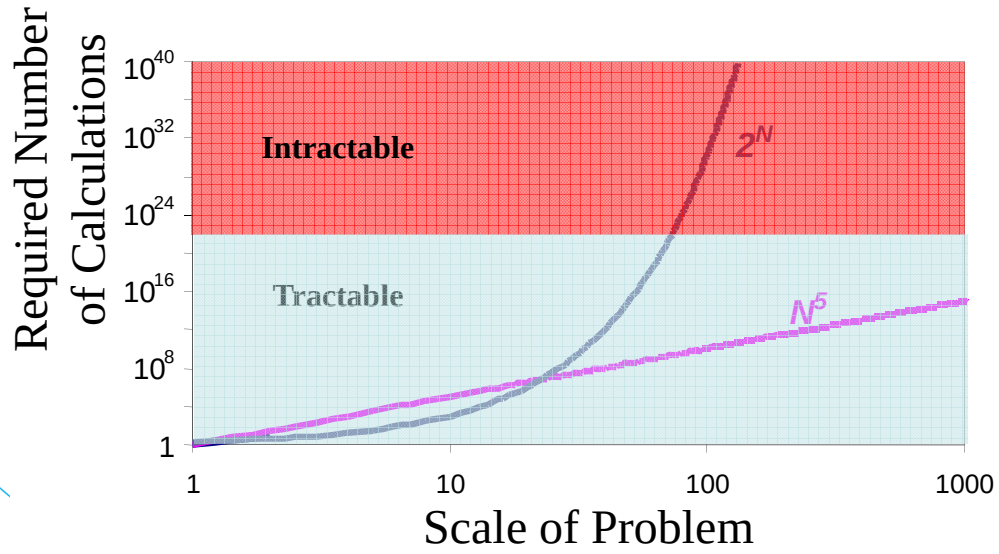
Classical Computing systems approaching hard limits



Components Rapidly approaching atomic dimensions - natural limit



Tractable ≡ PetaFLOPS (10^{15}) computer operating for 1 year

Certain Problems Will Remain Beyond The Reach of any Classical Computers

- **Simulation of quantum systems – chemistry/Bio**
- **Complex combinatorial optimization – AI**
- **Factoring large numbers – code breaking**

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Supercomputer Capabilities and Applications

Year	Supercomputer	Peak speed (Rmax)	Location	Power Co	Cost
				MW	$M
2008	IBM Roadrunner	1.026 PFLOPS	New Mexico, USA	2	100
		1.105 PFLOPS		2.4	100
2009	Cray Jaguar	1.759 PFLOPS	Oak Ridge, USA	7	104
2010	Tianhe-IA	2.566 PFLOPS	Tianjin, China	4	90
2011	Fujitsu K computer	10.51 PFLOPS	Kobe, Japan	10	100
2012	IBM Sequoia	16.32 PFLOPS	Livermore, USA	7.9	100
2012	Cray Titan	17.59 PFLOPS	Oak Ridge, USA	8.2	97
2020		Exaflop		~60	???

Note: 10MW can power 10,000 homes

Applications of supercomputers

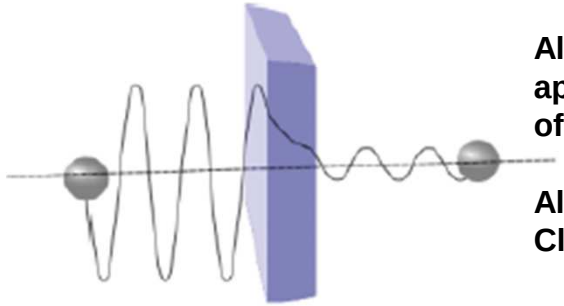
The stages of supercomputer application may be summarized in the following table:

Decade	Uses and computer involved
1970s	Weather forecasting, aerodynamic research (Cray-1).[72]
1980s	Probabilistic analysis,[73] radiation shielding modeling[74] (CDC Cyber).
1990s	Brute force code breaking (EFF DES cracker),[75]
2000s	3D nuclear test simulations as a substitute for legal conduct Nuclear Proliferation Treaty (ASCI Q).[76]
2010s	Molecular Dynamics Simulation (Tianhe-1A)[77]

Above data from WIKI

The palette of quantum phenomenon
Harnessing new resources

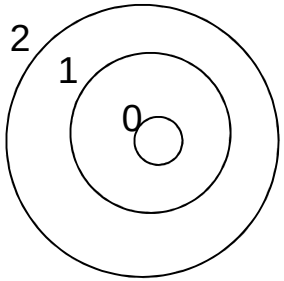
Quantum Tunneling



Allows an object to
appear on the other side
of a barrier it cannot penetrate

Allows chemical reactions impossible
Classically - speeds evolution

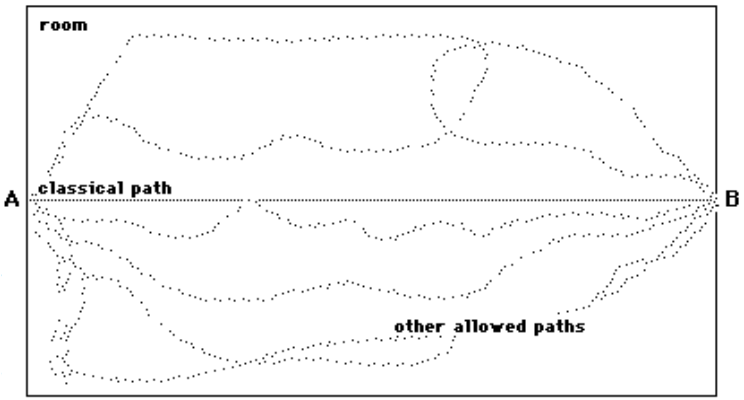
Energy Level Quantization



Electrons can only
Exist in discrete energy
States

Go from one state to the
Other without traversing
Intervening space

Superposition



A single quantum
object can evolve
along multiple paths
simultaneously

Allows for massive
parallelism in calculation

Entanglement

Distant, unconnected events are perfectly
correlated

More information transfer than possible
Classically - greatly improves efficiency

Teleportation

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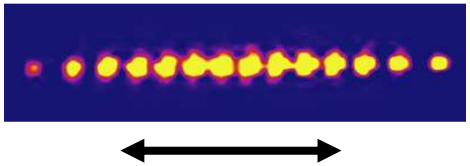
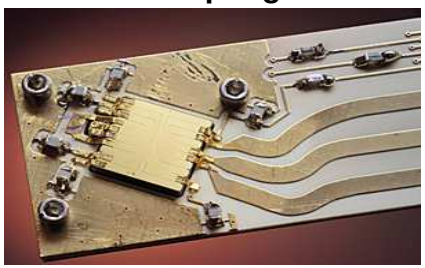
Quantum Computers Today
D-Wave has only scalable quantum processor

Trapped ions in linear Paul trap



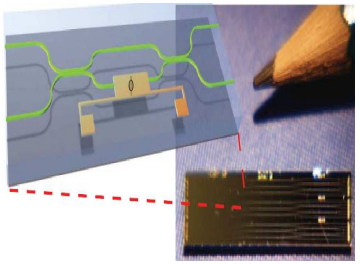
TODAY: World record of 14 entangled trapped ion qubits. Architecture not scalable.

New trapped ion quantum chip with microwave coupling

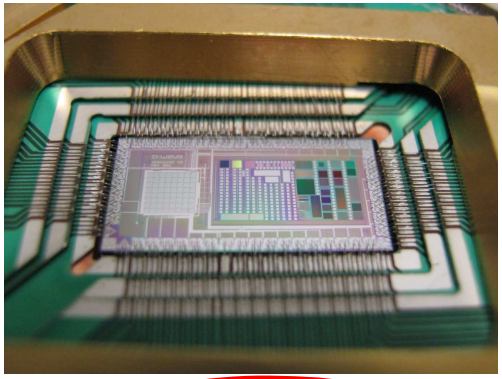


TODAY: A 2 qubit gold ion trap on aluminum nitride backing. Two ions hover above the middle of the square gold trap, which measures 7.4 millimeters on a side. The ions are manipulated and entangled using microwaves fed into wires on the trap from the three thick electrodes at the lower right[1].

Photonic quantum chip

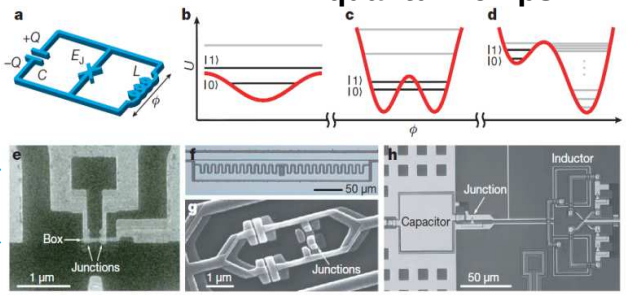


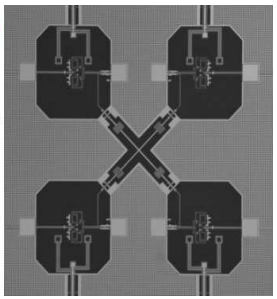
TODAY: A 10-qubit photonic chip containing 10 silica waveguide interferometers with thermo-optic controlled phase shifts for photonic quantum gates. Green lines show optical waveguides; yellow components are metallic contacts. Pencil tip shown for scale[2].



TODAY: DW-2 Rainier 500-qubit fully controllable chip.

Conventional superconducting quantum chips





TODAY: 3-qubit entanglement has been demonstrated in superconducting qubits[3].

Charge-based qubit (Schoelkopf)

Flux-based qubit (Mooij)

Phase-based qubit (Martinis)

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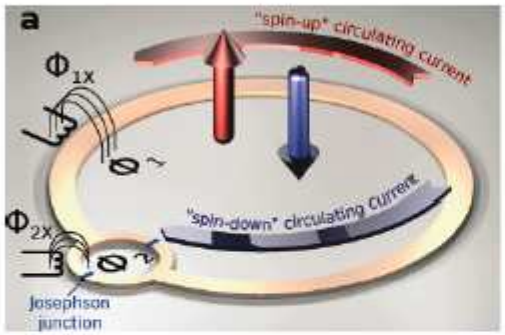
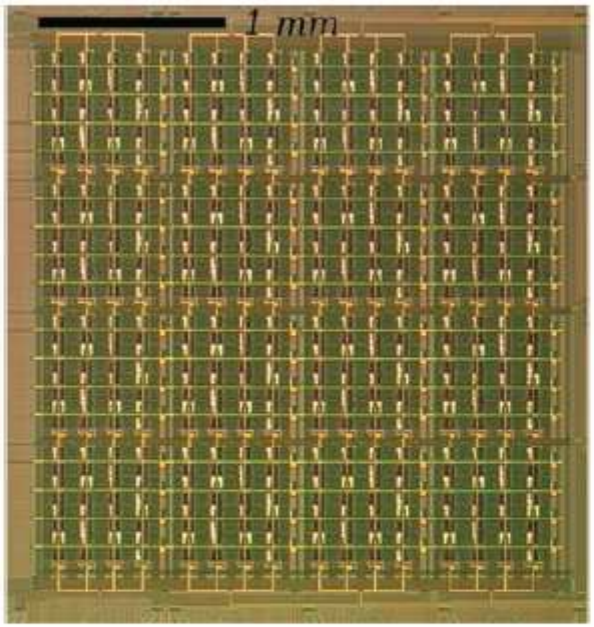
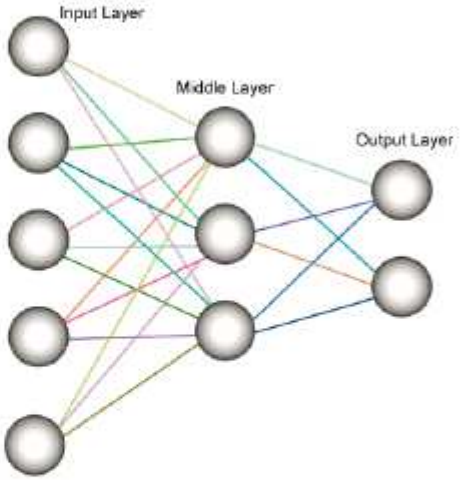
D-Wave's Scalable, Quantum Processor Architecture
A System of Programmable Interacting (Artificial) Spins



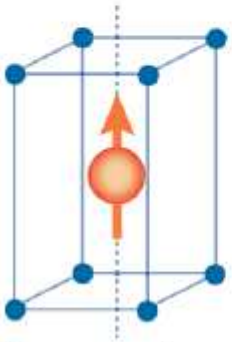
Artificial D-Wave Spin: RF SQUID



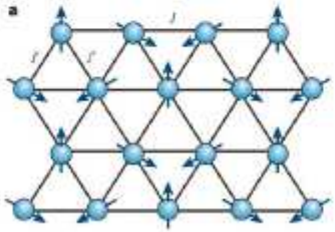
D-Wave Fully Programmable Quantum Spin Computer



Similar structure to Neural Network …



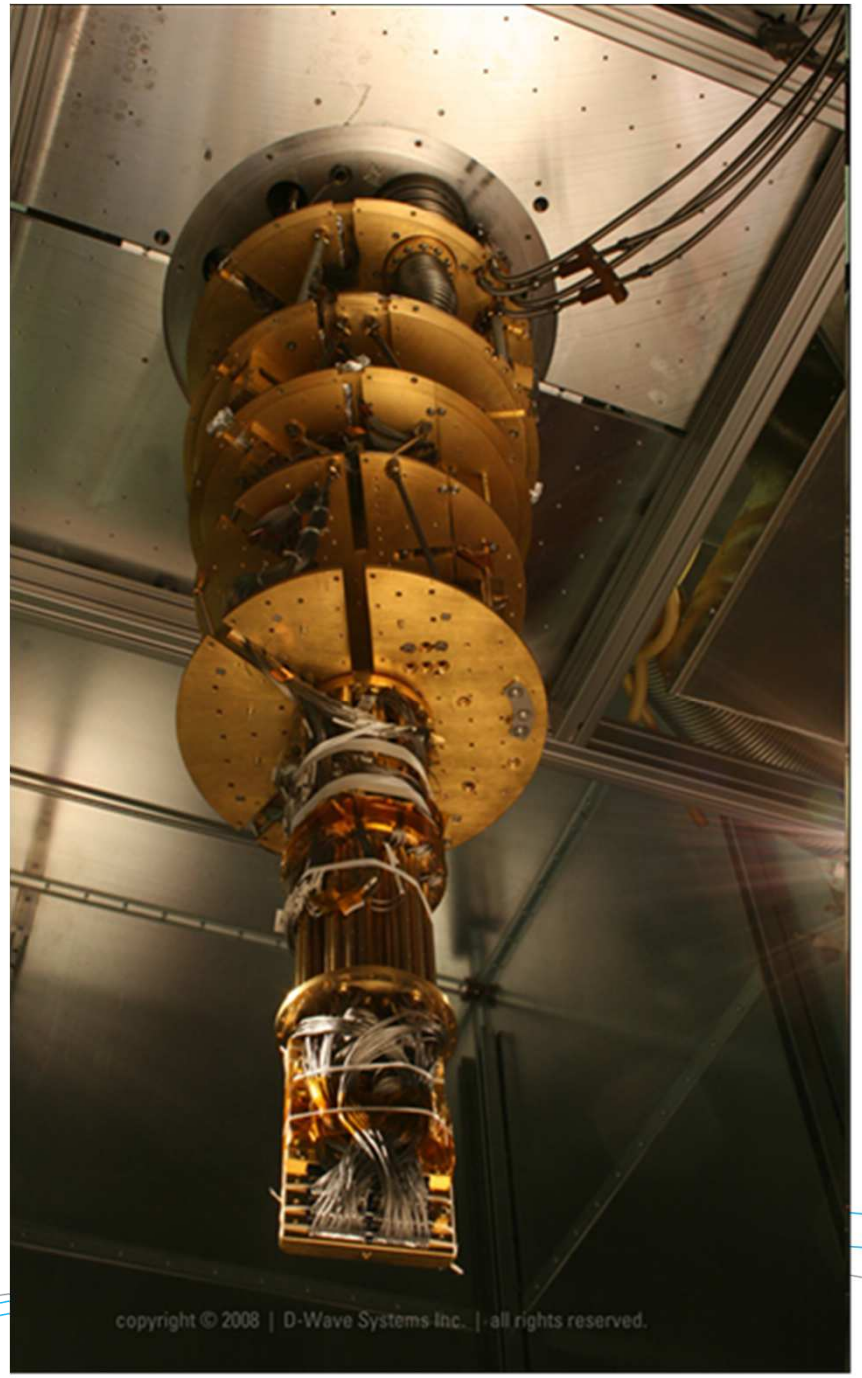
Single magnetic spin In a lattice



Interacting spin lattice

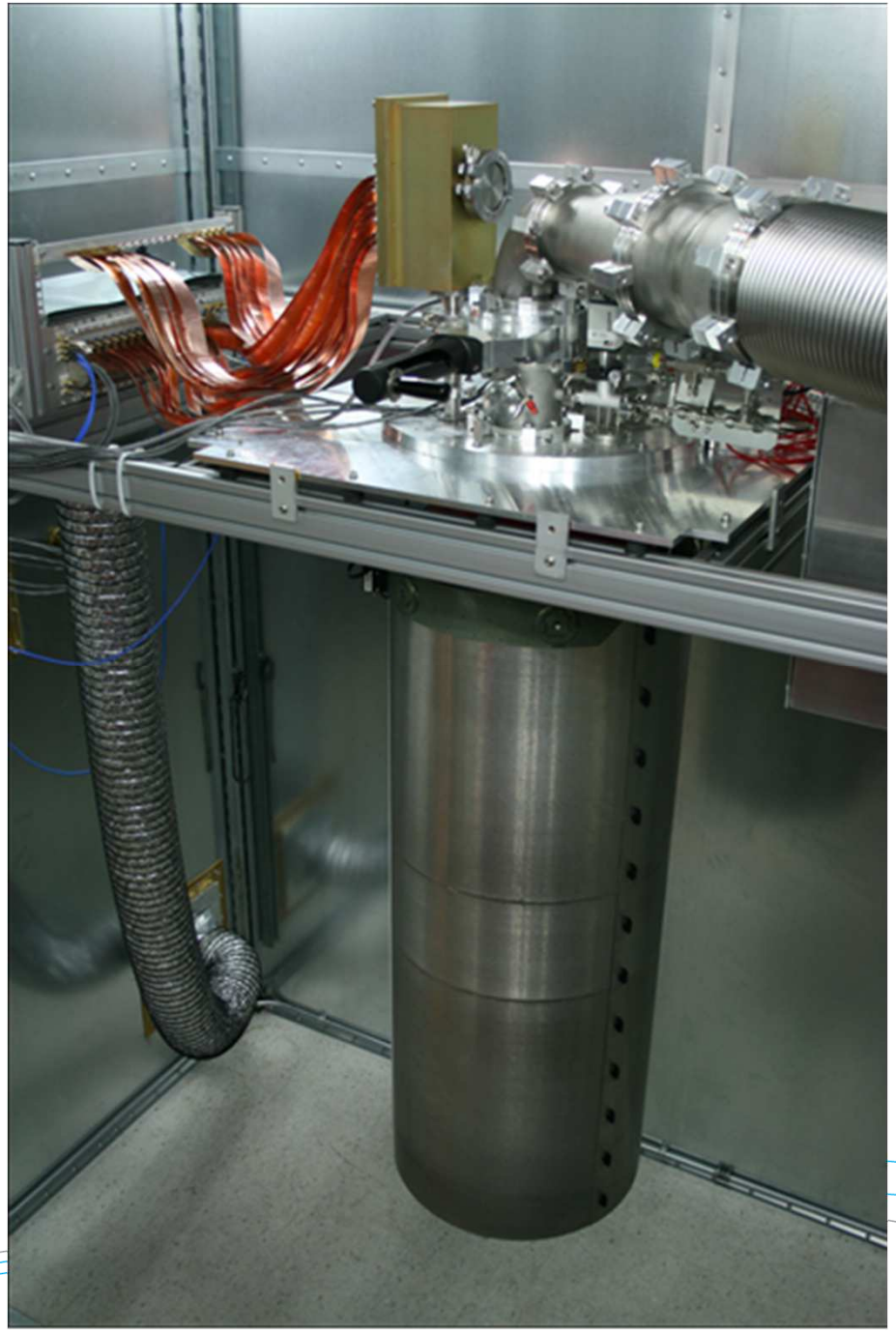
Processor environment

- **196 lines from room temperature to processor**
- **10 kg of metal at 20 milliKelvin; more than 100x colder than interstellar space**
- **1 nanoTesla in 3D across processor; 50,000x less than earth's magnetic field**



Footprint

- ~ 200 square feet
- Closed cycle fridge
- Consumes ~ 7.5 kW



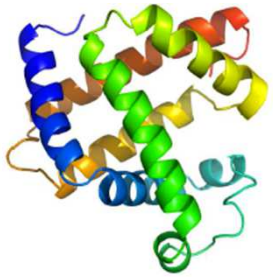
Applications examples:

- **Machine learning (connection to neural computation): AI**
- **Decision problems (NP) – example: factoring (code breaking)**
- **Optimization problems (NP-hard): pattern recognition, protein folding**

Bioinformatics

Image Labeling

Interpreting Text



Protein Structure and Function

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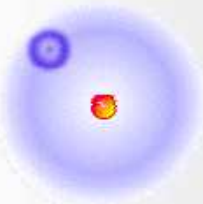
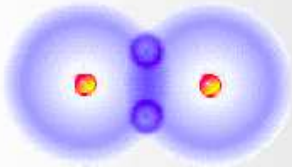
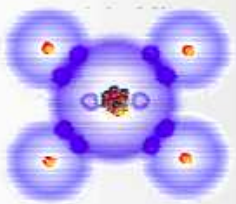
Nanosystem : Hydrogen Atom
Number of Electrons: 1
Number of Equations to Solve: 4
Memory Required, Quantum Computer: 12 qubits
Memory Required, Conventional Computer: 16 bits



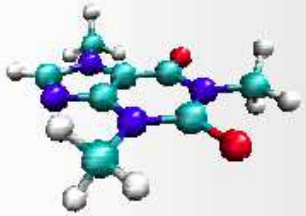
Nanosystem : Hydrogen Molecule
Number of Electrons: 2
Number of Equations to Solve: 16
Memory Required, Quantum Computer: 16 qubits
Memory Required, Conventional Computer: 256 bits



Nanosystem : Methane Molecule
Number of Electrons: 10
Number of Equations to Solve: 1,048,576
Memory Required, Quantum Computer: 48 qubits
Memory Required, Conventional Computer: 1 terabyte



Nanosystem : Caffeine Molecule
Number of Electrons: 102
Number of Equations to Solve: 10^{61}
Memory Required, Quantum Computer: 424 qubits
Memory Required, Conventional Computer: Impossible



Nanosystem : HIV protease binding pocket plus a protease inhibitor molecule
Number of Electrons: 1,000
Number of Equations to Solve: 10^{602}
Memory Required, Quantum Computer: 4,032 qubits
Memory Required, Conventional Computer: Impossible

Simulating even simple molecules will remain beyond the abilities of any conceivable computers that harness only classical information processing

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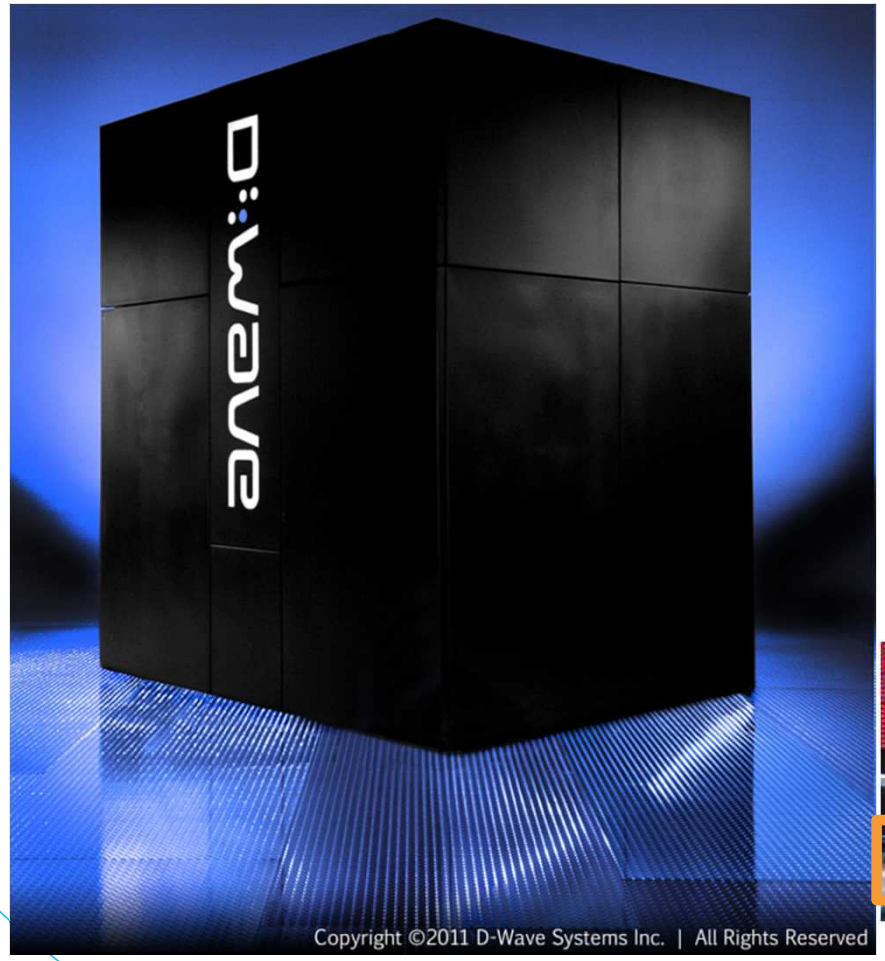
D-Wave One: First Commercial Sale of Quantum Computing System

\\Developing Applications for Classically Hard/Intractable Problems



Integrated 128 Qubit Computing System
Sold to Lockheed Martin/USC ISI

Application Areas

- Machine Learning
- Hard Optimization
- Reversible computation
- Monte Carlo

Google Car Classifier Demo
Neural Net Trained with D-Wave QC Processor

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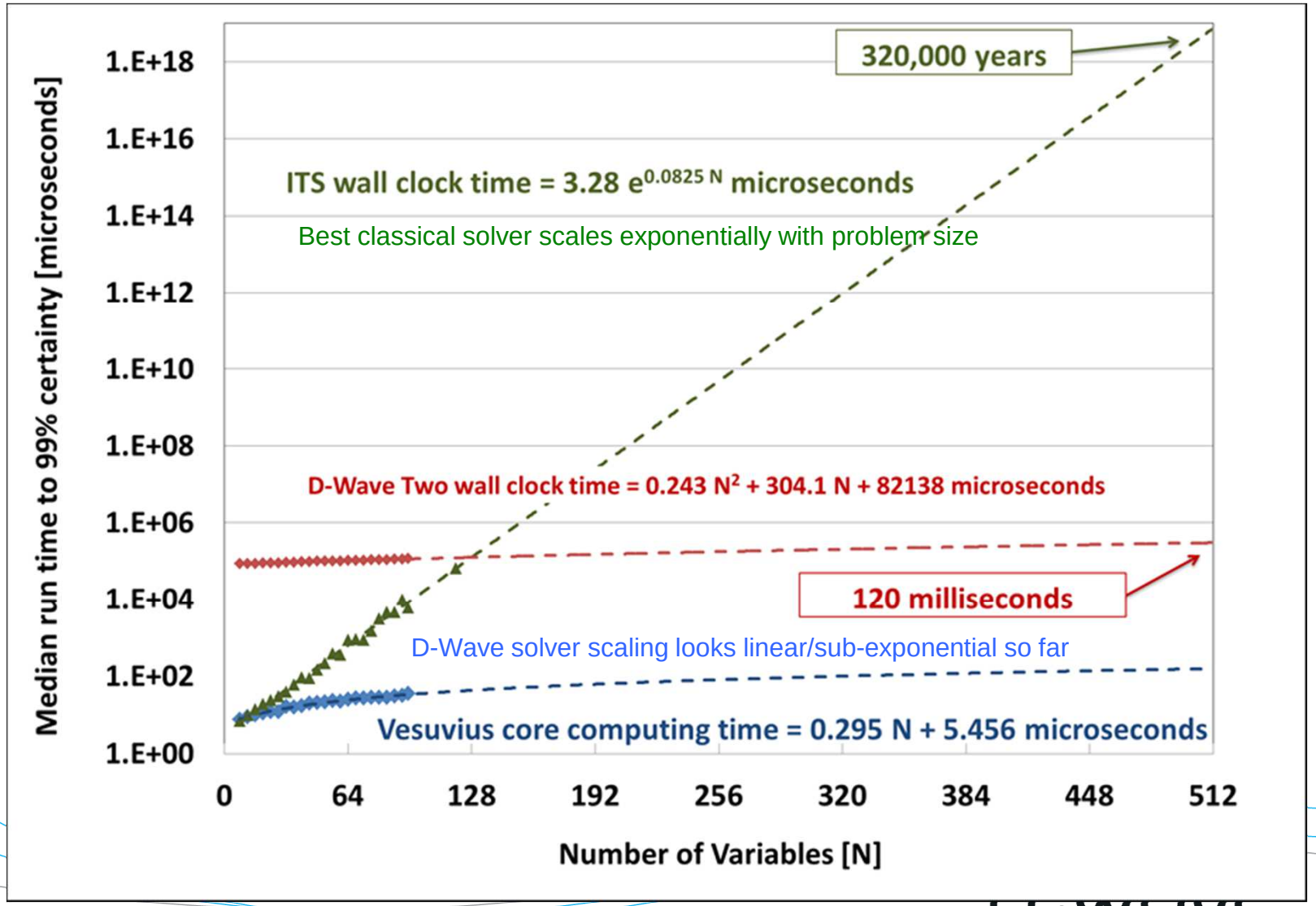
"If you invent a breakthrough in artificial intelligence, so machines can learn," Mr. Gates responded, "that is worth 10 Microsofts."

Bill Gates, quoted in NY Times, March 1, 2004

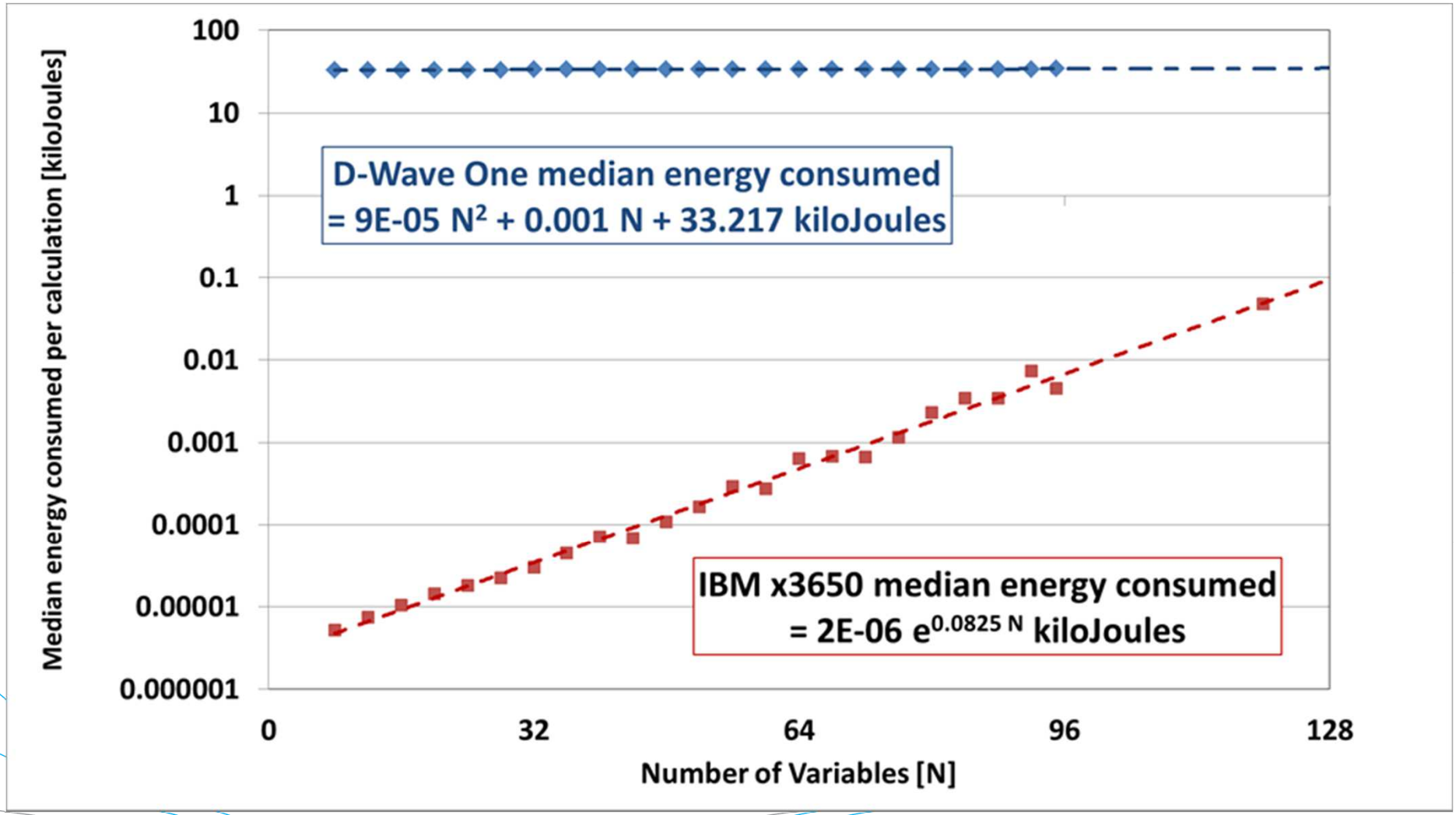
Benchmarking D-Wave Processor Performance

So far time to solution scales like nothing ever seen



Energy Consumption in Classical Computation Prohibitive for hard problems

D-Wave processor power consumption fixed at 7.5kW (cooling cost only)



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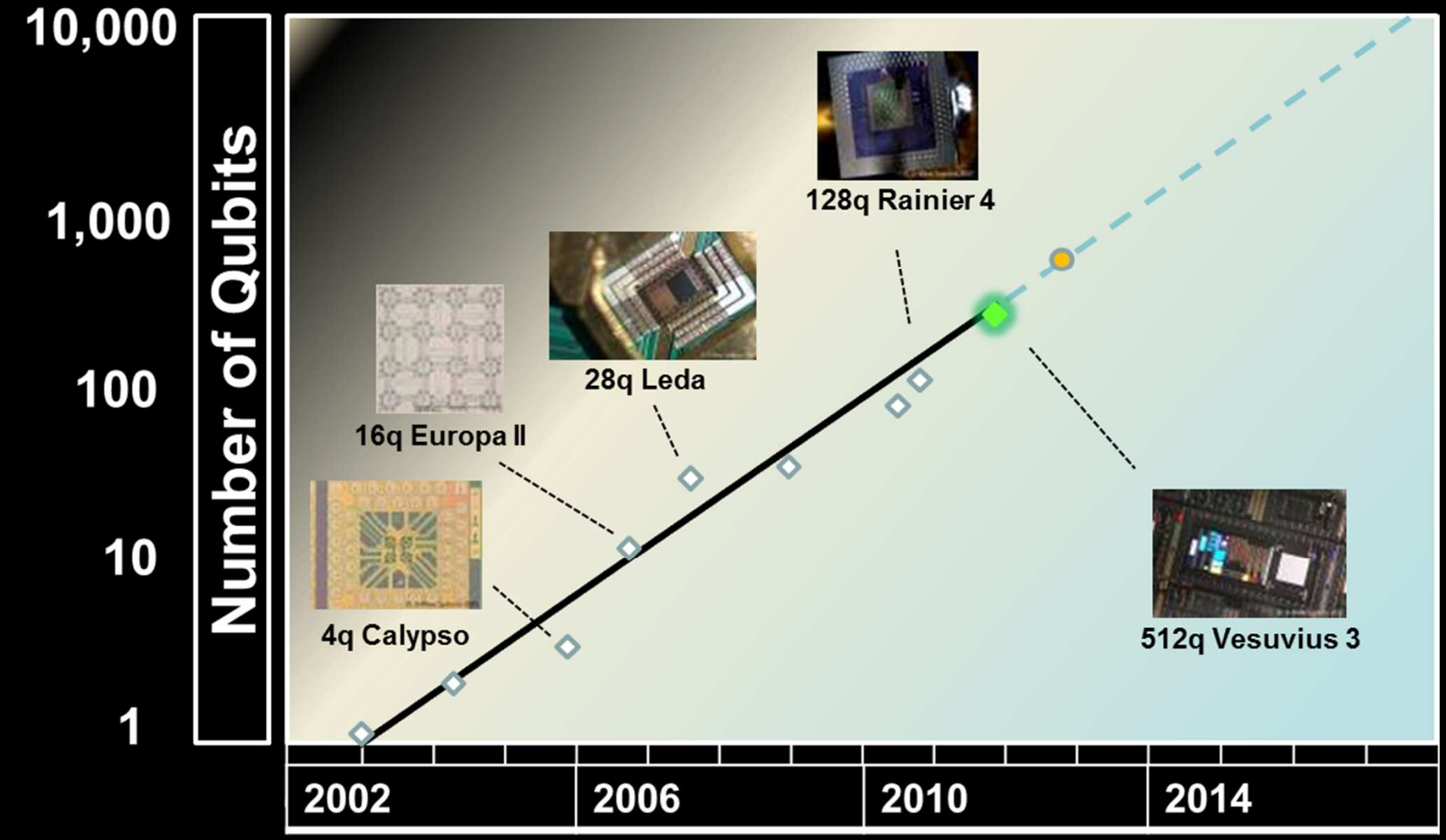
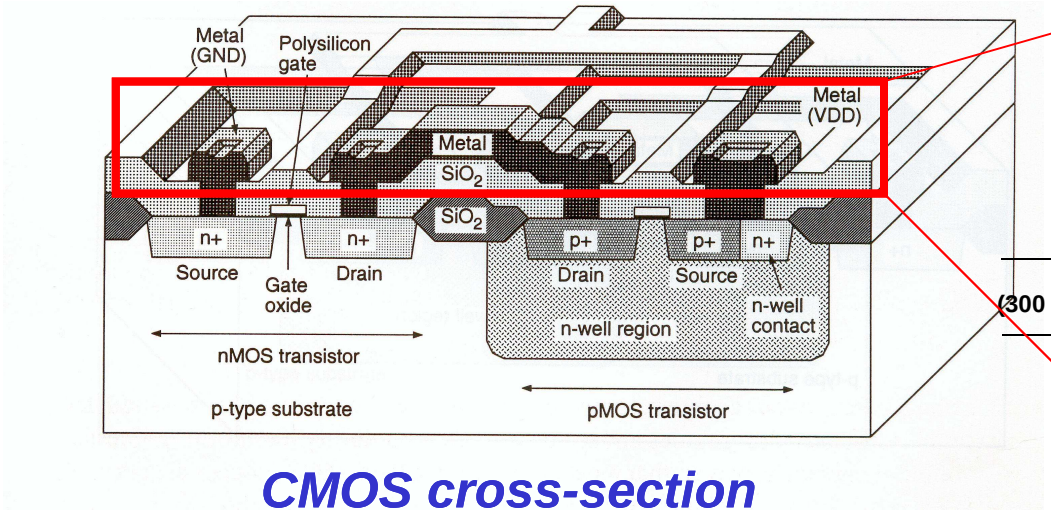
D-Wave Processor Roadmap



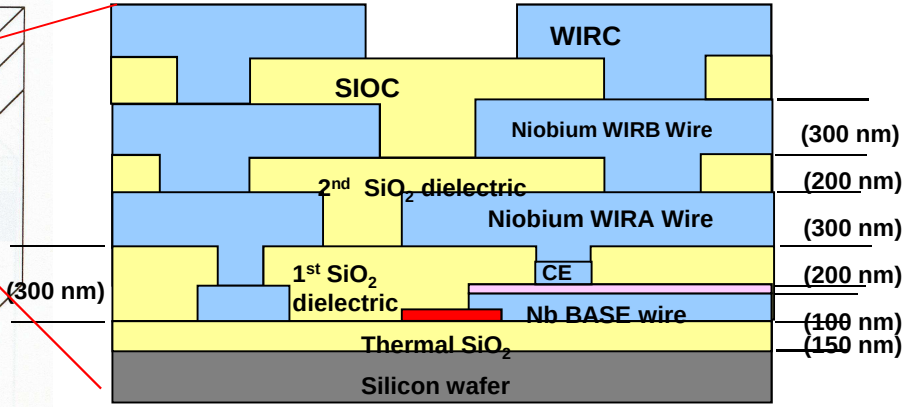
Fabrication

Perspectives on Historical Superconducting Fab Efforts

\\Superconducting Process is just upper wire-up layers in CMOS



CMOS cross-section



SC process cross-section

- **Superconducting process extremely simple compared to standard CMOS**
- just CMOS wire-up process (metals/dielectric stack)
- active device (Nb junction) a simple tunnel-junction .. same AlOx barrier employed in MRAM
- all elements are commodity processes in semiconductor industry
- major challenge to realizing large scale superconducting circuits are defect density, parametric targeting and spreads, going to high yields … all solved by semiconductor industry

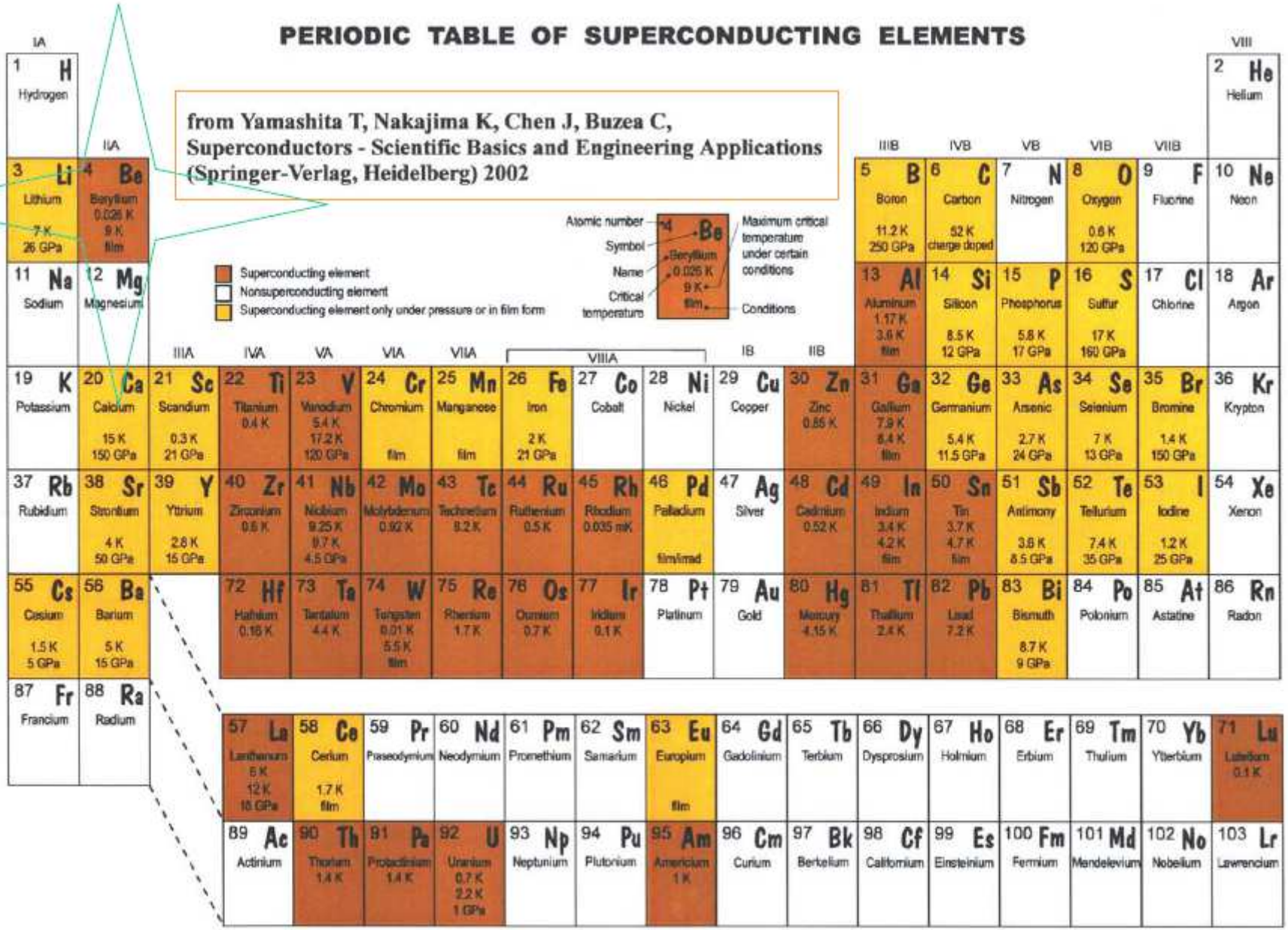
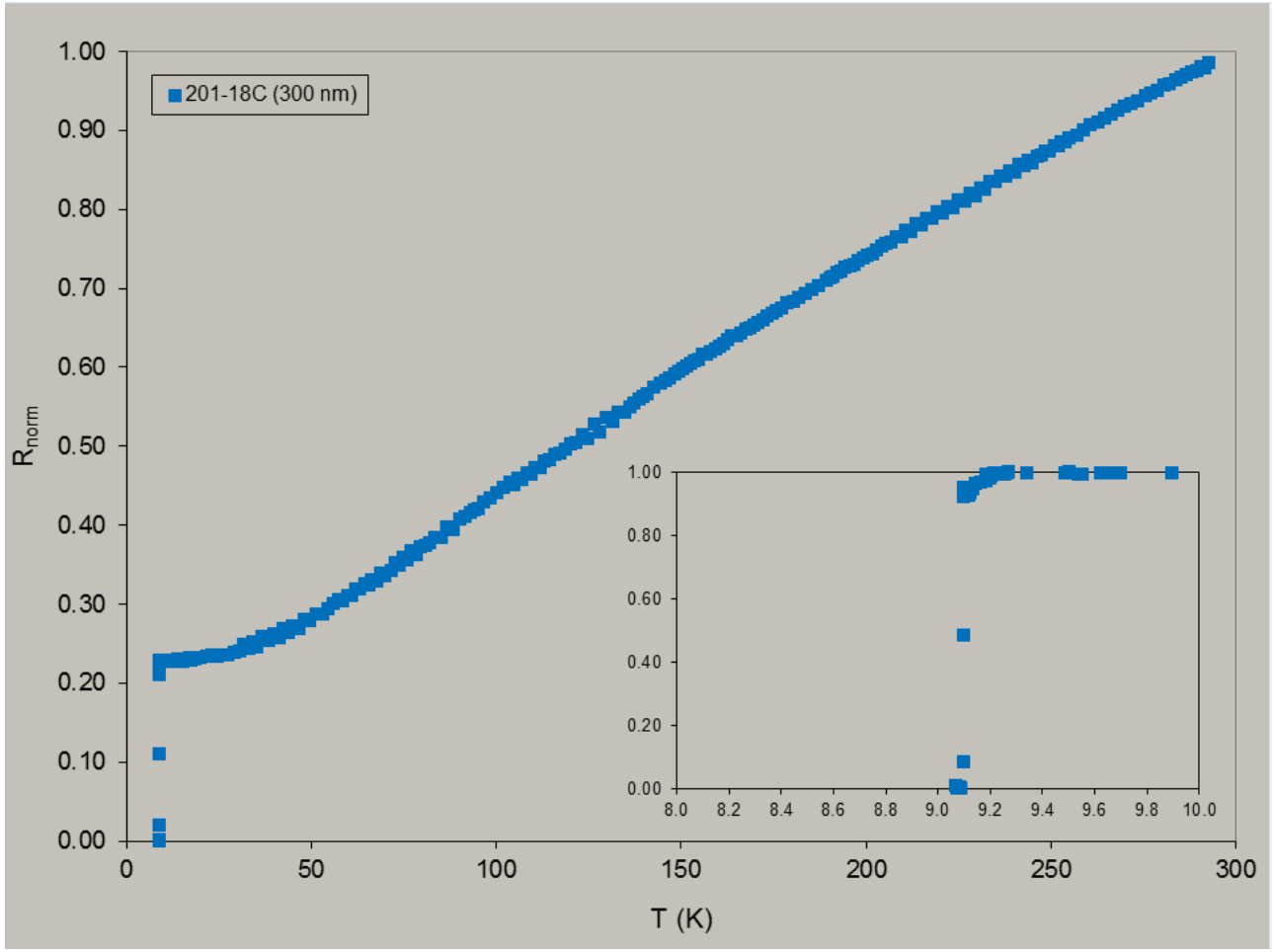


Figure 4. Periodic Table of elements with critical temperature at normal pressure, and maximum critical temperature attained under certain conditions (pressure, film form or charge injected) [Yamashita].

Superconductivity



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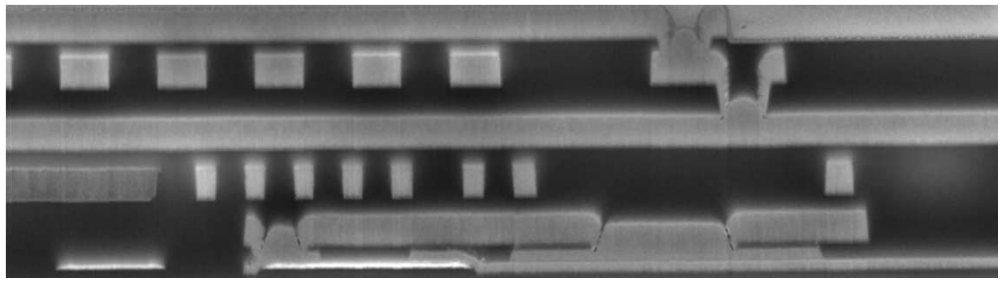
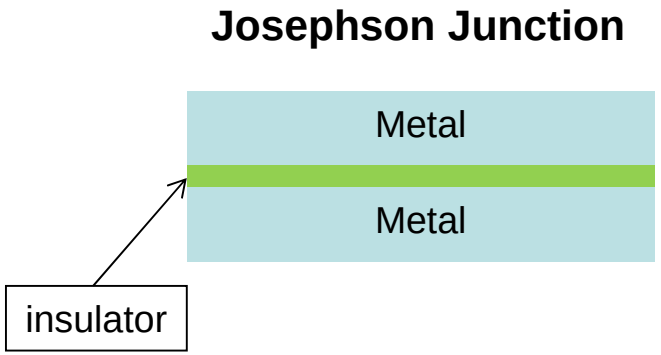
Current D-Wave Process
\\Level of Integration

Achieved 512-qubit level of integration in 6 years of process development

- Fully functional ~50,000 Josephson junctions (active element) SFQ circuits covering 2.8mm x 2.8mm circuit area
- Areal junction density consistent with 10^5 JJ/cm^2; scalable to 10^6 JJ/cm^2 and beyond for standard RSFQ design
- 6 Nb metal layers
- 1 Ti/Pt Resistor layer (Ti is adhesion layer only)
- 5 Planarized dielectric layers (SiO2)
- High-I_c VIA process (10-40mA/µm^2 measured for 0.7x0.7um VIA)
- 10^5 VIAs and 32,000 resistors in single product die



Current D-Wave Process Cross-Section



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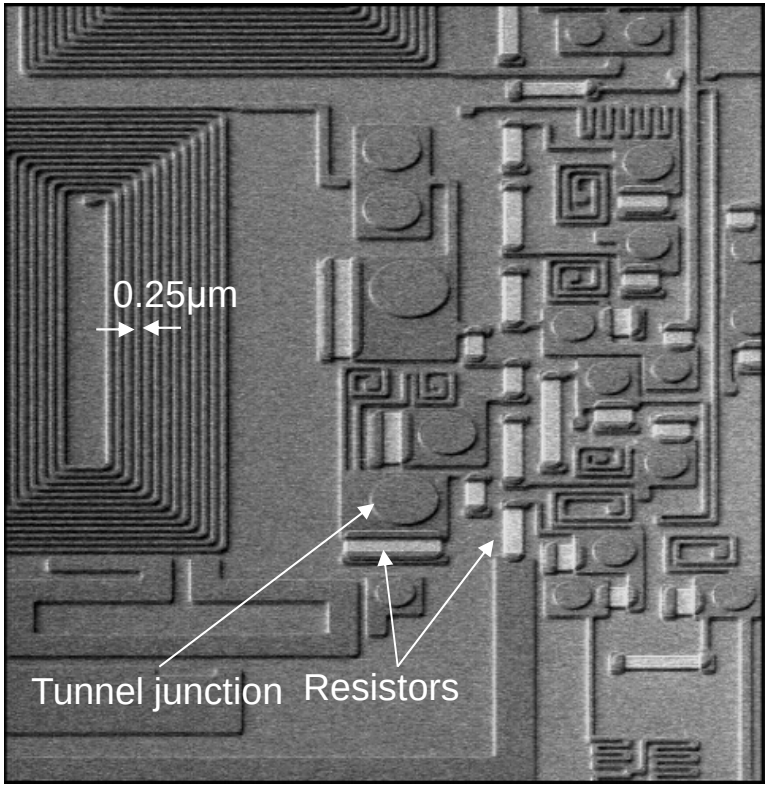
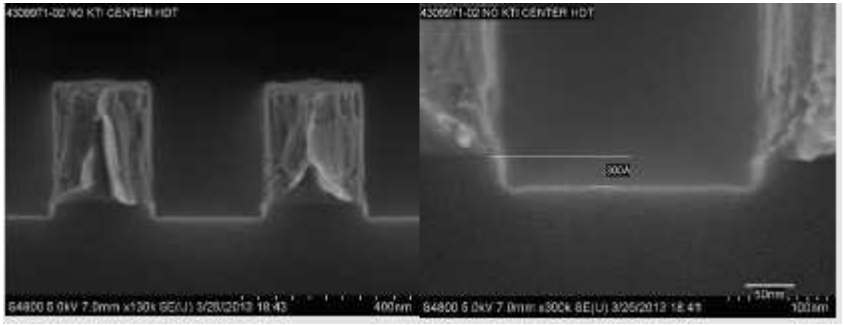
Current D-Wave Process
\\Critical Dimensions



Minimum Critical Dimensions

- 0.25 um Lines and Spaces
- 50nm overlay accuracy
- Josephson Junction (active device) 0.6um +/- 0.2um



Nb etches well with “F” based chemistry in RIE Etcher

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Test Infrastructure

\\Low Temperature Circuit Characteristics from room temp probing

Room Temperature Testing:

D-Wave utilizes Electroglas 4080 and 4090µ tools for wafer-level yield characterization

- All wafers are tested after full processing is completed; in-situ wafer level probing also conducted depending on learning cycle requirements (~30 wafers per month)
- Entire wafer lot (up to 25 200mm wafers) loaded and tested in each run

4K Test Infrastructure:

Developed cryogen-based 4K testing infrastructure capable of testing up to 50 die per week

- Junction parametric extraction for yield analysis and spreads within wafer and wafer-to-wafer
- Penetration depth measurements for inductance extractions and tracking
- VIA I_c and yield for all layers
- Resistor array testing to assess module yield and variability

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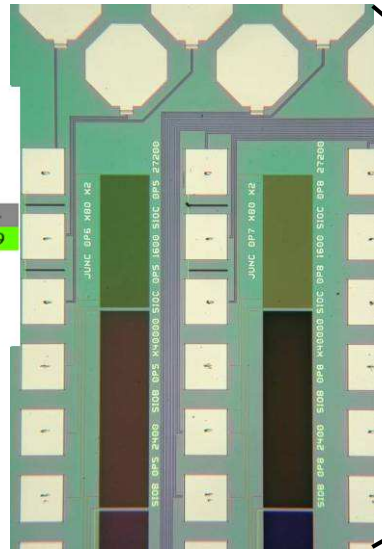
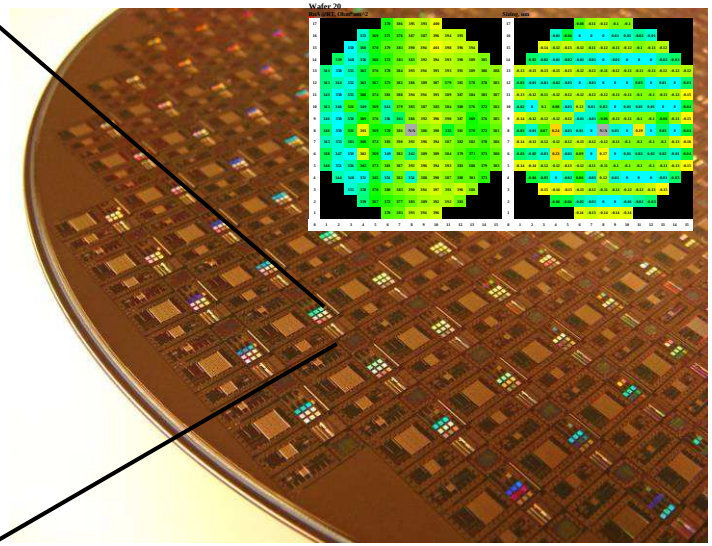
Test Infrastructure

\\Wafer Yield Characterization … Choosing Known Good Die

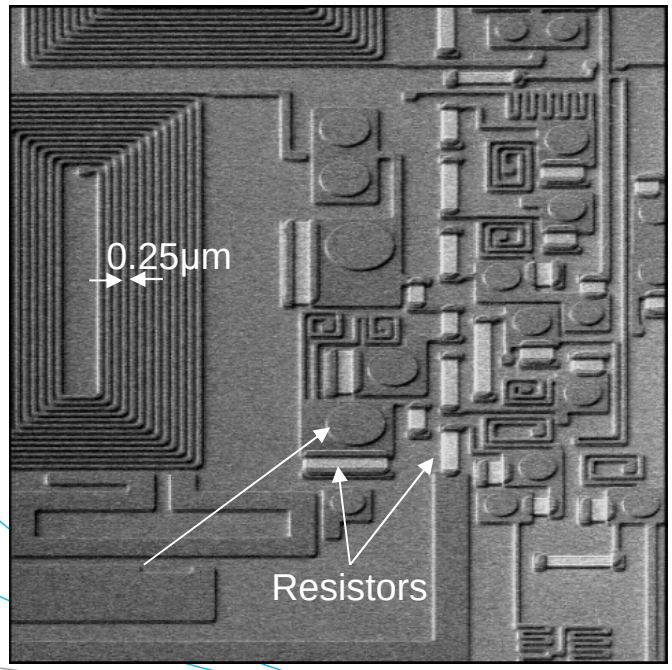
Junction R_nA Distribution

	622	---	617	611	611	612	612	612	607		
			615	612	612	613	615	616	616	618	616	
626	628	623	617	615	614	614	615	619	622	624	626	635
632	632	625	618	615	616	616	618	622	626	628	631	634
633	632	626	619	616	615	616	619	621	626	632	633	641
641	633	626	621	614	616	620	619	622	626	633	635	640
641	636	632	624	620	618	619	620	624	629	634	635	638	649
635	638	633	627	622	621	619	622	624	629	632	633	636	
635	636	635	628	624	622	621	620	623	626	629	631	636	
	633	634	629	625	621	620	620	621	622	627	633		
			635	624	619	618	618	620	624			





Wafer-Level SEM Inspection



PCM Wafer-Level Analysis

D-Wave utilizes extensive process characterization and monitoring structures for electrical and visual inspection of wafer yields.

In-situ metrology tools enable wafer-level visual inspection after each step is completed.

All parametric data assembled into wafer maps for easy known good die selection. Useful visualization tool for yield analysis.

SEM image on the left shows a 0.25µm wire and space DAC storage inductor (left in image) and associated demux circuitry for addressing and programming the DAC (right in image). Image was captured during routine in-situ inspection after BASE and JUNC steps.

D-Wave
The Quantum Computing Company™

Current D-Wave Process Overview

- D-Wave has operated a world-class superconducting foundry, centrally managed and distributed over state-of-the-art facilities in US and British Columbia
- The fully planarized, sub-micron, multilayer process is realized on 200mm wafers with 0.5μm minimum junction sizes, and 0.25μm lines and spaces, high-I_c sub-micron VIA, in a low temperature process
- Our process utilizes industry-standard semiconductor equipment optimized for superconducting processing. The process also uses the most modern tools for in-situ metrology, continuous characterization monitoring, and operational control