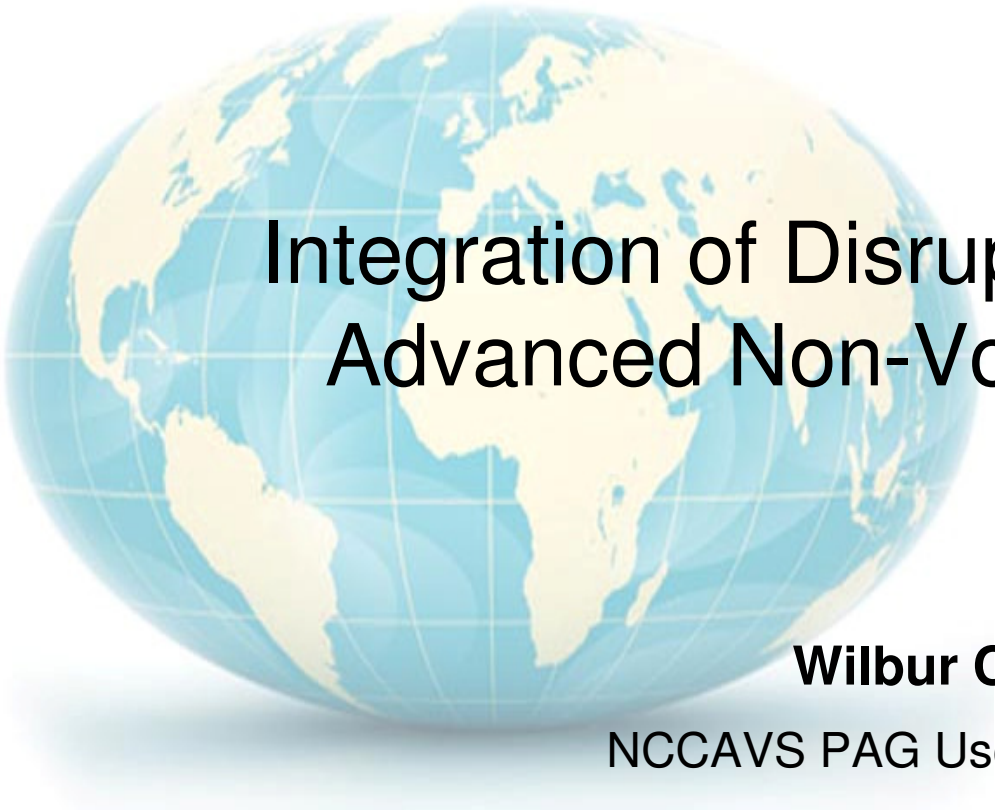
Creating a New Wave of Technology

SPECIALIZED FOUNDRY SERVICES

TELEFUNKEN Semiconductors



Integration of Disruptive Materials for Advanced Non-Volatile Memories

Wilbur Catabay

NCCAVS PAG User Group Meeting

"Plasma Applications in Novel Materials Processing"

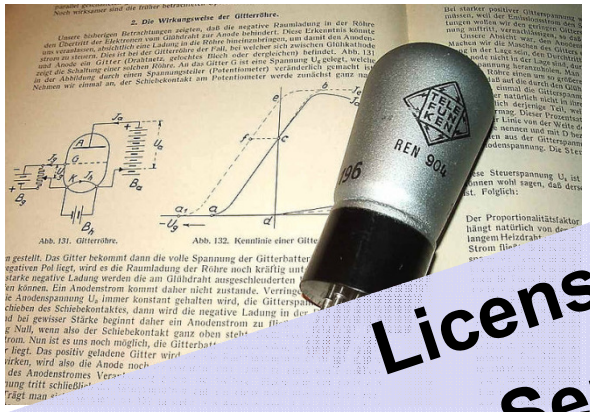
April 29, 2013

Outline

- TSI Semiconductor, TDCS Overview
- Non Volatile Memory Trends
- Solutions for NVM Memory Development
- Process Module Blocks
- Summary

Who is Telefunken

- Who, What is “Telefunken”?
  - German radio and television apparatus company, founded in Berlin in 1903



Licensed the name “Telefunken”
Telefunken Semiconductor International LLC = TSI

Telefunken alarm clock from c. 1995, designed by Philippe Starck

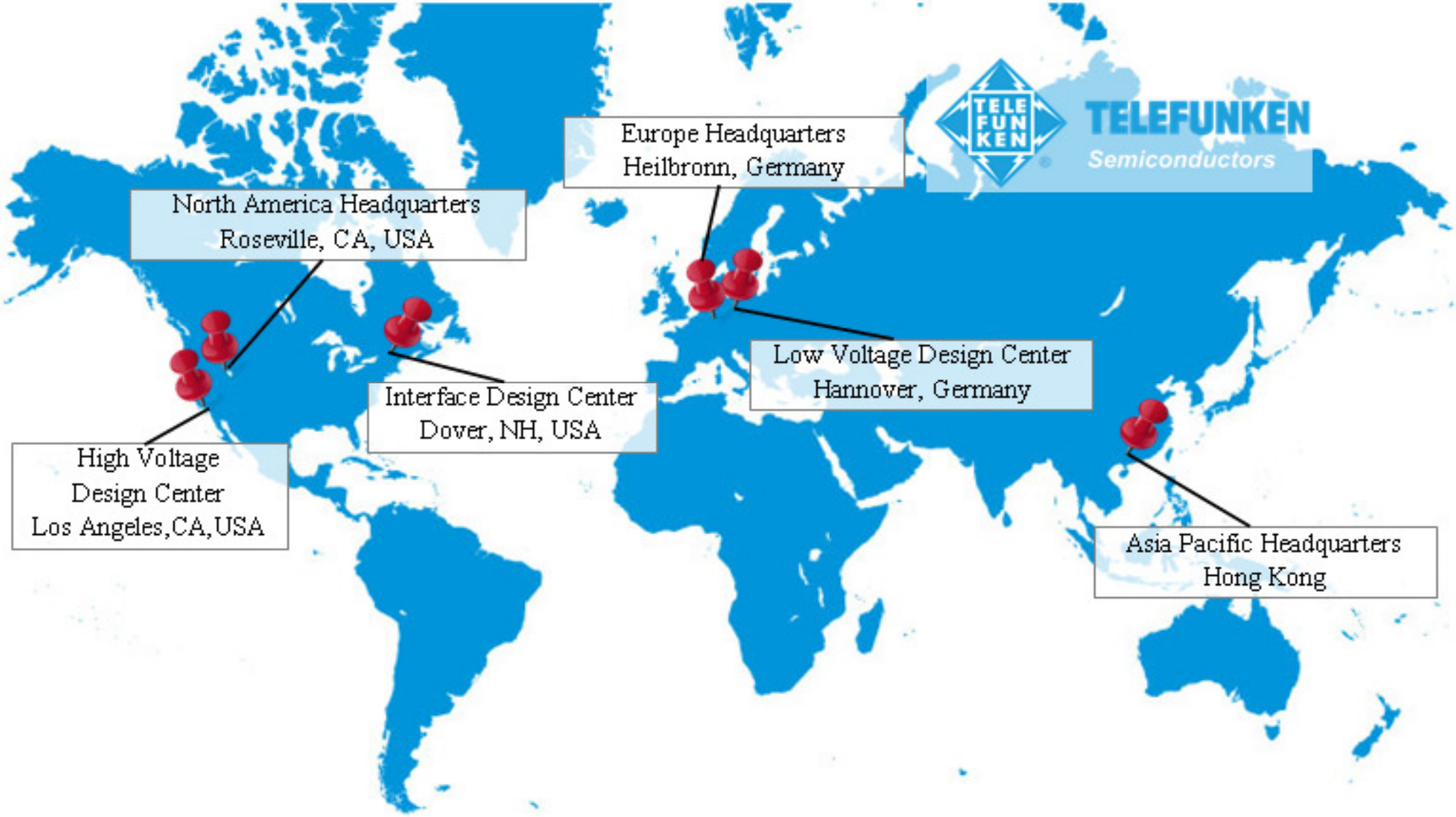
Telefunken water boiling from 2011

A modern Telefunken RC 881 cassette, CD player, and radio

Courtesy of Wiki

TSI Global

TELEFUNKEN Semiconductors International is a US company & Incorporated in State of Delaware



World-Class Foundry Technologies in Smart-Power, Bipolar, High Voltage, Power MOSFET, IGBT, Embedded Flash, and High Frequency Platforms

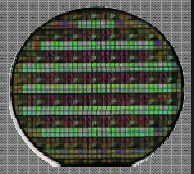
Foundry, Heilbronn, Germany

Foundry & TDCS, Roseville, California
Corporate Headquarters

TDCS – Technology Development & Commercialization Services

Our History

NEC



5-inch K-line Production

6-inch M-line Production

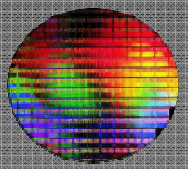
1984 1987 1990

DRAM Production High Volume

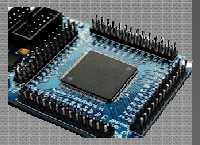
ISO 9000 Certification

RENESAS

Automotive Supplier



8-inch M-line Production



Memory, µprocessor, ASIC's

ISO 14001 Certification

4,500,000

Cumulative 4.5 Million Wafers

ISO / TS 16949 REGISTERED

ISO/TS 16949 Certification

FUNKEN

nductors

May 2011

TSI Semi acquires Renesas Roseville Manufacturing Facility

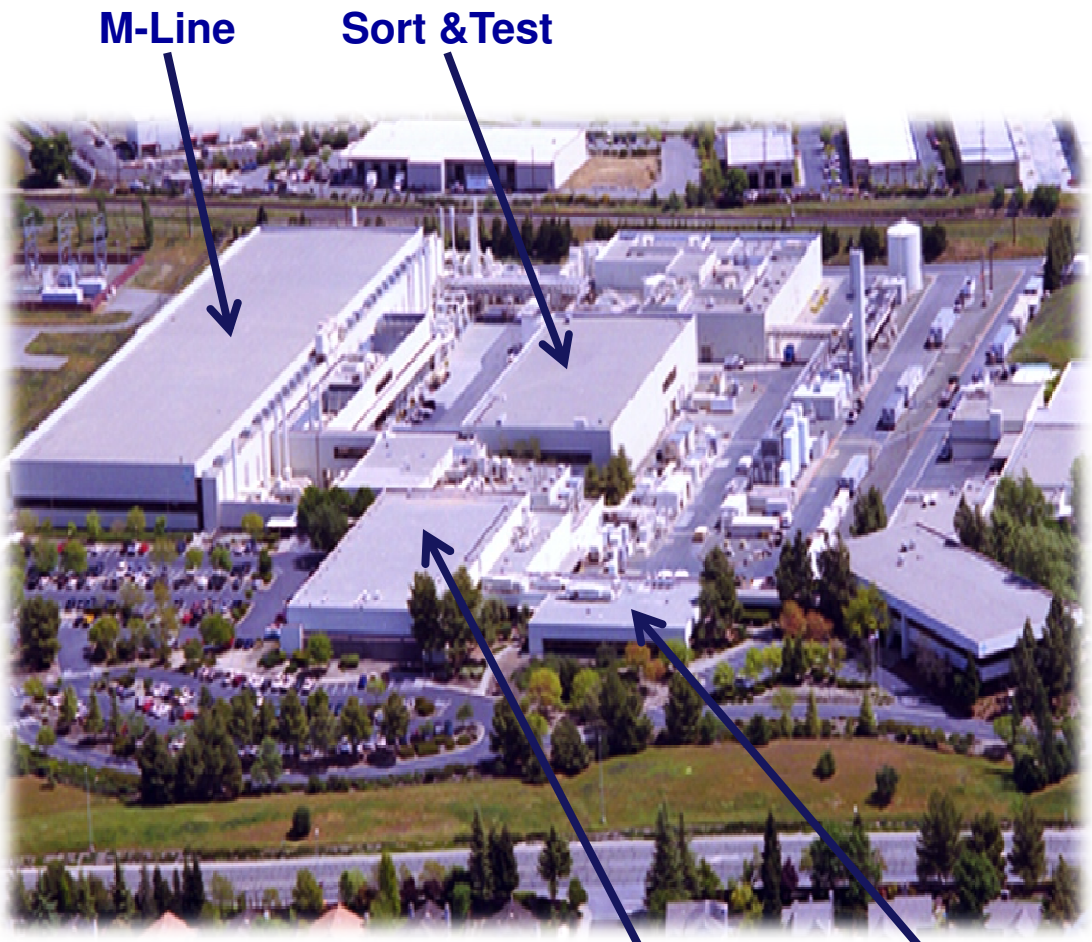
SVTC

TSI Semi Acquires SJ SVTC

or tool

nsion

Roseville Site Overview

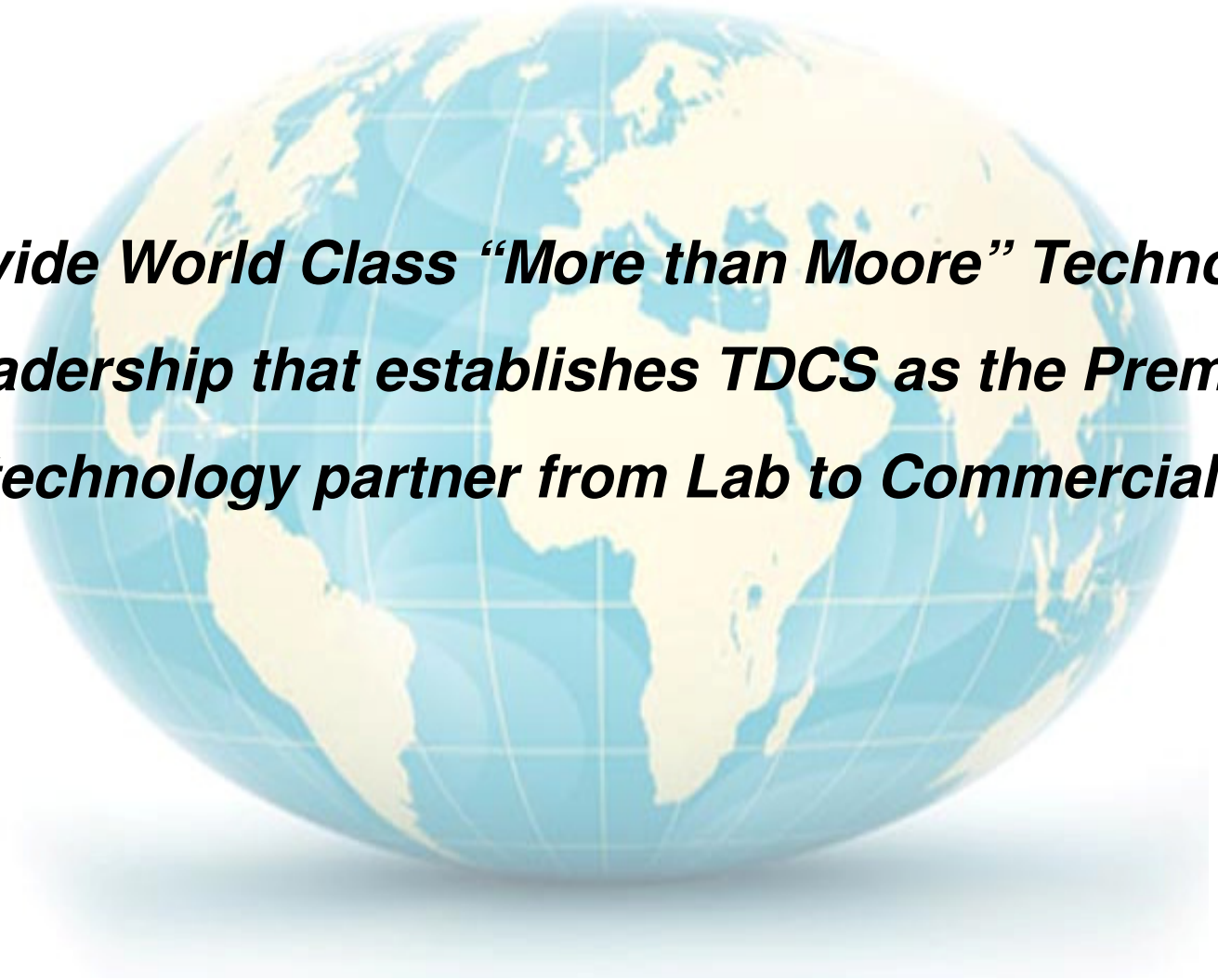


Roseville, California

Capabilities

- Production grade tools in Class 3 Clean Rooms
- 84,000 square feet of Fab Clean Room Space
- *Engineering Consultants and Program Managers*
- 24/7 Engineering, Operations & Maintenance
- Manufacturing Execution Systems (MES)
- IP Secure Environments
- Robust Quality Systems
- Automotive Registered
- Onsite Analytical Tools & Labs
- *Process Library*
- *Novel Materials*
- AlSiCu BEOL
- Lithography Capable to 110nm
- *Transparent Substrates*
- *Emerging Technology Capabilities*

TDCS Mission Statement



Provide World Class "More than Moore" Technology leadership that establishes TDCS as the Premier Nanotechnology partner from Lab to Commercialization

TDCS Range of Services

TDCS provides Technology Development & Commercialization Services in an open and flexible environment.

Infrastructure Access

Access to robust infrastructure for development & manufacturing needs

- R&D Wafer Processing
- Tool Hosting/ Clean Room Rental
- Hands on Access
- Tool Access
- Office Facilities
- Process Library

Engineering

Utilize blended pool of engineering services to support development efforts

- Blended Engineering Pool
- Project Management
- Analytical Services

Manufacturing

Pilot & low volume production or process transfer services to high volume partners

- Custom Process Flows
- Fast Transfer Services
- PDK's for High Voltage, MXS, Analog Devices

Value Chain

Provide total solutions through a network of service and product partners

TOPPAN PHOTOMASKS, INC. · entrepix YOUR CMP PARTNER · MEMC TECHNOLOGY IS BUILT ON US · SINGULUS · CORWIL TECHNOLOGY CORPORATION · SUSS MicroTec

Value Proposition

SPECIALIZED FOUNDRY SERVICES

We create a collaborative relationship with customers to enable the fastest and most cost effective time to market for technology and product commercialization while enabling customer IP independence

Fast Cycles of Learning	Flexible Capability	IP Independence	Cost-Effective Solutions
Technology Development Process	Production Grade Tools	Customer Retained IP	CAPEX Avoidance
Engineering Expertise & Availability	Development Environment	IP Security Processes	Variable Cost Access
Customer Program Management	Support for New Materials	Access to Recipe IP	Integrated Value Chain

Multi-disciplinary Engineering | Operational Excellence | Customer Program Management

BRIDGING THE GAP

SPECIALIZED FOUNDRY SERVICES

TELEFUNKEN Semiconductors

Research | Development | Manufacturing

Outline

- TSI Semiconductor, TDCS Overview
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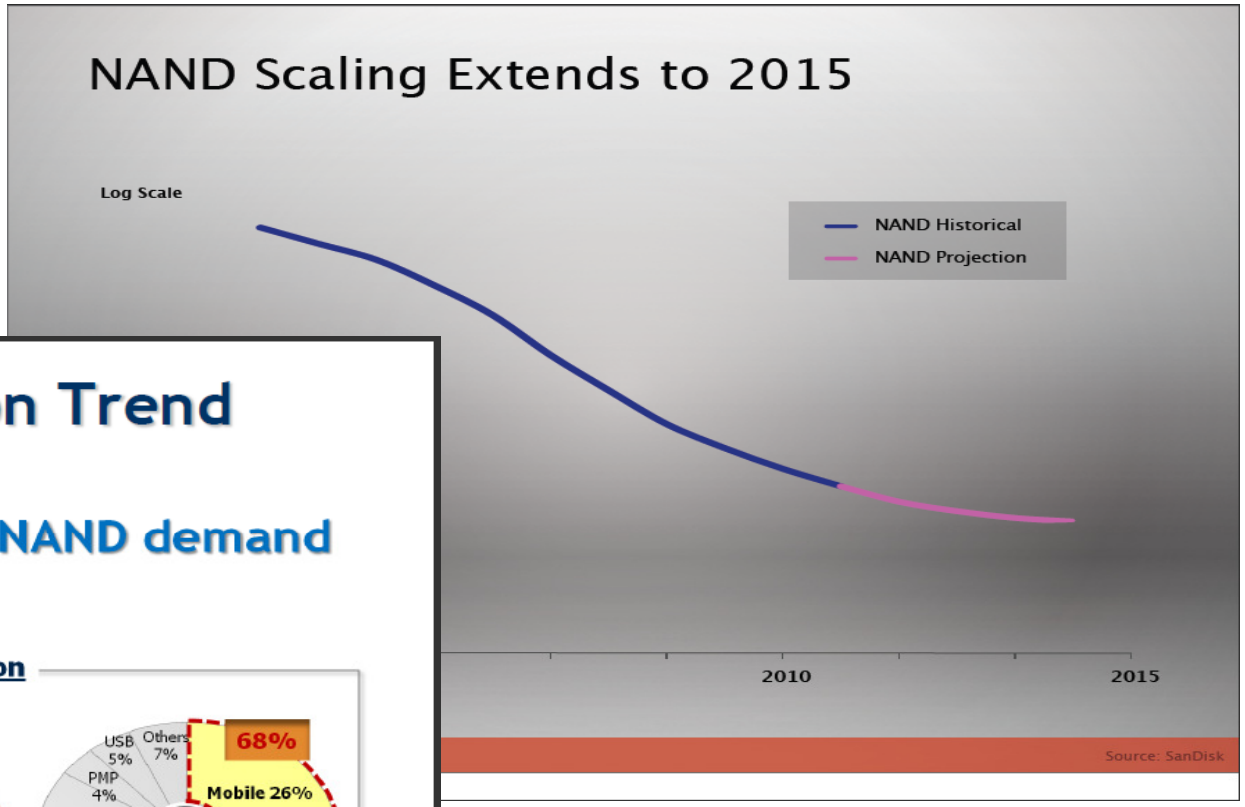
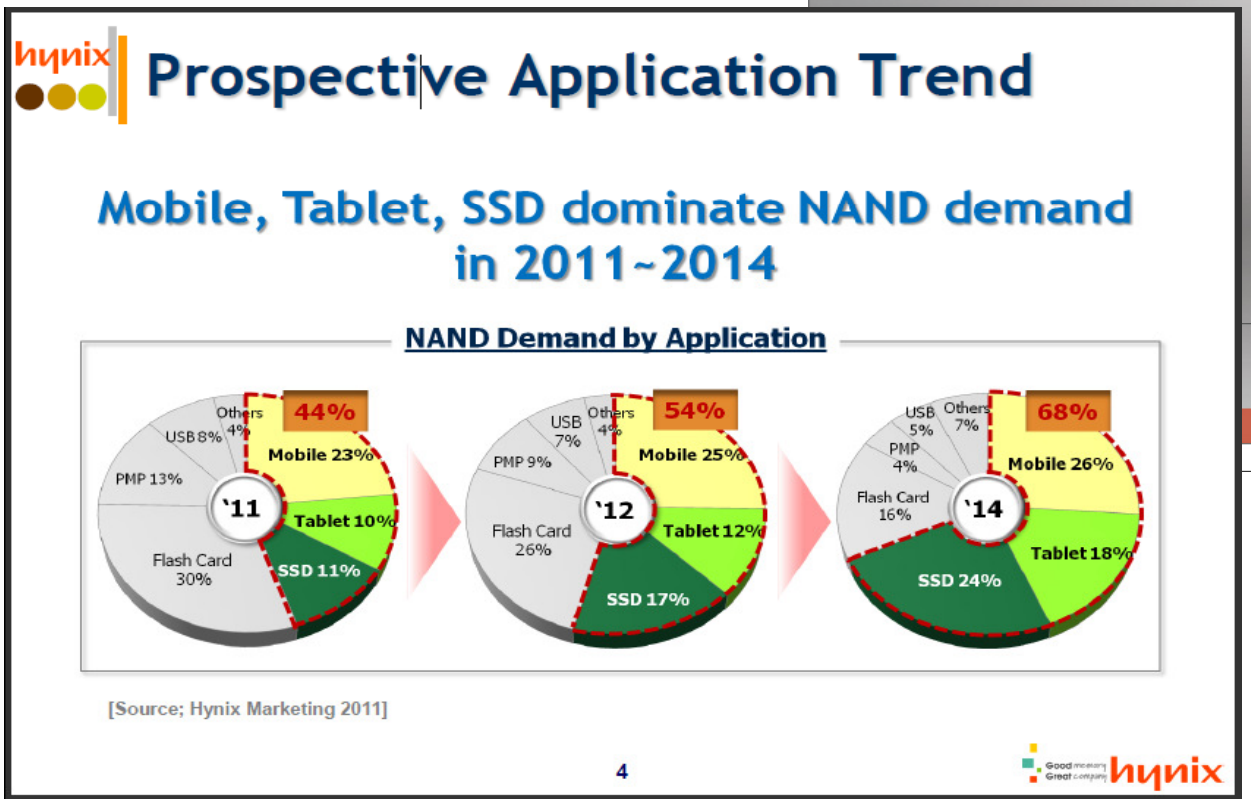
Trends in NAND Flash Memory and 3D

- **Mobile Applications**
- **Tablets**
- **SSD's**



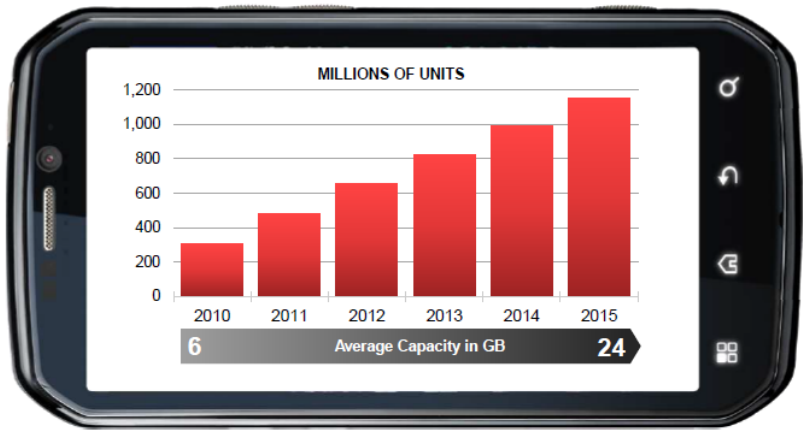


Courtesy of Flash Memory

And IEDM Conferences 2011

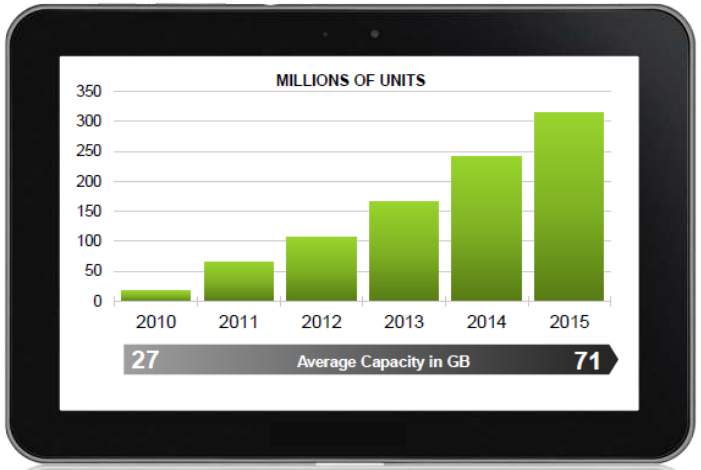
Growth Drivers for Memory Technology

Growth Driver 1: Smartphones



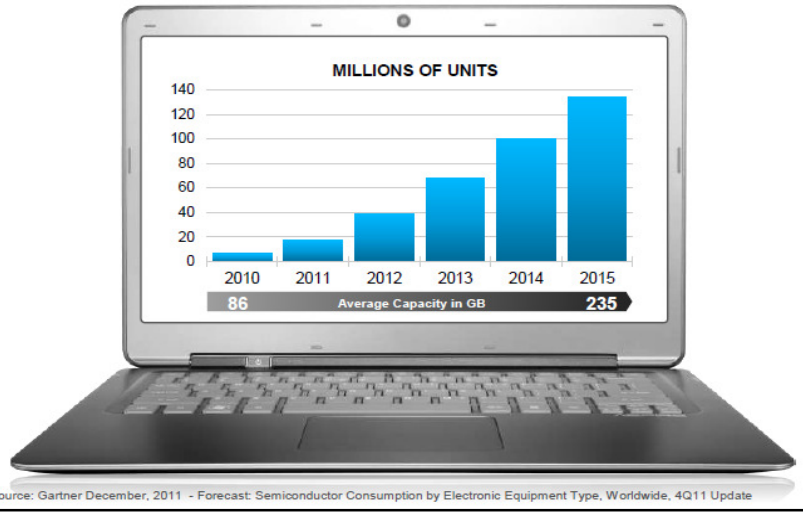
Source: Gartner December, 2011 - Forecast: Semiconductor Consumption by Electronic Equipment Type, Worldwide, 4Q11 Update

Growth Driver 2: Tablets



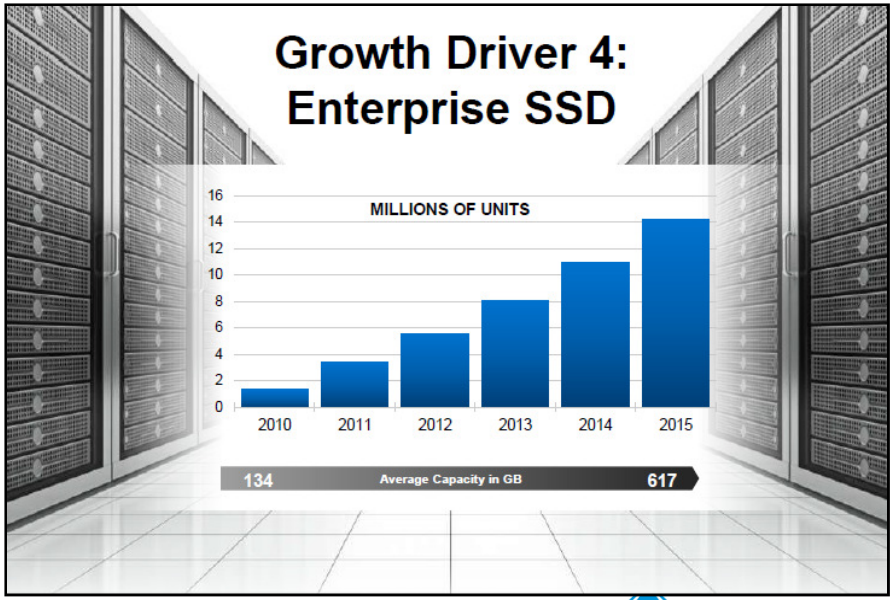
Source: Gartner December, 2011 - Forecast: Semiconductor Consumption by Electronic Equipment Type, Worldwide, 4Q11 Update

Growth Driver 3: PC SSD



Source: Gartner December, 2011 - Forecast: Semiconductor Consumption by Electronic Equipment Type, Worldwide, 4Q11 Update

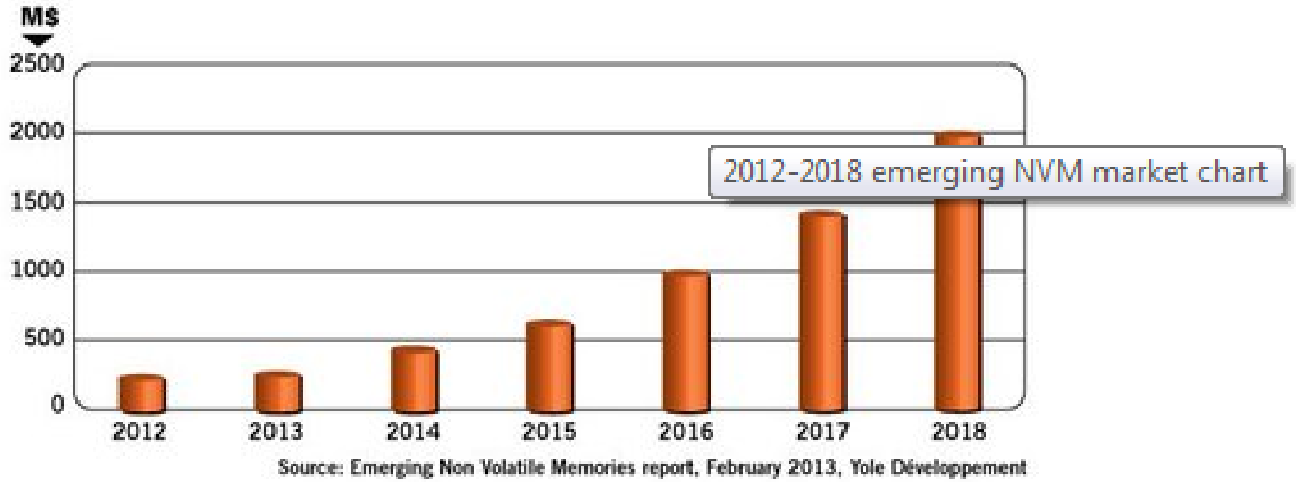
Growth Driver 4: Enterprise SSD



Emerging Memory Development

Yole Développement sees the PCM and MRAM markets reaching $1.6 billion in 2018

Yole Développement released a new report on Emerging Non-Volatile Memories (which include four major technologies: MRAM, PCM, RRAM and FeRAM). They see the market increasing ten-fold in the next five years to $2 billion by 2018 (of which STT-MRAM and PCM will take the major share of $1.6 billion) - mostly due to improved scalability and chip density.



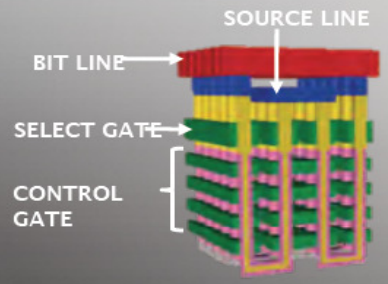
Source: Emerging Non Volatile Memories report, February 2013, Yole Développement

Courtesy of Yole

Trends in NAND Flash Memory and 3D

Adding the 3rd Dimension: BiCS and 3D Crosspoint

BIT COST SCALABLE (BICS)
3D NAND



> Potential to leverage existing NAND toolsets for continued cost declines
> Electron Storage in a vertical NAND string

Source: Toshiba VLSI, 2009

3D CROSSPOINT RESISTIVE RAM
3D RRAM

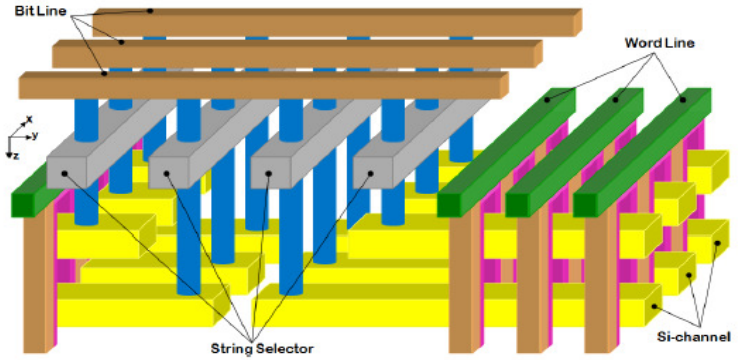
> On-g
requi
> Stora
Chan

Source:

Wednesday, August 10, 2011

Stacked 3D Cell Structures

Hybrid Stacked 3D



3D Cell Structure with Horizontal Poly-Si Channel

[IMW 2011 by Hynix]

24

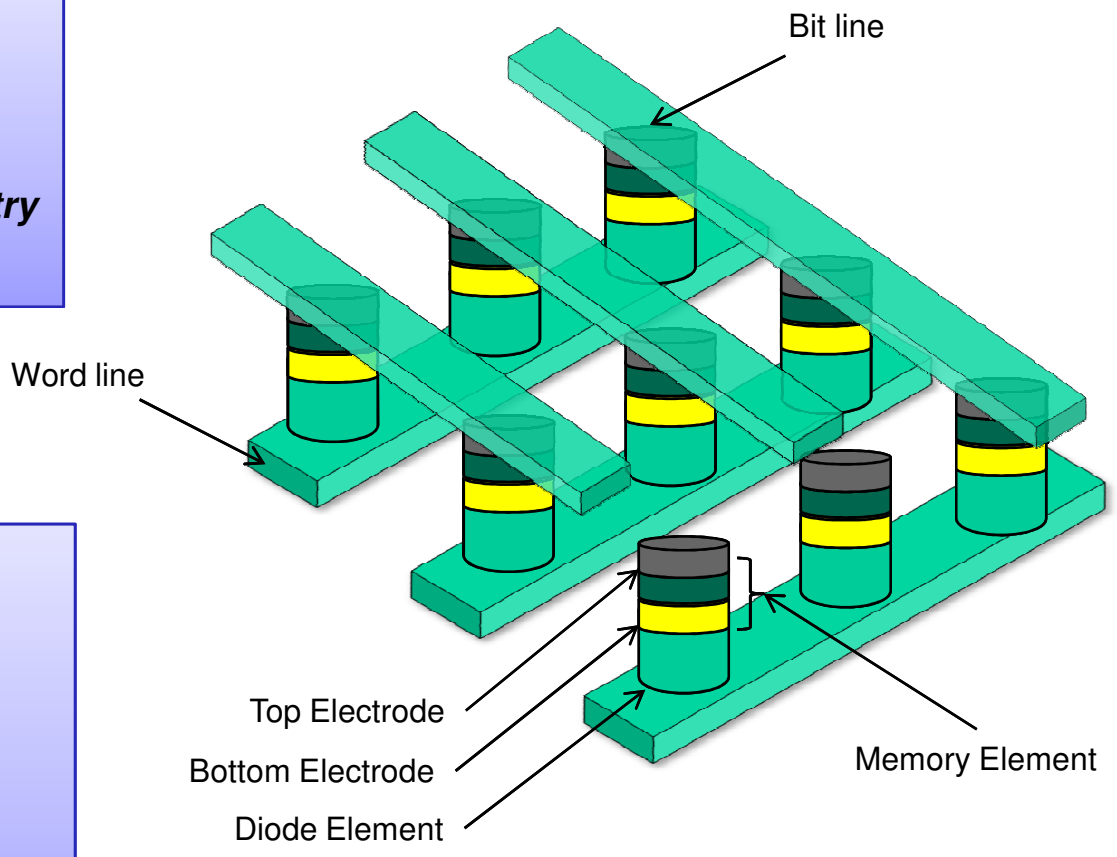
Courtesy of Flash Memory

And IEDM Conferences 2011

Advantages of 3D Integration

- ***Cross Point Memory (3D)***
  - ***Re-use of Interconnects***
  - ***Suitable for 3D Stacking***
  - ***Can be Integrated with CMOS circuitry***
  - ***Costs***

- ***Requirements to replace NAND***
  - ***Cell Size***
  - ***Capable of Multi-level***
  - ***Performance and Reliability***
  - ***Scalability***
  - ***Re-use of Fabrication Techniques***
  - ***Costs***



Emerging Memory Development

Device Type	HDD	DRAM	NAND Flash	FRAM	MRAM	STTRAM	PCRAM	NRAM
Maturity	Product	Product	Product	Product	Product	Prototype	Product	Prototype
Present Density	400Gb/in^2 [7]	8Gb/chip [9]	64Gb/chip [10]	128Mb/chip	32Mb/chip	2Mb/chip	512Mb/chip	NA
Cell Size (SLC)	(2/3)F^2	6F^2	4F^2	6F^2	20F^2	4F^2	5F^2	5F^2
MLC Capability	No	No	4bits/cell	No	2bits/cell	4bits/cell	4bits/cell	No
Program Energy/bit	NA	2pJ	10nJ	2pJ	120pJ	0.02pJ	100pJ	10pJ [11]
Access Time (W/R)	9.5/8.5ms [8]	10/10ns	200/25us	50/75ns	12/12ns	10/10ns	100/20ns	10/10ns [11]
Endurance/Retention	NA	10^{16}/64ms	10^5/10yr	10^{15}/10yr	10^{15}/10yr	10^{16}/10yr	10^5/10yr	10^{16}/10yr

Device Type	RRAM	CBRAM	SEM	Polymer	Molecular	Racetrack	Holographic	Probe
Maturity	Research	Prototype	Prototype	Research	Research	Research	Product	Prototype
Present Density	64Kb/chip	2Mb/chip	128Mb/chip	128b/chip	160Kb/chip	NA	515Gb/in^2	1Tb/in^2
Cell Size	6F^2	6F^2	4F^2	6F^2	6F^2	N/A	N/A	N/A
MLC Capability	2bits/cell	2bits/cell	No	2bits/cell	No	12bits/cell	N/A	N/A
Program Energy/bit	2pJ	2pJ	13pJ	NA	NA	2pJ	N/A	100pJ [12]
Access Time (W/R)	10/20ns	50/50ns	100/20ns	30/30ns	20/20ns	10/10ns	3.1/5.4ms	10/10us
Endurance/Retention	10^8/10yr	10^5/Months	10^9/days	10^4/Months	10^5/Months	10^{16}/10yr	10^5/50yr	10^5/NA

Kryder, et al. IEEE Transactions on Magnetics, Vol. 45, October 2009

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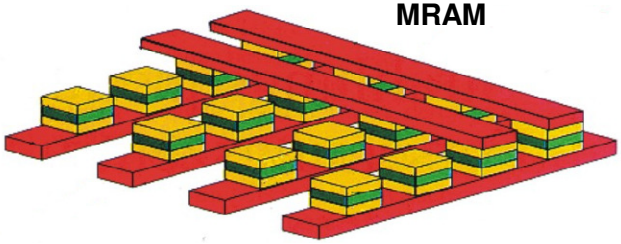
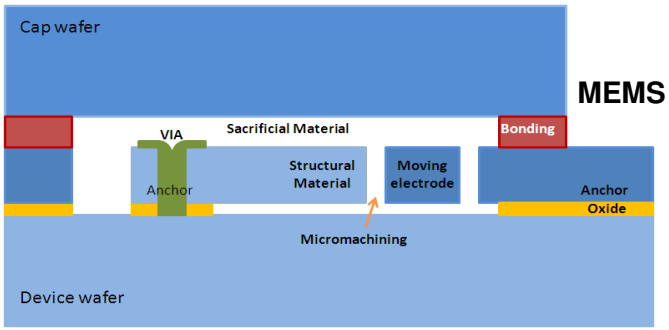
Enabling Technology Development

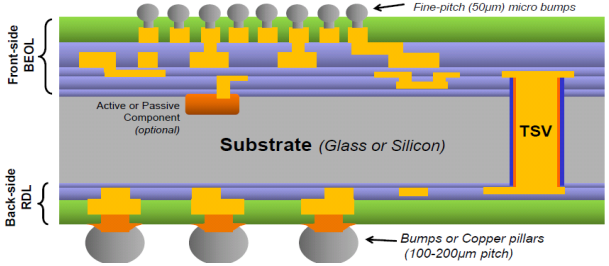
MRAM



MEMS

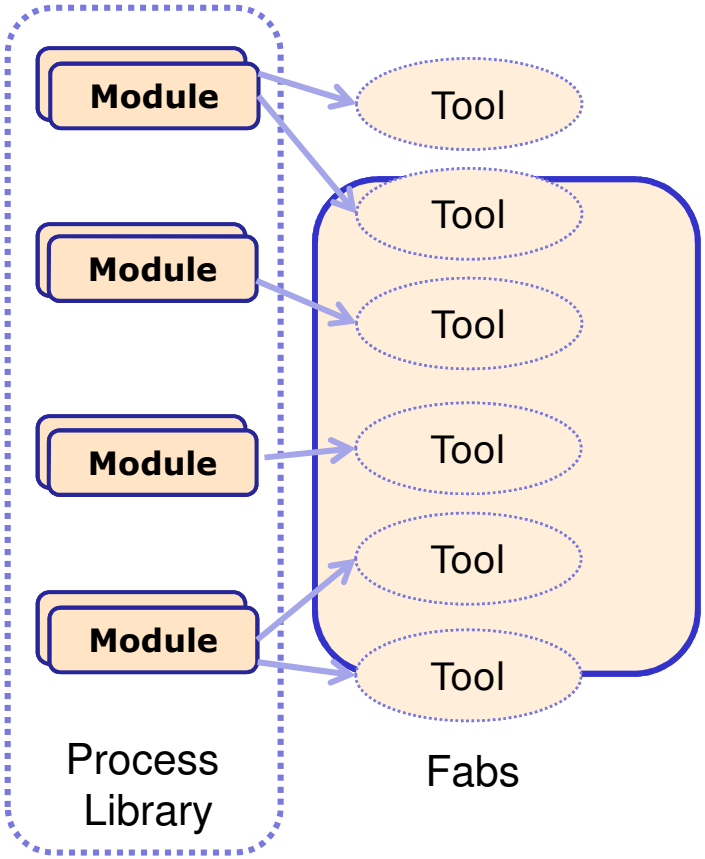


3-D TSV



Custom Integrated Process Flow

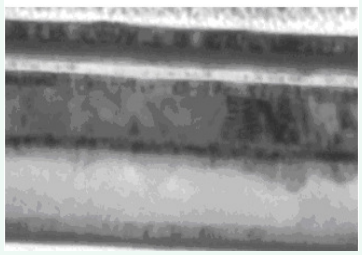
Engineering Services



Process library, tool set and engineering expertise enable development of custom integrated process flows for novel silicon based process technologies

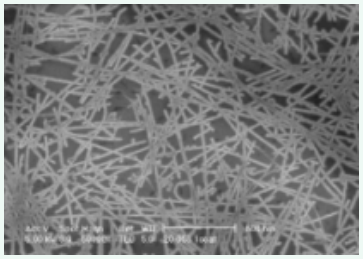
Process Module Blocks - Memory

Material Integration



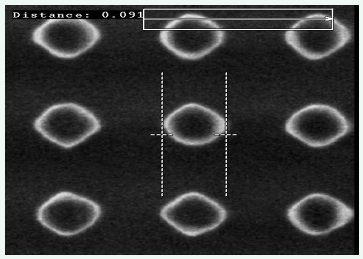
- DC ,*RF* & *Co*-Sputtering
- Metals, Metal Nitrides
- *Mag Stack & Anneal*

Novel Materials



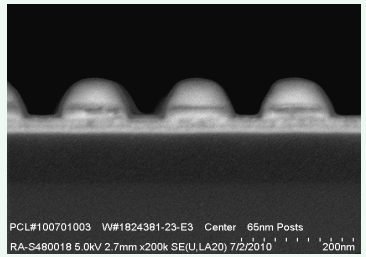
- Atomic Layer Deposition
- Metals, Oxides, Nitrides
- Carbon Nanotubes

Lithography



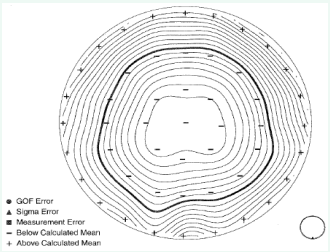
- 110nm Lithography
- DP Spacer Techniques
- <110nm L/S, 110nm Posts

Novel Etch



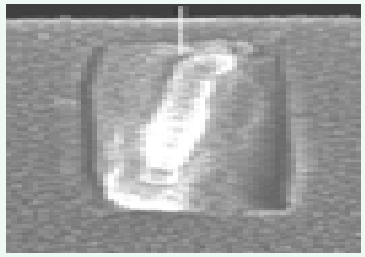
- Nobel Metals
- High Temp:170-350C
- Physical Ion Milling

Low Temp Process



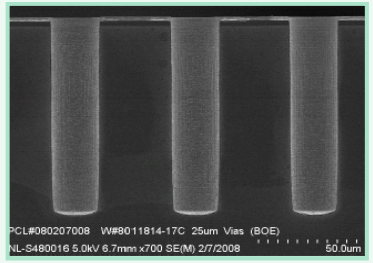
- <200C Modules
- Nitride, Oxide Films
- Ash & Cleans

CMP



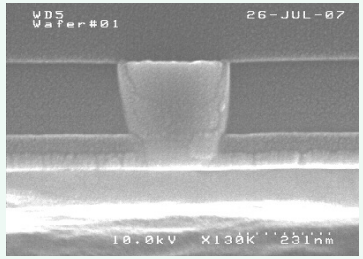
- Selective Slurries
- Oxide, Tungsten
- *Exotic Materials*

TSV



- DSiE
- *Cu*, W, Poly
- Barrier Materials

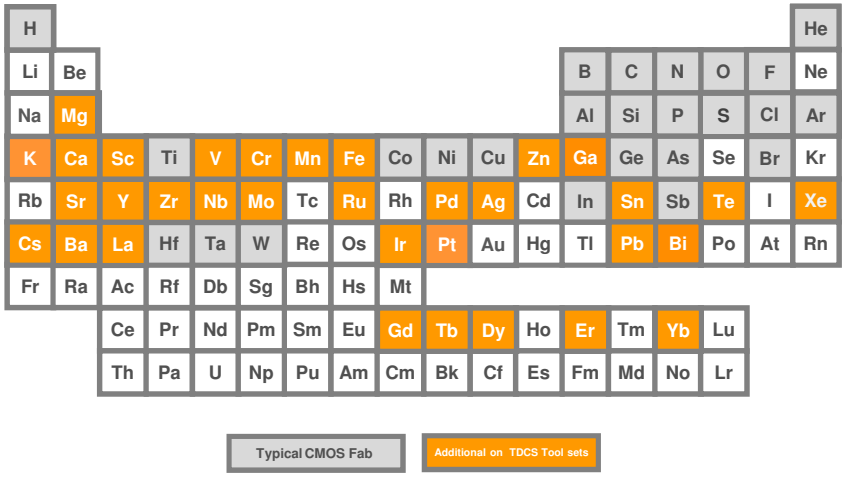
Interconnect



- Foundry CMOS
- Cu & Al interconnect
- Alignment

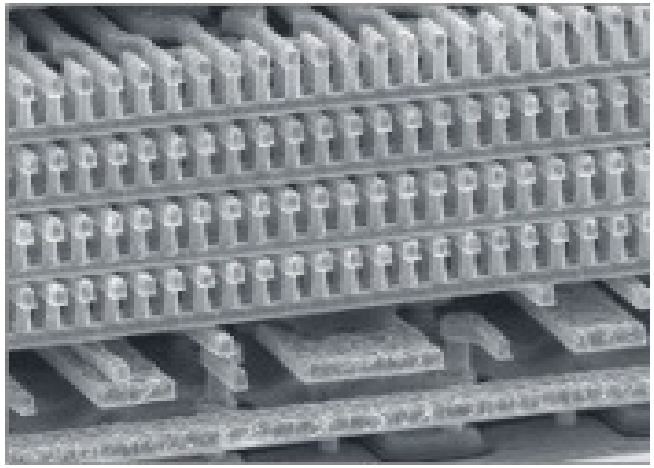
Non-Volatile Memory Materials

Memory Materials Development

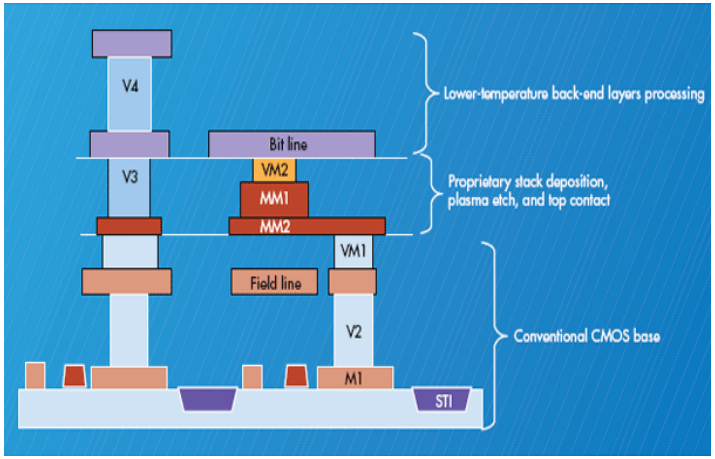


Device	Materials	Process Module's
MRAM	Co, Fe, B, Ni Ta, Ti, Pt, Mn, Ru, Mg, Ir, Al, Metal Oxides	▪ Low temp processing (<200C) ▪ Nobel Etch and Cleans ▪ AlCu Interconnect ▪ Interconnect with CMOS ▪ Materials Integration ▪ CMP ▪ Hardmask and Liner Integration ▪ Double Patterning
PCRAM	Ag, GeS2, GST (Ge, Sb, Te)	
ReRAM	Zr, Pr, Ca, Y, Pd, La, Complex Metal Oxides	
FeRAM	PZT (Pb, Zr, Ti, O), SBT (Sr, Bi, Ta, O), BLT (Bi, La, Ti, O)	
NRAM	CNT, W	
SQC	Nb/AlOx/Nb, TiPt	

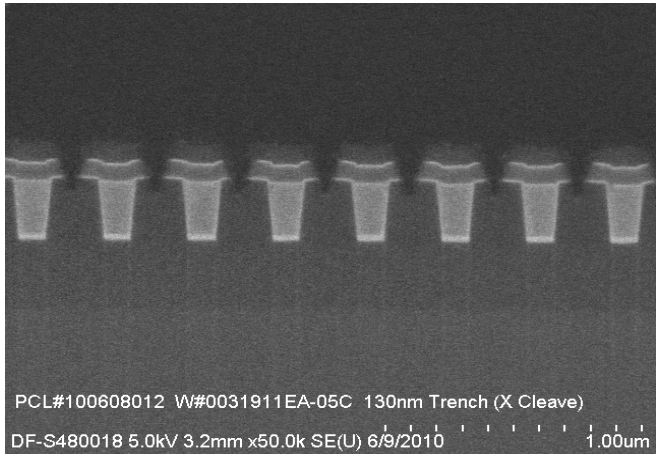
Sample Memory Technologies



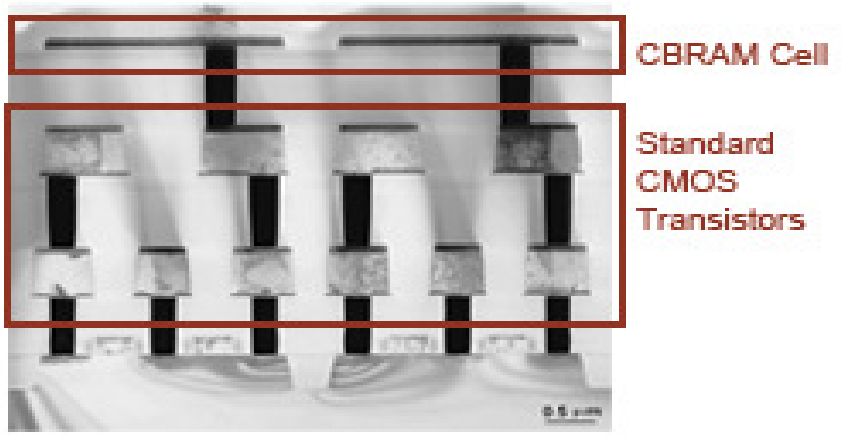
3-D Memory: Courtesy Sandisk



MRAM Memory: Courtesy Crocus



ReRAM Memory: Courtesy Company B



CBRAM Memory: Courtesy Adesto

Case Example: Key Fabrication Elements

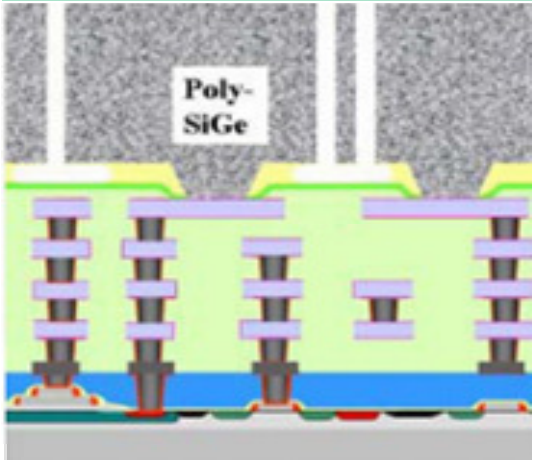
Key Fabrication Elements

- Integration of CMOS Wafers to Memory
- Etch Integration
- Low Temperature Module Blocks
- Inter-Dielectric Planarity

Device Integration on CMOS has Several Benefits

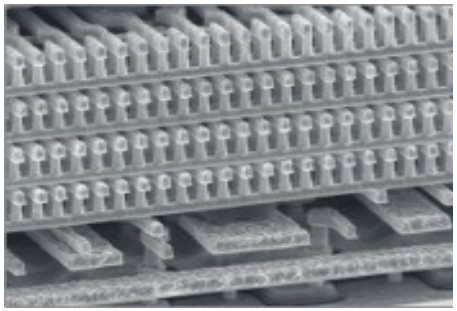
Discrete Device

e.g. MEMS, Memory, etc

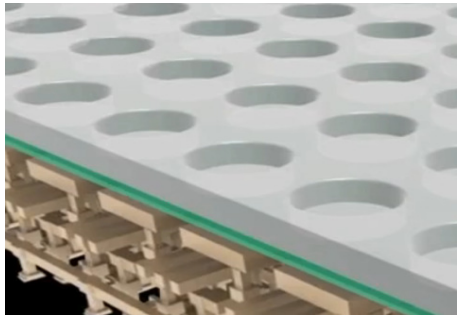


Monolithic integration of Discrete Devices and CMOS

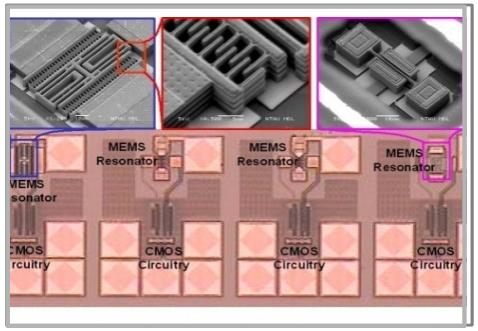
	Pro	***Con***
Compact Solution	▪ *Increase Chip Density* ▪ *Smaller Devices*	▪ *Integration challenges*
Device Performance	▪ *Less Interconnect* ▪ *Minimize parasitics* ▪ *Improved Device Performance*	▪ *Challenge for devices with thermal requirements*
Cost	▪ *Reduced Assembly* ▪ *Reduced Packaging* ▪ *Lower Cost of Ownership*	▪ *Potential Yield Mis-match between devices*



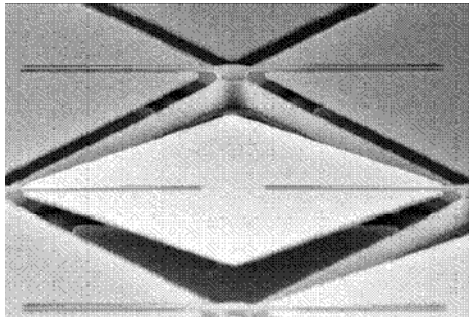
***3-D Memory**: Courtesy Sandisk*



***Lab-on-a-chip** integrates microfluidics, sensors and logic to more rapidly perform gene sequencing*



***MEMS Resonator on CMOS** used in RF domain: frequency references for oscillators, filters and mixers*



***Micro-Mirrors over CMOS** (picture courtesy of Spatial Photonics). Sample applications include Microdisplays*

Key Fabrication Elements

- Integration of CMOS Cu Wafers to Memory
- Etch Integration
- Low Temperature Module Blocks
- Inter-Dielectric Planarity

Spin Transfer Technologies raised $36 million to accelerate its OST-MRAM technology development

Spin Transfer Technologies (STT) announced that they raised $36 million in series A funding led by parent company, Allied Minds and Invesco Asset Management. STT will use the money to accelerate the development of its patented orthogonal spin transfer magneto resistive random access memory technology (OST-MRAM) - by scaling operation, hiring new employees and purchasing equipment.

Toshiba designed an STT-MRAM/SRAM hybrid cache for ultra-low power processors

Toshiba has a new hybrid cache design that uses STT-MRAM and SRAM combination. This is aimed towards next-generation low-power computer processors. These new computers will usually be off, and the time and power it takes to "wake up" is considerable. The new design can reduce the energy consumption by around half - and does not effect processing capacity.

Micron and A*STAR to jointly develop high density STT-MRAM

Micron and the A*STAR Data Storage Institute (DSI) from Singapore announced that they will jointly develop STT-RAM. The two companies will invest in a 3-year joint-research program to develop high-density STT-MRAM devices.

Toshiba and Hynix to co-develop and produce MRAM products

Toshiba and Hynix announced an agreement to jointly develop MRAM products. Once the development is complete, the companies intend to establish an MRAM production plant together. We believe the companies intend to develop STT-MRAM technology.

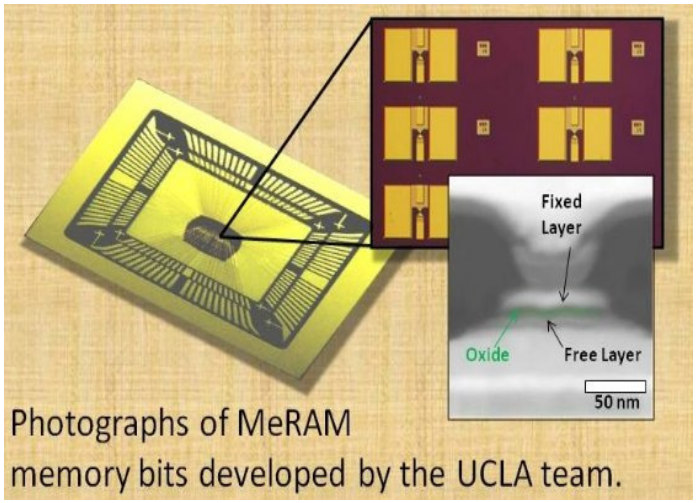
hynix TOSHIBA Leading Innovation

UCLA receives $5.5 million to continue STT-RAM research

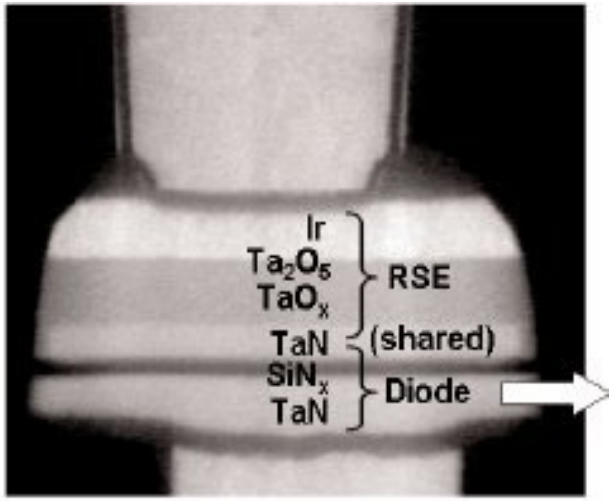
UCLA has been awarded $5.5 million from DARPA to continue develop STT-MRAM technologies. This is the second grant for this project, which brings the total DARPA grants to $10.5 million. The first stage has been completed a year early than planned - by meeting (and in fact significantly surpassing) speed, energy consumption and stability requirements of their STT-RAM (write times smaller than 5 nanoseconds and write energies lower than 0.25 picojoules per bit).

Courtesy of MRAM-info.com

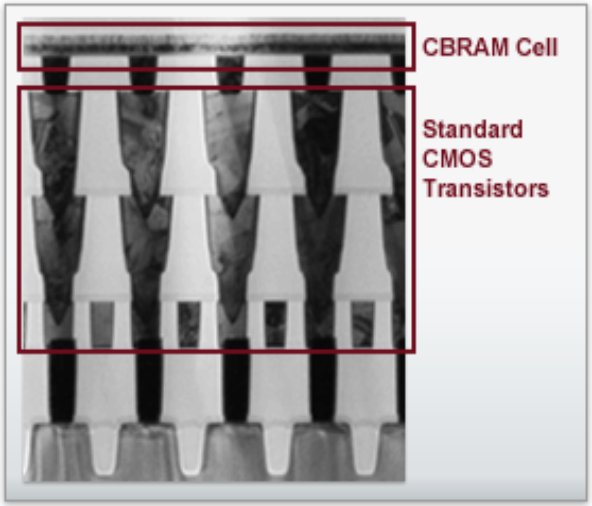
NVM Memory



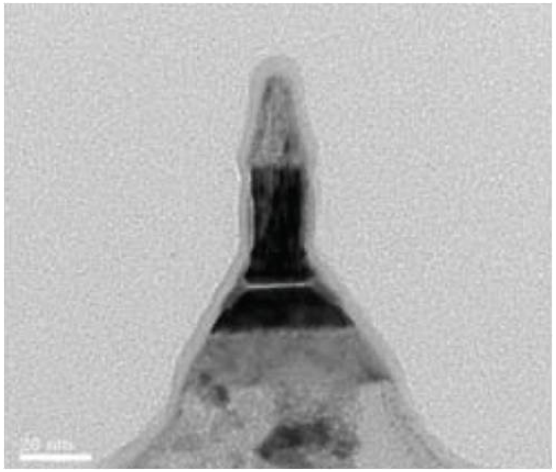
Photographs of MeRAM memory bits developed by the UCLA team.



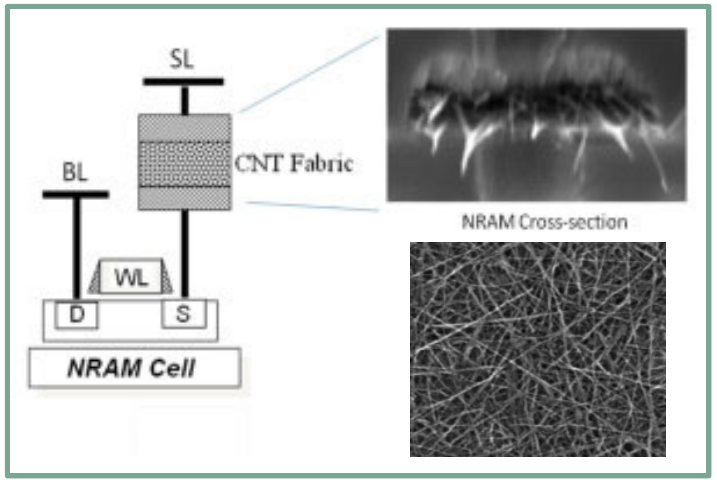
Panasonic ReRam



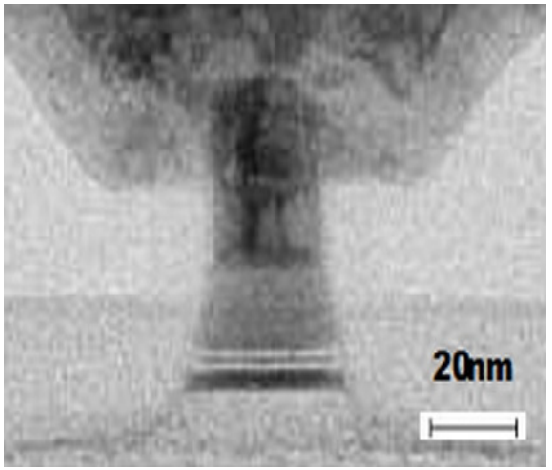
Adesto CBRAM



Samsung 17nm MTJ

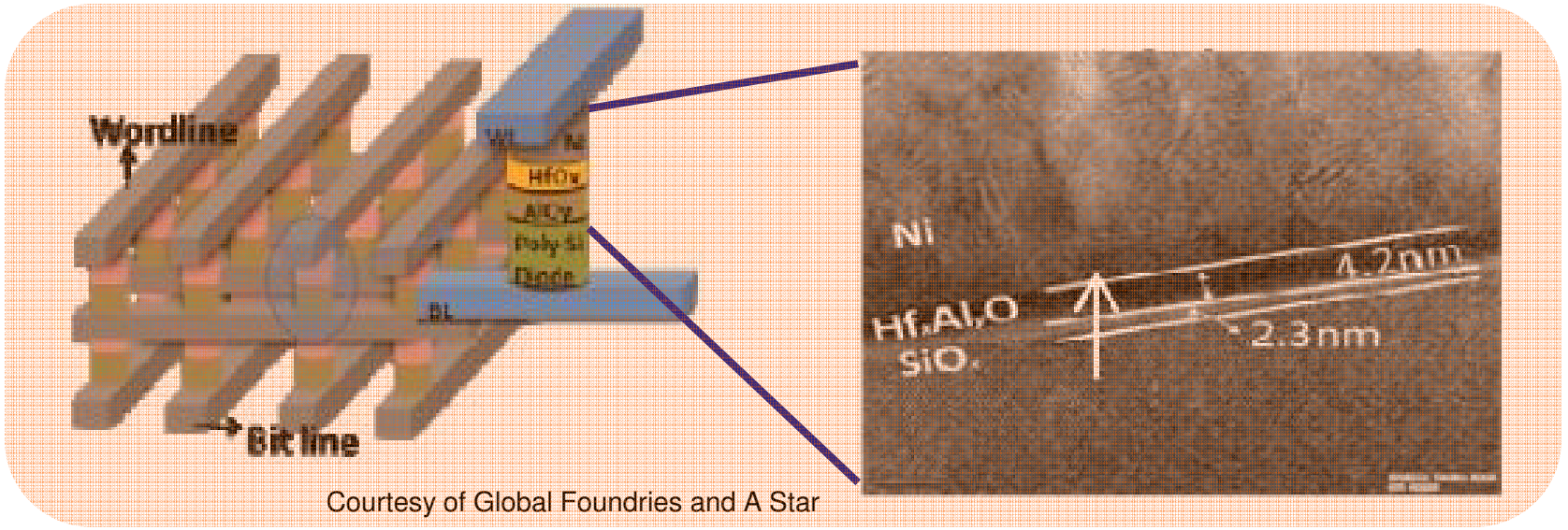


Nantero NRAM

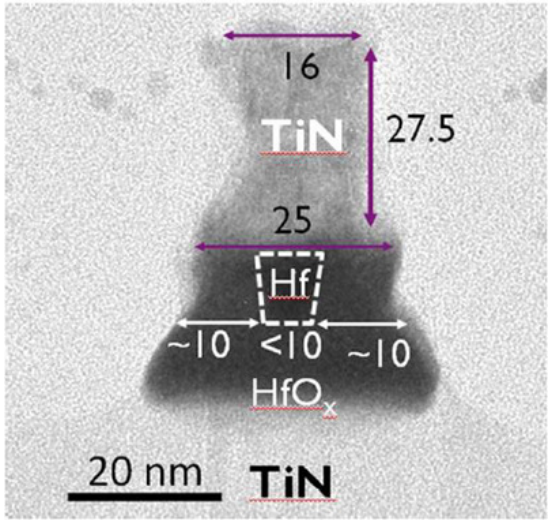


Toshiba MTJ

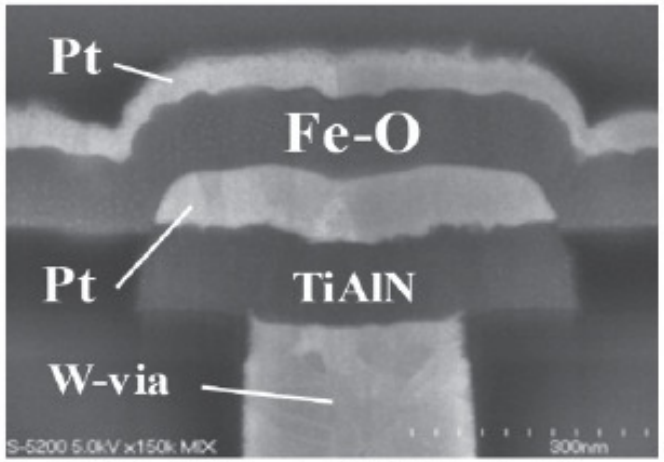
Resistive RAM



Courtesy of Global Foundries and A Star



Courtesy of IMEC



ReRAM Cell Using FeO Variable Resistance
Cross-section of the ReRAM memory cell prototyped by Matsushita Electric Industrial. Top and bottom electrodes are Pt.

Large Variation in Materials and Thicknesses, not one Etch Solution that fits all applications

Stack Thickness 500A to 1000A

Memory	Thickness (A)
Ta	100 - 500A
CoFeB	30A
MgO	15A
Ru	10A – 60A
CoFe	40A
PtMn	125A
GST	500A
Ag	--
La	--

Stack Thickness 1000A to 2.2um

Life Sciences	Thickness (A)
Ta	50A
Ru	10A - 20A
NiFe	20A
CoFe	475A

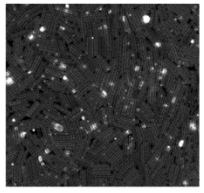


FIG. 45

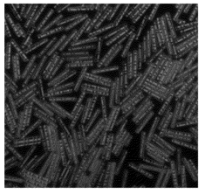


FIG. 46c

FIG. 46a

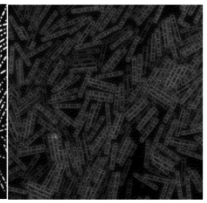
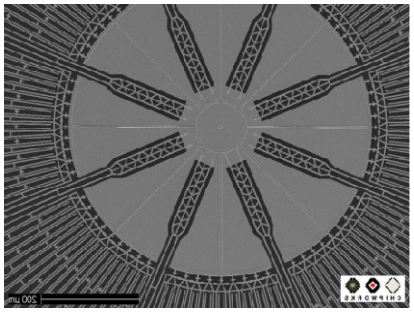


FIG. 46b

Stack Thickness 1000A to 1.4um

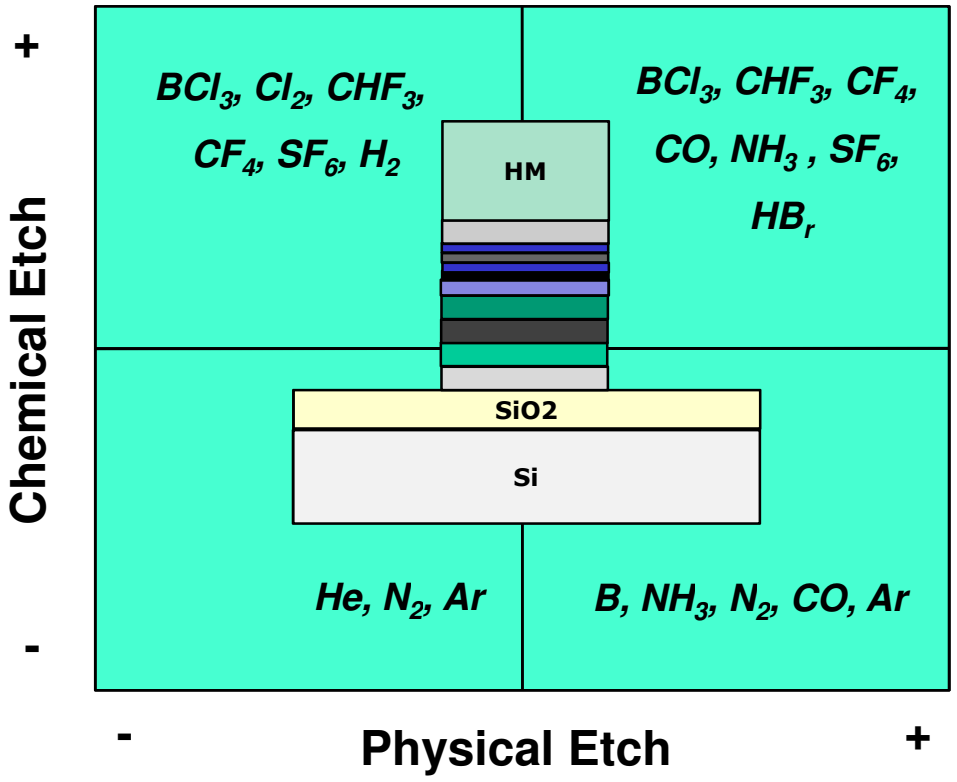
MEMS Compass	Thickness (A)
Co	500A
CoNi	600A
Ni	1000A
NiFe	500A
Al	10kA



Stack Thickness 500A to 2.2um

Other	Thickness (A)
Pt	1000A
PZT	Up to 2.2um
Nb	--

Novel Etch Solutions - Chemistry



Pressure Ranges	
Etch Types	**Torr**
Ion Milling	10^{-4} – 10^{-3}
Reactive Ion Etch	10^{-3} – 10^{-1}
Plasma Etch	10^{-1} - 5

<100 mTorr

Higher Energy

Physical Etch (Sputtering)
- Physical momentum transfer
- Anisotropic etch profile
- Low etch rate
- Poor selectivity
- Radiation damage possible

RIE (Reactive Ion Etch)
- Physical(ion) and chemical
- Anisotropic, controllable etch profile
- More selective than sputtering

Plasma Etching
- Chemical, thus faster by 10-1000X
- Isotropic etch profile
- High etch rate
- Good selectivity
- Less prone to radiation damage

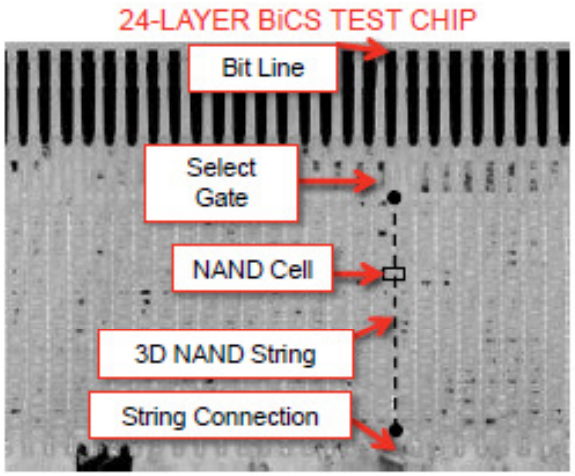
Higher Pressure

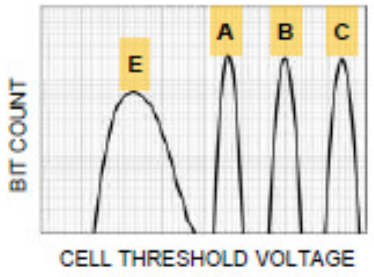
Etching of Novel Materials

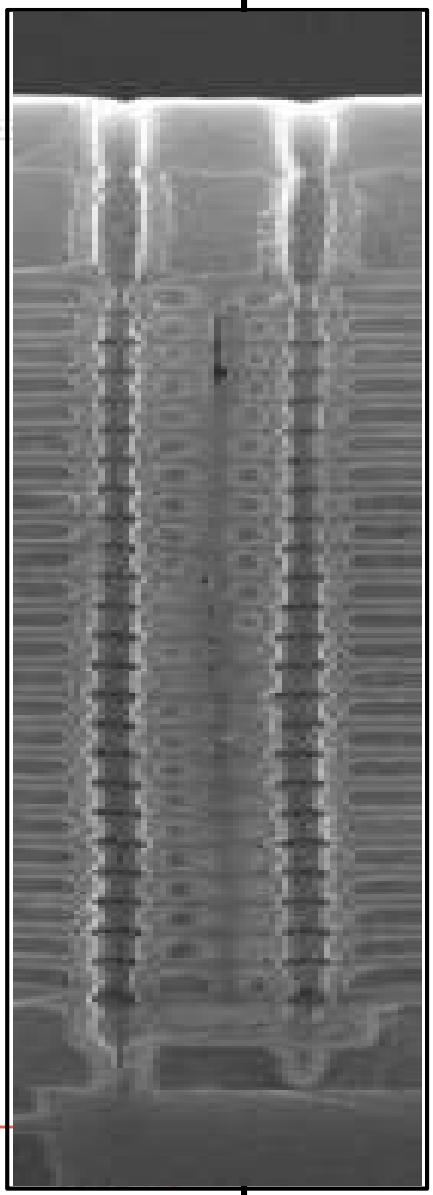
	LAM 9600	AMAT DPS2	Tegal 6540	Veeco Ion Mill
Gases Available	Chamber A (60C): BCl3,Cl2, Ar, N2, O2,SF6,He,O2 Chamber B (250C): DSQ O2, H20	Chamber A (250C): BCl3,Cl2, Ar Chamber B (65C): CF4, HeO2,HBr,Cl2	HRe 2.1 (30-80C): BCl3, Cl2, CHF3, CF4, Ar, O2 HRe 4.0 (170-350C): CO, Cl2, NH3, CF4, Ar, O2	Single Chamber: Ar
Materials Etched	Al, TiN/Al/Ti, TiW/TiAl, GST	Chamber A: High-k, Al2O3, TiN, TaN, Ru Chamber B: Metal Gate Stacks - Poly & metal alloys	HRe 2.1: Oxide, Ti, TiN, W, Ta, GST HRe 4.0: Ti, TiN, Nb, Pt, AlOx,Ta, PtMn, CoFe, MgO, Ru, Ag	Oxide, Ti, TiN, W, Ag, CoFe

Update on BiCS 3D NAND

- VERTICAL 3D NAND STRING STRUCTURE
- UTILIZES EXISTING WAFER FAB INFRASTRUCTURE
- DOES NOT NEED EUV
- KEY DEVELOPMENTS
  - 24-layer array development vehicle
  - Multi-level cell (MLC) functionality shown
- BRIDGE TO 3D ReRAM







SanDisk

ANALYST DAY || FEBRUARY 16, 2012

Summary

- We continue to see innovative and disruptive materials development for next generation NVM technologies
- The challenge for NVM developers is to find a suitable replacement for existing NAND performance for capacity, performance, reliability and costs
- TDCS offers a comprehensive set of capabilities to develop and integrate Novel Memory technologies
- There will be one winner (or more), but it's still in the validation stage!

Thank You

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