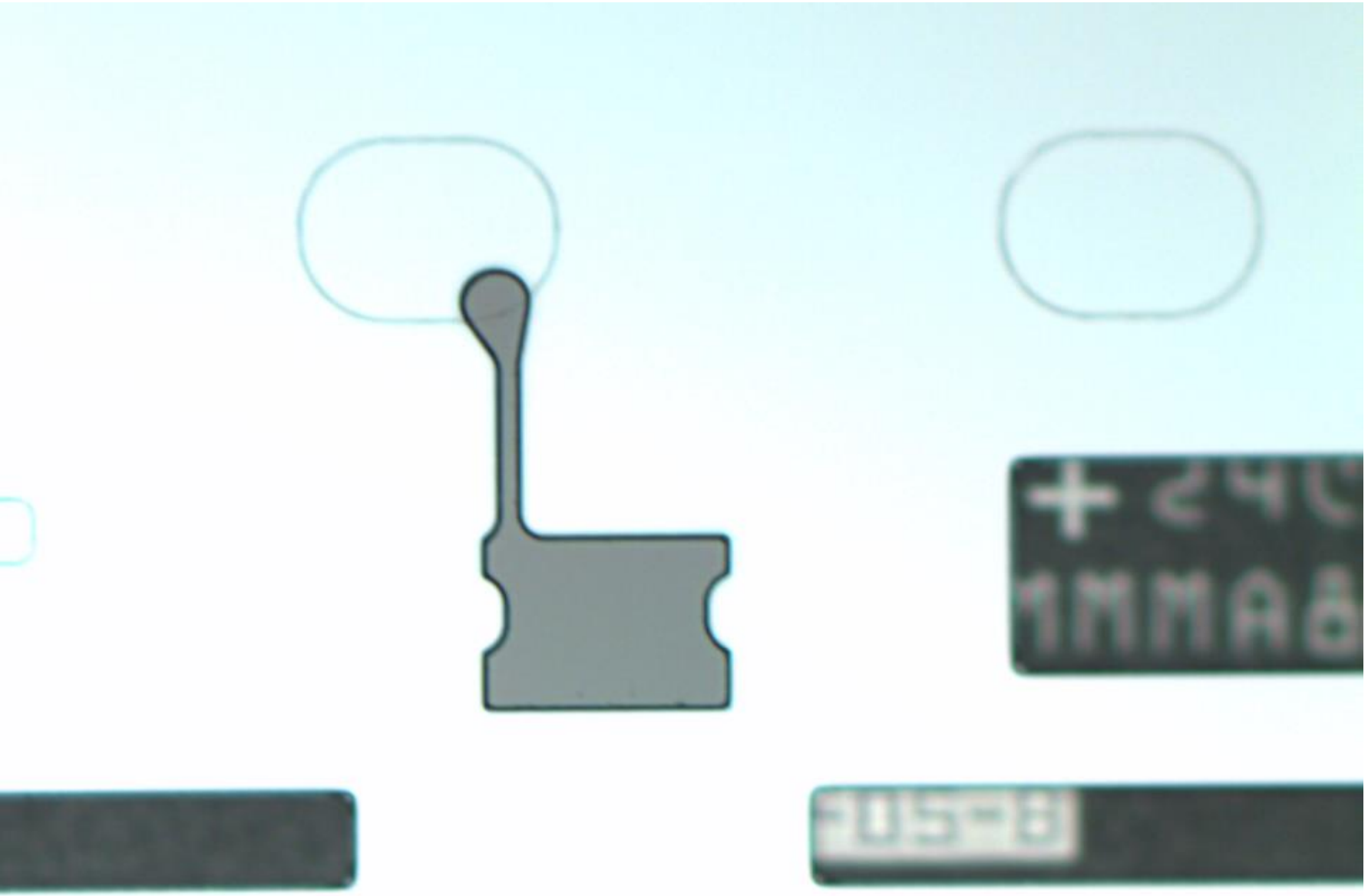
RIE / ICP ETCHING OF SiC using PLASMA-THERM VLR-700 ETCH TOOLS

by

Necmi Bilir, 2013

Final Shape of the Pad



PROCESSING STEPS:

Step-1: DEPOSITIONS

1-1 Etch-stop Layer Deposition (~1000A of PVD Cr)

1-2 PVD Deposition of SiC

1-3 Thickness Measurement

PROCESSING STEPS:

Step-2: Lithography for window openings

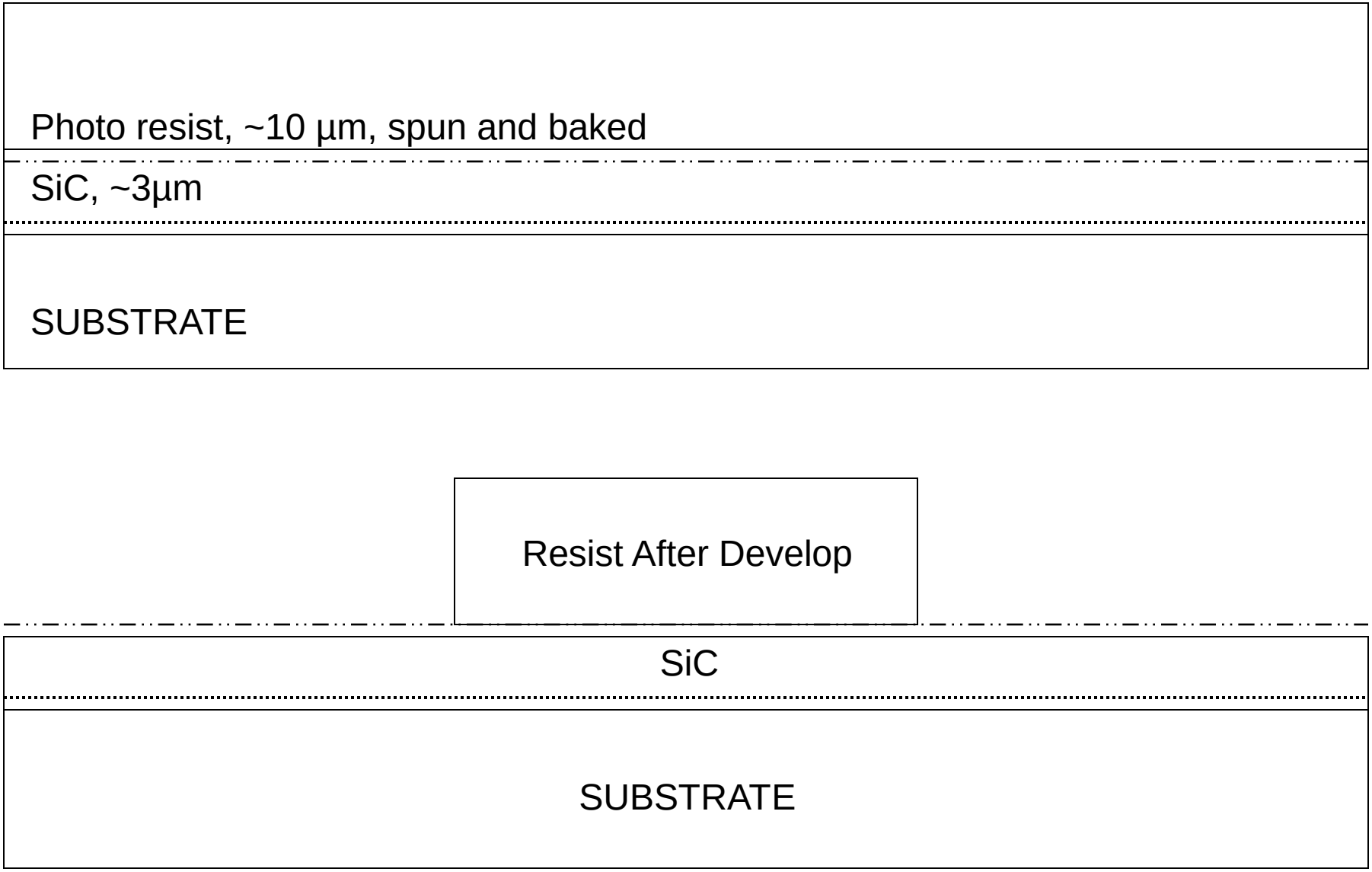
2-1	Deposit resist adhesion layer on SiC
2-2	Spin resist, expose and develop
2-3	RIE etch of SiC from window openings
2-4	Ion milling of Cr layer from window openings
2-5	Resist Strip and Wafer Cleaning

PROCESSING STEPS:

Step-3: Lithography for the Pad etch

3-1	Spin resist, expose and develop
3-2	RIE etch of SiC layer from field the area
3-3	Ion milling of the Cr layer from the field
3-4	Resist Strip and Wafer Cleaning
3-5	Process Audit (by FEI)

Schematics of Making the Pads

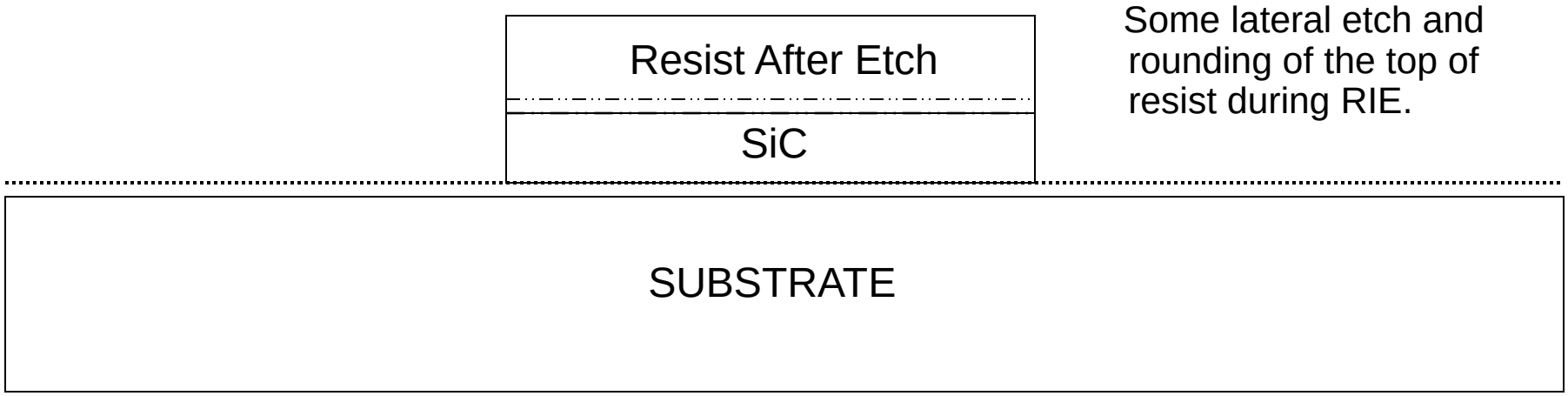


After Plasma Etching

PROCESS CHEMISTRY:

Fluorine chemistry mixed with oxygen gas

Chamber vacuum, gas flows and power optimized for etch selectivity



Some lateral etch and rounding of the top of resist during RIE.

PROCESSING CHALLENGES:

Etch Uniformity (within wafer and within the same run)

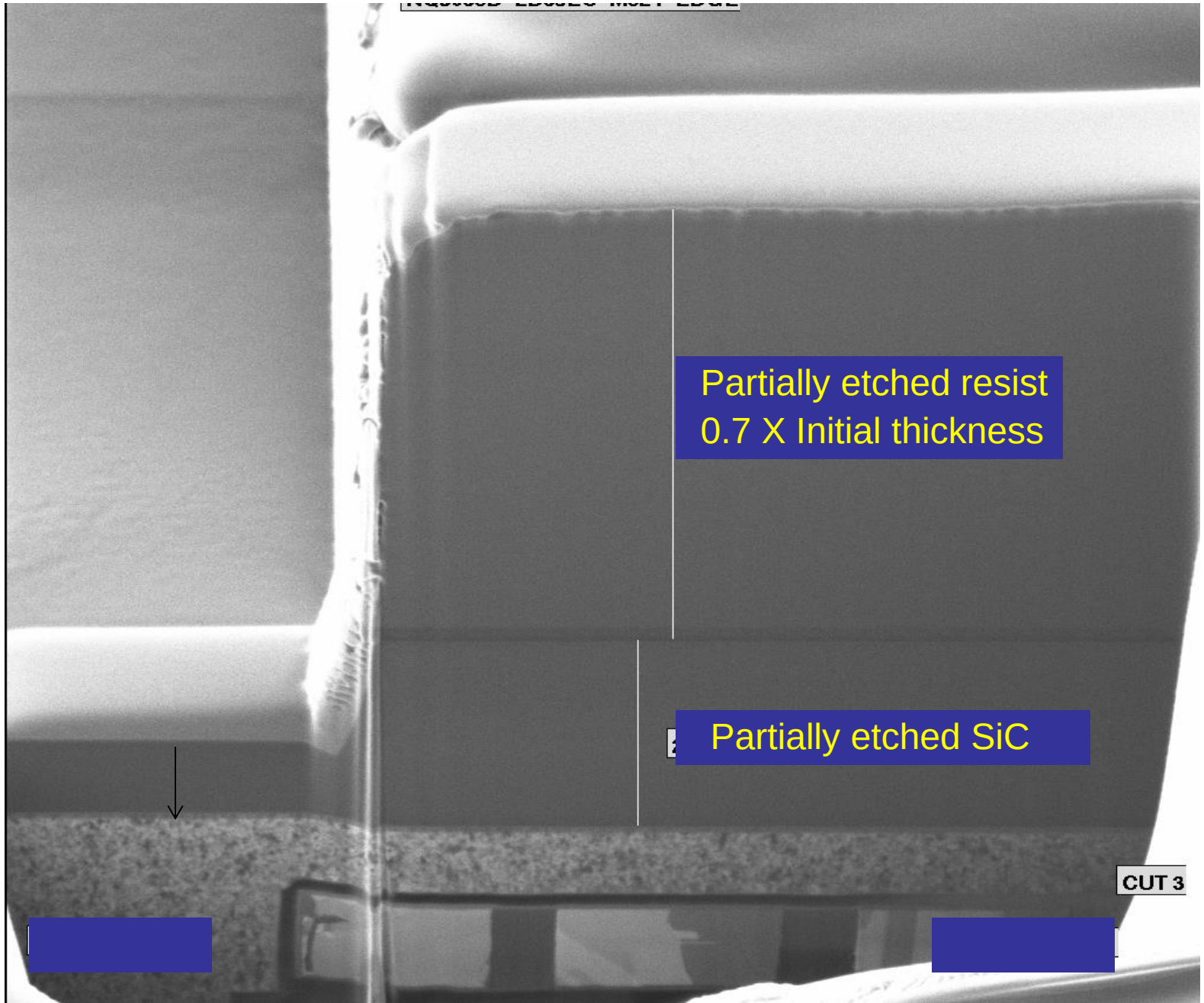
Etch Rate Test

Selectivity of the Etch Recipe

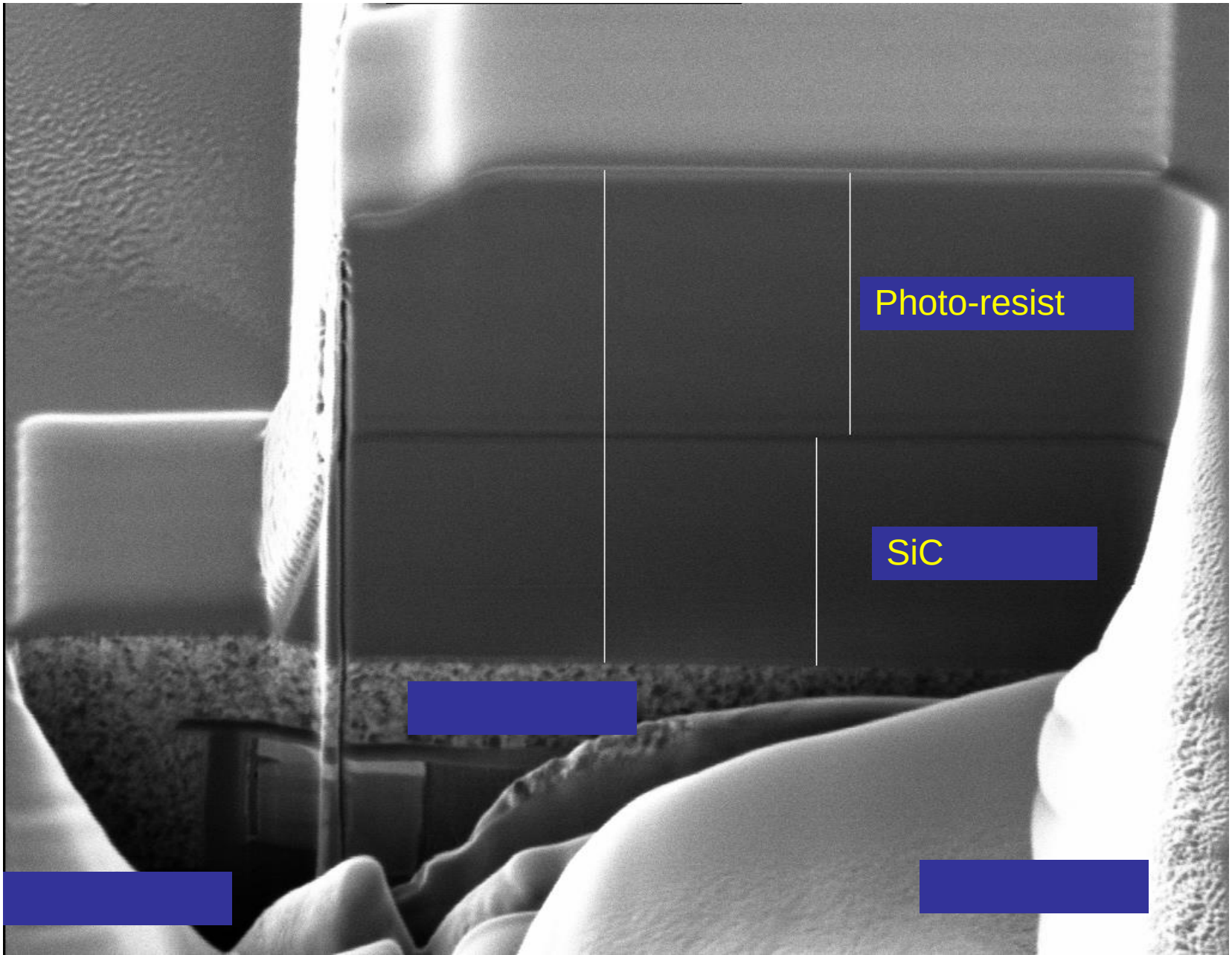
Vertical vs Lateral Etch (Edge slope of the final pad)

Residue build up at the edges

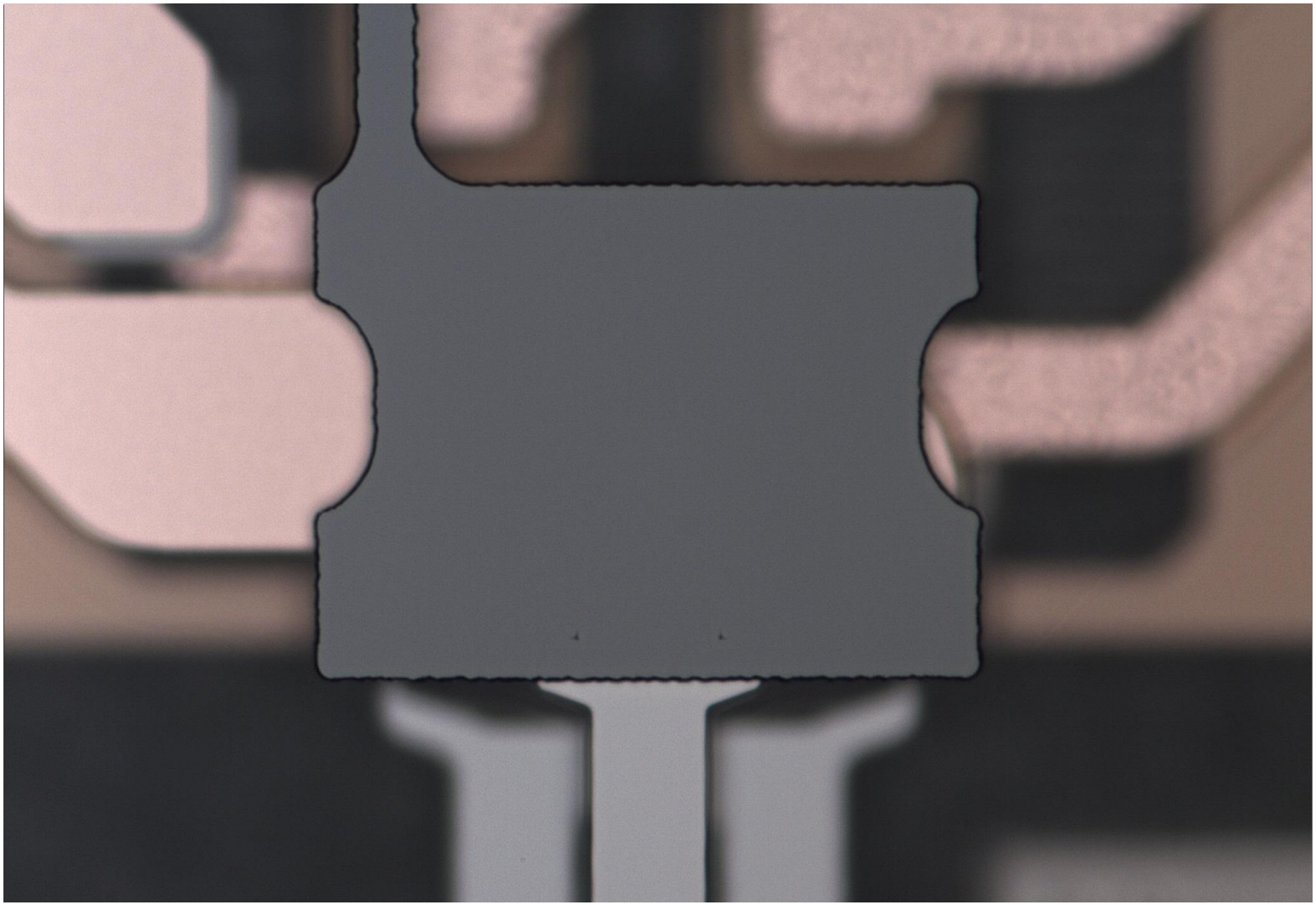
Original Etch-Rate Test



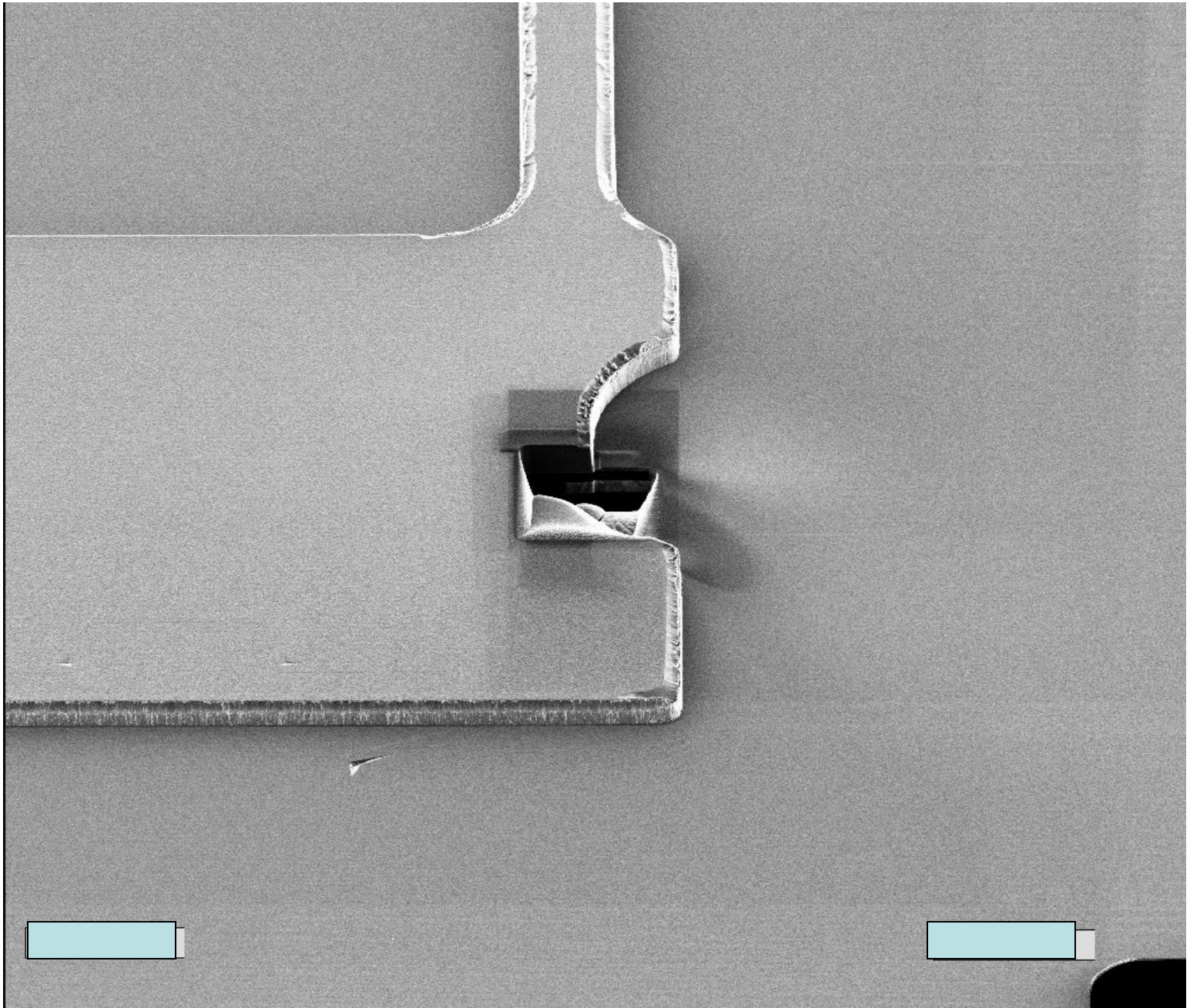
FIB cut before Resist Strip



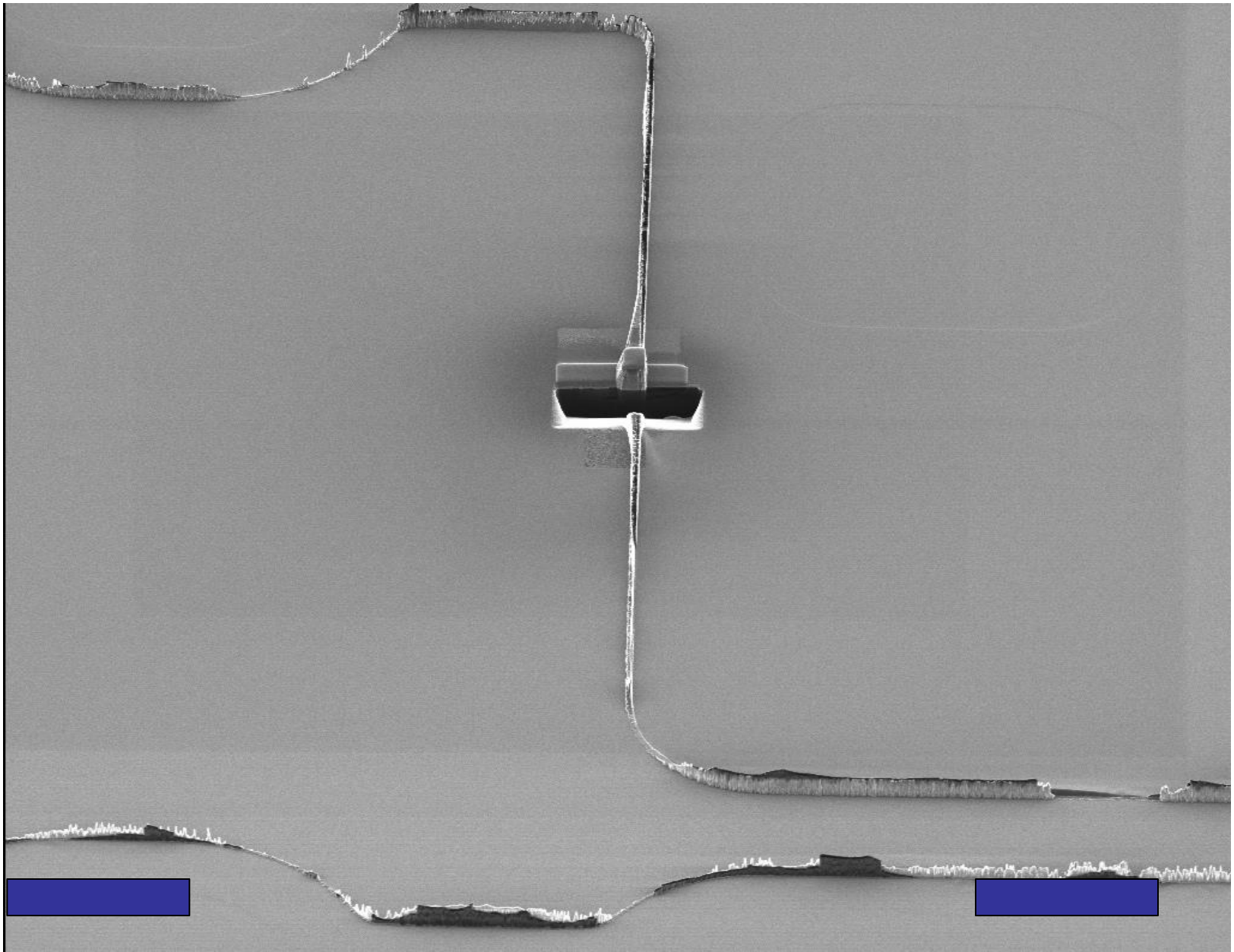
Final Pad – After Cr-Milling



After Resist Strip



Fencing Residues after Rework



Post resist strip and Cr-Mill x-section