

# EV Group

## Plasma Activation – An Enabling Technology for Wafer Bonding

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**PAG**  
**Semicon West 2010**



# Plasma Activation – An Enabling Technology for Wafer Bonding

## Outline

- **Why Bond – driving forces**
- Bonding Processes
- Alignment Processes
- PA (PLASMA Activated) Bonding

# Why Bond?

## Bonding allows

- Combining
  - Materials
    - Si
    - Glass
  - Processes
    - CMOS
    - MEMS
  - Functions
    - Mechanical
    - Sealing / Isolation ( hermeticity or micro channels )
    - Electrical
    - Thermal
    - Acoustic
- Parallel Processing
  - Up to 15,000 parts processed in one time
- Repartitioning
  - Cost / Performance
  - Decoupling of chip revisions
- Performance
  - Decreasing signal path length
  - Form factor
- Increased integration – easier for customer to design in (customer has digital I/O)

## This has enabled

- MEMS Devices
  - Accelerometers & Gyroscopes
    - Automotive
    - Gaming
  - Pressure sensors
- SOI wafers
- Microfluidics
- etc
- Increase Device Performance
  - Special substrates
  - Use the Z dimension
    - 3D ICs
- Combine Technologies
  - Combine technologies (Image sensor & processor)
- MOEMS Devices
  - Parallel assembly of image capture assemblies
  - Parallel assembly of image emitting devices
  - (Sensor/Emittor/Modulator with Optics)
- MEMs packaging
  - Decrease Cost
  - Hermetic packaging by WLP

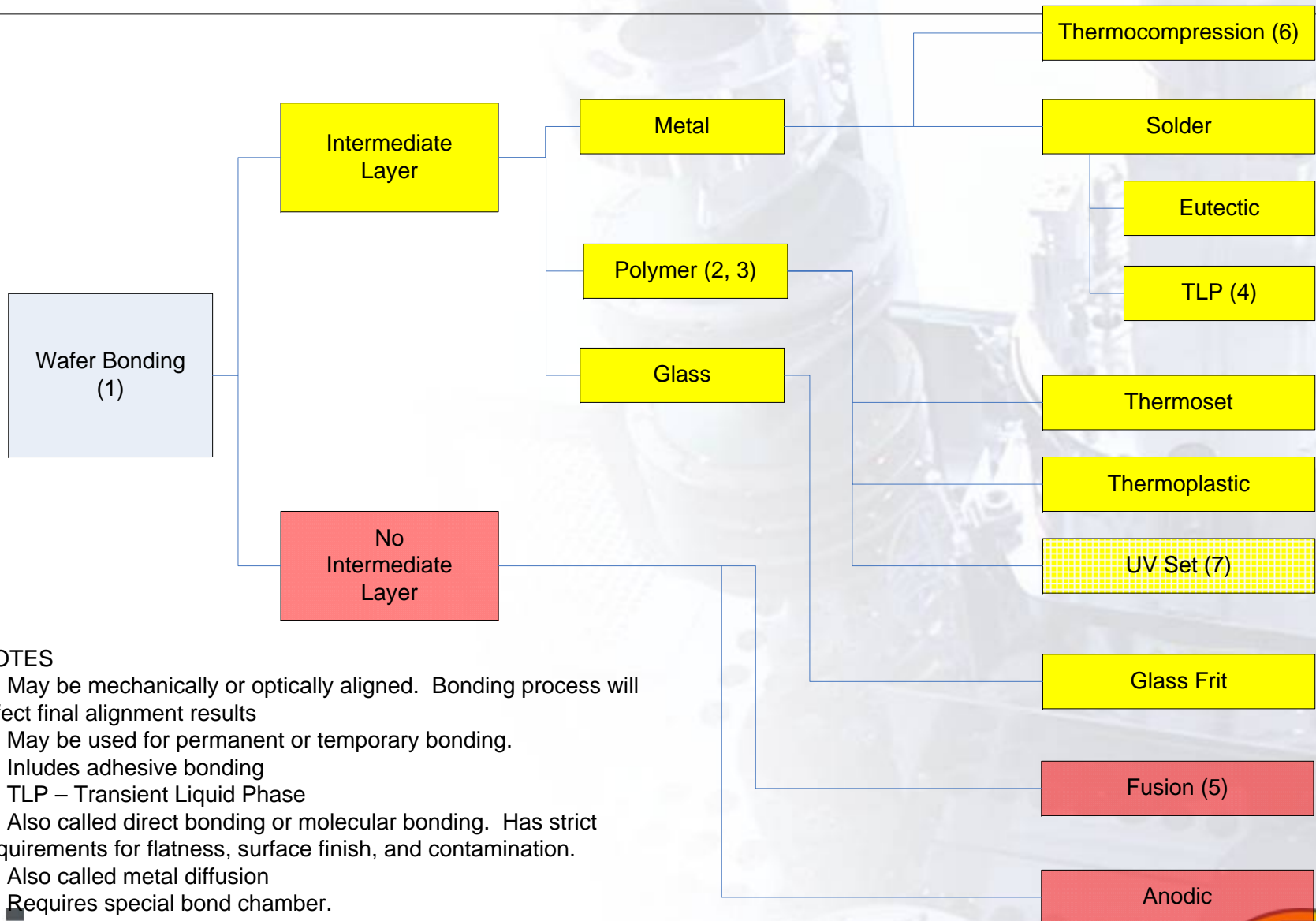
# Plasma Activation – An Enabling Technology for Wafer Bonding

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# Types of Bonding



## NOTES

1. May be mechanically or optically aligned. Bonding process will effect final alignment results
2. May be used for permanent or temporary bonding.
3. Includes adhesive bonding
4. TLP – Transient Liquid Phase
5. Also called direct bonding or molecular bonding. Has strict requirements for flatness, surface finish, and contamination.
6. Also called metal diffusion
7. Requires special bond chamber.

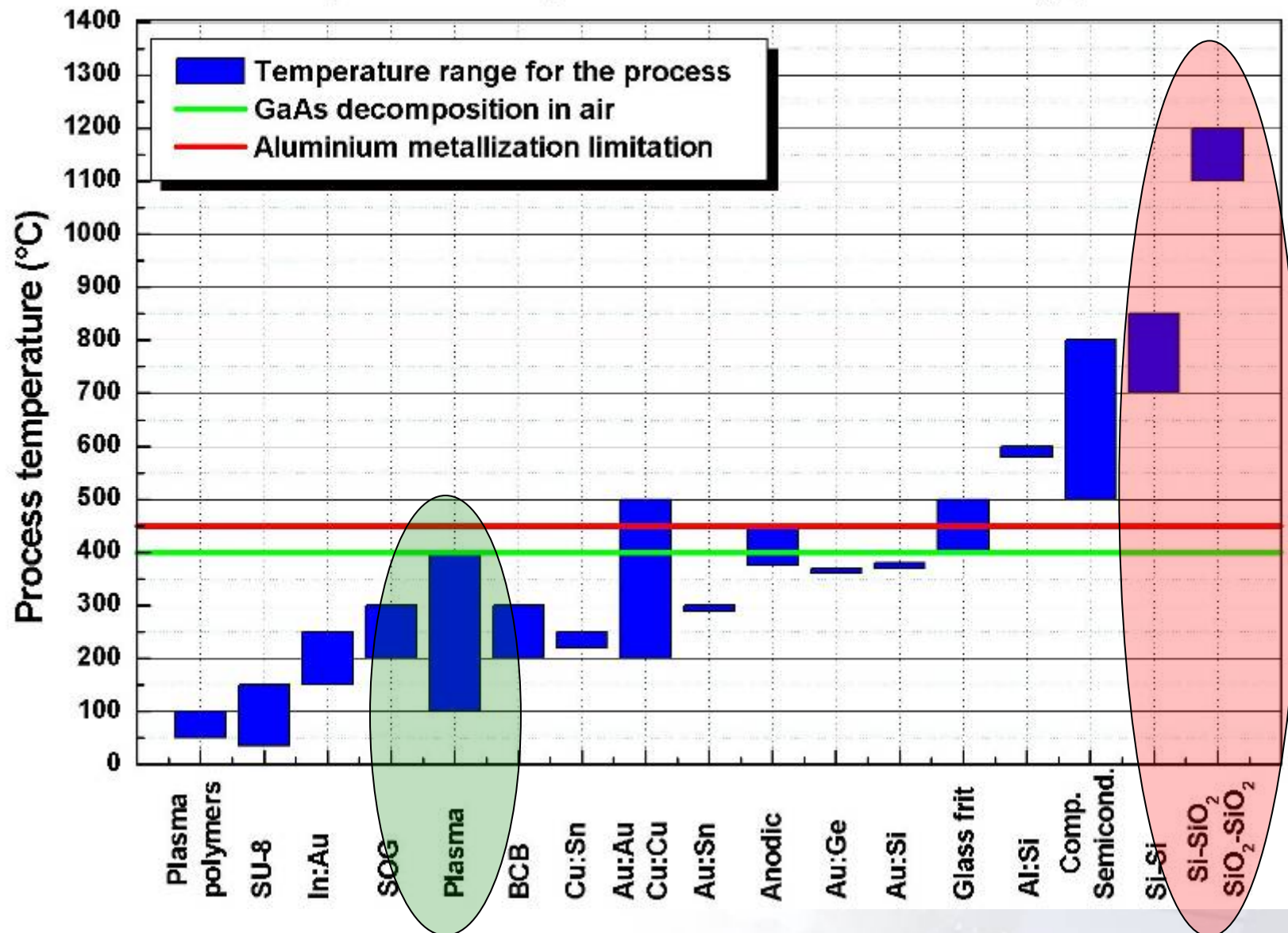
# Bonding Process Requirements

|                                      | No Intermediate Layer           |                          |                                 | Intermediate Layer                |                                |                               |                               |                               |                    |
|--------------------------------------|---------------------------------|--------------------------|---------------------------------|-----------------------------------|--------------------------------|-------------------------------|-------------------------------|-------------------------------|--------------------|
|                                      | Anodic Bonding (Electric Field) | Direct Bonding           | Plasma Activated Direct Bonding | Glass Frit                        | Thermo Compression             | Solder / Eutectic / TLP       | Adhesive                      | Epoxy (thermally cured)       | Epoxy (UV cured)   |
| Surface Roughness                    | < 20 nm                         | < 0.5nm                  | < 2 nm                          | < 1000 nm                         | < 2 nm                         | < 1000 nm                     | < 1000 nm                     | < 1000 nm                     | < 1000 nm          |
| Layer Thickness                      | NA                              | NA                       | NA                              | Determined by silk screen process | ~ 1000 nm each side            | ~ 1000 nm each side           | ?                             | ?                             | ?                  |
| Process Temperature                  | 400 - 500 C                     | 1000 C (anneal)          | Room Temp & 200-300 C anneal    | 400 - 500 C                       | 300 - 500 C depending on metal | 200 -500 C depending on metal | < 200 C depending on adhesive | < 200 C depending on adhesive | ~ Room Temperature |
| Cleanroom Environment (FS209E)       | 100                             | 10 or 1                  | 10                              | 1000                              | 10                             | 100                           | 100                           | 1000                          | 1000               |
| Sensitivity to Particles             | Medium                          | High                     | High                            | Low                               | Medium                         | Medium                        | Low                           | Low                           | Low                |
| Sensitivity to Surface Contamination | Medium                          | Very High                | Very High                       | Medium                            | High                           | High                          | Low                           | Low                           | Low                |
| Na present                           | Yes                             | No                       | No                              | No                                | No                             | No                            | No                            | No                            | No                 |
| Cycle Time (minutes)                 | 45 - 90                         | Bond ~ 1<br>Anneal - hrs | Bond ~ 1<br>Anneal hrs          | 45 - 90                           | 30 - 90                        | 30 - 60                       | 5 - 45                        | 15-30                         | 5 -15              |

# Bonding Process Performance

|   | No Intermediate Layer           |                |                                 | Intermediate Layer                |   |   |                          |                          |                          |
|---|---------------------------------|----------------|---------------------------------|-----------------------------------|---|---|--------------------------|--------------------------|--------------------------|
|   | Anodic Bonding (Electric Field) | Direct Bonding | Plasma Activated Direct Bonding | Glass Frit                        | Thermo Compression                            | Solder / Eutectic / TLP                                     | Adhesive                 | Epoxy (thermally cured)  | Epoxy (UV cured)         |
| CMOS Compatible                                 | No                              | No             | Yes                             | No                                | Yes   | Some  | Some                     | Yes                      | Yes                      |
| Electrically Conductive                         | No                              | No             | No                              | No                                | Yes   | Yes   | No                       | No                       | No                       |
| Vacuum Low < 1 mbar                             | Yes                             | Yes            | Yes                             | Yes                               | Yes   | Yes   | No                       | No                       | ?Yes                     |
| Vacuum High < 2 mbar                            | No                              | No             | Yes                             | No                                | Yes   | Yes   | No                       | No                       | No                       |
| Current Manufacturing Volume;                   | High Mature                     | High Mature    | Low Early                       | High Mature                       | Medium to High Mature                         | High Mature   | High Mature              | High Mature              | High Mature              |
| Mechanical Strength Sufficient for Backgrinding | Yes                             | Yes            | Yes                             | Yes                               | Yes   | Yes   | Yes                      | Yes                      | Yes                      |
| Max Post Bond Temperature                       | > 1000 C                        | > 1000 C       | > 1000 C                        | 350-450 C depending on Glass Frit | Limited by melting point of metal or eutectic | Limited by melting point of solder except for TLP is higher | Low, limited by adhesive | Low, limited by adhesive | Low, limited by adhesive |

# Maximum temperature ranges of common wafer bonding processes





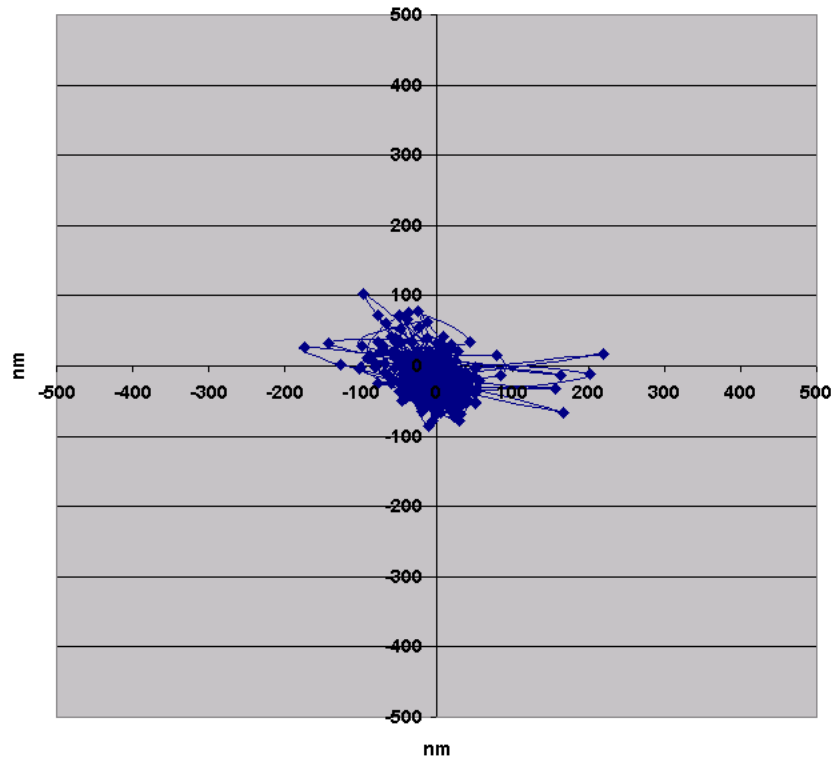
# Plasma Activation – An Enabling Technology for Wafer Bonding

## Outline

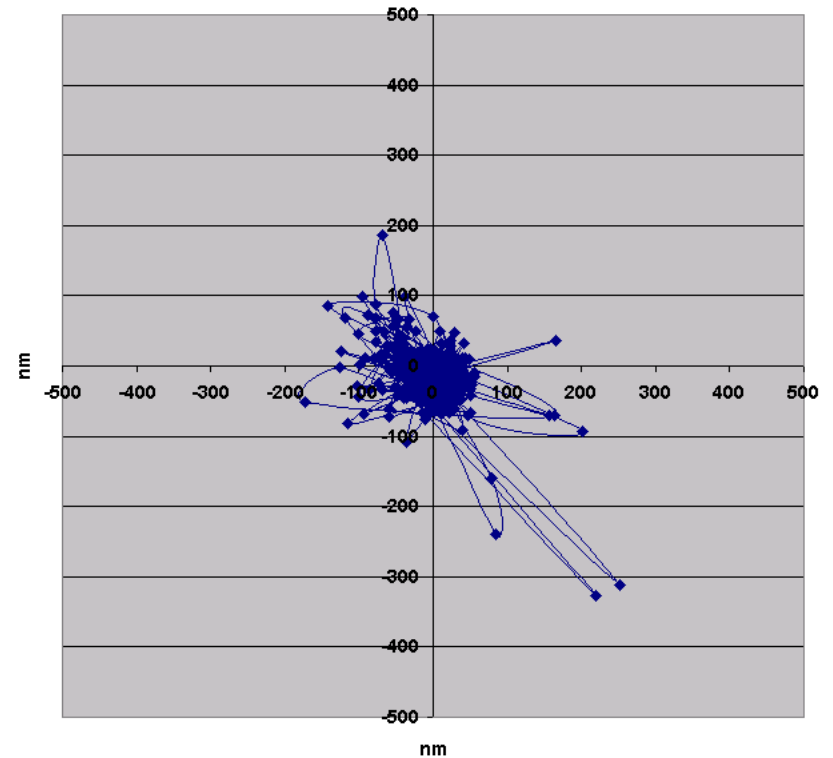
- Why Bond – driving forces
- Bonding Processes
- **Alignment Processes**
- PA (PLASMA Activated) Bonding

# SmartView<sup>®</sup>NT Results

Alignment Right



Alignment Left



|       | XR       | YR       |
|-------|----------|----------|
| Avg   | -6,78663 | -15,072  |
| Std   | 38,00791 | 26,95548 |
| 3*Std | 114,0237 | 80,86644 |

|       | XL       | YL       |
|-------|----------|----------|
| Avg   | 48,415   | 30,91665 |
| Std   | 61,07386 | 48,09172 |
| 3*Std | 183,2216 | 144,2751 |

## <200nm (3 Sigma) Alignment Capability

# SmartView<sup>®</sup>NT



invent

innovate

implement

*EV Group Confidential and Proprietary*



# Plasma Activation – An Enabling Technology for Wafer Bonding

- Wafer Growth During Bonding
  - Wafer Size 300 mm wafer
  - Silicon TCE ~3ppm
  - Alignment Temp 25C
  - Bond Process Temp 425C
- Results in wafer growth of ~380 um



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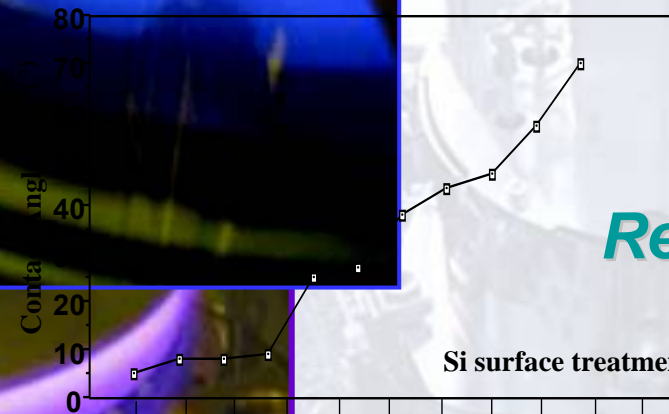
# Plasma Chemistry

Custom

Hydrogen

Oxygen

Reducing



Helium

Argon

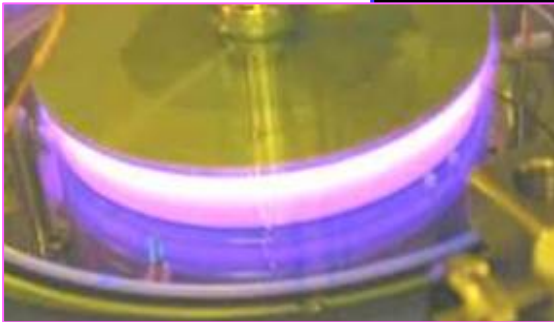
Non-Reactive

EV Group Confidential and Proprietary

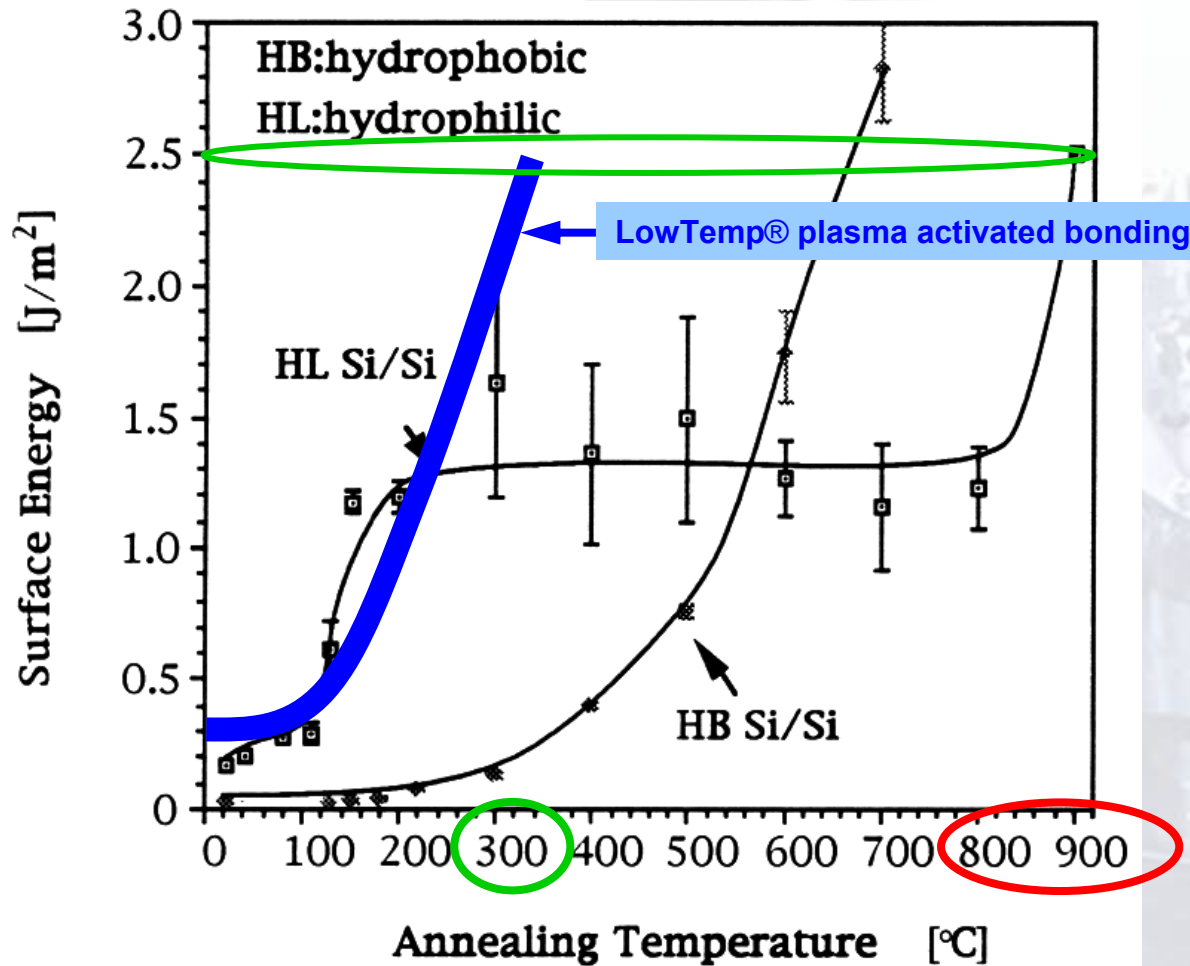


Reactive

Nitrogen

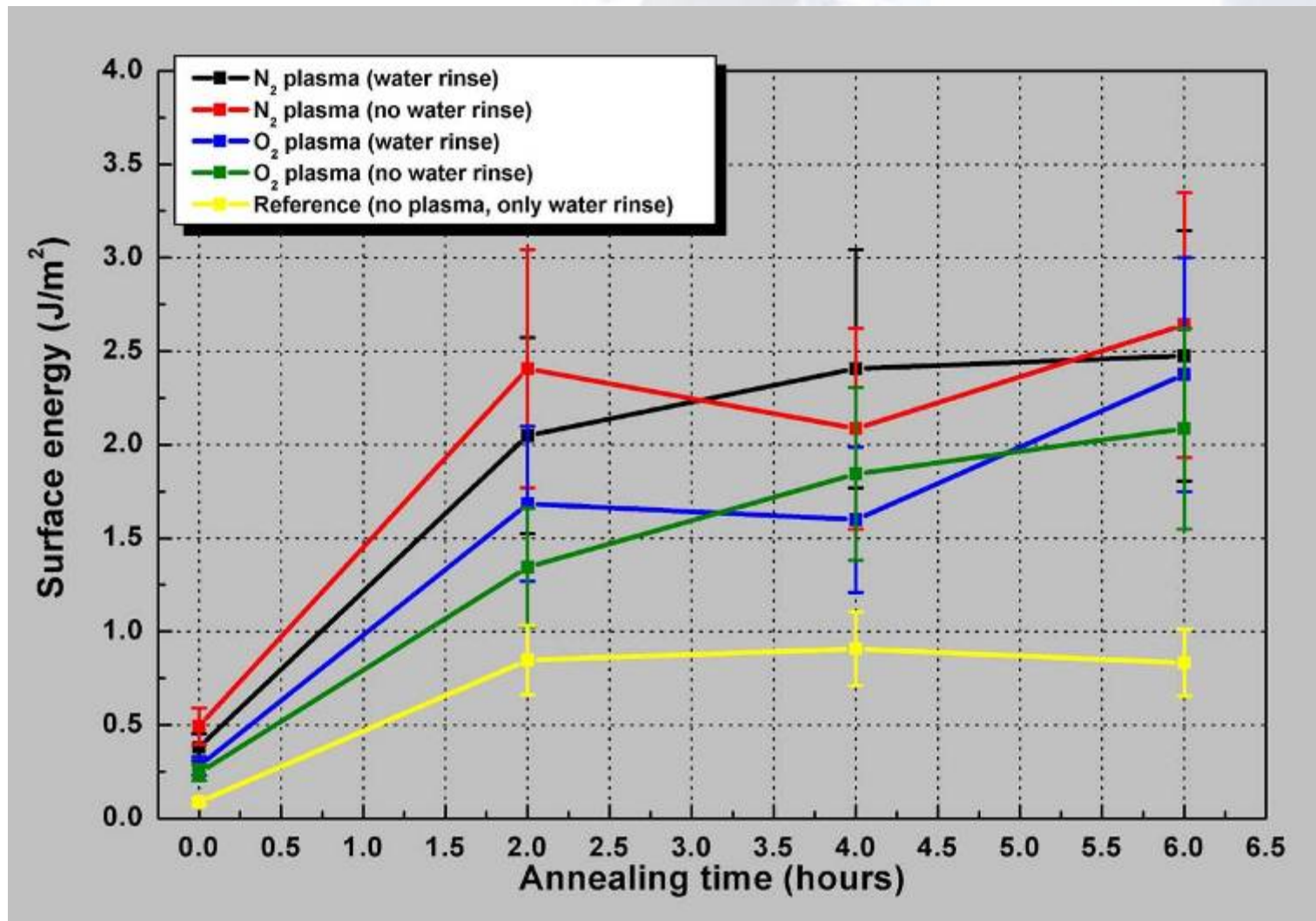


# Silicon Direct Bonding



Q.-Y. Tong and U. Gösele, *Semiconductor Wafer Bonding: Science and Technology* (Wiley, 1998).

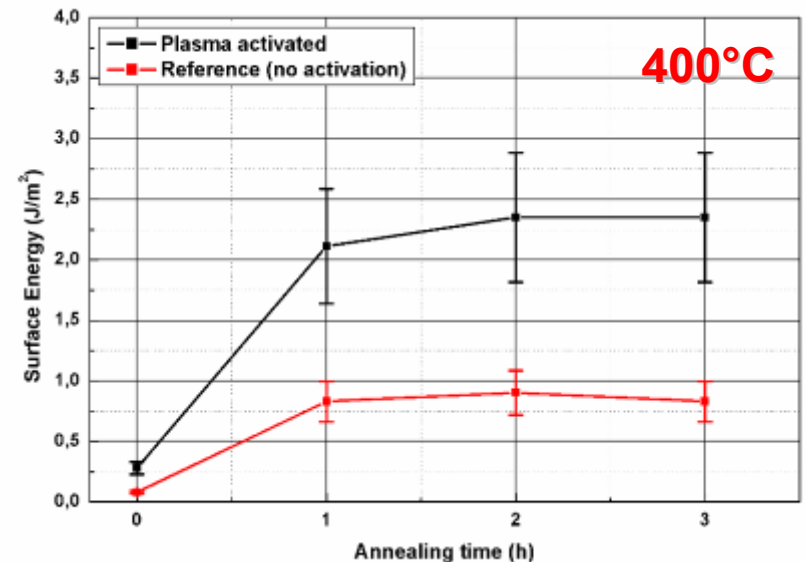
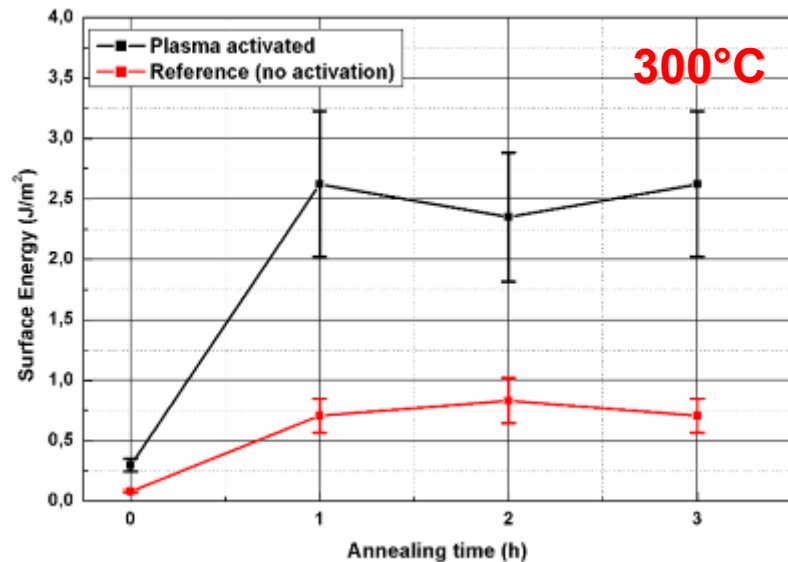
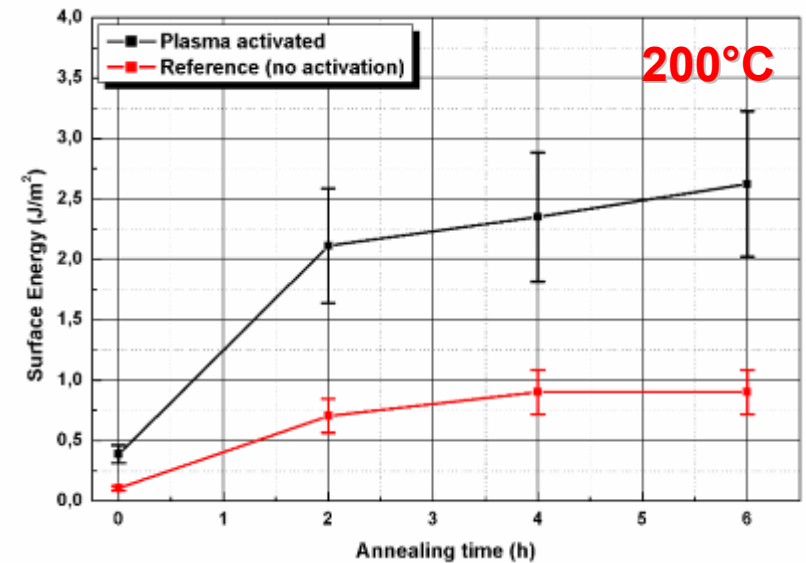
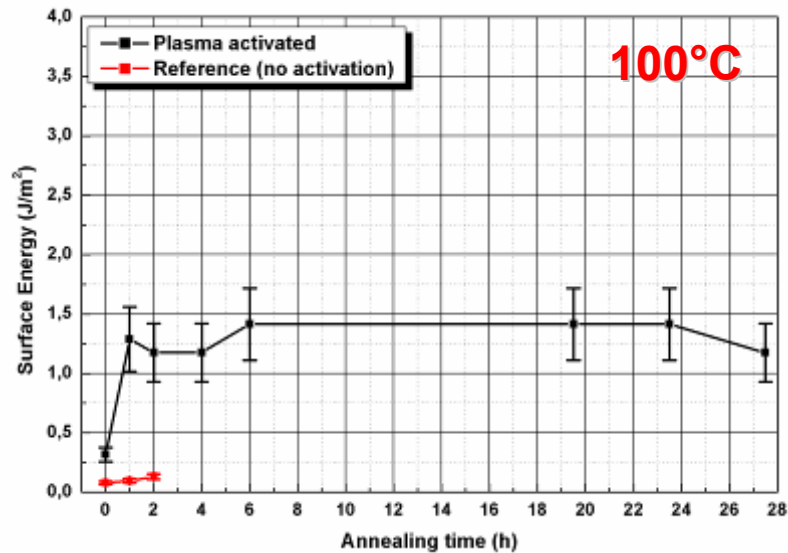
# Test 1: annealing at 200°C



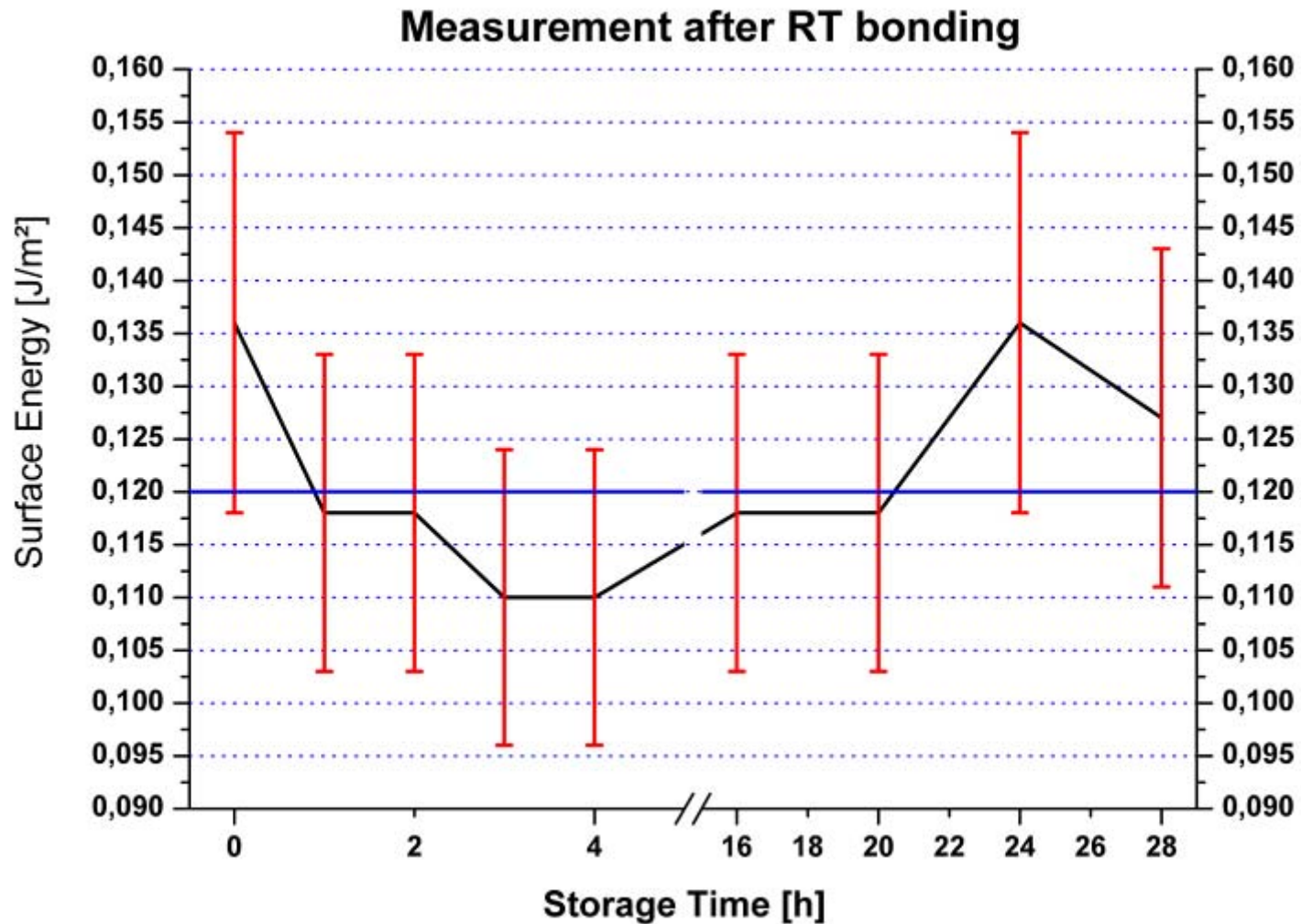
**Surface energy vs. annealing time at 200°C.**



# Surface Energy vs. Thermal Annealing Time



# Activation Lifetime



# Plasma Activation

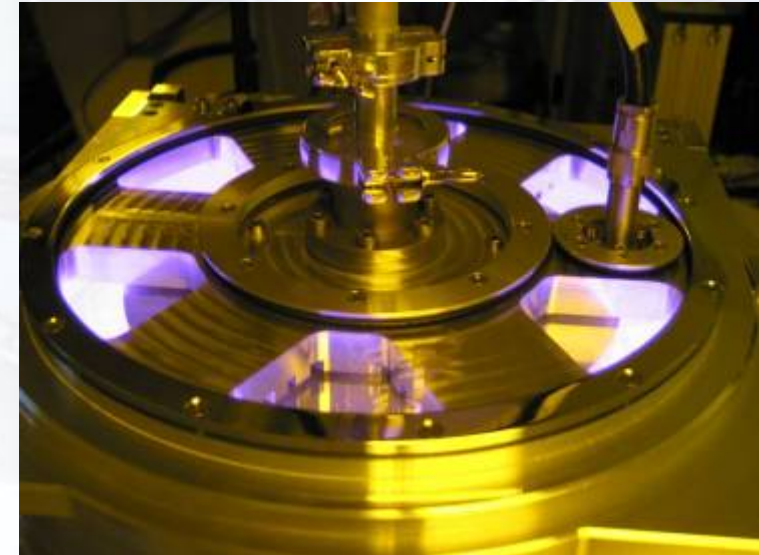
**Principle:**  
**Tailoring the surface chemistry**

**Result:**  
**Increased bond strength at low temperature**


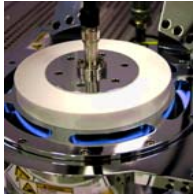




**Flexibility:**  
**Compliant with various materials  
(not only semiconductors)!**

**Technology:**  
**Fully compliant with state of the art wafer-  
to-wafer alignment and bonding equipment**

**Benefits:**  
**Expand wafer bonding applications field**  
**Bring bonding processes at industrial level**



**Economic:**  
**Equipment costs decrease**  
**Cost decrease per device (e.g. MEMS)**

| <br><br><b>LowTemp<sup>®</sup><br/>Plasma<br/>Chambers:</b> | <b>EVG810LT<br/>Chamber<br/>(150 mm)</b>  | <b>EVG810LT<br/>Chamber<br/>(200mm)</b>   | <b>EVG810LT<br/>Chamber<br/>(300mm)</b>  | <b>Full Gemini<br/>Platform</b>   | <b>EVG850LT<br/>Platform<br/>(200mm)</b>  |
|---|---|---|--|---|---|
|   |  |  |  |  |  |
| <b>Short Description:</b>   | Manual load dry activation chamber  | Manual or auto load dry activation chamber  | Manual or auto load dry activation chamber   | Auto-load Dry Activation Cluster Tool w/ Alignment and Compression Bond Chamber     | Auto-load Dry Activation Cluster Tool w/ Pre-Bond Chamber                           |
| <b>Max. Wafer Diameter</b>  | 150   | 200   | 300  | 200   | 200   |
| <b>Min. Wafer Diameter</b>  | pieces  | auto load: 100 (opt. 50)<br>man. load: pieces                                     | auto load: 200<br>man. load: pieces  | auto load: 50mm-100mm or 100mm - 200mm  | auto load: 50mm-100mm or 100mm - 200mm  |
| <b>Rack</b>   | yes   | yes   | yes  | yes   | yes   |
| <b>Automated Cover</b>  | optional  | yes   | yes  | yes   | yes   |
| <b>SmartView Integration-ex situ</b>  |   | yes   | yes  | yes   |   |
| <b>In situ Compatible</b>   |   | yes   | yes  | yes   | yes   |
| <b>Ex situ compatible</b>   | Standard  | Standard  | Standard   | Standard  | yes   |
| <b>Metal Ion Free</b>   | optional  | optional  | optional   | optional  | Standard  |
| <b>Supports Vacuum Packaging</b>  | only with <i>in situ</i> option   | only with <i>in situ</i> option   | only with <i>in situ</i> option  | yes   | yes   |
| <b>Supports (anodic, eutectic, glass frit, polymer...)dependent on configuration</b>  |   |   |  | yes   |   |
| <b>Supports optically aligned wafer bonding</b>   | yes   | yes   | yes  | yes   |   |



# Global Wafer Shape

## Specifications:

- **TTV  $\leq 3 \mu\text{m}$**
- **Bow/Warp**
  - $\leq 30 \mu\text{m}$  100mm**
  - $\leq 40 \mu\text{m}$  200mm**
  - $\leq 50 \mu\text{m}$  300mm**
- **Microroughness (measured by AFM,  $2 \times 2 \mu\text{m}^2$ ):**
  - $< 0.5 \text{ nm}$  (all wafer diameters): excellent results**
  - $< 1.0 \text{ nm}$ : good results**
  - $< 1.0\text{-}2 \text{ nm}$ : possible under some special conditions**

# Accepted Contamination Levels

- **Particles:**
  - **Incoming wafers:**
    - Si: <0.1 LPD/cm<sup>2</sup>, size >0.15μm
    - Oxide: <0.1 LPD/cm<sup>2</sup>, size >0.2μm

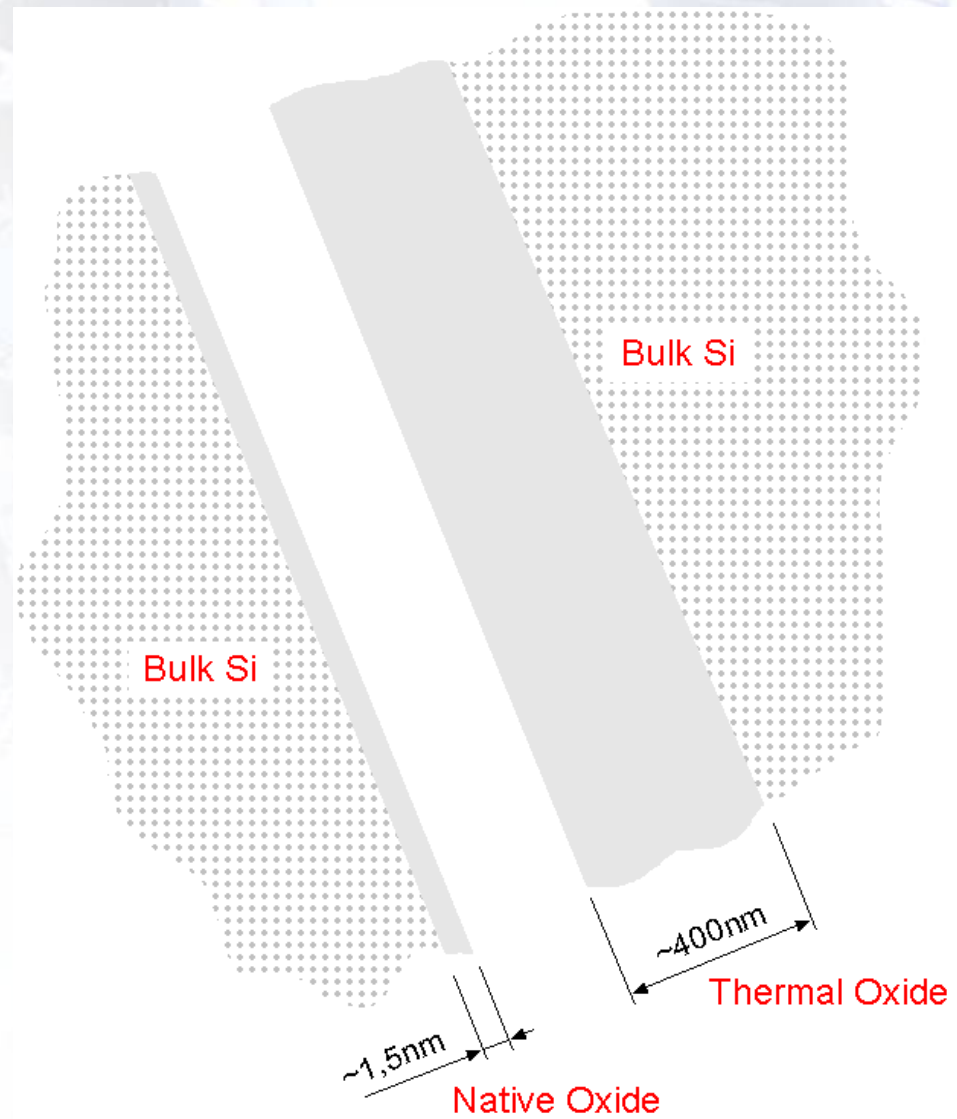
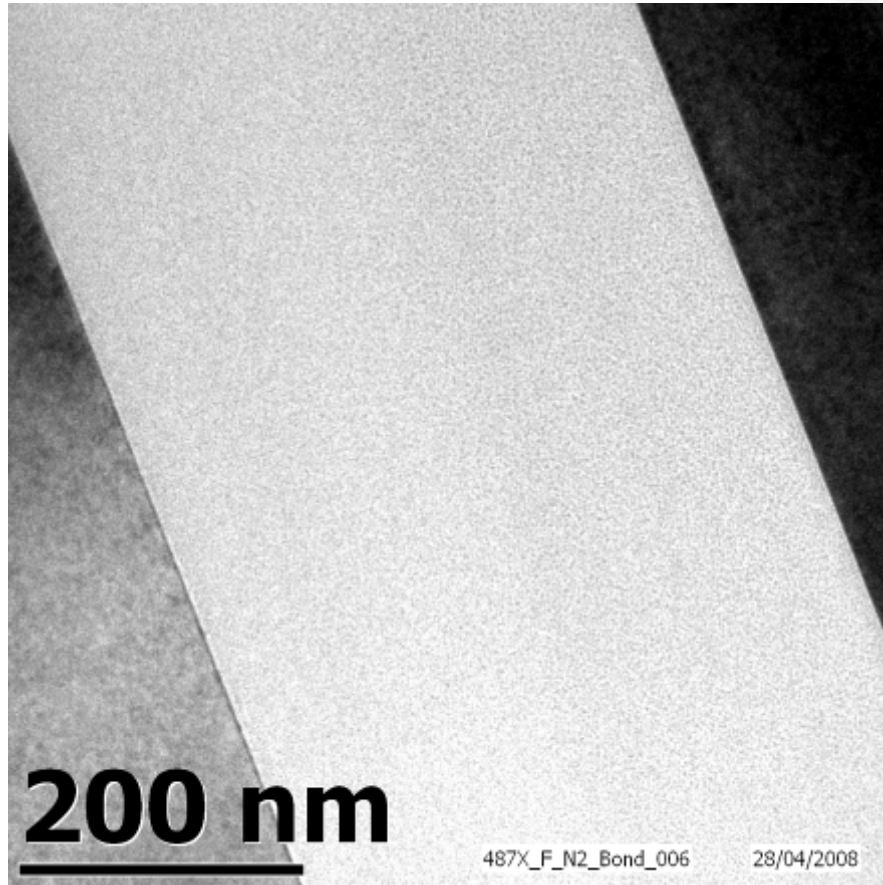
(0.1LPD = 8p/100mm, 12p/125mm, 18p/150mm, 31p/200mm, 71p/300mm)
  - **Wafers handling (environment):**

**Added: <0.015 LPD/cm<sup>2</sup>**  
(0.015LPD = 1p/100mm, 2p/125mm, 3p/150mm, 5p/200mm, 11p/300mm)
  - **Process stations (clean, plasma and pre-bond):**

**Added: - Si: <0.03 LPD/cm<sup>2</sup>, size >0.15μm**  
**- Oxide: <0.05 LPD/cm<sup>2</sup>, size >0.2μm**  
(0.03LPD = 2p/100mm, 4p/125mm, 6p/150mm, 9p/200mm, 21p/300mm  
0.05LPD = 4p/100mm, 6p/125mm, 9p/150mm, 16p/200mm, 35p/300mm)
- **Metal ions (Fe, Cu, Ni, Al, Na, K, Ca, Mg):**

**Equipment installation:  $\leq 5 \times 10^{10}$  atoms/cm<sup>2</sup>**  
**SOI production:  $\sim 10^9$  atoms/cm<sup>2</sup>**

# TEM Analysis



# Conclusion

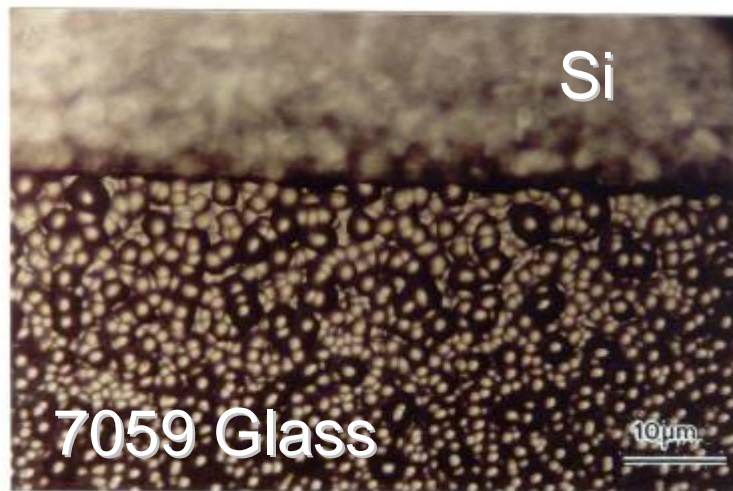
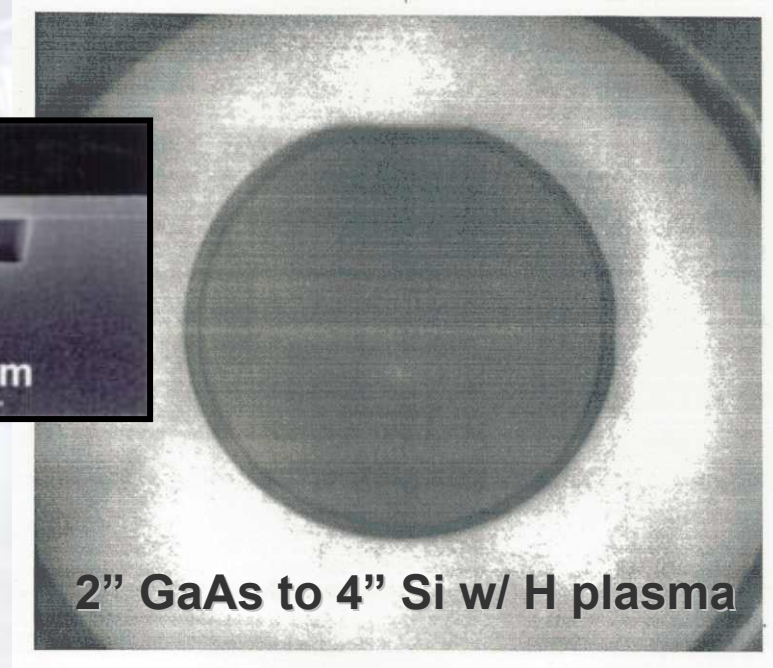
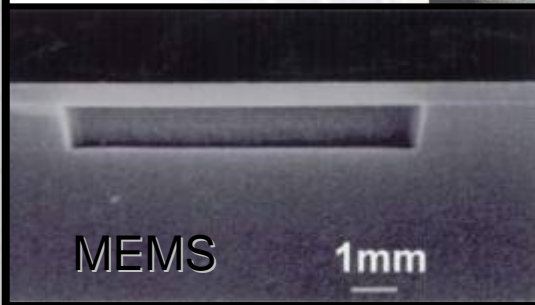
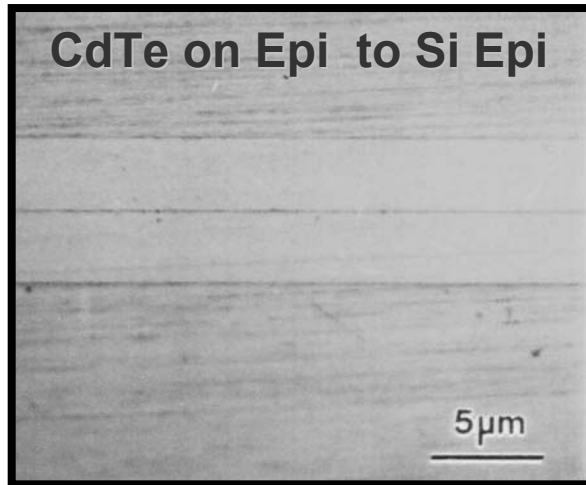
- Plasma activation of the surfaces overcomes the problem of high process temperatures needed for standard fusion bonding.
- Surface activation effect has a relatively long lifetime.
- Despite the long lifetime it is strongly recommended to pre-bond the substrates as soon as possible after activation for contamination reasons.
- Plasma activation doesn't increase surface microroughness.
- TEM investigation shows no visible bond interface line.



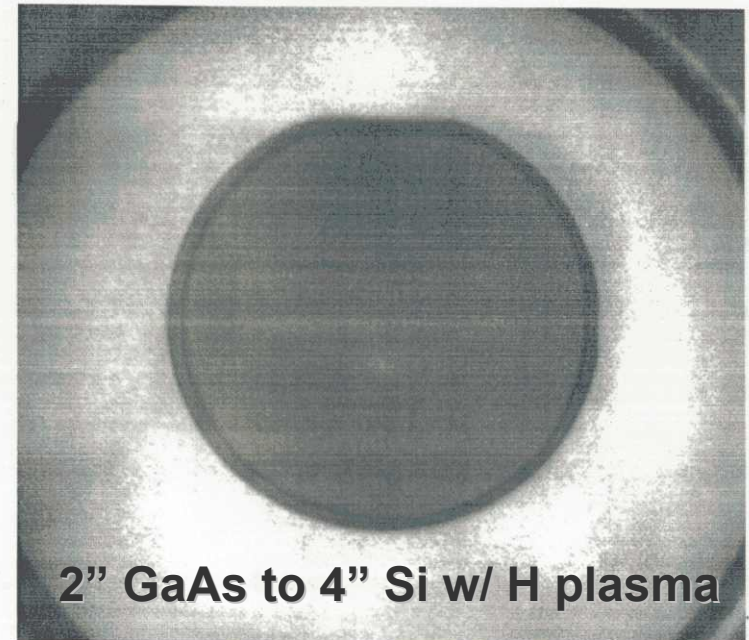
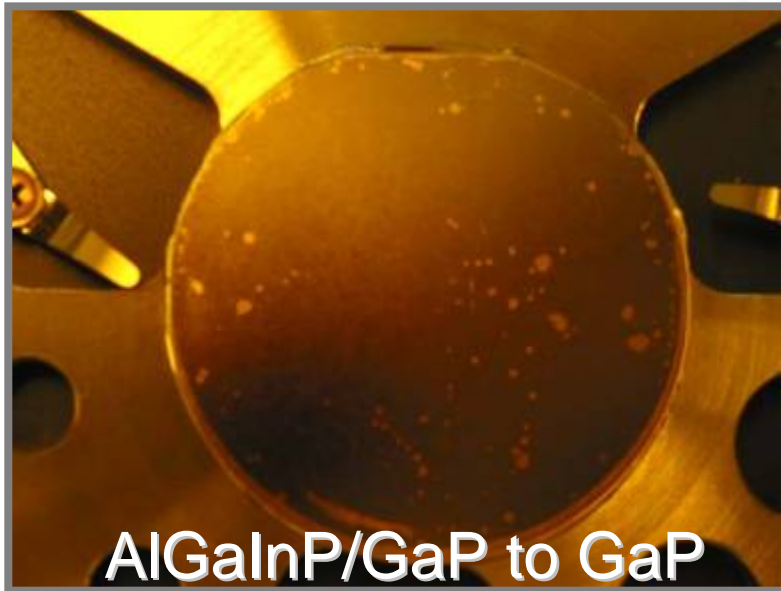
# Plasma Activated Wafer Bonding Applications

- **SOI → maximum bond strength reached below cleaving temperature**
- **MEMS: sealing → vacuum sealing compatible**
- **MEMS: materials combinations → low temperature allows stress management**
- **MEMS on CMOS (e.g. backside illuminated image sensors)**
- **Polymer materials for bio-compatible applications**

# Low Temperature Plasma Bonded Gallery

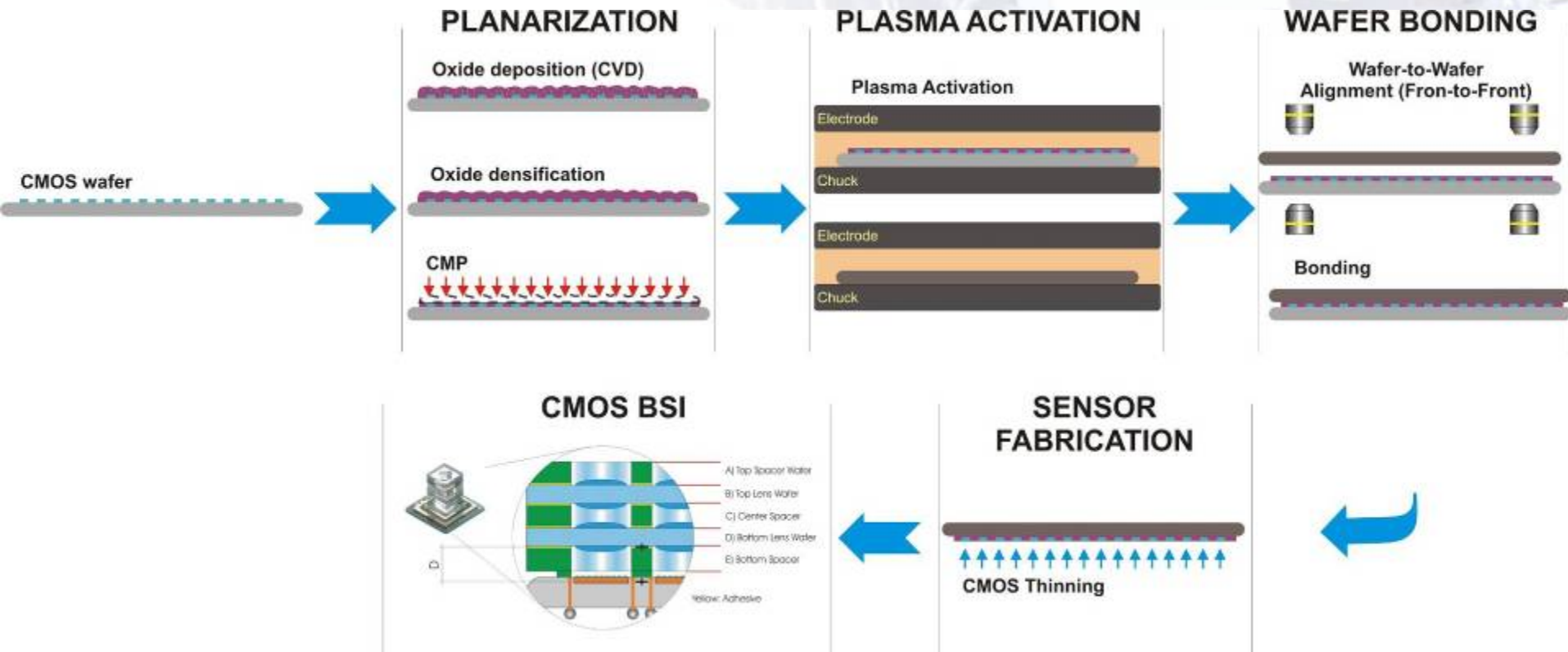


# Examples: Compound Semiconductors





# Wafer Bonding for CMOS BSI CIS: Fusion



# EV Group

Thank You for Your Attention  
Questions?

[www.EVGroup.com](http://www.EVGroup.com)



Triple i - The key to your success





# Bonding Process Variables

| Incoming   | In Chamber   | Outgoing   |
|--|--|--|
| <b>1.Wafer</b><br>a.Size<br>i.Diameter<br>ii.Thickness<br>b.Material<br>i.CTE<br>c.Bow & Warp<br>d.TTV<br>e.Vacuum integrity <sup>[1]</sup>                                  | <b>1.Wafer</b>   | <b>1.Wafer</b><br>a.Bow & warp<br>b.TTV<br>c.Breakage  |
| <b>1.Contact Layers</b><br>a.Thickness<br>b.TTV<br>c.Roughness<br>d.Bulk Composition<br>e.Surface Composition<br>f.Surface Particles<br>g.Surface Contamination<br>h.Pattern | <b>1.Standard Bond Chamber</b><br>a.Time<br>b.Temperature<br>c.Force <sup>[2]</sup><br>d.Atmosphere <sup>[3]</sup><br>e.Wafer to wafer spacing (flags)<br>f.Bow Pin<br>g.Voltage / current<br><b>2.Special Bond Chamber</b><br>a.UV energy<br>b.Plasma<br><b>3.Materials</b><br>a.Tg or Melting Point<br>b.Outgassing<br>c.Shrinkage<br>d.Adhesion<br>e.Flow | <b>1.Bond Layers</b><br>a.Percent bonded (voids)<br>b.Thickness<br>c.Strength<br>d.Hermeticity<br>e.Conductivity<br>f.Pattern<br><b>2.Atmosphere in cavities if present</b><br>a.Gas<br>b.Pressure |
| <b>1.Alignment</b><br><b>2.Spacing (gap between wafers)</b>  |  | <b>1.Alignment</b><br><b>2.Wafer to wafer spacing</b>  |

<sup>[1]</sup> Can the wafer be handled by backside vacuum or will edge handling or other special handling be required?

<sup>[2]</sup> Translates to pressure based on bond contact area

<sup>[3]</sup> Vacuum, forming gas, inert gas; no toxics or corrosive gasses.

## Color Code

Items in RED are controlled by upstream process

Items in Green are controlled by alignment system

Items in BLACK are controlled by bond chamber

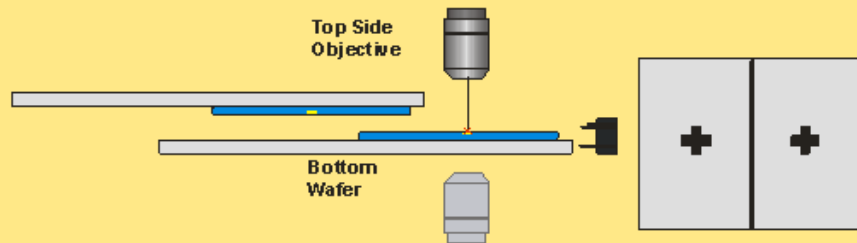
Items in BLUE are output variables

# SmartView® - Benefits

- **Supports all bond alignment methods**
    - Transparent Alignment
    - IR Alignment
    - Backside Alignment
    - SmartView (Face-to-Face) Alignment
  - **SmartView (Face to Face) Alignment Advantage**
    - Eliminates need for
      - IR transparent substrates which prevents high doping levels and requires metal line keep-outs around alignment targets.
- Or
- Backside alignment marks
  - This reduces the cost and simplifies the design

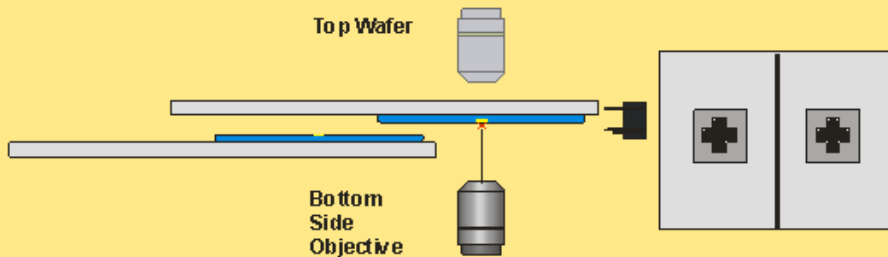
# SmartView® Face-to-Face Bond Aligner

- Proprietary Alignment Technique that allows for high alignment accuracy as needed for high density interconnects with **non-IR transparent wafers**.



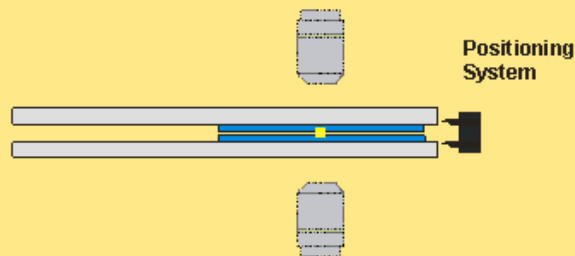
## No Z-travel

- Locate bottom wafer alignment marks with top objectives
- Digitize image
- Store position



## No re-focussing

- Align top wafer to digitized image



## Perfect result

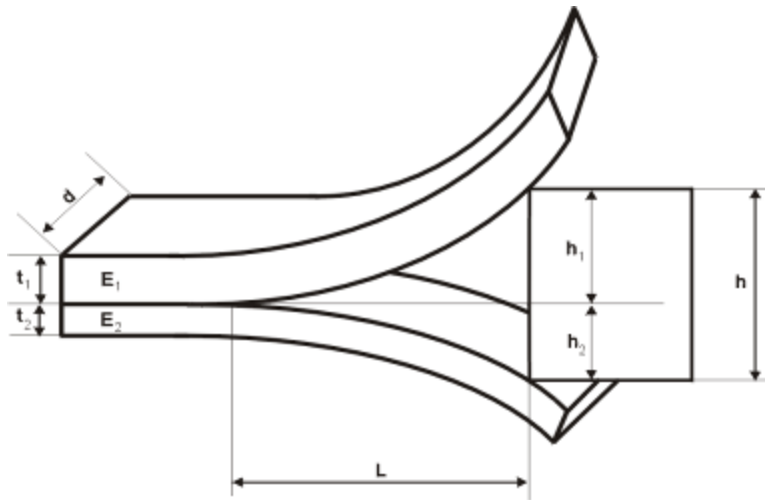
- Restore bottom wafer position
- Bring wafers in contact

US Patent: 6,214,692 B1



# Bond Strength Quantification

## Crack-opening method (Maszara, Razor blade)

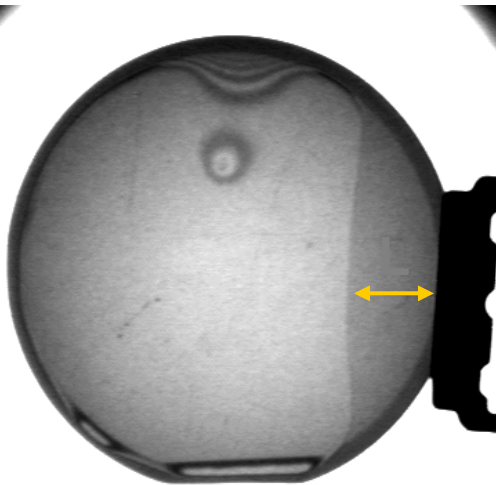


Dissimilar materials:

$$\gamma = \frac{1}{2}(\gamma_1 + \gamma_2) = \frac{3h^2}{16L^4} \frac{E_1 t_1^3 E_2 t_2^3}{E_1 t_1^3 + E_2 t_2^3}$$

Identical materials:

$$\gamma = \frac{3h^2 E t^3}{32L^4}$$



IR transmission image of a Si/Si bonded pair with a razor blade inserted at the bonded interface.

# TEM Analysis

After 1h annealing @ 300°C!

